LM3645 Synchronous Boost Quad LED Flash Driver with 2-A High-Side Current Sources

1 Features

- Quad independent led current source programmability
- Accurate and programmable LED current range from 0.525 mA to 2 A
- Optimized flash LED current during low battery conditions (I_{VFM})
- > 85% efficiency in torch mode (at 100 mA) and flash mode (at 1 A to 2 A)
- Grounded cathode LED operation for improved thermal management
- Dual hardware strobe enable (STR1, STR2)
- Synchronization input for RF power amplifier pulse events (TORCH/TX)
- Hardware torch enable (TORCH/Tx)
- Dual remote NTC monitoring (TEMP1, TEMP2)
- Fixed output voltage mode
- 1-MHz I^2C-compatible interface
  - (I^2C Address = 0x65)

2 Applications

- Camera phone white LED flash
- Digital still cameras
- Barcode scanners
- Handheld data terminals

3 Description

The LM3645 is a quad LED flash driver that provides a high level of adjustability within a small solution size.

The LM3645 utilizes a synchronous boost converter to provide power to the quad 2A constant current LED sources. The quad 256 level current sources provide the flexibility to adjust the current ratios between LED1, LED2, LED3 and LED4 with each driver capable of delivering a maximum of 2A. An adaptive regulation method ensures the current sources remain in regulation and maximizes efficiency.

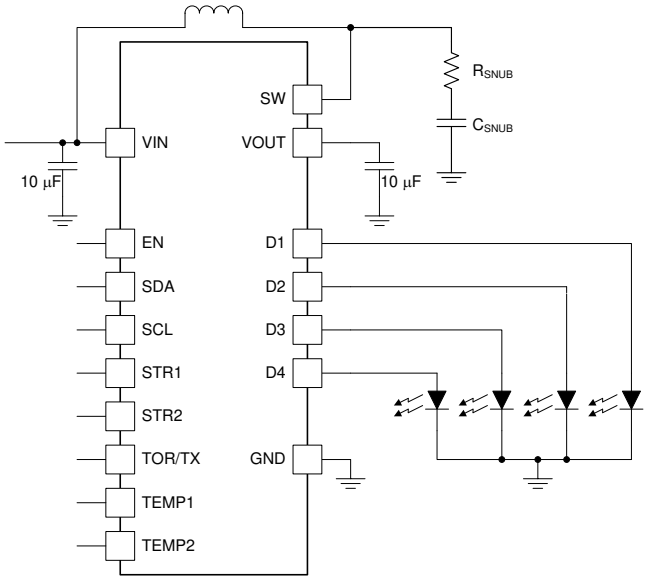
Features of the LM3645 are controlled via an I^2C-compatible interface. These features include: dual hardware flash pins and a hardware torch or Tx interrupt pin (STR1, STR2 and TORCH/TX), and dual NTC thermistor monitors. The device offers independently programmable currents in each output leg to drive the LEDs in a flash or movie mode (Torch) condition as well as a fast turn-on and turn-off IR Mode.

Two switching frequency options, overvoltage protection (OVP), and adjustable current limit allow for the use of tiny, low-profile inductors and 10µF ceramic capacitors. The device operates over a –40°C to +85°C ambient temperature range.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3645	DSBGA (25)	2.192mm × 1.927mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....3
5 Specifications....4
5.1 Absolute Maximum Ratings....4
5.2 ESD Ratings....4
5.3 Recommended Operating Conditions....4
5.4 Thermal Information....4
5.5 Electrical Characteristics....5
5.6 Timing Requirements....6
5.7 Switching Characteristics....6
5.8 Typical Characteristics....7
6 Detailed Description....10
6.1 Overview....10
6.2 Functional Block Diagram....11
6.3 Feature Description....11
6.4 Device Functioning Modes....18
6.5 Programming and Control....22
6.6 Register Descriptions....26
7 Application and Implementation....58
7.1 Application Information....58
7.2 Typical Application....58
8 Power Supply Recommendations....66
9 Layout....67
9.1 Layout Guidelines....67
9.2 Layout Example....68
10 Device and Documentation Support....69
10.1 Third-Party Products Disclaimer....69
10.2 Receiving Notification of Documentation Updates....69
10.3 Support Resources....69
10.4 Trademarks....69
10.5 Electrostatic Discharge Caution....69
10.6 Glossary....69
11 Revision History....69
12 Mechanical, Packaging, and Orderable Information....70

Copyright © 2026 Texas Instruments Incorporated

4 Pin Configuration and Functions

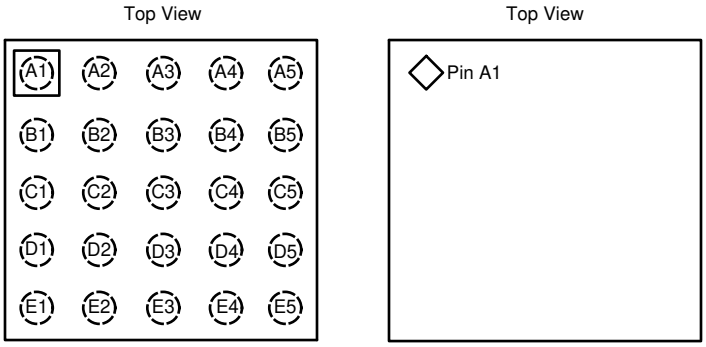


Figure 4-1. YCG Package, 25-Pin DSBGA

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A3	IN	P	Input voltage connection. Connect this pin to the input supply and bypass to GND with a 10-µF or larger ceramic capacitor
B1	SW	P	Drain connection for internal N-channel MOSFET and synchronous P-channel MOSFET switches
B2			
C1	OUT	P	Step-up DC-DC converter output. Connect 2 × 10-µF ceramic capacitors between this terminal and GND
C2			
C3			
C4			
A1	GND	G	Ground
A2			
E1	D1	P	High-side current source outputs for flash LEDs
E2			
D1	D2	P	
D2			
D4	D3	P	
D5			
E4	D4	P	
E5			
A4	EN	I	Active high hardware enable. Drive EN pin high to turn on the device. An internal pulldown resistor of 300 kΩ is between EN and GND.
A5	SDA	I/O	I^2C serial data input/output
B5	SCL	I	I^2C serial clock input
B3	STR1	I	Active high hardware flash enable. Drive STR1 high to turn on flash or IR pulse. An internal pulldown resistor of 300 kΩ is between STR1 and GND.
B4	STR2	I	Active high hardware flash enable. Drive STR2 high to turn on flash or IR pulse. An internal pulldown resistor of 300 kΩ is between STR2 and GND.
C5	TORCH/TX	I	Active high hardware torch enable or power amplifier synchronization input. Internal pulldown resistor of 300 kΩ between TORCH/TX and GND.
E3	TEMP1	I/O	Threshold detector for NTC temperature sensing and current scale back
D3	TEMP2	I/O	

Copyright © 2026 Texas Instruments Incorporated

5 Specifications

5.1 Absolute Maximum Ratings

overoperating free-air temperature range (unless otherwise noted)(1) (2)

	MIN	MAX	UNIT
IN, SW, OUT, LED1, LED2, LED3, LED4	−0.3	6	V
SDA, SCL, TORCH/TX, TEMP1, TEMP2, EN, STR1, STR2	−0.3 to the lesser of (V_{IN} + 0.3) w/ 6 V maximum		V
Continuous power dissipation(3)	Internally limited		
Junction temperature, T_{J-MAX}		150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) Internal thermal shutdown circuitry protects the device frompermanent damage. Thermal shutdown engages at T_J = 150°C (typical). Readback of the thermal shutdown bit resets the detection mechanism. Thermal shutdown is ensured bydesign.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{IN}	Normal operation	2.5	5.5	V
	Transient operation (no reset of the device)	2.3		
Junction temperature, T_J		−40	125	°C
Ambient temperature, T_A (3)		−40	85	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. Theseare stress ratings only, and functional operation of the device at these or any other conditionsbeyond those indicated under *recommended operating conditions* isnot implied. Exposure to absolute-maximum-rated conditions for extended periods may affect devicereliability.
(2) All voltages are with respect to the potential at the GNDterminal.
(3) In applications where high power dissipation and/or poor packagethermal resistance is present, the maximum ambient temperature may have to be derated. Maximumambient temperature (T_{A-MAX}) is dependent on the maximum operating junctiontemperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the devicein the application (P_{D-MAX}), and the junction-to-ambient thermal resistanceof the part/package in the application ($R_{\theta JA}$), as given by the followingequation: $T_{A-MAX} = T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})$.

5.4 Thermal Information

THERMAL METRIC(1)		LM3645 YCG (DSBGA) 25 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.5	°C/W

(1) For more information about traditional and new thermalmetrics, see the *Semiconductor and ICPackage Thermal Metrics* application report.

Copyright © 2026 Texas Instruments Incorporated

5.5 Electrical Characteristics

Typical limits tested at T_A = 25°C. Minimum and maximumlimits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤+85°C). Unless otherwise specified, V_{IN} = 3.6 V, EN = 1.8 V,V_{IO} = 1.8 V.(1) (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SOURCE						
$I_{LED1/2/3/4}$	Current source accuracy	V_{OUT} = 4 V, flash code = 0xFF = 2-A flash	–7%	2	7%	A
		V_{OUT} = 4 V, torch code = 0xFF = 360-mA torch	–10%	360	10%	mA
$I_{LEDx-Match}$	Current source matching (3)	V_{OUT} = 4 V, flash code = 0x40 = 500-mA flash		0.5%		
V_{HR}	LED1, LED2, LED3 and LED4 current source regulation voltage	V_{OUT} = 4 V, 1 A < $I_{LED1/2/3/4}$ ≤ 2 A		250		mV
		V_{OUT} = 4 V, 0 A ≤ $I_{LED1/2/3/4}$ ≤ 1 A		150		
STEP-UP DC-DC CONVERTER						
R_{PMOS}	PMOS switch on-resistance			35		mΩ
R_{NMOS}	NMOS switch on-resistance			30		mΩ
I_{CL}	Switch current limit	00 Setting	–12%	2	12%	A
		01 Setting	–12%	3	12%	
		10 Setting	–12%	4	12%	
		11 Setting	–12%	5	12%	
V_{OVP}	Overvoltage protection threshold	On threshold	5.55	5.7	5.85	V
		Off threshold	5.4	5.6	5.7	
V_{OUT}	Output voltage regulation	VM_VOLTAGE = 00, I_{OUT} = 0 A	–5%	4.0	5%	V
		VM_VOLTAGE = 01, I_{OUT} = 0 A	–5%	4.5	5%	
		VM_VOLTAGE = 10, I_{OUT} = 0 A	–5%	5	5%	
		VM_VOLTAGE = 11, I_{OUT} = 0 A	–5%	5.2	5%	
UVLO	Undervoltage lockout threshold	Falling V_{IN}	–2%	2.2	2%	V
V_{TRIP}	NTCx comparator trip threshold		–5%	0.6	5%	V
I_{NTC}	NTCx current		–6%	50	6%	µA
V_{IVFM}	Input voltage flash monitor trip threshold		–3%	2.9	3%	V
I_Q	Quiescent supply current	Device not switching pass mode (or IR pass mode)		0.320	1	mA
I_{SD}	Shutdown supply current	Device disabled, EN = 0 V, SW = V_{IN} 2.5 V ≤ V_{IN} ≤ 5.5 V		0.1	4	µA
I_{SB}	Standby supply current	Device disabled, EN = 1.8 V, SW = V_{IN} 2.5 V ≤ V_{IN} ≤ 5.5 V		1.6	10	µA
EN, TORCH/TX, STR1, STR2 VOLTAGE SPECIFICATIONS						
V_{IL}	Input logic low	2.3 V ≤ V_{IN} ≤ 5.5 V	0		0.4	V
V_{IH}	Input logic high	2.3 V ≤ V_{IN} ≤ 5.5 V	1.2		V_{IN}	V
I²C-COMPATIBLE INTERFACE SPECIFICATIONS (SCL, SDA)						
V_{IL}	Input logic low	2.3 V ≤ V_{IN} ≤ 5.5 V	0		0.4	V
V_{IH}	Input logic high	2.3 V ≤ V_{IN} ≤ 5.5 V	1.2		V_{IN}	V
V_{OL}	Output logic low	I_{LOAD} = 3 mA			400	mV

(1) Minimum (MIN) and Maximum (MAX) limits are specified by design,test, or statistical analysis. Typical (TYP) numbers are not verified, but do represent the mostlikely norm. Unless otherwise specified, conditions for typical specifications are:V_{IN} = 3.6 V and T_A = 25°C.
(2) All voltages are with respect to the potential at the GND pin.
(3) Matching is defined as the greater of the (I_{LEDMAX} - $I_{LEDAVERAGE}$)/$I_{LEDAVERAGE}$ or |(I_{LEDMIN}-$I_{LEDAVERAGE}$)|/$I_{LEDAVERAGE}$

Copyright © 2026 Texas Instruments Incorporated

5.6 Timing Requirements

			MIN	NOM	MAX	UNIT
t_1	SCL clock period	VIO = 1.8 V $R_{PULLUPS}$ = 1 kΩ 100 pF maximum loading	1			µs
t_2	Data in set-up time to SCL high		50			ns
t_3	Data out stable after SCL low		0			ns
t_4	SDA low set-up time to SCL low (start)		260			ns
t_5	SDA high hold time after SCL high (stop)		260			ns

5.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW-MAX}	Maximum switching frequency	2.3 V ≤ V_{IN} ≤ 5.5 V	–6%	4	6%	MHz

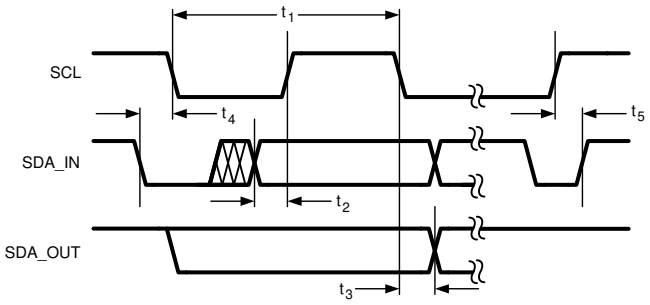
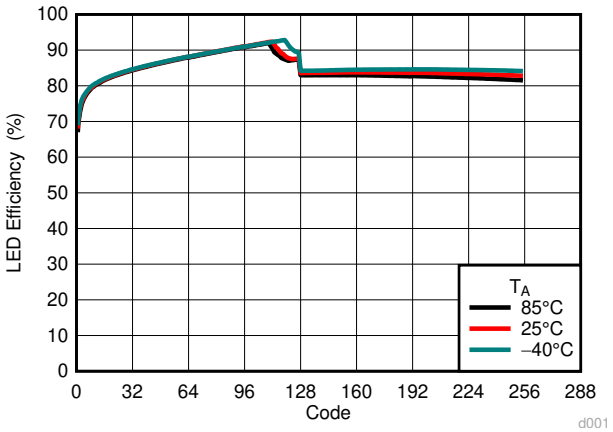


Figure 5-1. I²C-Compatible Interface Specifications

Copyright © 2026 Texas Instruments Incorporated

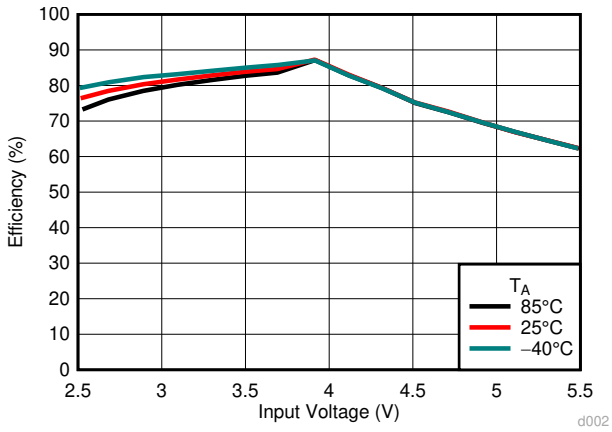
5.8 Typical Characteristics

I_{CL} = 5 A



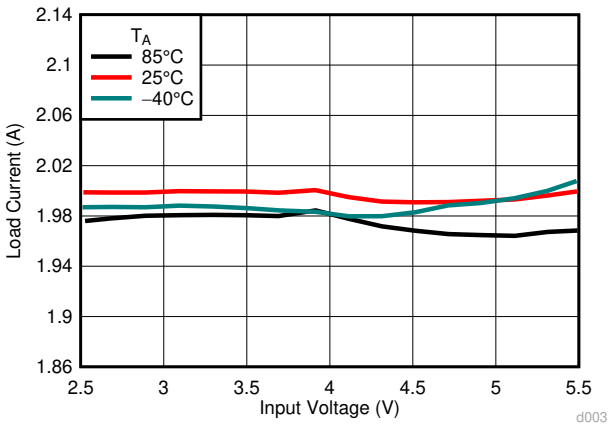
V_{IN} = 3.3 V f_{SW} = 4 MHz

Figure 5-2. Flash Efficiency vs Code Tri-Temp



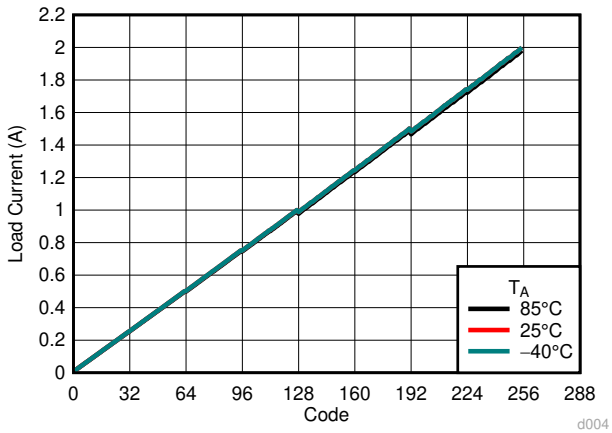
I_{LOAD} = 2 A f_{SW} = 4 MHz

Figure 5-3. Flash Efficiency vs Line Tri-Temp



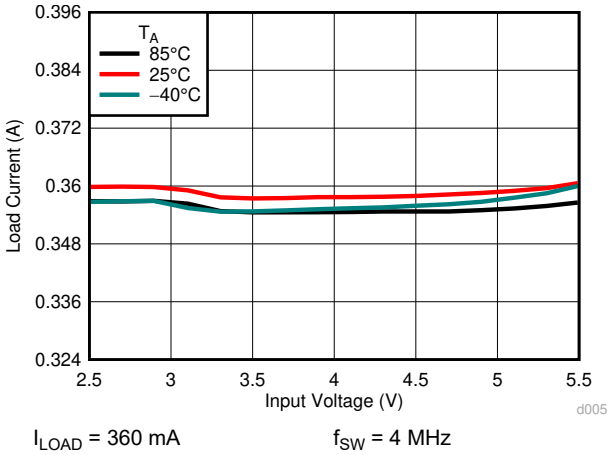
I_{LOAD} = 2 A f_{SW} = 4 MHz

Figure 5-4. Flash Current vs. Input Voltage



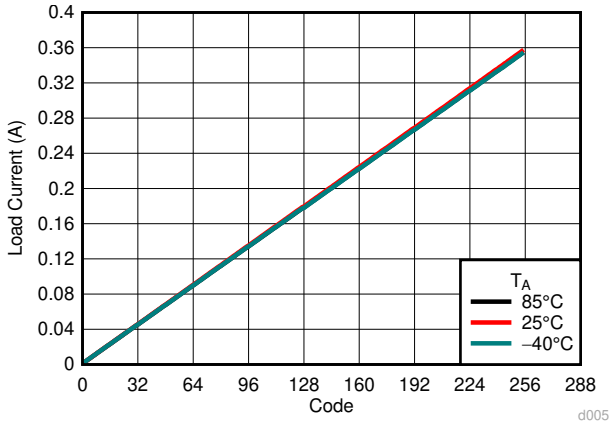
V_{IN} = 3.3 V f_{SW} = 4 MHz

Figure 5-5. Flash Current vs. Code



I_{LOAD} = 360 mA f_{SW} = 4 MHz

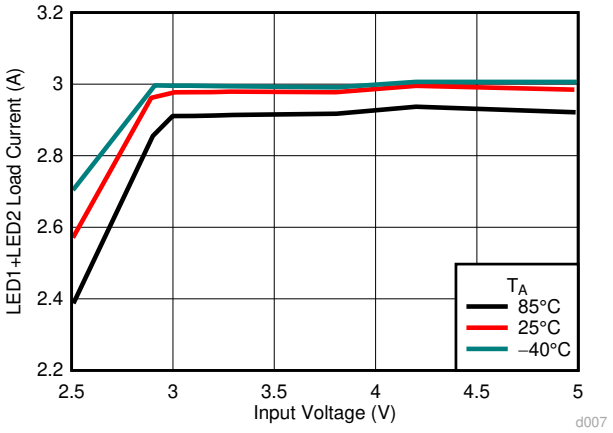
Figure 5-6. Torch Current vs. Input Voltage



V_{IN} = 3.3 V f_{SW} = 4 MHz

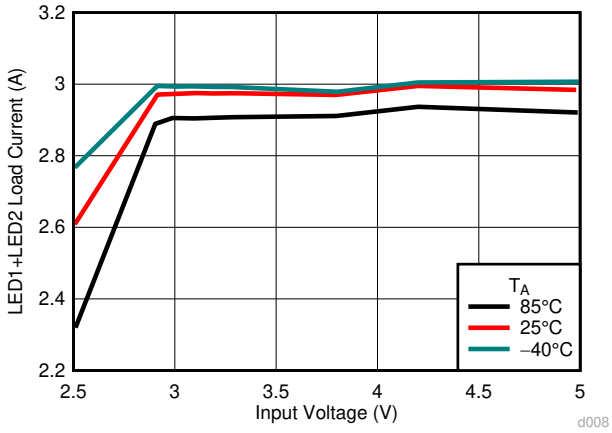
Figure 5-7. Torch Current vs. Code

Copyright © 2026 Texas Instruments Incorporated



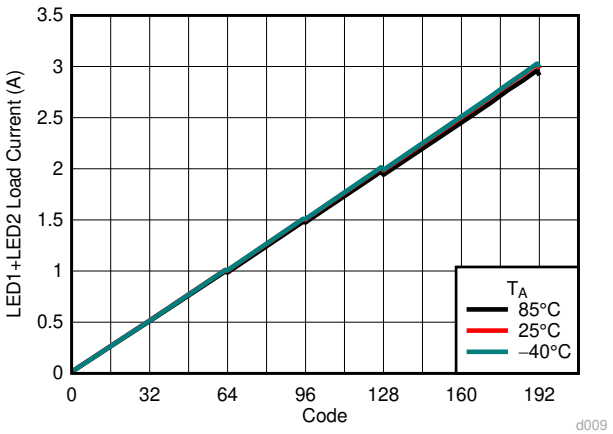
I_{LOAD} = 3 A f_{SW} = 2 MHz
two outputs tied

Figure 5-8. Flash Line Regulation



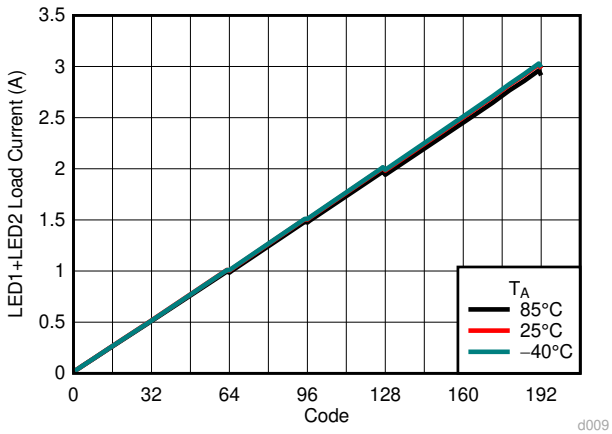
I_{LOAD} = 3 A f_{SW} = 4 MHz
two outputs tied

Figure 5-9. Flash Line Regulation



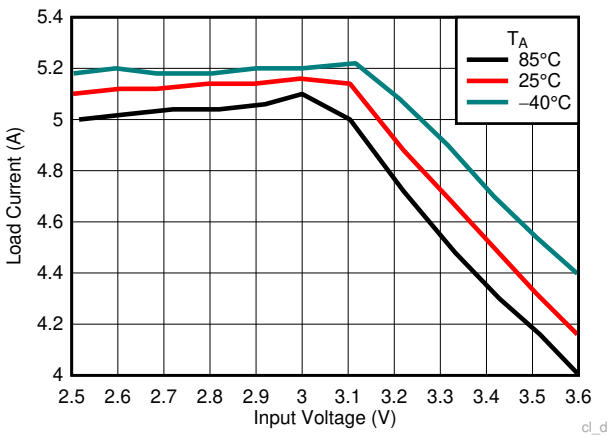
V_{IN} = 3.3 V f_{SW} = 2 MHz
two outputs tied

Figure 5-10. Flash Load Regulation



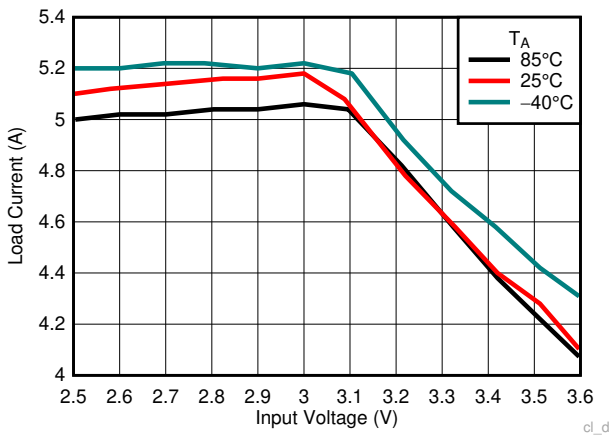
V_{IN} = 3.3 V f_{SW} = 4 MHz
two outputs tied

Figure 5-11. Flash Load Regulation



two outputs tied f_{SW} = 2 MHz

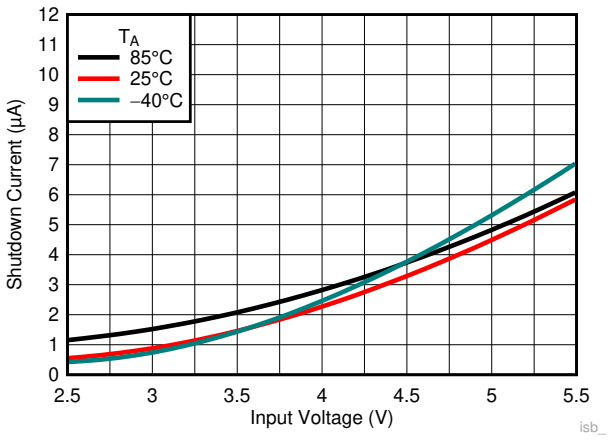
Figure 5-12. Current Limit



two outputs tied f_{SW} = 4 MHz

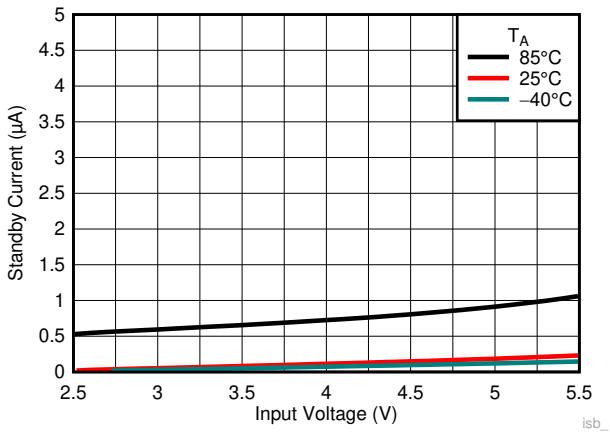
Figure 5-13. Current Limit

Copyright © 2026 Texas Instruments Incorporated



V_{EN} = V_{QC} = 0 V

Figure 5-14. Shutdown Current



V_{EN} = V_{QC} = 1.8 V

Figure 5-15. Standby Current

6 Detailed Description

6.1 Overview

The LM3645 is a high-power white LED flash driver capable of delivering up to 2 A in any of the four parallel LEDs. The device incorporates a 2-MHz or 4-MHz constant frequency-synchronous current-mode PWM boost converter and quad high-side current sources to regulate the LED current over the 2.3-V to 5.5-V input voltage range.

The LM3645 PWM DC/DC boost converter switches and boosts the output to maintain at least V_{HR} across each of the current sources (LED1/2/3/4). This minimum headroom voltage ensures that the current sources remain in regulation. If the input voltage is above the LED voltage + current source headroom voltage the device does not switch, but turns the P-channel MOSFET on continuously (Pass mode). In Pass mode the difference between (V_{IN} − I_{LED} × R_{PMOS}) and the voltage across the LED is dropped across the current source.

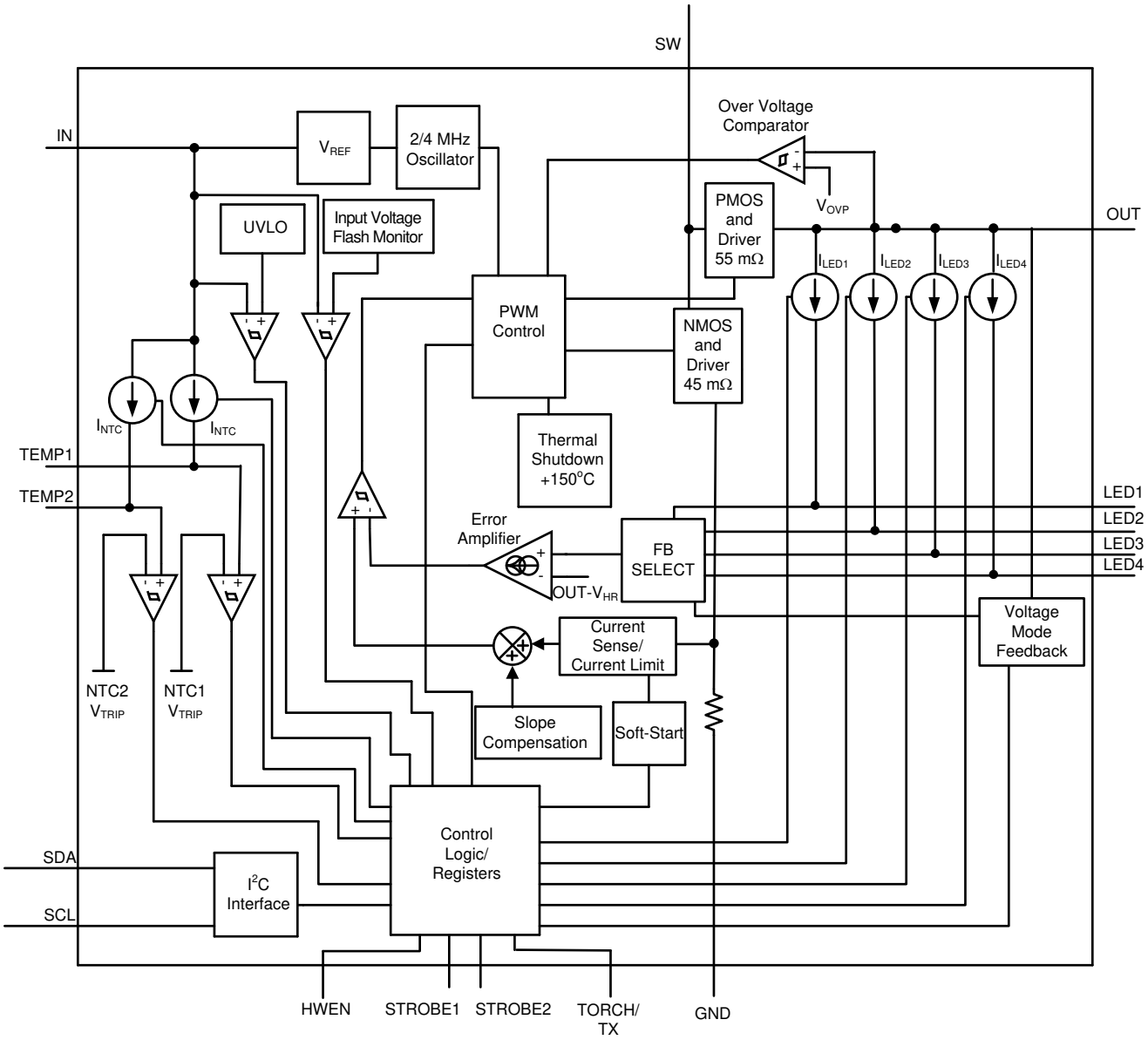
The LM3645 has logic inputs including two hardware Flash Enables (STROBE1 and STROBE2), and a hardware Torch Enable muxed with a Flash Interrupt input (TX) designed to interrupt the flash pulse during high battery-current conditions (TORCH/Tx, Tx = default). These logic inputs have internal 300-kΩ (typical) pulldown resistors to GND.

Additional features of the LM3645 include internal comparators for LED thermal sensing via external NTC thermistors (TEMP1, TEMP2) and an input voltage monitor that can reduce the Flash current during low V_{IN} conditions. It also has a Hardware Enable (EN) pin that can be used to reset the state of the device and the registers by pulling the EN pin to ground.

Control is done via an I^2C-compatible interface. This includes adjustment of the Flash and Torch current levels, changing the Flash Timeout Duration, and changing the switch current limit. Additionally, there are flag and status bits that indicate flash current time-out, LED over-temperature condition, LED failure (open/short), device thermal shutdown, TX interrupt, and V_{IN} undervoltage conditions.

Copyright © 2026 Texas Instruments Incorporated

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Power Amplifier Synchronization (TORCH/TX)

The TORCH/TX pin is either a Power Amplifier Synchronization input, or external torch enable. In Tx mode, this function is designed to reduce the flash LED current and thus limit the battery current during high battery current conditions such as PA transmit events. When the LM3645 is engaged in a Flash event, and the TX pin is pulled high, the LED current is forced into Torch Mode at the programmed Torch current setting. If the TX pin is then pulled low before the Flash pulse terminates, the LED current returns to the previous Flash current level. At the end of the Flash time-out, whether the TX pin is high or low, the LED current turns off. If a Tx event occurs during a flash, a flag will be set in the FLAG_RPT_REG register (bit[5] in reg 0x14).

6.3.2 Input Voltage Flash Monitor (IVFM)

The LM3645 has the ability to adjust the flash current based upon the voltage level present at the IN pin utilizing the Input Voltage Flash Monitor (IVFM). The adjustable threshold IVFM-D (set in register IVFM_THRES) ranges from 2.5 V to 3.25 V in 50-mV steps, with three different usage modes set in the IVFM_THRES register (Stop

Copyright © 2026 Texas Instruments Incorporated

and Hold, Adjust Down Only, Adjust Up/Down). The Voltage Fault Register has the IVFM flag (bit[4] reg 0x15) bit set when the input voltage crosses the IVFM-D value. Additionally, the IVFM-D threshold sets the input voltage boundary that forces the LM3645 to either stop ramping the flash current during start-up (Stop and Hold Mode) or to start decreasing the LED current during the flash (Down Adjust Only and Up/Down Adjust). In Adjust Up/Down mode, the IVFM-D value plus the hysteresis voltage threshold set the input voltage boundary that forces the LM3645 to start ramping the flash current back up towards the target.

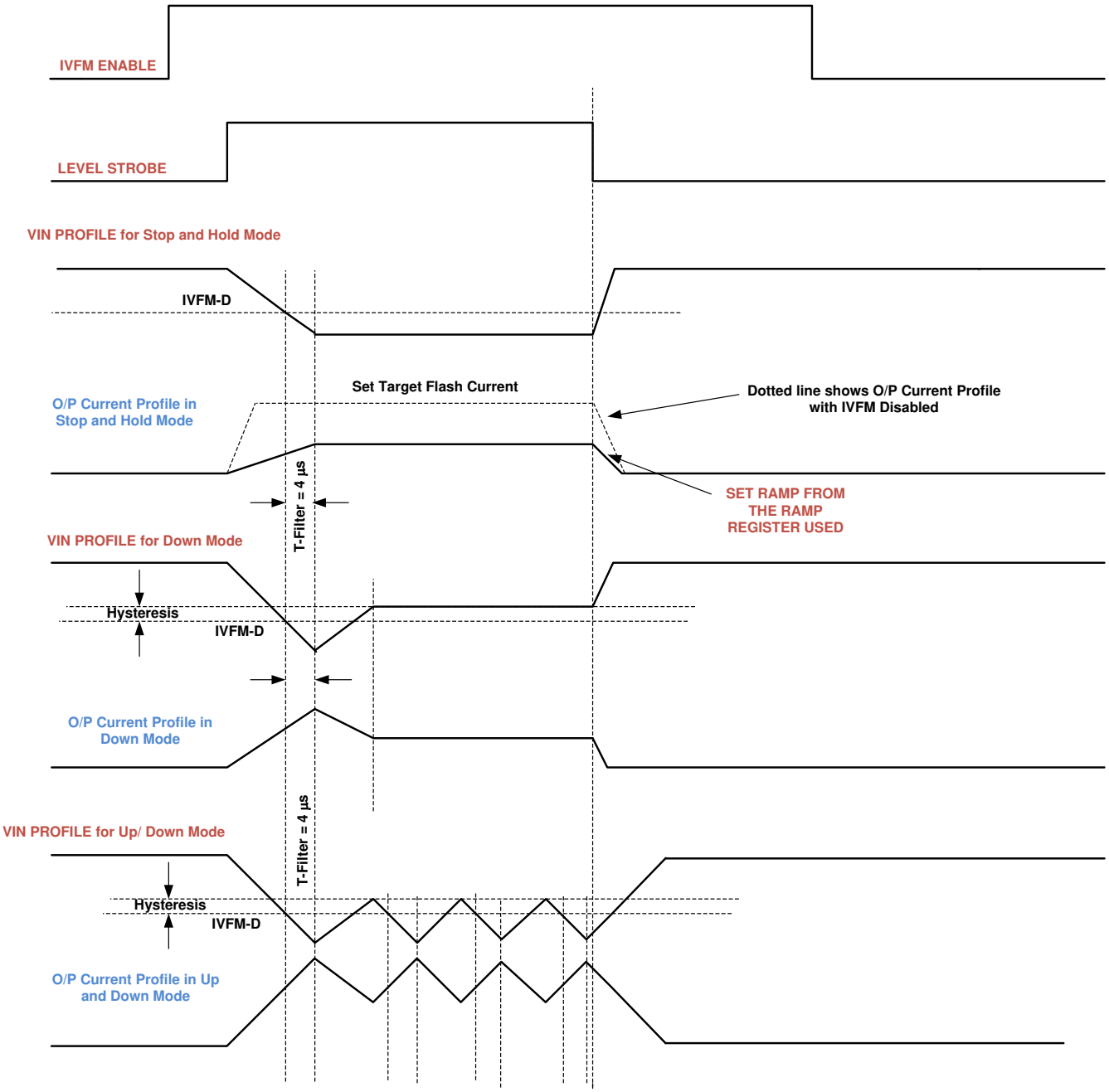


Figure 6-1. IVFM Modes

Copyright © 2026 Texas Instruments Incorporated

6.3.3 Fault/Protections

6.3.3.1 Fault Operation

If the LM3645 enters a fault condition, the device sets the appropriate flag in the Volt_Fault_Reg and Therm_Fault_Reg Registers (0x15 and 0x16), and places the device into standby by clearing the Dx_EN Bits ([3:0]) in CTRL_REG2 (0x01). The LM3645 remains in standby until an I^2C read of the fault registers is completed. Upon clearing the flags/faults, the device can be restarted (Flash, Torch, IR, etc.). If the fault is still present, the LM3645 re-enters the fault state and enters standby again. When a fault flag bit is present in either of the fault registers, the D_MODE register (0x02) becomes read only.

Note

It is recommended that the fault registers be read either before a device enable or after a device disable. Failure to do so can cause inadvertent enabling of the device upon a read of the fault registers if an enable command has been issued prior to clearing any fault flags.

6.3.3.2 Flash Time-Out

The Flash Time-Out period sets the amount of time that the Flash Current is being sourced to the current sources (LED1/2/3/4). The LM3645 has 16 timeout levels (bits [3:0] in reg 0x0A) ranging from 10 ms to 400 ms or from 40 ms to 1.6 s depending upon the time-out multiplier bit ([4] in reg 0x0A). Additionally, there is an option to disable the time-out all together however care must be taken to ensure that the LEDs are not held in a high current condition longer than they are rated for, and care must be taken to ensure LM3645 does not hit the thermal scaleback or thermal shutdown faults. Additionally, changing the time out duration while in a flash event is not recommended as doing so will force the flash duration to be extended.

6.3.3.3 Overvoltage Protection (OVP)

The output voltage is limited to typically 5.7 V. In situations such as an open LED, the LM3645 raises the output voltage in order to try and keep the LED current at its target value. When V_{OUT} reaches 5.7 V (typical) the overvoltage comparator trips and turns off the internal N-channel MOSFET . When V_{OUT} falls below the "**V_{OVP} Off Threshold**", the LM3645 begins switching again. The Dx_EN bits are cleared, and the OVP flag is set (bit[6] in reg 0x15), when an OVP condition is present for three rising OVP edges. This prevents momentary OVP events from forcing the device to shut down.

When operating in voltage mode, the OVP protection mechanism is enabled, however the fault reporting and shut down functions are not enabled.

6.3.3.4 Current Limit

The LM3645 features four selectable inductor current limits that are programmable through the I^2C-compatible interface. When the inductor current limit is reached, the LM3645 terminates the charging phase of the switching cycle. Switching resumes at the start of the next switching period. If the overcurrent condition persists, the device operates continuously in current limit.

Since the current limit is sensed in the NMOS switch, there is no mechanism to limit the current when the device operates in Pass Mode (current does not flow through the NMOS in pass mode). In Boost mode or Pass mode if V_{OUT} falls below 2.3 V, the device stops switching, and the P-channel MOSFET operates as a current source limiting the current to 200 mA. This prevents damage to the LM3645 and excessive current draw from the battery during output short-circuit conditions. The output enable bits are not cleared upon a Current Limit event, but a flag is set (bit [4] in reg 0x14).

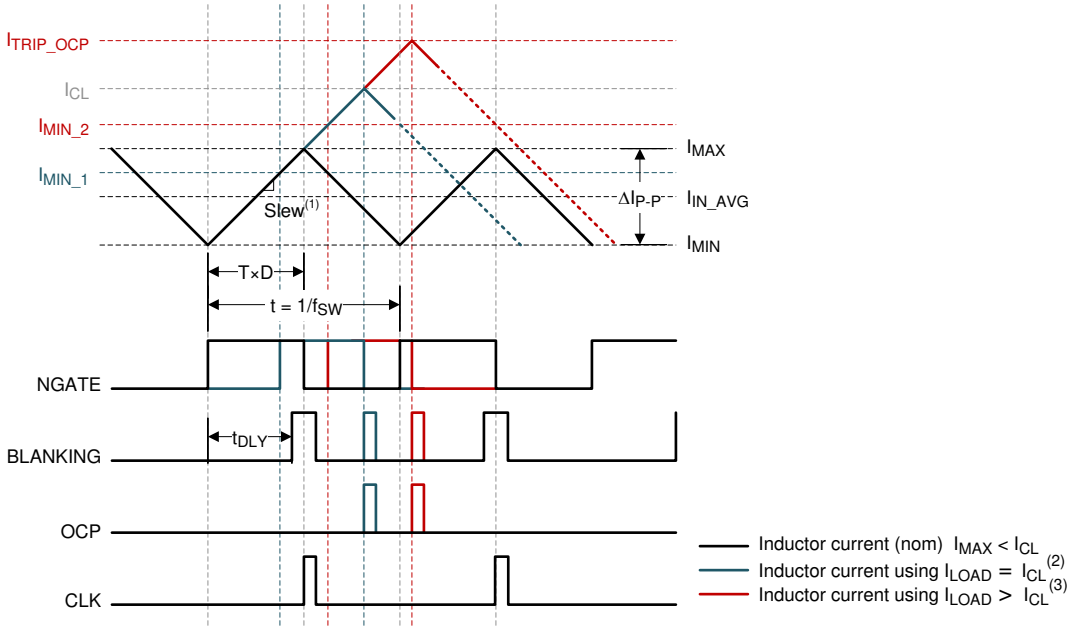
The over current protection (OCP) circuit compares the inductor current to the input current limit (I_{CL}) setting after a fixed blanking time of t_{DLY}. The blanking time ensures that the OCP signal does not false fire as the low-side NMOS of the boost converter turns on. Use Equation 1 to estimate the maximum recommended total LED current to ensure proper current limit level operation accounting for the delay time.

Copyright © 2026 Texas Instruments Incorporated

$$I_{LOAD} \leq \left(I_{CL} + \frac{V_{IN}}{2 \times L} \times \left(\frac{D}{f_{SW}} - 2 \times t_{DLY} \right) \right) \times (1 - D) \times \eta \quad (1)$$

where

- D is the duty cycle
- η is the boost efficiency
- I_{CL} is the current limit setting
- L is the inductance value
- f_{SW} is the boost switching frequency



(See Equation 2)
(See Equation 1)

Figure 6-2. Current Limit Timing

$$Slew = \frac{\Delta I_{P-P}}{D \times T} \quad (2)$$

6.3.3.5 NTC Thermistor Input/Outputs (TEMP1, TEMP2)

The TEMP1 and TEMP2 pins serve as a threshold detector and bias source for negative temperature coefficient (NTC) thermistors. When the voltage at TEMPx goes below the programmed threshold, the LM3645 device transitions into one of these three modes:

- Force standby mode
- Force torch mode
- Report only mode (bits [5:2] in reg 0x0D)

The device allows adjustment of the NTC threshold voltage from 250 mV to 1 V in 50 mV steps (bits [7:0] in reg 0x0F). Additionally, the NTC1 and NTC2 voltage levels provide an indicator of the remotely sensed temperature. The NTC bias current is adjustable in 25 µA steps from 25 µA to 100 µA (bits [7:6] in reg 0x0D). The NTC1

Copyright © 2026 Texas Instruments Incorporated

and NTC2 detection circuitry can be enabled or disabled via the NTC_MODE Register (bits [1:0] in reg 0x0D). If enabled, the NTC block turns on and off during the start and stop of a Flash/Torch/IR event.

Additionally, the NTC input looks for an open NTC connection and a shorted NTC connection. If the NTC input falls below 100 mV, the NTC short flag is set, and the device is disabled (bits [7:6] in reg 0x16). If the NTC input rises above 2.0 V, the NTC Open flag is set, and the device is disabled (bits [5:4] in reg 0x16). These fault detections can be individually disabled or enabled via the NTC Open Fault Enable bit (bits [2] in reg 0x13) and the NTC Short Fault Enable bit (bit [0] in reg 0x13).

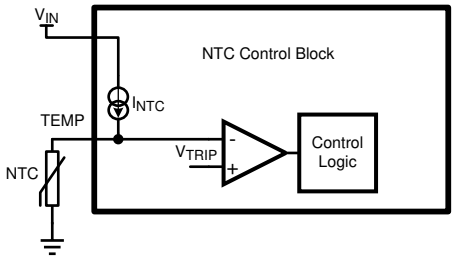


Figure 6-3. Temp Detection Diagram

To further extend the functionality of the NTC inputs, the voltage on both TEMP1 and TEMP2 can be read back to provide real time feedback regarding the temperature at the point of detection (bits [7:0] in reg 0x10). When either TEMP1 or TEMP2 pin is enabled, a 4-bit ADC is enabled and continually updates the NTC Voltage Register. The voltage on both TEMP1 and TEMP2 are measured if either NTC detection block is enabled. In this case, the data read into the NTC voltage register for the disabled TEMP detection block can be random and can be ignored. Only enabled TEMP blocks yield accurate readings.

Each NTC block can be associated with any of the four outputs. **Each Dx Output should only be assigned to one of the NTC detection blocks.**

Copyright © 2026 Texas Instruments Incorporated

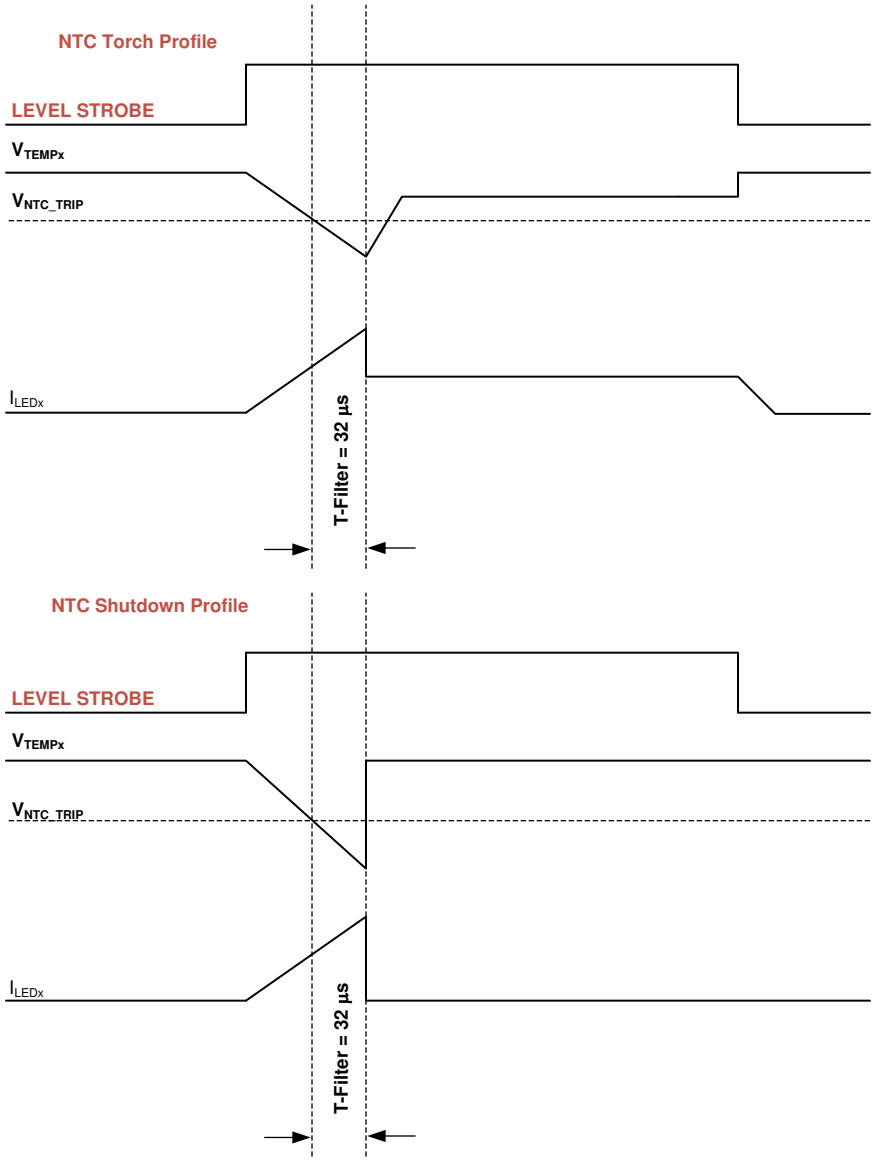


Figure 6-4. NTC Detection Diagram

6.3.3.6 Thermal Scale Back

In the event that the LM3645 junction temperature reaches 125°C, the device will adjust the LED current in one of two different ways; turn off the current completely or force the current to a torch level (bits [5:4] in reg 0x13). The thermal scale back feature can be enabled or disabled as well (bit [3] in reg 0x13). The torch scale back mode is valid for flash mode and IR mode only. If the torch scaleback mode is used in torch mode, no action will occur. The force standby mode option is valid in all modes.

Copyright © 2026 Texas Instruments Incorporated

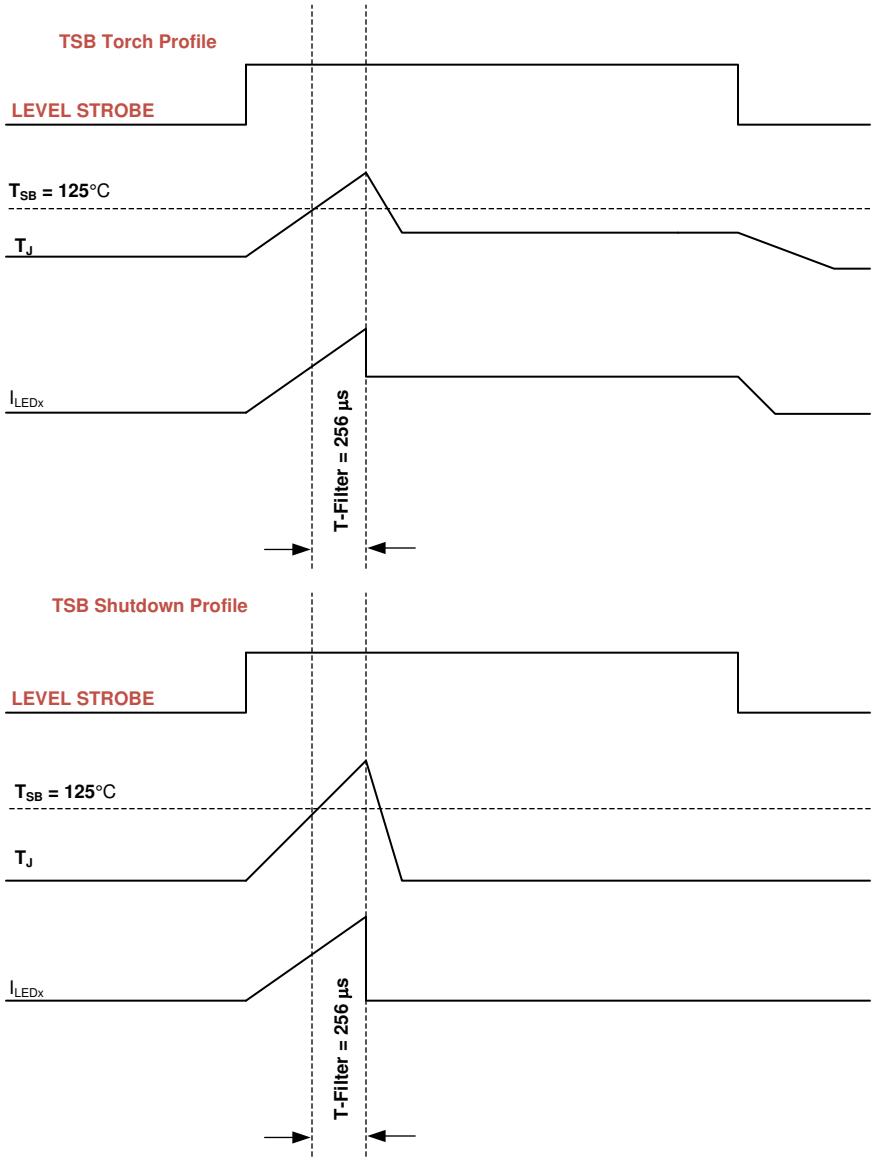


Figure 6-5. TSB Adjust Modes

6.3.3.7 Thermal Shutdown (TSD)

When the LM3645 die temperature reaches 150°C, the thermal shutdown detection circuit trips, forcing the LM3645 into standby and writing a '1' to the corresponding bit of the Thermal Fault Report Register (bit [0] in reg 0x16). The LM3645 is only allowed to restart after the Thermal Fault Report Register (0x17) is read, clearing the fault flag. Upon restart, if the die temperature is still above 150°C, the LM3645 resets the Fault flag and re-enters standby.

6.3.3.8 Undervoltage Lockout (UVLO)

The LM3645 has an internal comparator that monitors the voltage at IN and forces the LM3645 into standby if the input voltage drops to 2.2 V. If the UVLO monitor threshold is tripped, the UVLO flag bit is set in the VOLT_FAULT Register (bit [7] in reg 0x15). If the input voltage rises above 2.2 V, LM3645 is not available for operation until there is an I^2C read of the VOLT_FAULT_REG Register (0x15). Upon a read, the Flags1 register is cleared, and normal operation can resume if the input voltage is greater than 2.3 V.

Copyright © 2026 Texas Instruments Incorporated

6.3.3.9 LED and/or VOUT Short Fault

The LED Fault flags read back a '1' if the device is active in Flash, IR or Torch mode and either active LED output experiences a short condition. The Output Short Fault flags (bits [3:0] in reg 0x15) reads back a '1' if the device is active in Flash, Torch or IR mode and the boost output experiences a short condition. An LED short condition is determined if the voltage at LED1, LED2, LED3 or LED4 goes below 500 mV (typ.) while the device is in Torch or Flash mode. Only the output detecting a short will be shutdown. There is a deglitch time of 256 µs before the LED Short flag is valid and a deglitch time of 2.048 ms before the VOUT Short flag (bit[6] in reg 0x15) is valid. The LED Short Faults can be reset to '0' by removing power to the input pin , setting EN to '0', setting the SW RESET bit to a '1', or by reading back the Voltage Fault Register (0x15). The Dx_EN bits are cleared upon an LED and/or V_{OUT} short fault.

6.3.3.10 Fault Behavior Table

Each fault has a specific interaction behavior with the output enable control (Dx_EN bits). Some faults are global in nature while others are specific to a certain output or function.

Table 6-1. Fault Behavior Table

Fault	Dx_EN Clear?	VM_EN Clear?
FTO1	D1_EN	No Clear
FTO2	D2_EN	No Clear
FTO3	D3_EN	No Clear
FTO4	D4_EN	No Clear
ICL	No Clear	No Clear
TX	No Clear	No Clear
LED1_Short	D1_EN	No Clear
LED2_Short	D2_EN	No Clear
LED3_Short	D3_EN	No Clear
LED4_Short	D4_EN	No Clear
IVFM_TRIP	No Clear	No Clear
OUT_SHORT	All Dx_EN	Yes
OVP	All Dx_EN	Yes
UVLO	All Dx_EN	Yes
TSD	All Dx_EN	Yes
TSB	All Dx_EN if shutdown mode	Yes is if assigned to shutdown mode
NTC1_TRIP	NTC1 Assigned Dx_EN if shutdown mode	No Clear
NTC2_TRIP	NTC2 Assigned Dx_EN if shutdown mode	No Clear
NTC1_OPEN	Clear if NTC1 Assigned Dx_EN	No Clear
NTC2_OPEN	Clear if NTC2 Assigned Dx_EN	No Clear
NTC1_SHORT	Clear if NTC1 Assigned Dx_EN	No Clear
NTC2_SHORT	Clear if NTC2 Assigned Dx_EN	No Clear

6.4 Device Functioning Modes

6.4.1 Flash Mode

In Flash Mode, the LED current sources (LED1/2/3/4) provide 256 target current levels from 7.325 mA to 2 A. Once the Flash sequence is activated the current source (LED) ramps up to the programmed Flash current by stepping through all current steps until the programmed current is reached. The headroom in the four current sources can be regulated to provide 7.325 mA to 2 A on each of the four output legs.

When the device is enabled in Flash Mode through the DMODE Register (reg 0x02) and Dx_EN bits in Control Register 2 (bits [3:0] in reg 0x01), all Dx_EN bits cleared after a flash time-out event. If a flash event is initiated

Copyright © 2026 Texas Instruments Incorporated

by a strobe pin, the Dx_EN bits do not clear at the end of the pulse unless a fault or timeout occurs allowing multiple flash pulses to occur without further I2C interaction.

6.4.2 Torch Mode

In Torch mode, the LED current sources (LED1/2/3/4) provide 256 target current levels from 0.525 mA to 360 mA. The Torch currents are adjusted via the Dx Torch Brightness Registers. Torch mode is activated by the Enable Register (setting Dx_MODE, bits to '10'), or by pulling the TORCH/TX pin HIGH when the pin is enabled (Control Register2) and set to Torch Mode. Once the TORCH sequence is activated the active current sources (LED1/2/3/4) ramps up to the programmed Torch current by stepping through all current steps until the programmed current is reached. The rate at which the current ramps is determined by the value chosen in the Torch_Ramp register.

Torch Mode is not affected by Flash Timeout or by a TX Interrupt event.

6.4.3 IR Mode

In IR Mode, the target LED current is equal to the value stored in the LED1/2/3/4 Flash Brightness Registers. When IR mode is enabled on any of the outputs, the boost converter turns on and set the output equal to the input (pass-mode) or to the selected voltage mode depending upon the state of the voltage mode settings. At this point, toggling the STROBE pins enables and disables the LED1/2/3/4 current sources (if enabled via the Dx Mode bits). The strobe pins can only be set to be Level sensitive, meaning all timing of the IR pulse is externally controlled. If the strobe pin is set to edge mode, the LM3645 device times out after the end of the set duration. In IR Mode, the current sources either ramp quickly or do not ramp the LED outputs to the target based upon the ramp time setting chosen.

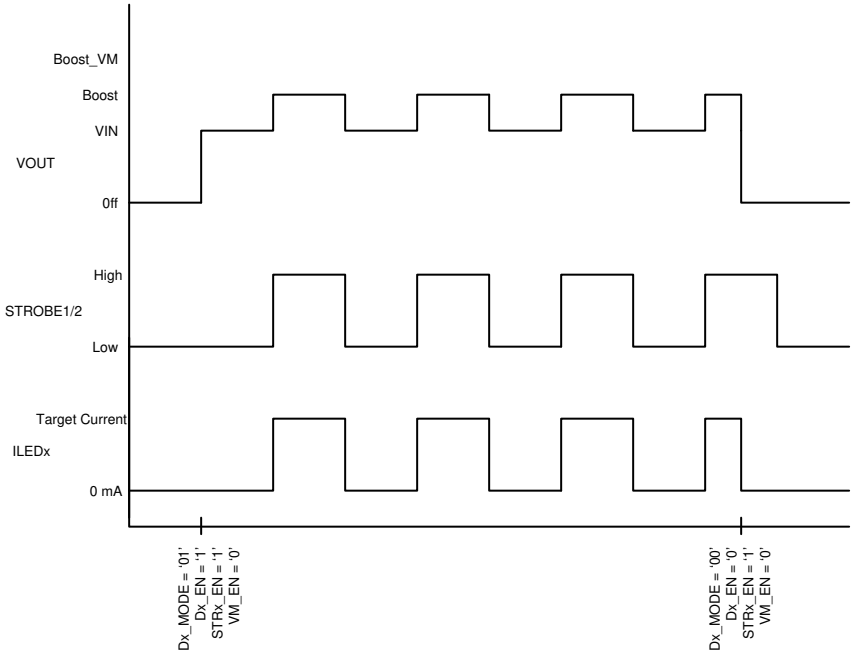


Figure 6-6. IR Mode with Boost

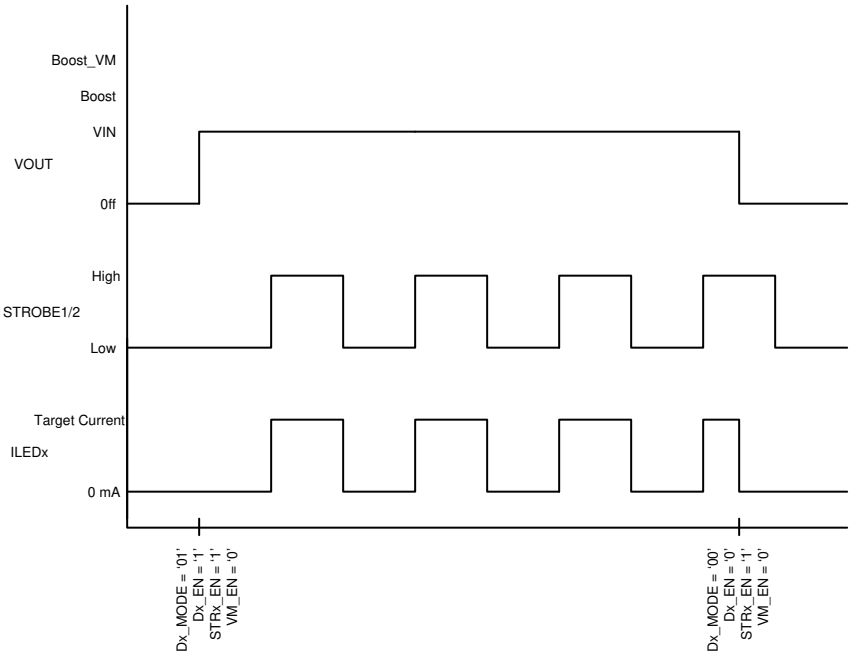


Figure 6-7. IR Mode Pass Only

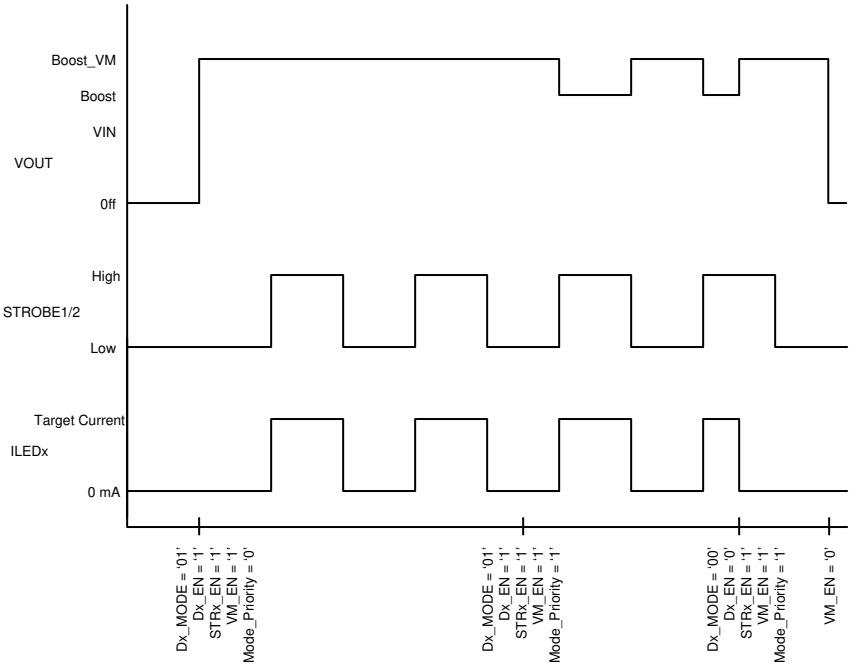


Figure 6-8. IR Mode Voltage Mode Enabled

6.4.4 Voltage Mode

LM3645 has the ability to turn the DC/DC boost converter typically used to power the four LED outputs into a general purpose fixed output power rail (bit [0] in reg 0x00) for use in other system applications that need voltage conversion. Four user selectable regulation voltage levels can be generated; 4.0 V, 4.5 V, 5.0V and 5.2 V (bits [7:6] in register 0x00). Voltage Mode can be used in conjunction with driving LEDs and will behave based upon the Output Mode Priority Bit (bit [1] in reg 0x00). If the bit is set to '0', maintaining voltage regulation is of highest importance. In Voltage Mode priority mode, care must be taken to manage the on chip thermal dissipation. If the

Copyright © 2026 Texas Instruments Incorporated

bit is set to '1', the boost is allowed to regulate to a level that is optimized for driving the enabled LEDs. In LED drive priority mode, the output voltage returns to the target voltage mode level at the termination of LED driving.

In voltage mode, there are current limitations for each mode due to the peak switch node voltage. Using a 1-Ω resistor and 4-nF capacitance for the snubber, the maximum allowed currents are as follows:

- 4.0 V mode = 3 A peak current
- 4.5 V mode = 1.5 A peak current
- 5.0 V mode = 750 mA peak current
- 5.2 V mode = Not recommended

6.4.5 Mode Transitions

The LM3645 can immediately transition between modes, it is best practice to transition from mode to mode by first entering standby. Implementing a standby period minimizes input current and output voltage transients, and provides an overall resetting of all timers and state machines. Additionally, all external control pins should be at '0' during the standby state to ensure proper timing and synchronization.

6.4.6 Boost Operation

6.4.6.1 Start-Up (Enabling The Device)

Turn on of the LM3645 modes can be done through a combination of Control Register1, Control Register2, D_Mode Register and Strobe Control Register depending upon which mode is enabled. On start-up, when V_{OUT} is less than V_{IN} the internal synchronous P-channel MOSFET turns on as a current source and delivers 200 mA (typical) to the output capacitor. During this time the current source (LED) is off. When the voltage across the output capacitor reaches 2.2 V (typical) the current source turns on. At turnon the current source steps through each FLASH or TORCH level until the target LED current is reached unless voltage mode is enabled with the LED outputs disabled. This gives the device a controlled turnon and limits inrush current from the V_{IN} supply.

6.4.6.2 Pass Mode

The LM3645 starts up in Pass Mode and stays there until Boost Mode is needed to maintain regulation. If the voltage difference between V_{OUT} and V_{LED} falls below V_{HR}, the device switches to Boost Mode. In Pass Mode the boost converter does not switch, and the synchronous P-channel MOSFET turns fully on bringing V_{OUT} up to $V_{IN} - I_{LED} \times R_{PMOS}$. In Pass Mode the inductor current is not limited by the peak current limit.

6.4.6.3 Output Voltage Regulation

In LED drive mode, the LM3645 boost will either operate in pass mode if the output voltage minus the LED voltage is greater than the target current source headroom voltage. If the output can no longer operate in pass mode, the DC/DC boost will turn on and constantly monitor all enabled outputs and ensure that the output with the highest forward voltage LED always has the correct headroom voltage.

In Voltage drive mode, the output is always regulated to the target value so long as the output voltage is less than the input voltage. If the input voltage is higher than the output voltage, the device will not be regulated and will instead operate in pass mode.

Table 6-2. Output Voltage Assignment Table

Voltage Mode EN	Output Mode Priority	LED Current On	IR Mode Enabled	Output Level
0	X	0	0	Disabled
0	X	0	1	Pre-Charge Mode ($V_{OUT} = V_{IN}$)
0	X	1	X	$V_{OUT} = V_{LED} + V_{HR}$. Highest enabled LED sets output voltage
1	0	X	X	Output set to regulated voltage specified in voltage mode voltage bits
1	1	0	X	Output set to regulated voltage specified in voltage mode voltage bits
1	1	1	X	$V_{OUT} = V_{LED} + V_{HR}$. Highest enabled LED sets output voltage

Copyright © 2026 Texas Instruments Incorporated

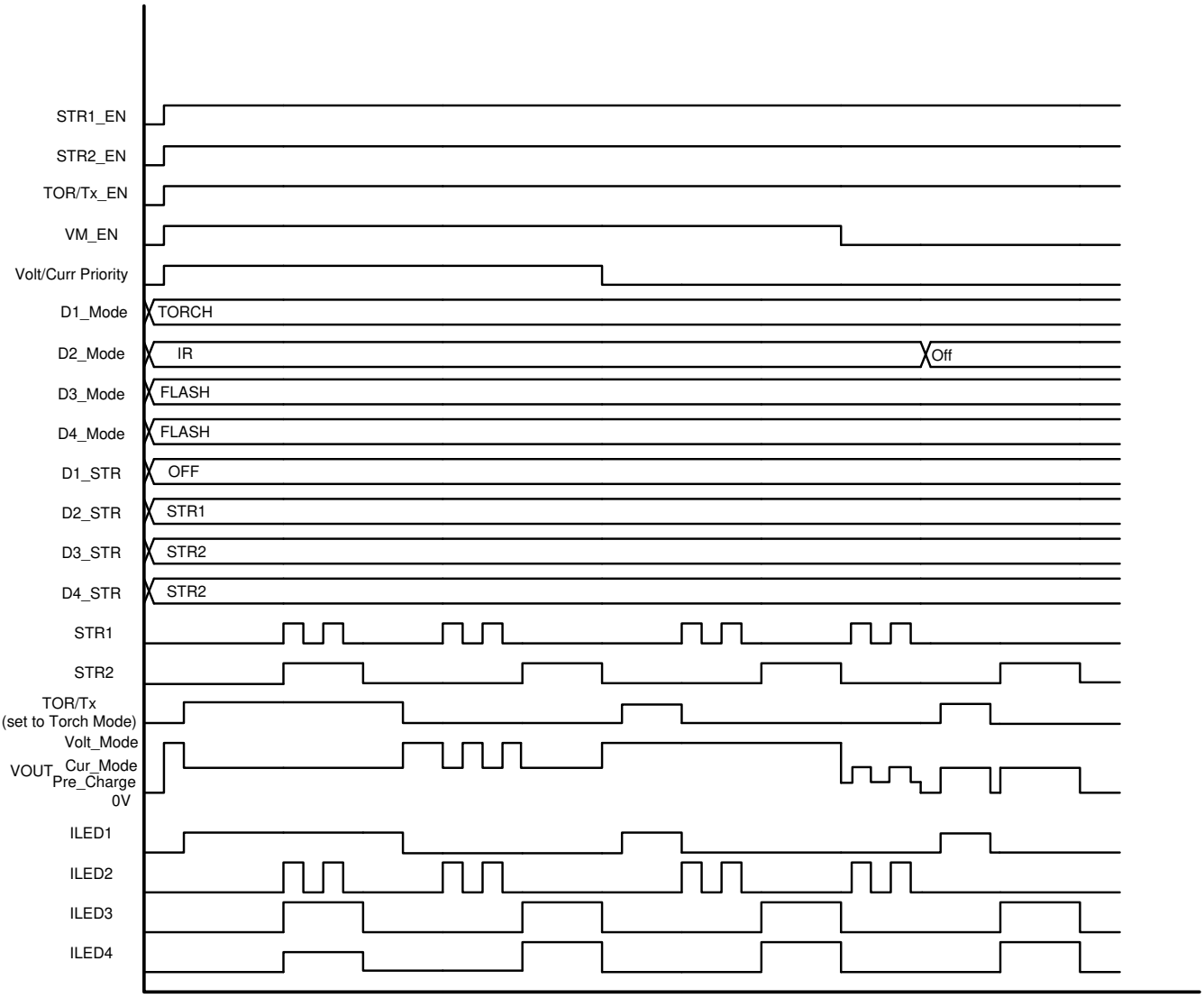


Figure 6-9. Output Voltage and Mode Diagram

6.5 Programming and Control

6.5.1 Dx_EN Bits

In order for current to flow in the LEDs, the appropriate Dx_EN bits in Configuration Register 2 must be set to logic '1' (bits [3:0) in reg 0x01). When enabled, the Dx outputs will behave based upon the mode that pin is set to (DMODE register). If the Dx_EN bit is set to a '0', the output will remain off regardless of the mode the output is placed in. At the end of an I2C controlled flash event when a time-out occurs, the Dx_EN bits will auto-clear. If the mode is changed during an I2C controlled flash, the Dx_EN bit will not autoclear. When used along with the strobe pins, the Dx_EN pins do not automatically reset unless a fault event occurs.

6.5.2 STR1 and STR2 Usage

Two external synchronization Strobe pins are available to enable the four LED outputs in either Flash or IR mode. Each of the four outputs can be assigned to either Strobe pin via the Strobe Control Register (bits [7:0] in reg 0x03). Each output assigned to a strobe pin must be set to the same LED mode, either all Flash or all IR. **Additionally, no output should be assigned to both strobe pins.** If D1 is assigned to STR1, it should not be assigned to STR2 as well.

Copyright © 2026 Texas Instruments Incorporated

If the LM3645 is already enabled, the minimum strobe duration in either level or edge mode must be 10 µs. This restriction applies to both flash and IR mode operation. If the LM3645 is in standby and either strobe pin is asserted, it is recommended that the strobe duration be no less than 1ms to ensure that the boost has enough time to reach the proper level to ensure current into the LED can regulate.

Note

It is recommended that the STR1 and STR2 pins be held low before enabling the outputs assigned to each strobe pin.

Table 6-3. Strobe Control Truth Table

STRx EN	STRx Pin	Dx Mode	Action
X	X	Off	Off
0	X	IR	IR PreCharge Mode, I2C
0	X	Flash	Flash, I2C
1	0	IR	IR PreCharge Mode, I2C
1	1	IR	IR Current Pulse Mode, Strobe Controlled
1	0	Flash	Off
1	1	Flash	Flash, Strobe Controlled

6.5.3 TOR/TX Usage

When the TOR/TX pin is configured for use as a hardware controlled torch enable (bits [7:6] in reg 0x01), all outputs assigned to Torch Mode in the Diode Mode Register (bits [7:0] in reg 0x02) will be enabled or disabled via the external pin.

Note

If configured to the Torch configuration, it is recommended that the TOR/TX pin be held low before enabling the outputs assigned to Torch Mode.

Table 6-4. Torch Control Truth Table

TOR EN	TOR/TX Mode	TOR PIN	Dx Mode	Action
0	X	0	Off	Off
0	X	X	Torch	Torch, I2C Controlled
1	0	X	Torch	Torch, I2C Controlled
1	1	0	Torch	Off
1	1	1	Torch	Externally Enabled Torch Mode

Copyright © 2026 Texas Instruments Incorporated

6.5.4 Control State Diagram

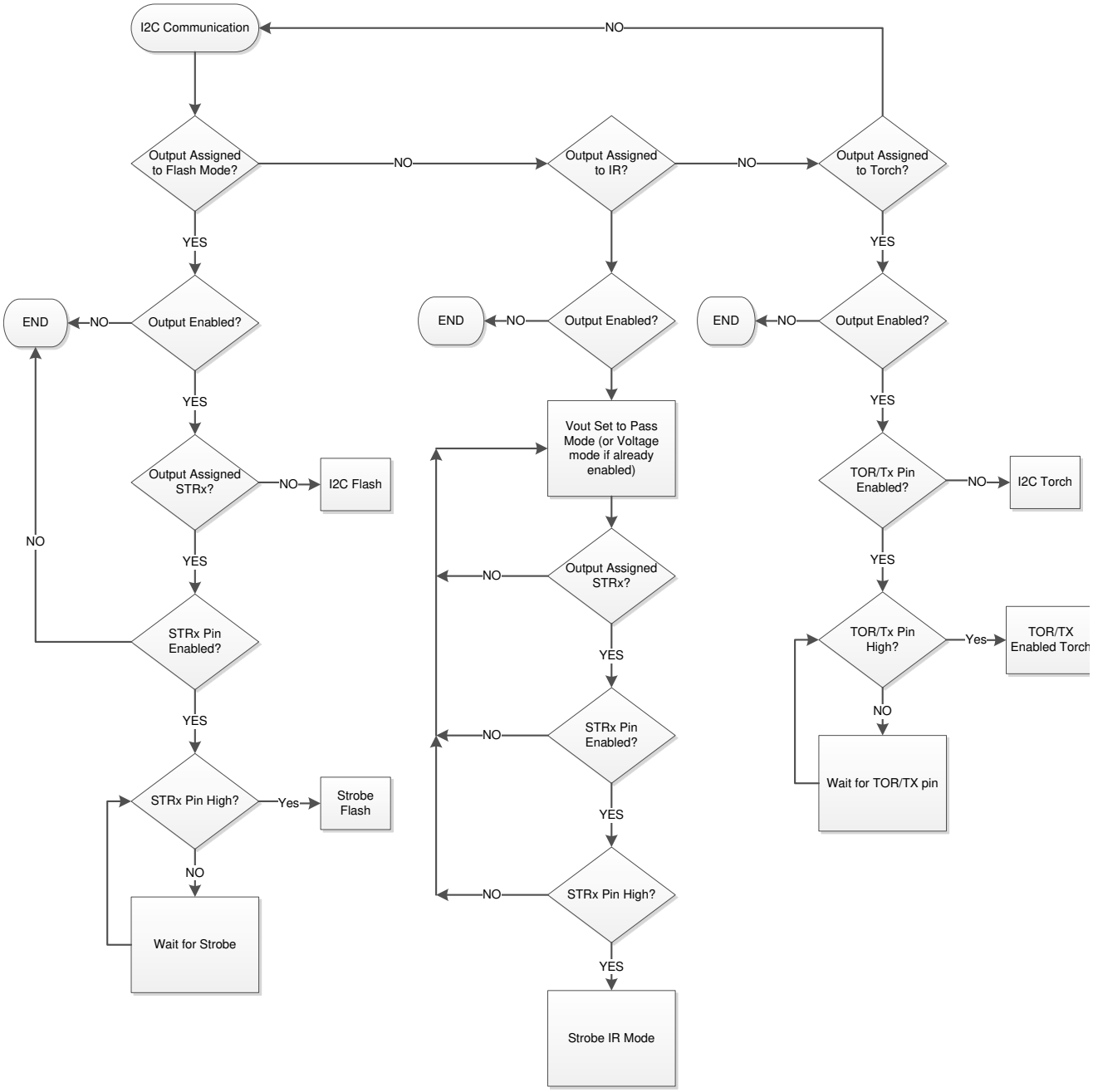


Figure 6-10. Mode Control Diagram

Copyright © 2026 Texas Instruments Incorporated

6.5.5 I²C-Compatible Interface

6.5.5.1 Data Validity

The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when SCL is LOW.

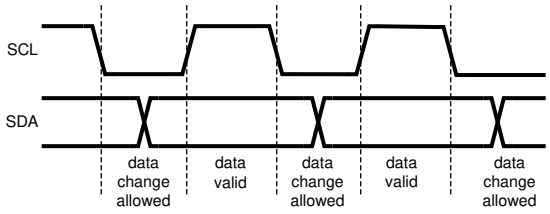


Figure 6-11. Data Validity Data

A pullup resistor between the controller's VIO line and SDA must be greater than [**(VIO - V_{OL}) / 3 mA**] to meet the V_{OL} requirement on SDA. Using a larger pullup resistor results in lower switching current with slower edges, while using a smaller pullup results in higher switching currents with faster edges.

6.5.5.2 Start and Stop Conditions

START and STOP conditions classify the beginning and the end of the I²C session. A START condition is defined as the SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP conditions. The I²C bus is considered busy after a START condition and free after a STOP condition. During data transmission, the I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

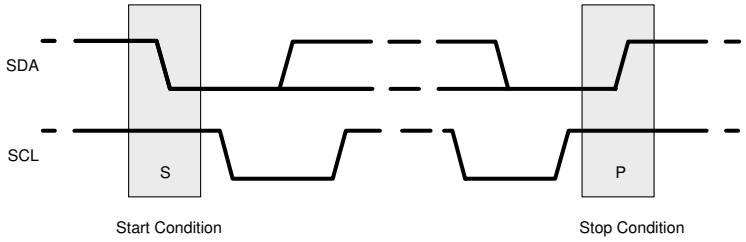


Figure 6-12. Start and Stop Conditions

6.5.5.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LM3645 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LM3645 generates an acknowledge after each byte is received. There is no acknowledge created after data is read from the device.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM3645 7-bit address is 0x65. For the eighth bit, a '0' indicates a WRITE and a '1' indicates a READ. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register.

Copyright © 2026 Texas Instruments Incorporated

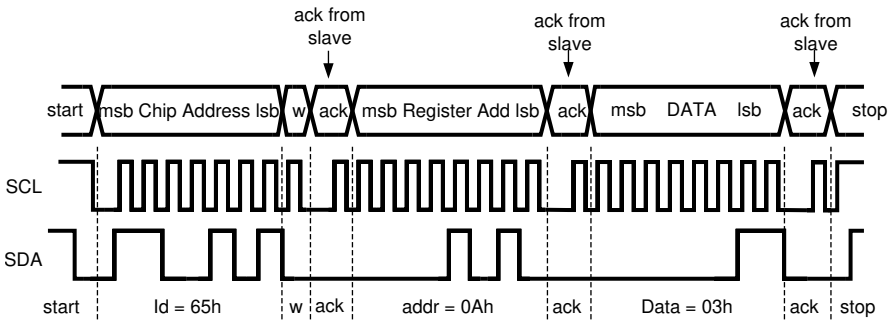


Figure 6-13. Write Cycle W = Write (SDA = "0") R = Read (SDA = "1") Ack = Acknowledge (SDA Pulled Down by Either Master or Slave) ID = Chip Address, 65h for LM3645

6.5.5.4 I²C-Compatible Chip Address

The device address for the LM3645 is 1100101 (0x65). After the START condition, the I²C-compatible master sends the 7-bit address followed by an eighth read or write bit (R/W). R/W = 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the device address selects the register address to which the data is written. The third byte contains the data for the selected register.

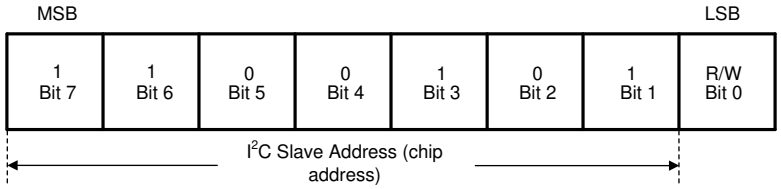


Figure 6-14. I²C-Compatible Chip Address

6.6 Register Descriptions

Copyright © 2026 Texas Instruments Incorporated

6.6.1 MainReg Registers

Table 6-5 lists the memory-mapped registers for the MainReg registers. All register offset addresses not listed in Table 6-5 should be considered as reserved locations and the register contents should not be modified.

Table 6-5. MAINREG Registers

Address	Acronym	Register Name	Section
0x0	CTRL_REG1	Control Register 1	Go
0x1	CTRL_REG2	Control Register 2	Go
0x2	D_MODE_REG	Diode Mode Register	Go
0x3	STR_CTRL_REG	Strobe Control Register	Go
0x4	STR_TIME_REG	Strobe Timing Register	Go
0x5	D1_FLASH_REG	D1 Flash Current Register	Go
0x6	D2_FLASH_REG	D2 Flash Current Register	Go
0x7	D3_FLASH_REG	D3 Flash Current Register	Go
0x8	D4_FLASH_REG	D4 Flash Current Register	Go
0x9	D1_TORCH_REG	D1 Torch Current Register	Go
0xA	D2_TORCH_REG	D2 Torch Current Register	Go
0xB	D3_TORCH_REG	D3 Torch Current Register	Go
0xC	D4_TORCH_REG	D4 Torch Current Register	Go
0xD	NTC_MODE_REG	NTC Control Register	Go
0xE	NTC_ASSIGN_REG	NTC Assignment Register	Go
0xF	NTC_VOLT_REG	NTC Voltage Register	Go
0x10	NTC_READ_REG	NTC Read Register	Go
0x11	IVFM_SET_REG	Input Voltage Monitor Register	Go
0x12	CUR_RAMP_REG	Current Ramp Register	Go
0x13	FAULT_CTRL_REG	Fault Control Register	Go
0x14	FLAG_RPT_REG	Flag Report Register	Go
0x15	VOLT_FAULT_REG	Voltage Fault Report Register	Go
0x16	THERM_FAULT_REG	Thermal Fault Report Register	Go
0x17	LAST_CUR_REG1	Last Adjusted Current Register D1	Go
0x18	LAST_CUR_REG2	Last Adjusted Current Register D2	Go
0x19	LAST_CUR_REG3	Last Adjusted Current Register D3	Go
0x1A	LAST_CUR_REG4	Last Adjusted Current Register D4	Go
0x1B	DEV_INFO_REG	Device Info Register	Go

Complex bit access types are encoded to fit into small table cells. Table 6-6 shows the codes that are used for access types in this section.

Table 6-6. MainReg Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

Copyright © 2026 Texas Instruments Incorporated

6.6.1.1 CTRL_REG1 Register (Address = 0x0) [reset = 0x80]

CTRL_REG1 is shown in Figure 6-15 and described in Table 6-7.

Return to Summary Table.

The CTRL_REG1 register handles control when operating in voltage output mode and configures the parameters associated with the DC/DC boost converter

Figure 6-15. CTRL_REG1 Register

7	6	5	4	3	2	1	0
VM_Voltage		Freq_Select	Curr_Lim		Boost_Mode	Mode_Priority	VM_EN
R/W-2b10		R/W-1b0	R/W-2b00		R/W-1b0	R/W-1b0	R/W-1b0

Table 6-7. CTRL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VM_Voltage	R/W	2b10	Voltage Mode Value 2b00 = 4.0 V 2b01 = 4.5 V. Max. Output Current = 1.5A 2b10 = 5.0 V. Max. Output Current = 0.75A 2b11 = 5.2 V. Not recommended
5	Freq_Select	R/W	1b0	Sets the DC/DC Switching Frequency 1b0 = 2 MHz 1b1 = 4 MHz
4-3	Curr_Lim	R/W	2b00	Inductor Current Limit 2b00 = 2 A 2b01 = 3 A 2b10 = 4 A 2b11 = 5 A
2	Boost_Mode	R/W	1b0	Boost Mode 1b0 = Automatic 1b1 = Force Pass
1	Mode_Priority	R/W	1b0	Output Mode Priority Enable 1b0 = Voltage Mode Priority 1b1 = LED Drive Priority
0	VM_EN	R/W	1b0	Voltage Mode Enable 1b0 = Disabled 1b1 = Enabled

Copyright © 2026 Texas Instruments Incorporated

6.6.1.2 CTRL_REG2 Register (Address = 0x1) [reset = 0x0]

CTRL_REG2 is shown in Figure 6-16 and described in Table 6-8.

Return to Summary Table.

CTRL_REG2 configures the input and output pins. The Dx_EN bits determine whether or not to enable the Dx current sources, while the upper four bits enable and disable the Strobe1, Strobe2 and Tor/Tx pins. When the Dx_EN bits are set to a '1' and the enabled outputs are assigned to either strobe pin or the tor/tx pin, the LEDs will remain off until the externally control pins are set to a '1'. If an Dx_EN bit is set to a '1' and that output is not assigned to an external control pin, the device will begin the turn on sequence assigned to that output. When used in conjunciton with the external control pins, the Dx_EN pins will remain set to a '1' (if enabled) until a fault or a time-out occurs. If the external control pins are not used and a fault or time-out occurs, the device will automatically clear the Dx_EN bit of the offending output.

Figure 6-16. CTRL_REG2 Register

7	6	5	4	3	2	1	0
TOR/TX_Mode	TOR/TX_EN	STR2_EN	STR1_EN	D4_EN	D3_EN	D2_EN	D1_EN
R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0

Table 6-8. CTRL_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TOR/TX_Mode	R/W	1b0	Torch or Tx Mode Select 1b0 = Tx Mode 1b1 = Torch Mode
6	TOR/TX_EN	R/W	1b0	Tor/Tx Pin Enable 1b0 = Disabled 1b1 = Enabled
5	STR2_EN	R/W	1b0	Strobe2 Enable 1b0 = Disabled 1b1 = Enabled
4	STR1_EN	R/W	1b0	Strobe1 Pin Enable 1b0 = Disabled 1b1 = Enabled
3	D4_EN	R/W	1b0	D4 Output Enable 1b0 = Disabled 1b1 = Enabled
2	D3_EN	R/W	1b0	D3 Output Enable 1b0 = Disabled 1b1 = Enabled
1	D2_EN	R/W	1b0	D2 Output Pin Enable 1b0 = Disabled 1b1 = Enabled

Copyright © 2026 Texas Instruments Incorporated

Table 6-8. CTRL_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	D1_EN	R/W	1b0	D1 Output Pin Enable 1b0 = Disabled 1b1 = Enabled

Copyright © 2026 Texas Instruments Incorporated

6.6.1.3 D_MODE_REG Register (Address = 0x2) [reset = 0x0]

D_MODE_REG is shown in Figure 6-17 and described in Table 6-9.

Return to Summary Table.

The D_MODE_REG sets the mode performance of each current source output. The DC/DC boost will adjust based upon the active modes and LEDs enabled. The mode requiring the highest output voltage will take priority.

Figure 6-17. D_MODE_REG Register

7	6	5	4	3	2	1	0
D4_MODE		D3_MODE		D2_MODE		D1_MODE	
R/W-2b00		R/W-2b00		R/W-2b00		R/W-2b00	

Table 6-9. D_MODE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	D4_MODE	R/W	2b00	2b00 = Off 2b01 = IR 2b10 = Torch 2b11 = Flash
5-4	D3_MODE	R/W	2b00	2b00 = Off 2b01 = IR 2b10 = Torch 2b11 = Flash
3-2	D2_MODE	R/W	2b00	2b00 = Off 2b01 = IR 2b10 = Torch 2b11 = Flash
1-0	D1_MODE	R/W	2b00	2b00 = Off 2b01 = IR 2b10 = Torch 2b11 = Flash

Copyright © 2026 Texas Instruments Incorporated

6.6.1.4 STR_CTRL_REG Register (Address = 0x3) [reset = 0x0]

STR_CTRL_REG is shown in Figure 6-18 and described in Table 6-10.

Return to Summary Table.

The STR_CTRL_REG assigns which current sources become enabled when either of the two Strobe pins become active. Each Dx output should only be assigned to one strobe pin at a time.

Figure 6-18. STR_CTRL_REG Register

7	6	5	4	3	2	1	0
D4_STR2	D3_STR2	D2_STR2	D1_STR2	D4_STR1	D3_STR1	D2_STR1	D1_STR1
R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0

Table 6-10. STR_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	D4_STR2	R/W	1b0	D4 Controlled by STR2 1b0 = Disabled 1b1 = Enabled
6	D3_STR2	R/W	1b0	D3Controlled by STR2 1b0 = Disabled 1b1 = Enabled
5	D2_STR2	R/W	1b0	D2 Controlled by STR2 1b0 = Disabled 1b1 = Enabled
4	D1_STR2	R/W	1b0	D1 Controlled by STR2 1b0 = Disabled 1b1 = Enabled
3	D4_STR1	R/W	1b0	D4 Controlled by STR1 1b0 = Disabled 1b1 = Enabled
2	D3_STR1	R/W	1b0	D3 Controlled by STR1 1b0 = Disabled 1b1 = Enabled
1	D2_STR1	R/W	1b0	D2 Controlled by STR1 1b0 = Disabled 1b1 = Enabled
0	D1_STR1	R/W	1b0	D1 Controlled by STR1 1b0 = Disabled 1b1 = Enabled

Copyright © 2026 Texas Instruments Incorporated

6.6.1.5 STR_TIME_REG Register (Address = 0x4) [reset = 0xA]

STR_TIME_REG is shown in Figure 6-19 and described in Table 6-11.

Return to Summary Table.

STR_TIME_REG sets the flash time-out durations, as well as Strobe type

Figure 6-19. STR_TIME_REG Register

7	6	5	4	3	2	1	0
STR2_LE	STR1_LE	TO_DISABLE	FTO_MULT	FTO_DUR			
R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-4b1010			

Table 6-11. STR_TIME_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STR2_LE	R/W	1b0	STR2 Level or Edge Trigger 1b0 = Level 1b1 = Edge
6	STR1_LE	R/W	1b0	STR1 Level or Edge Trigger 1b0 = Level 1b1 = Edge
5	TO_DISABLE	R/W	1b0	Timeout Disable 1b0 = Time-Out Enabled 1b1 = Time-Out Disabled
4	FTO_MULT	R/W	1b0	4x Time-Out Multiplier 1b0 = 1x Gain 1b1 = 4x Gain

Copyright © 2026 Texas Instruments Incorporated

Table 6-11. STR_TIME_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	FTO_DUR	R/W	4b1010	Flash Time-Out Duration 4b0000 = 10 ms 4b0001 = 20 ms 4b0010 = 30 ms 4b0011 = 40 ms 4b0100 = 50 ms 4b0101 = 60 ms 4b0110 = 70 ms 4b0111 = 80 ms 4b1000 = 90 ms 4b1001 = 100 ms 4b1010 = 150 ms (Default) 4b1011 = 200 ms 4b1100 = 250 ms 4b1101 = 300 ms 4b1110 = 350 ms 4b1111 = 400 ms

Copyright © 2026 Texas Instruments Incorporated

6.6.1.6 D1_FLASH_REG Register (Address = 0x5) [reset = 0x0]

D1_FLASH_REG is shown in Figure 6-20 and described in Table 6-12.

Return to Summary Table.

D1_FLASH_REG sets the desired Flash and IR current levels

Figure 6-20. D1_FLASH_REG Register

7	6	5	4	3	2	1	0
D1_FLASH							
R/W-8b00000000							

Table 6-12. D1_FLASH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	D1_FLASH	R/W	8b00000000	ILED = [7.8(mA) x Code(decimal)] + 7.325 mA

Copyright © 2026 Texas Instruments Incorporated

6.6.1.7 D2_FLASH_REG Register (Address = 0x6) [reset = 0x0]

D2_FLASH_REG is shown in Figure 6-21 and described in Table 6-13.

Return to Summary Table.

D2_FLASH_REG sets the desired Flash and IR current levels

Figure 6-21. D2_FLASH_REG Register

7	6	5	4	3	2	1	0
D2_FLASH							
R/W-8b00000000							

Table 6-13. D2_FLASH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	D2_FLASH	R/W	8b00000000	ILED = [7.8(mA) x Code(decimal)] + 7.325 mA

Copyright © 2026 Texas Instruments Incorporated

6.6.1.8 D3_FLASH_REG Register (Address = 0x7) [reset = 0x0]

D3_FLASH_REG is shown in Figure 6-22 and described in Table 6-14.

Return to Summary Table.

D3_FLASH_REG sets the desired Flash and IR current levels

Figure 6-22. D3_FLASH_REG Register

7	6	5	4	3	2	1	0
D3_FLASH							
R/W-8b00000000							

Table 6-14. D3_FLASH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	D3_FLASH	R/W	8b00000000	ILED = [7.8(mA) x Code(decimal)] + 7.325 mA

Copyright © 2026 Texas Instruments Incorporated

6.6.1.9 D4_FLASH_REG Register (Address = 0x8) [reset = 0x0]

D4_FLASH_REG is shown in Figure 6-23 and described in Table 6-15.

Return to Summary Table.

D4_FLASH_REG sets the desired Flash and IR current levels

Figure 6-23. D4_FLASH_REG Register

7	6	5	4	3	2	1	0
D4_FLASH							
R/W-8b00000000							

Table 6-15. D4_FLASH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	D4_FLASH	R/W	8b00000000	ILED = [7.8(mA) x Code(decimal)] + 7.325 mA

Copyright © 2026 Texas Instruments Incorporated

6.6.1.10 D1_TORCH_REG Register (Address = 0x9) [reset = 0x0]

D1_TORCH_REG is shown in Figure 6-24 and described in Table 6-16.

Return to Summary Table.

D1_TORCH_REG sets the desired D1 Torch current level

Figure 6-24. D1_TORCH_REG Register

7	6	5	4	3	2	1	0
D1_Torch							
R/W-8b00000000							

Table 6-16. D1_TORCH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	D1_Torch	R/W	8b00000000	ILED = [1.41(mA) x Code(decimal)] + 0.525 mA

Copyright © 2026 Texas Instruments Incorporated

6.6.1.11 D2_TORCH_REG Register (Address = 0xA) [reset = 0x0]

D2_TORCH_REG is shown in Figure 6-25 and described in Table 6-17.

Return to Summary Table.

D2_TORCH_REG sets the desired D2 Torch current level

Figure 6-25. D2_TORCH_REG Register

7	6	5	4	3	2	1	0
D2_Torch							
R/W-8b00000000							

Table 6-17. D2_TORCH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	D2_Torch	R/W	8b00000000	ILED = [1.41(mA) x Code(decimal)] + 0.525 mA

Copyright © 2026 Texas Instruments Incorporated

6.6.1.12 D3_TORCH_REG Register (Address = 0xB) [reset = 0x0]

D3_TORCH_REG is shown in Figure 6-26 and described in Table 6-18.

Return to Summary Table.

D3_TORCH_REG sets the desired D3 Torch current level

Figure 6-26. D3_TORCH_REG Register

7	6	5	4	3	2	1	0
D3_Torch							
R/W-8b00000000							

Table 6-18. D3_TORCH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	D3_Torch	R/W	8b00000000	ILED = [1.41(mA) x Code(decimal)] + 0.525 mA

Copyright © 2026 Texas Instruments Incorporated

6.6.1.13 D4_TORCH_REG Register (Address = 0xC) [reset = 0x0]

D4_TORCH_REG is shown in Figure 6-27 and described in Table 6-19.

Return to Summary Table.

D4_TORCH_REG sets the desired D4 Torch current level

Figure 6-27. D4_TORCH_REG Register

7	6	5	4	3	2	1	0
D4_Torch							
R/W-8b00000000							

Table 6-19. D4_TORCH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	D4_Torch	R/W	8b00000000	ILED = [1.41(mA) x Code(decimal)] + 0.525 mA

Copyright © 2026 Texas Instruments Incorporated

6.6.1.14 NTC_MODE_REG Register (Address = 0xD) [reset = 0x40]

NTC_MODE_REG is shown in Figure 6-28 and described in Table 6-20.

Return to Summary Table.

NTC_MODE_REG Enables and disables the two NTC blocks and sets the drive current and current reduction mode

Figure 6-28. NTC_MODE_REG Register

7	6	5	4	3	2	1	0
NTC_Current		NTC2_MODE		NTC1_MODE		NTC2_EN	NTC1_EN
R/W-2b01		R/W-2b00		R/W-2b00		R/W-1b0	R/W-1b0

Table 6-20. NTC_MODE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	NTC_Current	R/W	2b01	2b00 = 25 µA 2b01 = 50 µA 2b10 = 75 µA 2b11 = 100 µA
5-4	NTC2_MODE	R/W	2b00	2b00 = Force Shutdown 2b01 = Force Torch 2b10 = Report Only 2b11 = Report Only
3-2	NTC1_MODE	R/W	2b00	2b00 = Force Shutdown 2b01 = Force Torch 2b10 = Report Only 2b11 = Report Only
1	NTC2_EN	R/W	1b0	1b0 = NTC2 is disabled 1b1 = NTC2 is enabled
0	NTC1_EN	R/W	1b0	1b0 = NTC1 is disabled 1b1 = NTC1 is enabled

Copyright © 2026 Texas Instruments Incorporated

6.6.1.15 NTC_ASSIGN_REG Register (Address = 0xE) [reset = 0x0]

NTC_ASSIGN_REG is shown in Figure 6-29 and described in Table 6-21.

Return to Summary Table.

NTC_ASSIGN_REG determines how each of the Dx output pins responds to a NTC1 or NTC2 event. No output should be assigned to both NTC detection blocks.

Figure 6-29. NTC_ASSIGN_REG Register

7	6	5	4	3	2	1	0
NTC2_D4	NTC2_D3	NTC2_D2	NTC2_D1	NTC1_D4	NTC1_D3	NTC1_D2	NTC1_D1
R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0

Table 6-21. NTC_ASSIGN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	NTC2_D4	R/W	1b0	1b0 = D4 Ignore 1b1 = D4 Assigned
6	NTC2_D3	R/W	1b0	1b0 = D3 Ignore 1b1 = D3 Assigned
5	NTC2_D2	R/W	1b0	1b0 = D2 Ignore 1b1 = D2 Assigned
4	NTC2_D1	R/W	1b0	1b0 = D1 Ignore 1b1 = D1 Assigned
3	NTC1_D4	R/W	1b0	1b0 = D4 Ignore 1b1 = D4 Assigned
2	NTC1_D3	R/W	1b0	1b0 = D3 Ignore 1b1 = D3 Assigned
1	NTC1_D2	R/W	1b0	1b0 = D2 Ignore 1b1 = D2 Assigned
0	NTC1_D1	R/W	1b0	1b0 = D1 Ignore 1b1 = D1 Assigned

Copyright © 2026 Texas Instruments Incorporated

6.6.1.16 NTC_VOLT_REG Register (Address = 0xF) [reset = 0x0]

NTC_VOLT_REG is shown in Figure 6-30 and described in Table 6-22.

Return to Summary Table.

NTC_VOLT_REG sets the NTC trip voltage

Figure 6-30. NTC_VOLT_REG Register

7	6	5	4	3	2	1	0
NTC2_Set				NTC1_Set			
R/W-4b0000				R/W-4b0000			

Table 6-22. NTC_VOLT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	NTC2_Set	R/W	4b0000	NTC2 Trip Voltage. '0000' = 250 mV, '1111' = 1 V, 50 mV steps
3-0	NTC1_Set	R/W	4b0000	NTC1 Trip Voltage. '0000' = 250 mV, '1111' = 1 V, 50 mV steps

Copyright © 2026 Texas Instruments Incorporated

6.6.1.17 NTC_READ_REG Register (Address = 0x10) [reset = 0x0]

NTC_READ_REG is shown in Figure 6-31 and described in Table 6-23.

Return to Summary Table.

An I2C read of the NTC_READ_REG fetches the voltage on the NTC1 and NTC2 pin for temperature readback

Figure 6-31. NTC_READ_REG Register

7	6	5	4	3	2	1	0
NTC2_READ				NTC1_READ			
R-4b0000				R-4b0000			

Table 6-23. NTC_READ_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	NTC2_READ	R	4b0000	NTC2 Trip Voltage. '0000' = 250 mV, '1111' = 1 V, 50 mV steps
3-0	NTC1_READ	R	4b0000	NTC1 Trip Voltage. '0000' = 250 mV, '1111' = 1 V, 50 mV steps

Copyright © 2026 Texas Instruments Incorporated

6.6.1.18 IVFM_SET_REG Register (Address = 0x11) [reset = 0x80]

IVFM_SET_REG is shown in Figure 6-32 and described in Table 6-24.

Return to Summary Table.

The IVFM_SET_REG configures the input voltage monitor trip point, mode, hystersis and UVLO functionality. The Ramp Disable option for the Flash_Ramp should not be used if IVFM is enabled.

Figure 6-32. IVFM_SET_REG Register

7	6	5	4	3	2	1	0
UVLO_EN	IVFM_HYST	IVFM_THRES				IVFM_MODE	
R/W-1b1	R/W-1b0	R/W-4b0000				R/W-2b00	

Table 6-24. IVFM_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UVLO_EN	R/W	1b1	1b0 = UVLO is disabled 1b1 = UVLO is enabled
6	IVFM_HYST	R/W	1b0	1b0 = 0 mV 1b1 = 50 mV
5-2	IVFM_THRES	R/W	4b0000	4b0000 = 2.5 V 4b0001 = 2.55 V 4b0010 = 2.6 V 4b0011 = 2.65 V 4b0100 = 2.7 V 4b0101 = 2.75 V 4b0110 = 2.8 V 4b0111 = 2.85 V 4b1000 = 2.9 V 4b1001 = 2.95 V 4b1010 = 3.0 V 4b1011 = 3.05 V 4b1100 = 3.1 V 4b1101 = 3.15 V 4b1110 = 3.2 V 4b1111 = 3.25 V
1-0	IVFM_MODE	R/W	2b00	2b00 = Disabled 2b01 = Stop and Hold 2b10 = Down Adjust 2b11 = Up/Down Adjust

Copyright © 2026 Texas Instruments Incorporated

6.6.1.19 CUR_RAMP_REG Register (Address = 0x12) [reset = 0x39]

CUR_RAMP_REG is shown in Figure 6-33 and described in Table 6-25.

Return to Summary Table.

The CUR_RAMP_REG sets the ramp time of the LEDs currents in Torch, Flash and IR modes. The Ramp Disable option for the Flash_Ramp should not be used if IVFM is enabled.

Figure 6-33. CUR_RAMP_REG Register

7	6	5	4	3	2	1	0
RFU	IR_Ramp		Flash_Ramp		Torch_Ramp		
R/W-1b0	R/W-2b01		R/W-2b11		R/W-3b001		

Table 6-25. CUR_RAMP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RFU	R/W	1b0	Reserved
6-5	IR_Ramp	R/W	2b01	2b00 = Ramp Disabled 2b01 = 32 µs 2b10 = 64 µs 2b11 = 128 µs
4-3	Flash_Ramp	R/W	2b11	2b00 = Ramp Disabled 2b01 = 256 µs 2b10 = 512 µs 2b11 = 1024 µs
2-0	Torch_Ramp	R/W	3b001	3b000 = Ramp Disabled 3b001 = 1 ms 3b010 = 32 ms 3b011 = 64 ms 3b100 = 128 ms 3b101 = 256 ms 3b110 = 512 ms 3b111 = 1024 ms

Copyright © 2026 Texas Instruments Incorporated

6.6.1.20 FAULT_CTRL_REG Register (Address = 0x13) [reset = 0x19]

FAULT_CTRL_REG is shown in Figure 6-34 and described in Table 6-26.

Return to Summary Table.

Enables and disables the NTC fault detection and Thermal scale back blocks, along with boost related operation

Figure 6-34. FAULT_CTRL_REG Register

7	6	5	4	3	2	1	0
SW_RESET	RFU	THERM_SB		THERM_SB_EN	NTC_OPEN_EN	NTC_SHORT_EN	LED_SHORT_EN
R/W-1b0	R-1b0	R/W-2b01		R/W-1b1	R/W-1b0	R/W-1b0	R/W-1b1

Table 6-26. FAULT_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SW_RESET	R/W	1b0	1b0 = No Reset 1b1 = Reset
6	RFU	R	1b0	Reserved
5-4	THERM_SB	R/W	2b01	Thermal Scale Back 2b00 = Force Shutdown 2b01 = Force Torch 2b10 = Report Only 2b11 = Report Only
3	THERM_SB_EN	R/W	1b1	Thermal Scale Back Enable 1b0 = TSB Disabled 1b1 = TSB Enabled
2	NTC_OPEN_EN	R/W	1b0	1b0 = NTC Open Detection Disabled 1b1 = NTC Open Detection Enabled
1	NTC_SHORT_EN	R/W	1b0	1b0 = NTC Short Detection Disabled 1b1 = NTC Short Detection Enabled
0	LED_SHORT_EN	R/W	1b1	1b0 = LED Short Detection Disabled 1b1 = LED Short Detection Enabled

Copyright © 2026 Texas Instruments Incorporated

6.6.1.21 FLAG_RPT_REG Register (Address = 0x14) [reset = 0x0]

FLAG_RPT_REG is shown in Figure 6-35 and described in Table 6-27.

Return to Summary Table.

The FLAG_RPT_REG reports the flag events that can occur. These event flags do not need to be cleared to allow a restart and are for status only.

Figure 6-35. FLAG_RPT_REG Register

7	6	5	4	3	2	1	0
RFU		Tx	ICL	FTO4	FTO3	FTO2	FTO1
R-2b00		R-1b0	R-1b0	R-1b0	R-1b0	R-1b0	R-1b0

Table 6-27. FLAG_RPT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RFU	R	2b00	Reserved
5	Tx	R	1b0	Transmit Interrupt
4	ICL	R	1b0	Inductor Current Limit
3	FTO4	R	1b0	Flash Time-Out D4
2	FTO3	R	1b0	Flash Time-Out D3
1	FTO2	R	1b0	Flash Time-Out D2
0	FTO1	R	1b0	Flash Time-Out D1

Copyright © 2026 Texas Instruments Incorporated

6.6.1.22 VOLT_FAULT_REG Register (Address = 0x15) [reset = 0x0]

VOLT_FAULT_REG is shown in Figure 6-36 and described in Table 6-28.

Return to Summary Table.

The VOLT_FAULT_REG register signals voltage faults that occur during any of the operating modes.

Figure 6-36. VOLT_FAULT_REG Register

7	6	5	4	3	2	1	0
UVLO	OVP	OUT_SHORT	IVFM_Trip	LED4_Short	LED3_Short	LED2_Short	LED1_Short
R-1b0	R-1b0	R-1b0	R-1b0	R-1b0	R-1b0	R-1b0	R-1b0

Table 6-28. VOLT_FAULT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UVLO	R	1b0	Under Voltage Lock Out
6	OVP	R	1b0	Over Voltage Protection
5	OUT_SHORT	R	1b0	Boost Output Short
4	IVFM_Trip	R	1b0	Input Voltage Monitor Tripped
3	LED4_Short	R	1b0	LED4 Short Detection
2	LED3_Short	R	1b0	LED3 Short Detection
1	LED2_Short	R	1b0	LED2 Short Detection
0	LED1_Short	R	1b0	LED1 Short Detection

Copyright © 2026 Texas Instruments Incorporated

6.6.1.23 THERM_FAULT_REG Register (Address = 0x16) [reset = 0x0]

THERM_FAULT_REG is shown in Figure 6-37 and described in Table 6-29.

Return to Summary Table.

The THERM_FAULT_REG is used to report termperature related faults that occur during any of the operating modes

Figure 6-37. THERM_FAULT_REG Register

7	6	5	4	3	2	1	0
NTC2_SHORT	NTC1_SHORT	NTC2_OPEN	NTC1_OPEN	NTC2_TRIP	NTC1_TRIP	TSB	TSD
R-1b0	R-1b0	R-1b0	R-1b0	R-1b0	R-1b0	R-1b0	R-1b0

Table 6-29. THERM_FAULT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	NTC2_SHORT	R	1b0	NTC2 Shorted
6	NTC1_SHORT	R	1b0	NTC1 Shorted
5	NTC2_OPEN	R	1b0	NTC2 Open
4	NTC1_OPEN	R	1b0	NTC1 Open
3	NTC2_TRIP	R	1b0	NTC2 Trip
2	NTC1_TRIP	R	1b0	NTC1 Trip
1	TSB	R	1b0	Thermal Scale Back
0	TSD	R	1b0	Thermal Shutdown

Copyright © 2026 Texas Instruments Incorporated

6.6.1.24 LAST_CUR_REG1 Register (Address = 0x17) [reset = 0x0]

LAST_CUR_REG1 is shown in Figure 6-38 and described in Table 6-30.

Return to Summary Table.

Stores the last current value reported as a fraction of full scale in the event of a current scale back event (IVFM, thermal scale back, etc)

Figure 6-38. LAST_CUR_REG1 Register

7	6	5	4	3	2	1	0
LAST_CUR							
R-8b00000000							

Table 6-30. LAST_CUR_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_CUR	R	8b00000000	Last Current Adjust Register

Copyright © 2026 Texas Instruments Incorporated

6.6.1.25 LAST_CUR_REG2 Register (Address = 0x18) [reset = 0x0]

LAST_CUR_REG2 is shown in Figure 6-39 and described in Table 6-31.

Return to Summary Table.

Stores the last current value reported as a fraction of full scale in the event of a current scale back event (IVFM, thermal scale back, etc)

Figure 6-39. LAST_CUR_REG2 Register

7	6	5	4	3	2	1	0
LAST_CUR							
R-8b00000000							

Table 6-31. LAST_CUR_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_CUR	R	8b00000000	Last Current Adjust Register

Copyright © 2026 Texas Instruments Incorporated

6.6.1.26 LAST_CUR_REG3 Register (Address = 0x19) [reset = 0x0]

LAST_CUR_REG3 is shown in Figure 6-40 and described in Table 6-32.

Return to Summary Table.

Stores the last current value reported as a fraction of full scale in the event of a current scale back event (IVFM, thermal scale back, etc)

Figure 6-40. LAST_CUR_REG3 Register

7	6	5	4	3	2	1	0
LAST_CUR							
R-8b00000000							

Table 6-32. LAST_CUR_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_CUR	R	8b00000000	Last Current Adjust Register

Copyright © 2026 Texas Instruments Incorporated

6.6.1.27 LAST_CUR_REG4 Register (Address = 0x1A) [reset = 0x0]

LAST_CUR_REG4 is shown in Figure 6-41 and described in Table 6-33.

Return to Summary Table.

Stores the last current value reported as a fraction of full scale in the event of a current scale back event (IVFM, thermal scale back, etc)

Figure 6-41. LAST_CUR_REG4 Register

7	6	5	4	3	2	1	0
LAST_CUR							
R-8b00000000							

Table 6-33. LAST_CUR_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_CUR	R	8b00000000	Last Current Adjust Register

Copyright © 2026 Texas Instruments Incorporated

6.6.1.28 DEV_INFO_REG Register (Address = 0x1B) [reset = 0x41]

DEV_INFO_REG is shown in Figure 6-42 and described in Table 6-34.

Return to Summary Table.

Stores Device Information

Figure 6-42. DEV_INFO_REG Register

7	6	5	4	3	2	1	0
DEV_ID				REV_ID			
R-4b0100				R-4b0001			

Table 6-34. DEV_INFO_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DEV_ID	R	4b0100	Device ID
3-0	REV_ID	R	4b0001	Revision Info

Copyright © 2026 Texas Instruments Incorporated

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The LM3645 can drive four flash LEDs at currents up to 2 A per LED. The total LED current the LM3645 boost can deliver is 5 A (I_{LED1} + I_{LED2}+ I_{LED3}+ I_{LED4}). The 2-MHz or 4-MHz DC-DC boost regulator allows for the use of small value discrete external components.

7.2 Typical Application

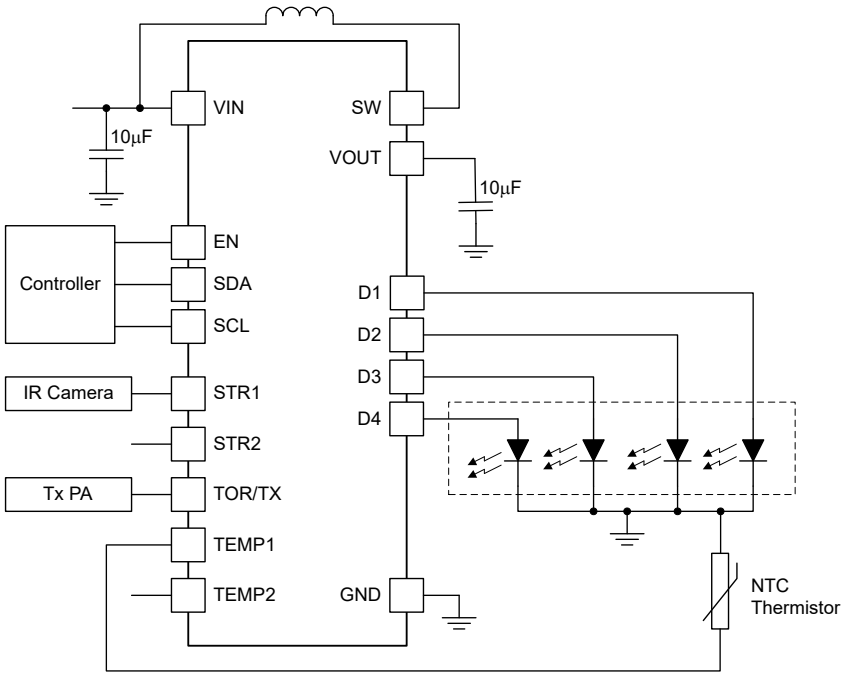


Figure 7-1. LM3645 Typical Application

7.2.1 Design Requirements

Example requirements based on default register values:

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.3 V to 5.5 V
Brightness control	I^2C Register
LED configuration	4 parallel flash LEDs
Boost switching frequency	2 MHz (4 MHz selectable)
Flash brightness	500 mA per LED

7.2.2 Output Control Examples

The LM3645 is highly configurable enabling multiple different LED drive use cases. To highlight the flexibility, sample sequences for different use cases are provided. Additional features such as Tx control and NTC

Copyright © 2026 Texas Instruments Incorporated

interactions can be enabled and disabled in each mode, however they are not included in the following examples for simplicity.

7.2.2.1 Four Channel Flash with Strobe1 Trigger Starting in Standby

The following sequence highlights how to control all four current sources in Flash mode starting with the LM3645 in standby.

I2C Address	Data	Comments
0x02	0xFF	Sets Outputs to Flash Mode
0x03	0x0F	Assigns Outputs to Strobe1
0x04	0x0A	Sets Flash timeout to 150 ms with STR1 configured to a Level Strobe
0x05	0x3F	Sets LED1 Current to 500 mA
0x06	0x3F	Sets LED2 Current to 500 mA
0x07	0x3F	Sets LED3 Current to 500 mA
0x08	0x3F	Sets LED4 Current to 500 mA
0x01	0x5F	Enables Flash mode with Tx Enabled. Waiting for Strobe to trigger
Strobe goes high and LM3645 runs in Flash mode. Flash will end upon STR1 going low or Timeout occurring. Repeated Strobe events are possible without further I2C communication so long as a timeout does not occur.		

7.2.2.2 Four Channel Flash with Strobe1 Trigger Starting in I2C Torch

The following sequence highlights how to control all four current sources in Flash mode after I2C Torch mode has already been enabled.

I2C Address	Data	Comments
0x02	0xAA	Sets Outputs to Torch Mode
0x03	0x0F	Assigns Outputs to Strobe1
0x04	0x0A	Sets Flash timeout to 150 ms with STR1 configured to a Level Strobe
0x05	0x3F	Sets LED1 Flash Current to 500 mA
0x06	0x3F	Sets LED2 Flash Current to 500 mA
0x07	0x3F	Sets LED3 Flash Current to 500 mA
0x08	0x3F	Sets LED4 Flash Current to 500 mA
0x09	0x20	Sets LED1 Torch Current to 50 mA
0x0A	0x20	Sets LED2 Torch Current to 50 mA
0x0B	0x20	Sets LED3 Torch Current to 50 mA
0x0C	0x20	Sets LED4 Torch Current to 50 mA
0x01	0xDF	Enables Torch mode with Tx Enabled
Stay in Torch Mode until ready for flash		
0x02	0xFF	Sets Outputs to Flash Mode. LED current goes to off state waiting for strobe
Strobe goes high and LM3645 runs in Flash mode. Flash will end upon STR1 going low or Timeout occurring. Repeated Strobe events are possible without further I2C communication so long as a timeout does not occur.		

7.2.2.3 Mixed Mode Functionality

Figure 7-2 highlights how to control LED1 and LED2 in flash mode, with LED3 set to IR Mode and LED 4 set to external Torch Mode.

Copyright © 2026 Texas Instruments Incorporated

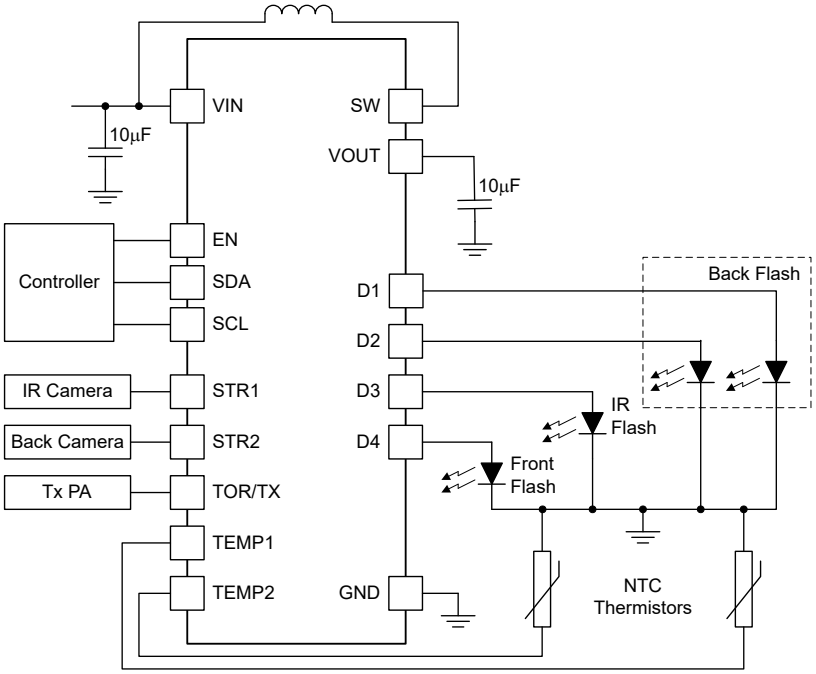


Figure 7-2. Mixed Mode Use Case

I2C Address	Data	Comments
0x02	0x9F	Sets LED1 and LED2 to Flash Mode, LED3 to IR Mode and LED4 to Torch
0x03	0x43	Sets LED 1 and 2 to Strobe1, sets LED3 to strobe2 and does not assign LED4 to strobe
0x04	0x0A	Sets Flash timeout to 150 ms with STR1 configured to a Level Strobe
0x05	0x20	Sets LED1 Flash Current to 500 mA
0x06	0x20	Sets LED2 Flash Current to 500 mA
0x07	0x80	Sets LED3 Flash Current to 1A
0x0C	0x20	Sets LED4 Torch Current to 50 mA
0x01	0xFF	Enables LED1/2/3/4 and Enables Strobe1, Strobe2 and Torch Pins, waiting for external control

Because an output is assigned to IR Mode (LED3), the OUT pin voltage increases to approximately VIN until current is delivered to the outputs. If Strobe1 goes high, LED1 and LED2 enable in Flash. If Strobe2 goes high, LED3 operates in IR Mode. If TOR/TX goes high LED4 enable in Torch Mode.

7.2.2.4 Voltage Mode Only

The following sequence highlights how to place the LM3645 into fixed output voltage mode with the current sources disabled.

I2C Address	Data	Comments
0x00	0x99	Enables voltage mode with 5V, 5A current limit and 2 MHz operation enabled

7.2.2.5 Voltage Mode With Advanced IR

The following sequence highlights how to place the LM3645 into fixed output voltage mode with two of the LED outputs enabled and both strobe pins (D1 assigned to STR1, D4 assigned to STR2)

I2C Address	Data	Comments
0x02	0x41	Sets D1 and D4 to IR mode

Copyright © 2026 Texas Instruments Incorporated

0x03	0x81	Sets D1 to STR1 and D4 to STR2
0x04	0x20	Time out Enabled with 10 ms duration
0x05	0x80	Sets D1 Current to 1A
0x08	0x80	Sets D4 Current to 1A
0x12	0x20	Sets IR ramp time to 32 µs
0x00	0x1B	Enables voltage mode with 4V, 5A current limit and 2 MHz operation enabled. LED Drive Priority
VOUT goes to 4V with the current sources disabled		
0x01	0x39	D1 and D4 outputs enabled with STR1 and STR2 enabled
When the strobe pins go high, the current to the LED outputs will ramp to their target. When the strobe pins go low, the LED outputs stop delivering current and VOUT will stay at 4V ready for the next strobe pulses.		

7.2.3 Detailed Design Procedure

7.2.3.1 Snubber Requirement

The LM3645 requires a snubber circuit attached to the SW (switch) node to suppress voltage spikes during switching. It is recommended that a 1 ohm resistor in series with a 4 nF capacitance be used. The ceramic snubber capacitor must have a minimum voltage rating of 6.3V and the effective capacitance must take into account the effects of DC bias.

7.2.3.2 Output Capacitor Selection

The LM3645 is designed to operate with a single 10-µF ceramic output capacitor, however two 10 µF capacitors in parallel is recommended to minimize LED current ripple. When the boost converter is running, the output capacitor supplies the load current during the boost converter on-time. When the NMOS switch turns off, the inductor energy is discharged through the internal PMOS switch, supplying power to the load and restoring charge to the output capacitor. This causes a sag in the output voltage during the on-time and a rise in the output voltage during the off-time. The output capacitor is therefore chosen to limit the output ripple to an acceptable level depending on load current and input/output voltage differentials and also to ensure the converter remains stable. To maintain stable boost operation, it is recommended that a minimum effective output capacitance (accounting for DC bias, temperature and part to part variation) be greater than **3 µF**.

Larger capacitors such as a 22-µF or capacitors in parallel can be used if lower output voltage ripple is desired. To estimate the output voltage ripple considering the ripple due to capacitor discharge (ΔV_Q) and the ripple due to the capacitors ESR (ΔV_{ESR}) use the following equations:

For continuous conduction mode, the output voltage ripple due to the capacitor discharge is:

$$\Delta V_Q = \frac{I_{LED} \times (V_{OUT} - V_{IN})}{f_{SW} \times V_{OUT} \times C_{OUT}} \tag{3}$$

The output voltage ripple due to the output capacitors ESR is found by:

$$\Delta V_{ESR} = R_{ESR} \times \left(\frac{I_{LED} \times V_{OUT}}{V_{IN}} + \Delta I_L \right)$$

where

$$\Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \tag{4}$$

In ceramic capacitors the ESR is very low so the assumption is that 80% of the output voltage ripple is due to capacitor discharge and 20% from ESR.

7.2.3.3 Input Capacitor Selection

Choosing the correct size and type of input capacitor helps minimize the voltage ripple caused by the switching of the LM3645 boost converter and reduce noise on the boost converter's input pin that can feed through and disrupt internal analog signals. In the typical application circuit a 10-µF ceramic input capacitor works well. It is

Copyright © 2026 Texas Instruments Incorporated

important to place the input capacitor as close as possible to the LM3645 input (IN) pin. This reduces the series resistance and inductance that can inject noise into the device due to the input switching currents.

7.2.3.4 Inductor Selection

The LM3645 is designed to use a 0.47-µH or 1-µH inductor. When the device is boosting (V_{OUT} > V_{IN}) the inductor is typically the largest area of efficiency loss in the circuit. Therefore, choosing an inductor with the lowest possible series resistance is important. Additionally, the saturation rating of the inductor should be greater than the maximum operating peak current of the LM3645. This prevents excess efficiency loss that can occur with inductors that operate in saturation. For proper inductor operation and circuit performance, ensure that the inductor saturation and the peak current limit setting of the LM3645 are greater than I_{PEAK} in the following calculation:

$$I_{PEAK} = \frac{I_{LOAD}}{\eta} \times \frac{V_{OUT}}{V_{IN}} + \Delta I_L \quad \text{where} \quad \Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \tag{5}$$

where

- f_{SW} = 2 MHz or 4 MHz

7.2.4 Application Curves

Ambient temperature is 25°C, input voltage is 3.6 V, EN = V_{IN}, C_{IN} = 2 × 10 µF, C_{OUT} = 2 × 10 µF and L = 1 µH, unless otherwise noted.

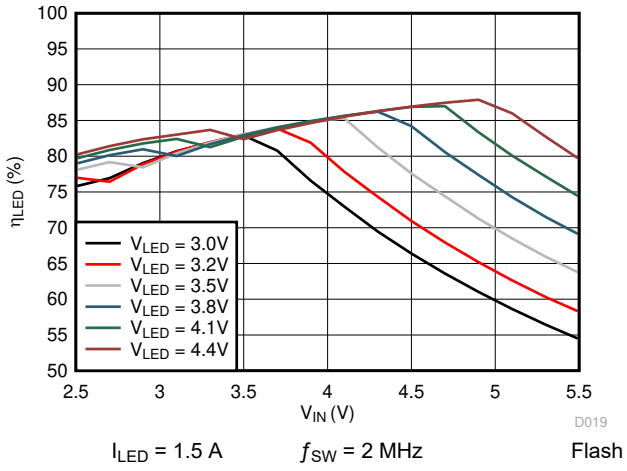


Figure 7-3. 2-MHz LED Efficiency vs Input Voltage

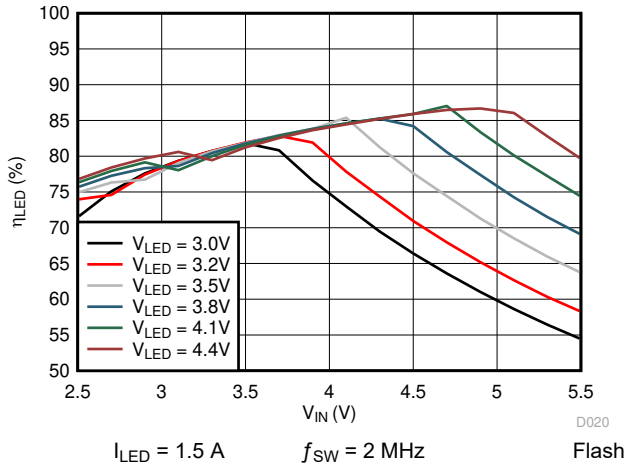
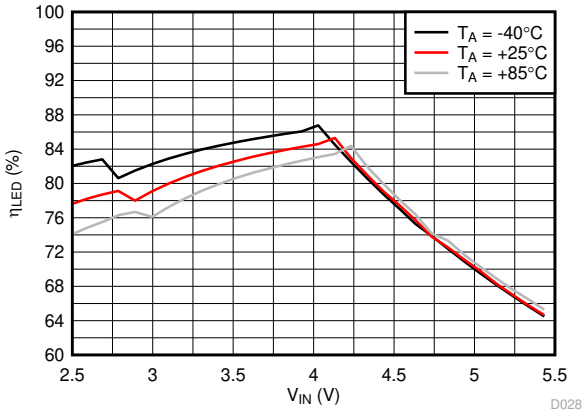


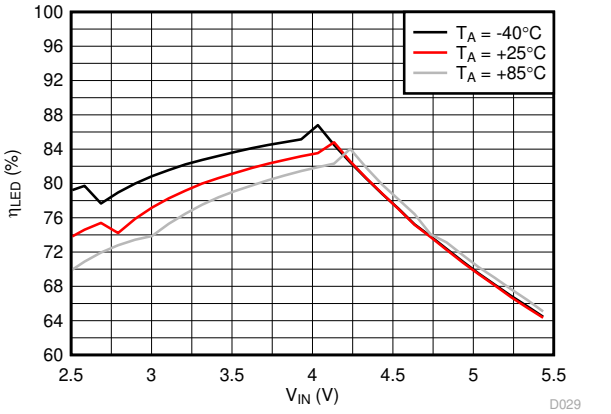
Figure 7-4. 4-MHz LED Efficiency vs Input Voltage

Copyright © 2026 Texas Instruments Incorporated



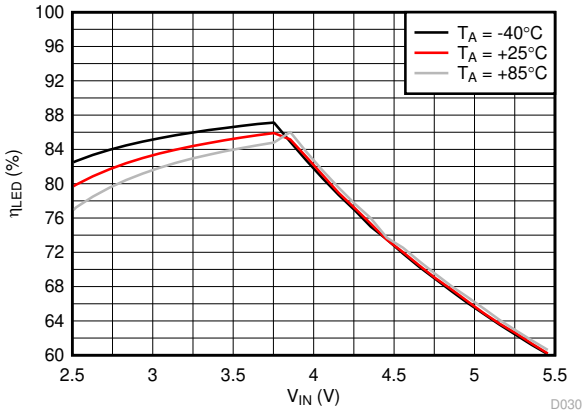
I_{LED} = 1.5 A f_{SW} = 2 MHz Flash
V_{LED} = 3.55 V

Figure 7-5. LED Efficiency vs Input Voltage



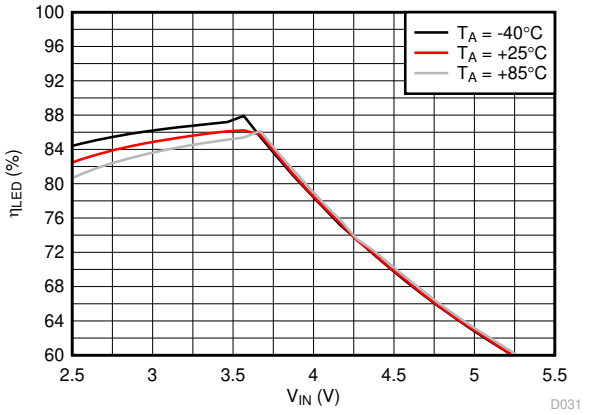
I_{LED} = 1.5 A f_{SW} = 4 MHz Flash
V_{LED} = 3.55 V

Figure 7-6. LED Efficiency vs Input Voltage



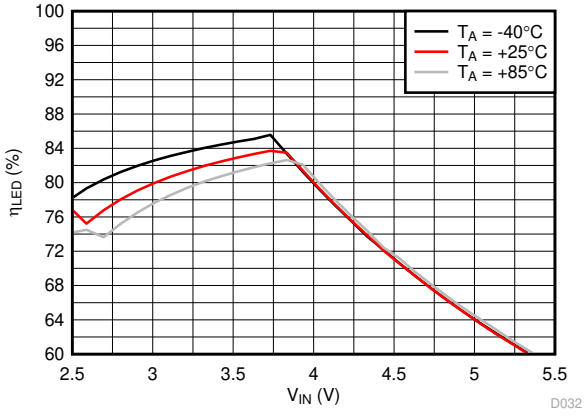
I_{LED} = 1 A f_{SW} = 2 MHz Flash
V_{LED} = 3.32 V

Figure 7-7. LED Efficiency vs Input Voltage



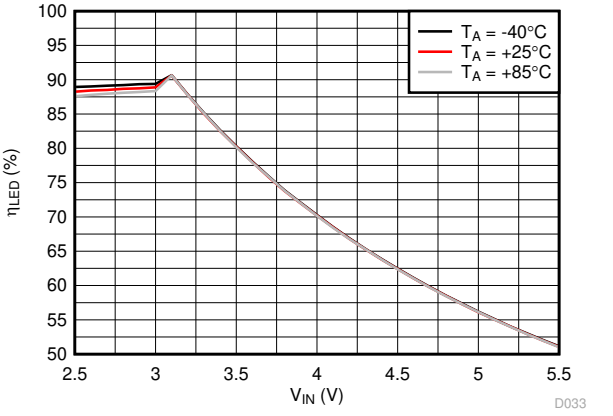
I_{LED} = 729 mA f_{SW} = 2 MHz Flash
V_{LED} = 3.18 V

Figure 7-8. LED Efficiency vs Input Voltage



$I_{LED1\ and\ LED2}$ = 729 mA Flash
V_{LED} = 3.18 V f_{SW} = 2 MHz

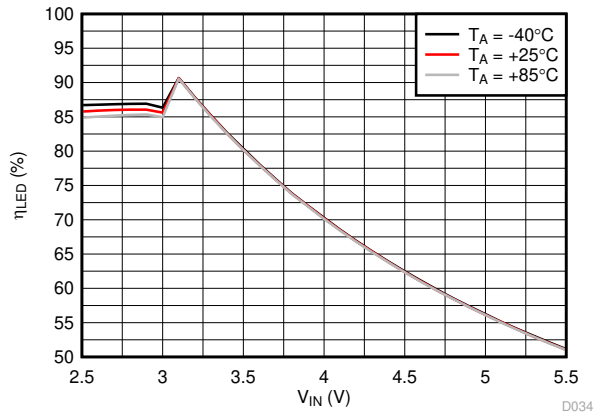
Figure 7-9. LED Efficiency vs Input Voltage



I_{LED} = 179 mA Torch
V_{LED} = 2.83 V f_{SW} = 2 MHz

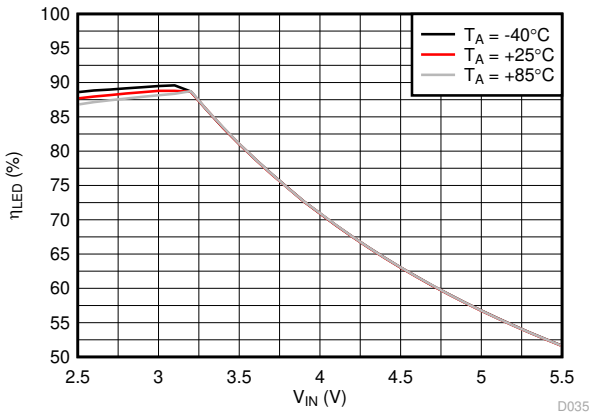
Figure 7-10. LED Efficiency vs Input Voltage

Copyright © 2026 Texas Instruments Incorporated



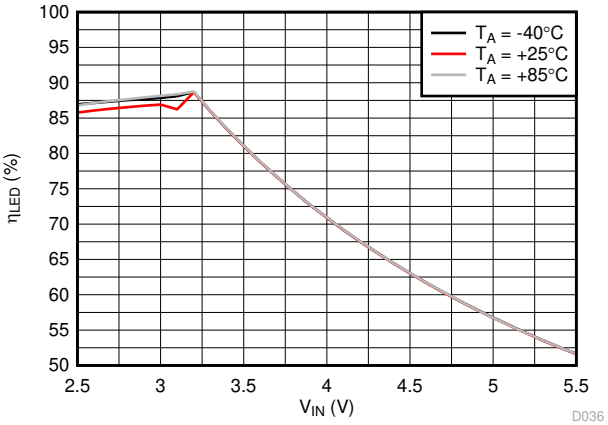
I_{LED} = 179 mA f_{SW} = 4 MHz
V_{LED} = 2.83 V Torch

Figure 7-11. LED Efficiency vs Input Voltage



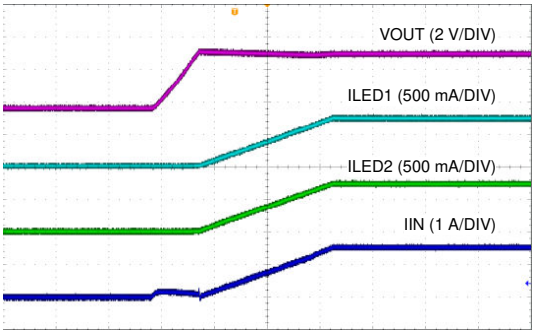
$I_{LED1\ and\ LED2}$ = 179 mA f_{SW} = 2 MHz
V_{LED} = 2.83 V Torch

Figure 7-12. LED Efficiency vs Input Voltage



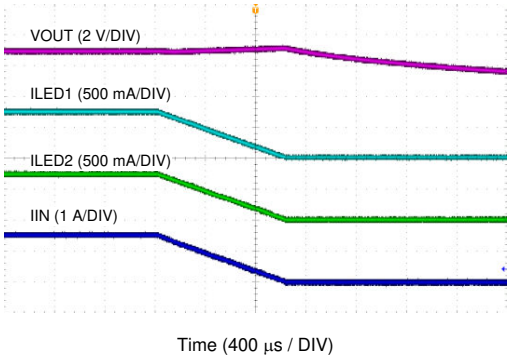
$I_{LED1\ and\ LED2}$ = 179 mA f_{SW} = 4 MHz
V_{LED} = 2.83 V Torch

Figure 7-13. LED Efficiency vs Input Voltage



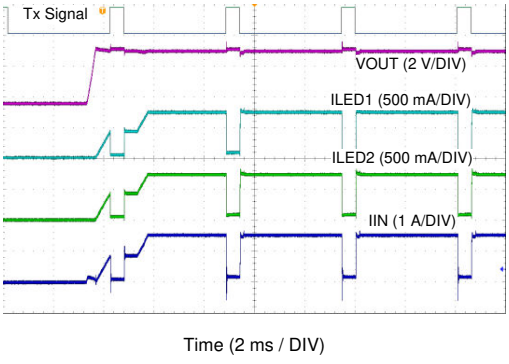
I_{LED1} = I_{LED2} = 730 mA f_{SW} = 2 MHz
V_{LED} = 3.18 V

Figure 7-14. Start-Up



I_{LED1} = I_{LED2} = 730 mA f_{SW} = 2 MHz
V_{LED} = 3.18 V

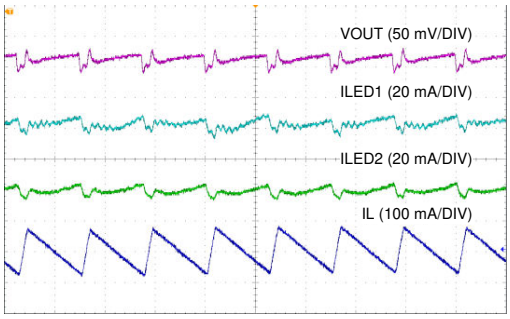
Figure 7-15. Ramp Down



I_{LED1} = I_{LED2} = 730 mA f_{SW} = 2 MHz
V_{LED} = 3.18 V

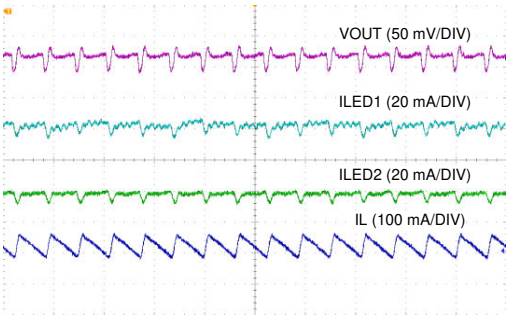
Figure 7-16. TX Interrupt

Copyright © 2026 Texas Instruments Incorporated



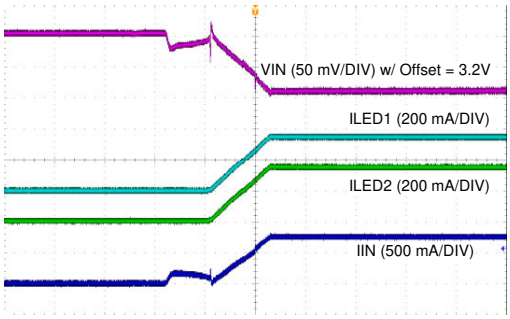
$I_{LED1} = I_{LED2}$ = 730 mA f_{SW} = 2 MHz
V_{LED} = 3.18 V

Figure 7-17. Ripple @ 2 MHz



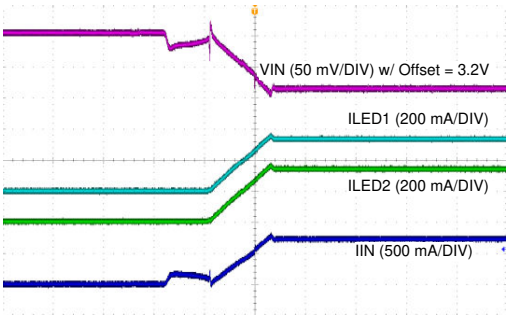
$I_{LED1} = I_{LED2}$ = 730 mA f_{SW} = 4 MHz
V_{LED} = 3.18 V

Figure 7-18. Ripple @ 4 MHz



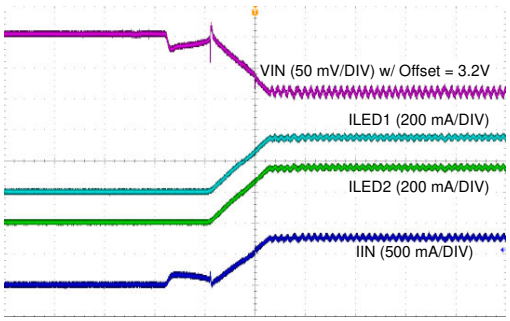
$I_{LED1} = I_{LED2}$ = 730 mA f_{SW} = 2 MHz
V_{LED} = 3.18 V V_{IVFM} = 3.2 V

Figure 7-19. IVFM - Ramp and Hold



$I_{LED1} = I_{LED2}$ = 730 mA f_{SW} = 2 MHz
V_{LED} = 3.18 V V_{IVFM} = 3.2 V

Figure 7-20. IVFM - Down Adjust Only



$I_{LED1} = I_{LED2}$ = 730 mA f_{SW} = 2 MHz
V_{LED} = 3.18 V V_{IVFM} = 3.2 V

Figure 7-21. IVFM - Up and Down Adjust

Copyright © 2026 Texas Instruments Incorporated

8 Power Supply Recommendations

The LM3645 is designed to operate from an input voltage supply range between 2.3 V and 5.5 V. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the LM3645 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

Copyright © 2026 Texas Instruments Incorporated

9 Layout

9.1 Layout Guidelines

The high switching frequency and large switching currents of the LM3645 make the choice of layout important. Follow these guidelines to ensure the device is stable and maintains proper LED current regulation across its intended operating voltage and current range.

- Place C_{IN} on the top layer (same layer as the LM3645) and as close to the device as possible. The input capacitor conducts the driver currents during the low-side MOSFET turn-on and turn-off and can detect current spikes over 1 A in amplitude. Connecting the input capacitor through short, wide traces to both the IN and GND pins reduces the inductive voltage spikes that occur during switching which can corrupt the V_{IN} line.
- Place C_{OUT} on the top layer (same layer as the LM3645) and as close as possible to the OUT and GND pin. The returns for both C_{IN} and C_{OUT} should come together at one point, as close to the GND pin as possible. Connecting C_{OUT} through short, wide traces reduce the series inductance on the OUT and GND pins that can corrupt the V_{OUT} and GND lines and cause excessive noise in the device and surrounding circuitry.
- Connect the inductor on the top layer close to the SW pin. There should be a low-impedance connection from the inductor to SW due to the large DC inductor current, and at the same time the area occupied by the SW node should be small so as to reduce the capacitive coupling of the high dV/dT present at SW that can couple into nearby traces.
- Avoid routing logic traces near the SW node so as to avoid any capacitively coupled voltages from SW onto any high-impedance logic lines such as TOR/Tx, STR1, STR2, EN, SDA, and SCL. A good approach is to insert an inner layer GND plane underneath the SW node and between any nearby routed traces. This creates a shield from the electric field generated at SW.
- Terminate the Flash LED cathodes directly to the GND pin of the LM3645. If possible, route the LED returns with a dedicated path so as to keep the high amplitude LED currents out of the GND plane. For Flash LEDs that are routed relatively far away from the LM3645, a good approach is to sandwich the forward and return current paths over the top of each other on two layers. This helps reduce the inductance of the LED current paths.

Copyright © 2026 Texas Instruments Incorporated

9.2 Layout Example

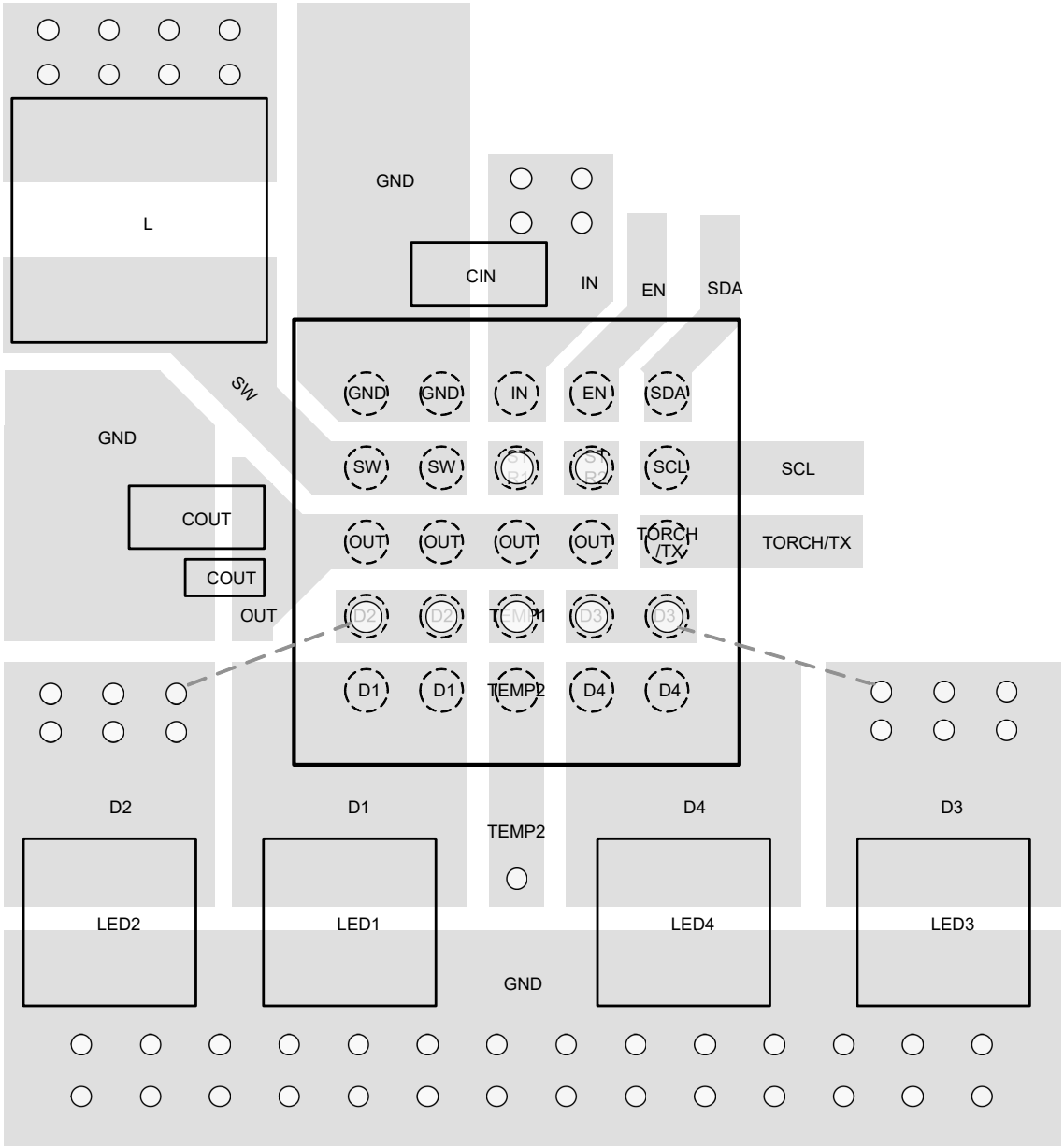


Figure 9-1. Layout Example

Copyright © 2026 Texas Instruments Incorporated

10 Device and Documentation Support

10.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

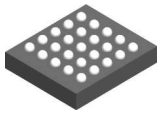
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2024	*	Initial release

Copyright © 2026 Texas Instruments Incorporated

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

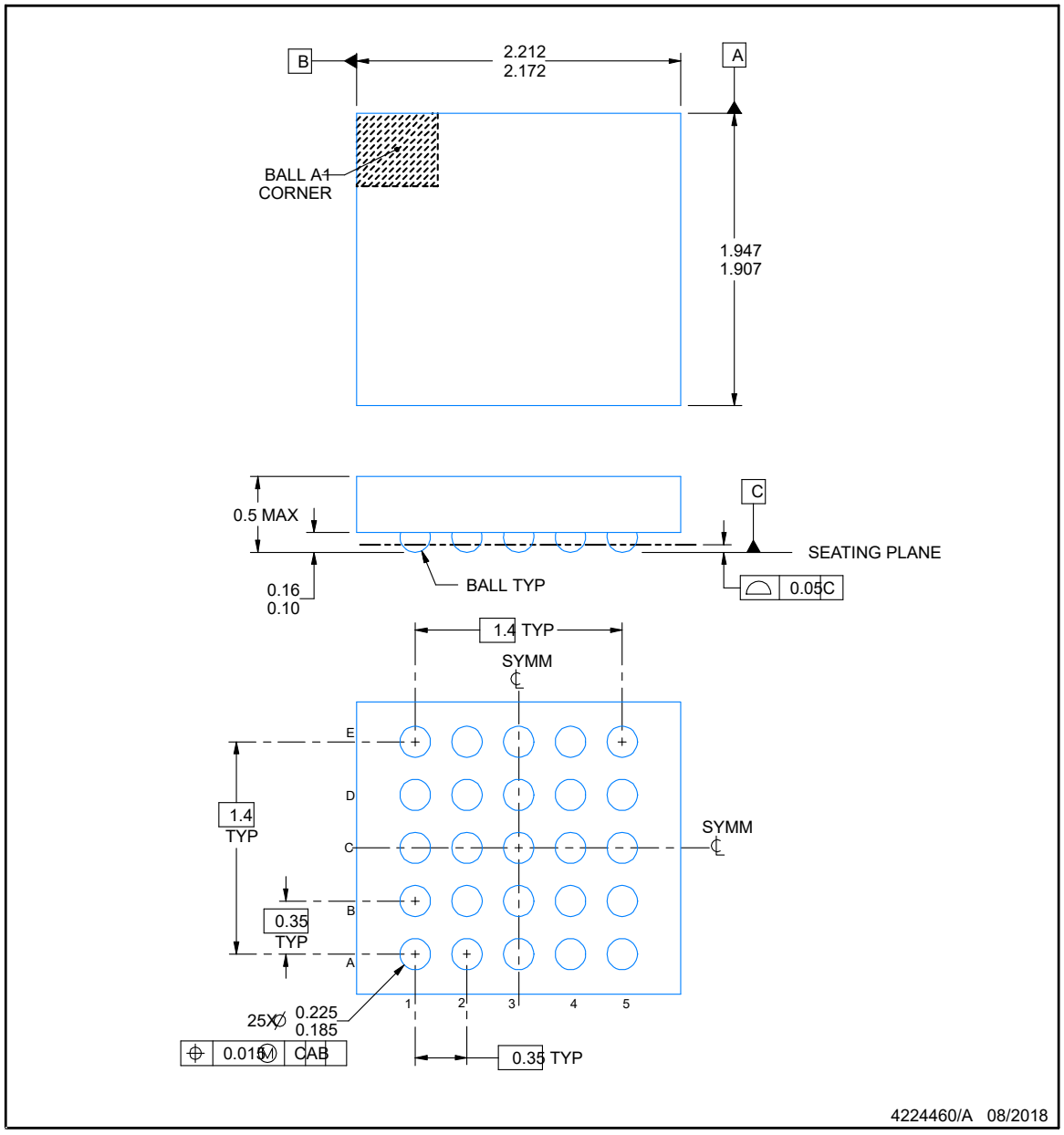


PACKAGE OUTLINE

YCG0025-C01

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

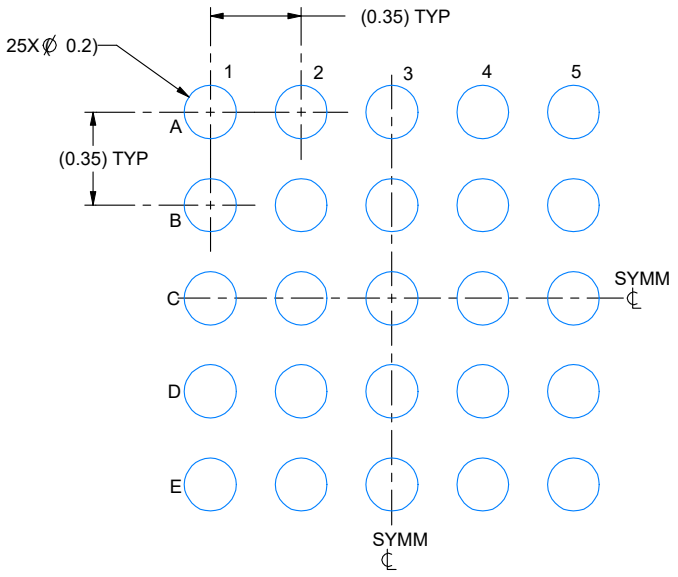
Copyright © 2026 Texas Instruments Incorporated

EXAMPLE BOARD LAYOUT

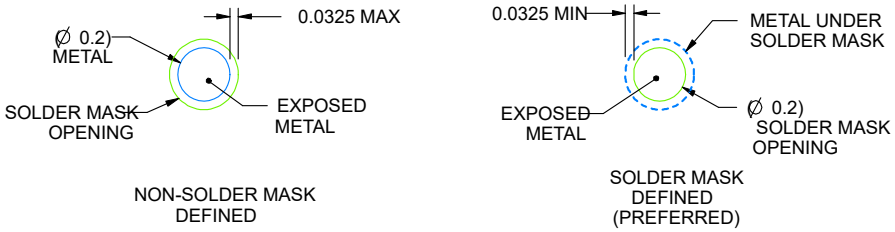
YCG0025-C01

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

4224460/A 08/2018

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

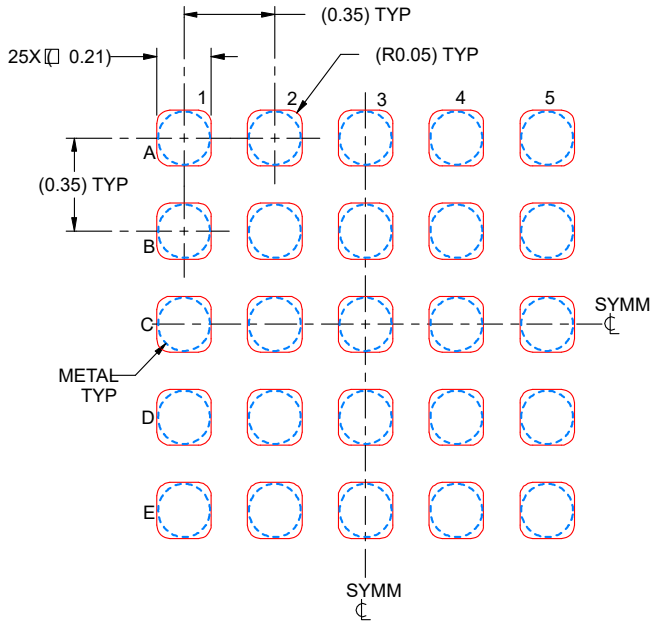
Copyright © 2026 Texas Instruments Incorporated

EXAMPLE STENCIL DESIGN

YCG0025-C01

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 40X

4224460/A 08/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may o?er better paste release.

Copyright © 2026 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM3645YCGR	Active	Production	DSBGA (YCG) | 25	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	LM3645
LM3645YCGR.A	Active	Production	DSBGA (YCG) | 25	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	See LM3645YCGR	LM3645

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

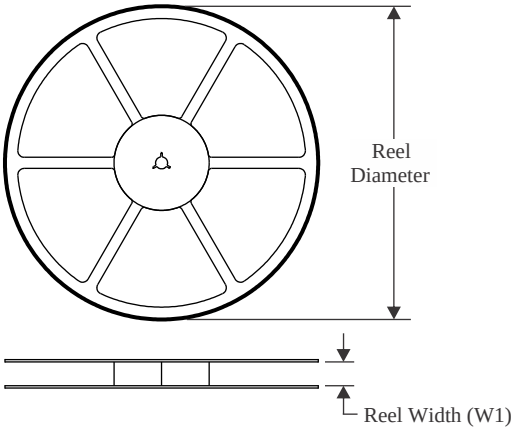
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

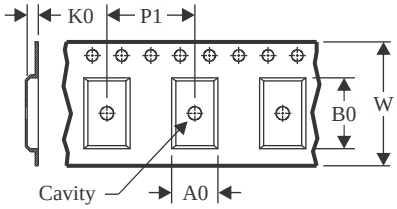
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

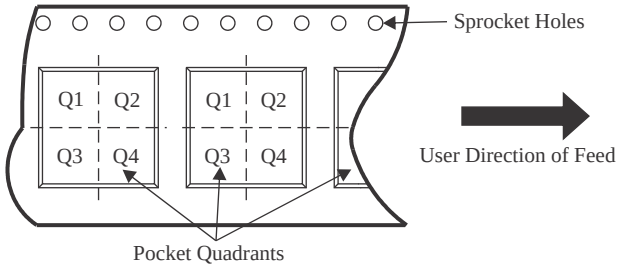


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

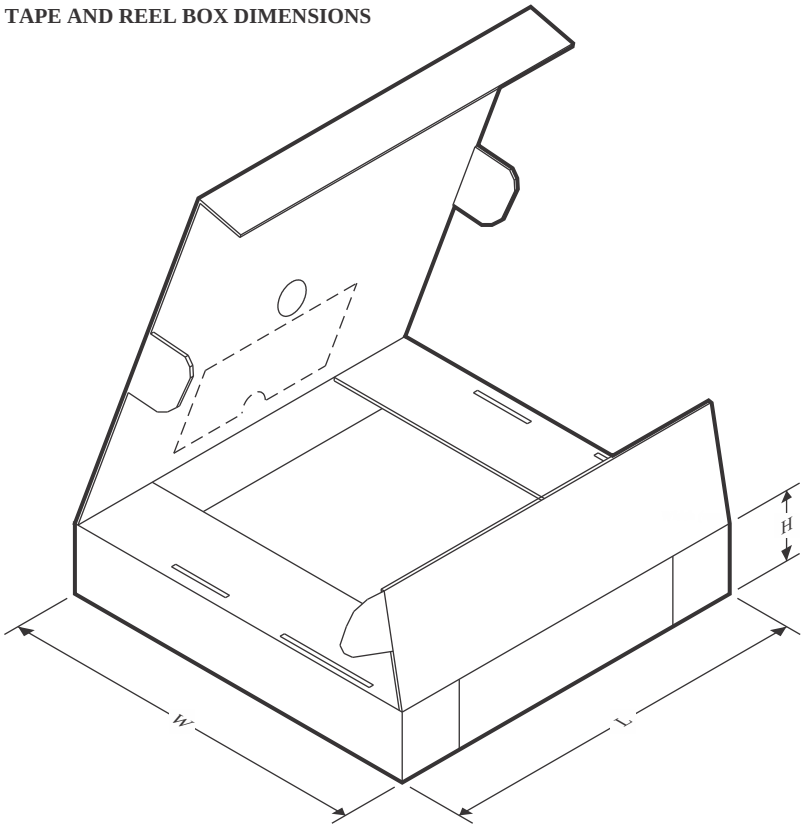
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3645YCGR	DSBGA	YCG	25	3000	180.0	8.4	2.06	2.32	0.7	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3645YCGR	DSBGA	YCG	25	3000	182.0	182.0	20.0

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025