LM4917 Boomer™ Audio Power Amplifier Series Ground-Referenced, 95mW Stereo Headphone Amplifier

Check for Samples: LM4917

FEATURES

- **Ground Referenced Outputs**
- **High PSRR**
- **Available in Space-Saving TSSOP Package**
- **Ultra Low Current Shutdown Mode**
- **Improved Pop and Click Circuitry eliminates Noises During Turn-On and Turn-Off Transitions**
- **1.4 – 3.6V Operation**
- **No Output Coupling Capacitors, Snubber Networks, Bootstrap Capacitors**
- **Shutdown Either Channel Independently**

APPLICATIONS

- **Notebook PCs**
- **Desktop PCs**
- **Mobile Phone**
- **PDAs**
- **Portable Electronic Devices**

KEY SPECIFICATIONS

- **Improved PSRR at 1kHz: 70dB (Typ)**
- **Power Output at V_{DD} = 3V, R_L = 16Ω, THD ≦ 1%: 95mW (Typ)**
- **Shutdown Current: 0.01μA (Typ)**

DESCRIPTION

The LM4917 is a stereo, output capacitor-less headphone amplifier capable of delivering 95mW of continuous average power into a 16Ω load with less than 1% THD+N from a single 3V power supply.

The LM4917 provides high quality audio reproduction with minimal external components. A ground referenced output eliminates the output coupling capacitors typically required by single-ended loads, reducing component count, cost and board space consumption. This makes the LM4917 ideal for mobile phones and other portable equipment where board space is at a premium. Eliminating the output coupling capacitors also improves low frequency response.

The LM4917 operates from a single 1.4V to 3.6V power supply, features low 0.02% THD+N and 70dB PSRR. Independent right/left channel low-power shutdown controls provide power saving flexibility for mono/stereo applications. Superior click and pop suppression eliminates audible transients during start up and shutdown. Short circuit and thermal overload protection protects the device during fault conditions.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Boomer is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2004–2013, Texas Instruments Incorporated

Block Diagram

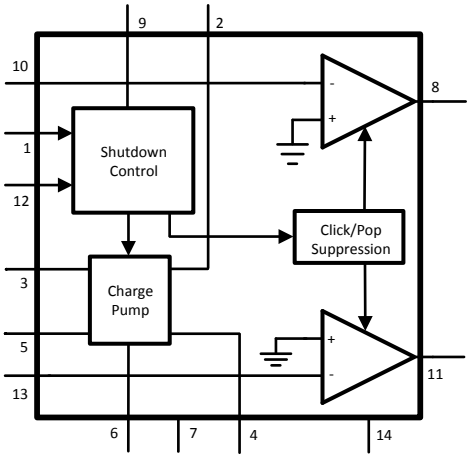


Figure 1. Circuit Block Diagram

Typical Application

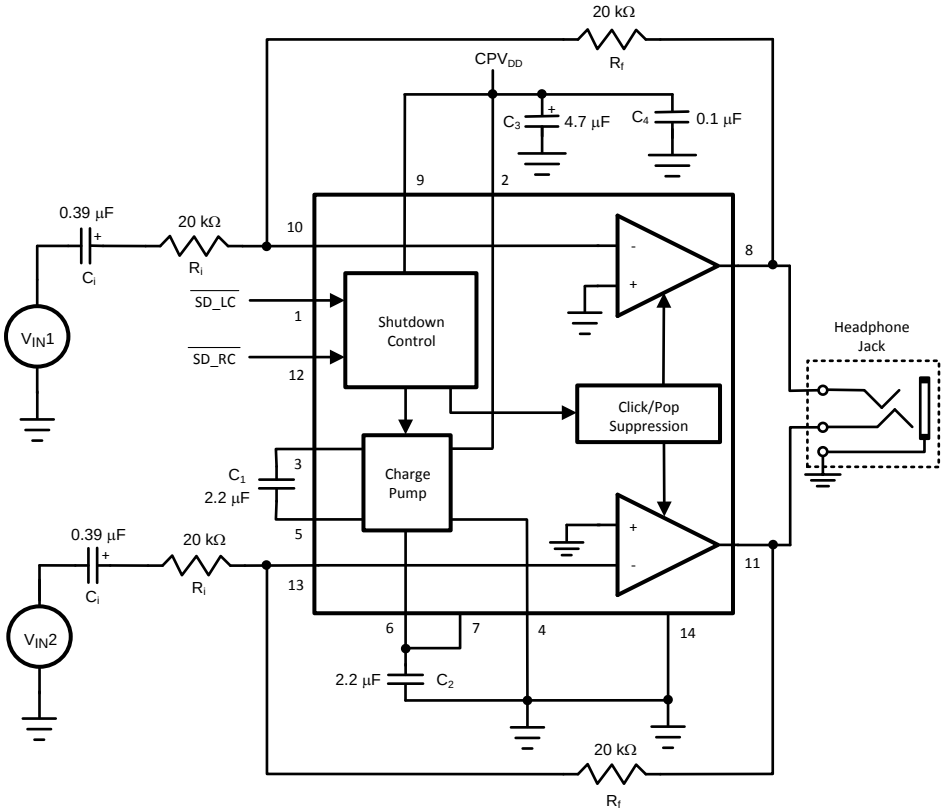
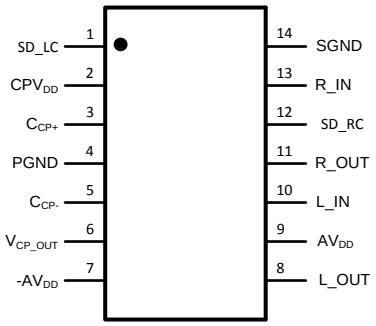
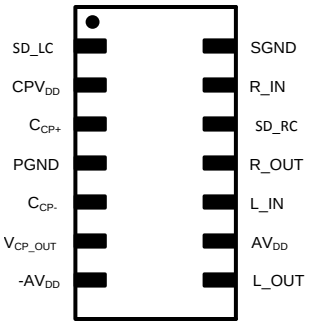


Figure 2. Typical Audio Amplifier Application Circuit

Copyright © 2004–2013, Texas Instruments Incorporated



TSSOP Package
Top View
See Package Number PW



WSON Package
Top View
See Package Number NHK0014A

PIN DESCRIPTIONS

Pin	Name	Function
1	SD_LC	Active_Low Shutdown, Left Channel
2	CP_{VDD}	Charge Pump Power Supply
3	C_{CP+}	Positive Terminal-Charge Pump Flying Capacitor
4	PGND	Power Ground
5	C_{CP-}	Negative Terminal- Charge Pump Flying Capacitor
6	V_{CP_OUT}	Charge Pump Output
7	$-AV_{DD}$	Negative Power Supply-Amplifier
8	L_OUT	Left Channel Output
9	AV_{DD}	Positive Power Supply-Amplifier
10	L_IN	Left Channel Input
11	R_OUT	Right Channel Output
12	SD_RC	Active_Low Shutdown, Right Channel
13	R_IN	Right Channel Input
14	SGND	Signal Ground

Copyright © 2004–2013, Texas Instruments Incorporated

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Absolute Maximum Ratings(1)

Supply Voltage		4.0V
Storage Temperature		−65°C to +150°C
Input Voltage		-0.3V to V_{DD} + 0.3V
Power Dissipation(2)		Internally Limited
ESD Susceptibility(3)		2000V
ESD Susceptibility(4)		200V
Junction Temperature		150°C
Thermal Resistance	θ_{JC} (TSSOP)	40°C/W
	θ_{JA} (TSSOP)	109°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not specify performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions that ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given; however, the typical value is a good indication of device performance.
(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4917, see power de-rating currents for more information.
(3) Human body model, 100pF discharged through a 1.5kΩ resistor.
(4) Machine Model, 220pF-240pF discharged through all pins.

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤ T_A ≤ 85°C
	Supply Voltage (V_{DD})(1)	1.4V ≤ V_{CC} ≤ 3.6V

(1) If the product is in shutdown mode and V_{DD} exceeds 3.6V (to a max of 4V V_{DD}) then most of the excess current will flow through the ESD protection circuits. If the source impedance limits the current to a max of 10mA, then the part will be protected. If the part is enabled when V_{DD} is above 4V circuit performance will be curtailed or the part may be permanently damaged.

Copyright © 2004–2013, Texas Instruments Incorporated

Electrical Characteristics V_{DD} = 3V(1)

The following specifications apply for V_{DD} = 3V, A_V = 1, and 16Ω load unless otherwise specified. Limits apply to T_A = 25°C.

Symbol	Parameter	Conditions	LM4917		Units (Limits)
			Typ(2)	Limit(3)(4)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A, both channels enabled	11	20	mA (max)
		V_{IN} = 0V, I_O = 0A, one channel enabled	9		mA
I_{SD}	Shutdown Current	V_{SD_LC} = V_{SD_RC} = GND	0.01	1	µA (max)
V_{OS}	Output Offset Voltage	R_L = 32Ω	1	10	mV (max)
P_O	Output Power	THD+N = 1% (max); f = 1kHz, R_L = 16Ω	95	50	mW (min)
		THD+N = 1% (max); f = 1kHz, R_L = 32Ω	82		mW
THD+N	Total Harmonic Distortion + Noise	P_O = 50mW, f = 1kHz, R_L = 32Ω (A-weighted) single channel	0.02		%
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV sine p-p, f = 1kHz f = 20kHz	 70 55		dB
SNR	Signal-to-Noise Ratio	R_L = 32Ω, P_{OUT} = 20mW, f = 1kHz	100		dB
V_{IH}	Shutdown Input Voltage High		V_{IH} = 0.7*CPV_{DD}		V (min)
V_{IL}	Shutdown Input Voltage Low		V_{IL} = 0.3*CPV_{DD}		V (max)
T_{WU}	Wake Up Time From Shutdown		339		µs (max)
X_{TALK}	Crosstalk	R_L = 16Ω, P_O = 1.6mW, f = 1kHz	70		dB
I_L	Input Leakage Current		±0.1		nA

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Typicals are measured at 25°C and represent the parametric norm.
(3) Limits are specifed to Texas Instruments' AOQL (Average Outgoing Quality Level).
(4) Datasheet min/max specification limits are specified by design, test, or statistical analysis.

External Components Description

(See Figure 1)

Components		Functional Description
1.	R_i	Inverting input resistance which sets the closed-loop gain in conjunction with R_f. This resistor also forms a high-pass filter with C_i at $f_c = 1 / (2\pi R_i C_i)$.
2.	C_i	Input coupling capacitor which blocks the DC voltage at the amplifier's input terminals. Also creates a high-pass filter with R_i at $f_c = 1 / (2\pi R_i C_i)$. Refer to the section **Proper Selection of External Components,** for an explanation of how to determine the value of C_i.
3.	R_f	Feedback resistance which sets the closed-loop gain in conjunction with R_i.
4.	C_1	Flying capacitor. Low ESR ceramic capacitor (≤100mΩ)
5.	C_2	Output capacitor. Low ESR ceramic capacitor (≤100mΩ)
6.	C_3	Tantalum capacitor. Supply bypass capacitor which provides power supply filtering. Refer to the POWER SUPPLY BYPASSING section for information concerning proper placement and selection of the supply bypass capacitor.
7.	C_4	Ceramic capacitor. Supply bypass capacitor which provides power supply filtering. Refer to the POWER SUPPLY BYPASSING section for information concerning proper placement and selection of the supply bypass capacitor.

Copyright © 2004–2013, Texas Instruments Incorporated

Typical Performance Characteristics

THD+N vs Frequency
V_{DD} = 1.4V, R_L = 32Ω, P_O = 1mW

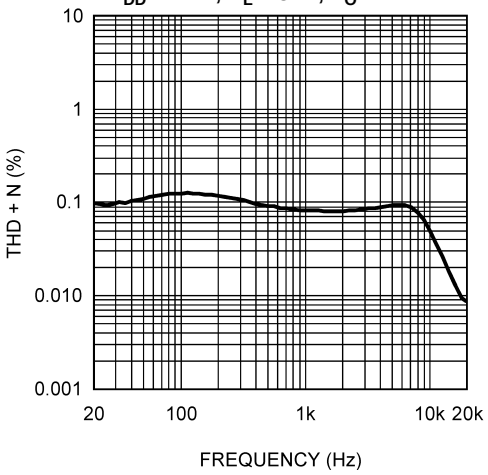


Figure 3.

THD+N vs Frequency
V_{DD} = 1.8V, R_L = 16Ω, P_O = 5mW

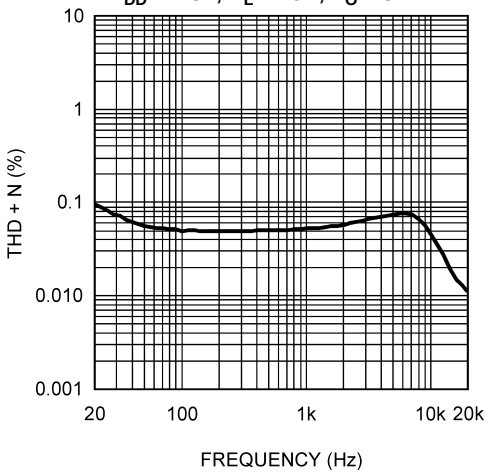


Figure 4.

THD+N vs Frequency
V_{DD} = 1.8V, R_L = 32Ω, P_O = 5mW

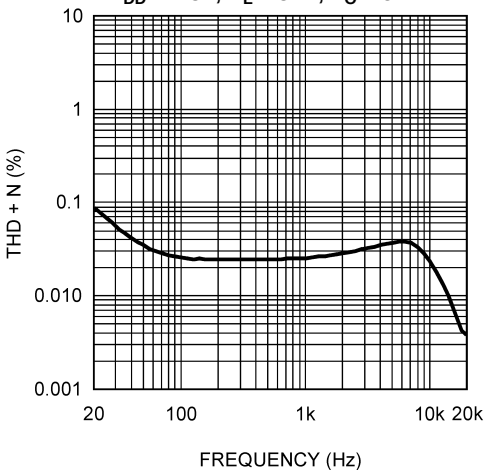


Figure 5.

THD+N vs Frequency
V_{DD} = 1.8V, R_L = 32Ω, P_O = 10mW

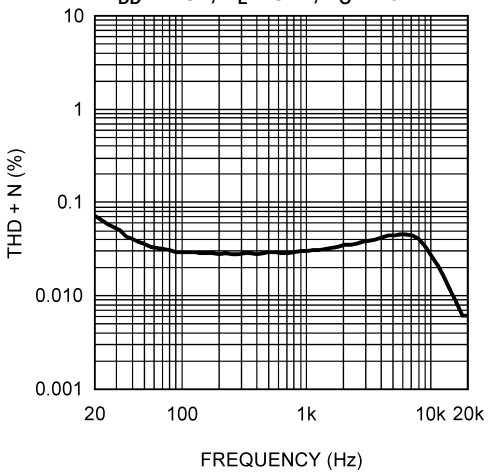


Figure 6.

THD+N vs Frequency
V_{DD} = 3.0V, R_L = 16Ω, P_O = 10mW

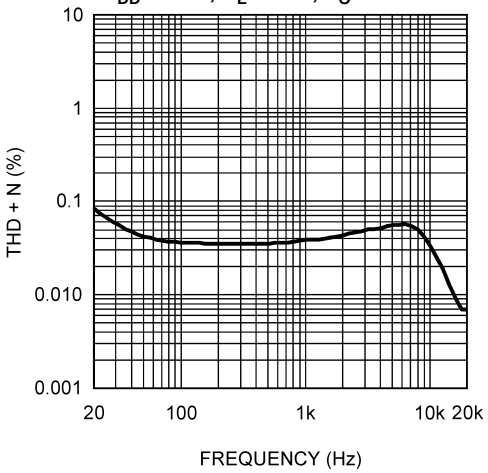


Figure 7.

THD+N vs Frequency
V_{DD} = 3.0V, R_L = 16Ω, P_O = 25mW

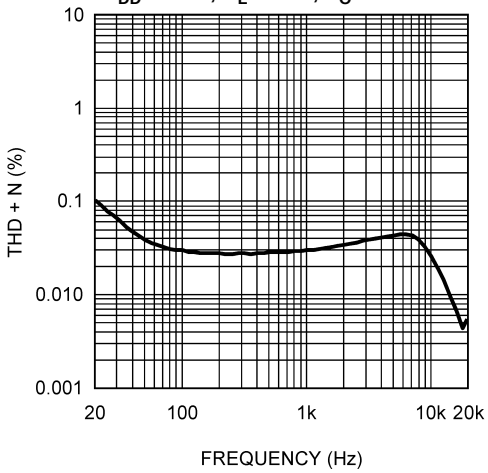


Figure 8.

Copyright © 2004–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

THD+N vs Frequency
V_{DD} = 3.0V, R_L = 16Ω, P_O = 50mW

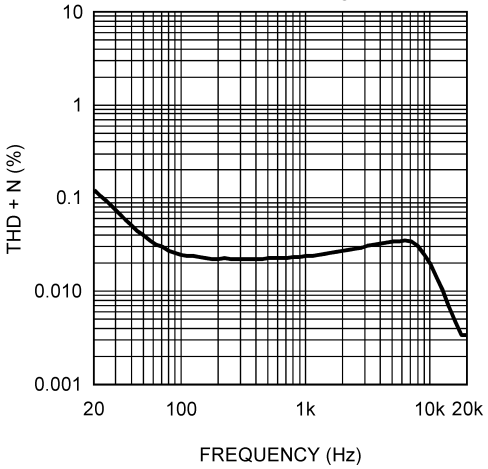


Figure 9.

THD+N vs Frequency
V_{DD} = 3.0V, R_L = 32Ω, P_O = 5mW

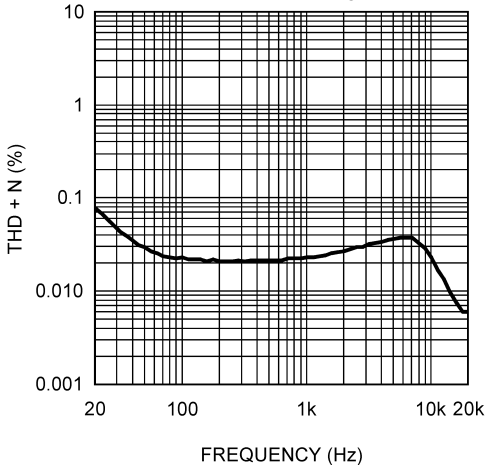


Figure 10.

THD+N vs Frequency
V_{DD} = 3.0V, R_L = 32Ω, P_O = 10mW

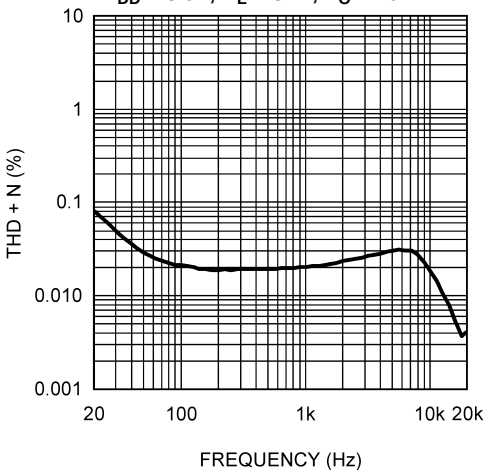


Figure 11.

THD+N vs Frequency
V_{DD} = 3.0V, R_L = 32Ω, P_O = 25mW

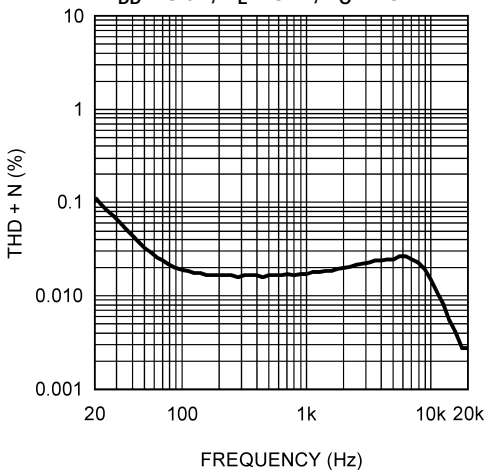


Figure 12.

Gain Flatness vs Frequency
R_{IN} = 20kΩ, C_{IN} = 0.39µF

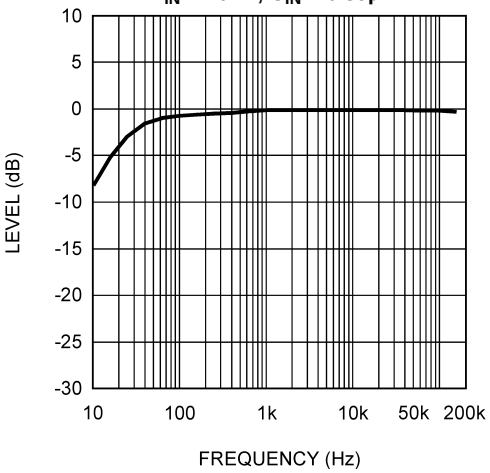


Figure 13.

Output Power vs Supply Voltage
R_L = 16Ω

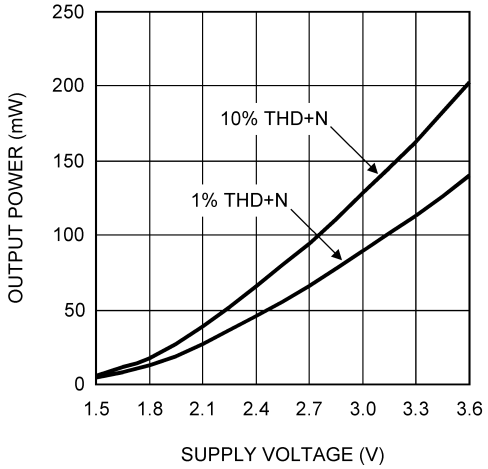


Figure 14.

Typical Performance Characteristics (continued)

Output Power vs Supply Voltage
R_L = 32Ω

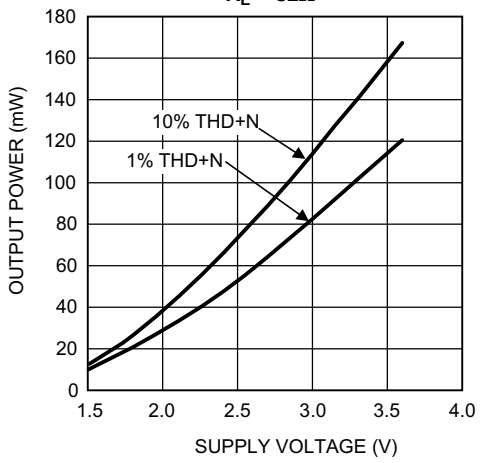


Figure 15.

PSRR vs Frequency
V_{DD} = 1.8V, R_L = 16Ω

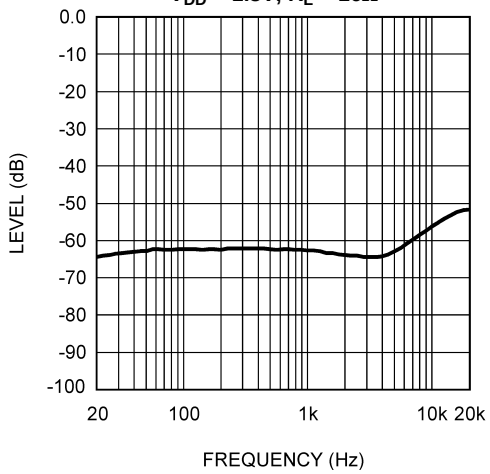


Figure 16.

PSRR vs Frequency
V_{DD} = 1.8V, R_L = 32Ω

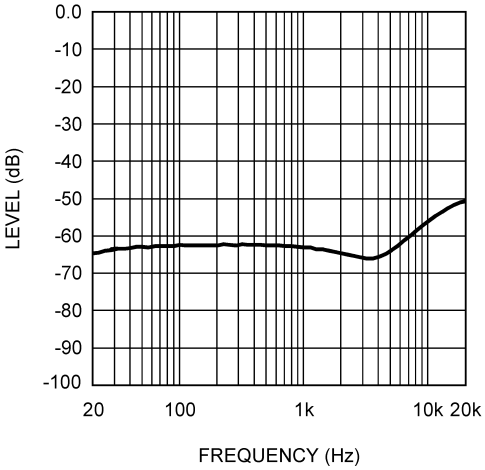


Figure 17.

PSRR vs Frequency
V_{DD} = 3.0V, R_L = 16Ω

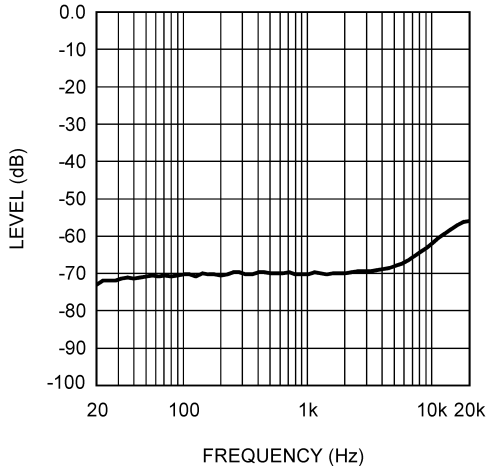


Figure 18.

PSRR vs Frequency
V_{DD} = 3.0V, R_L = 32Ω

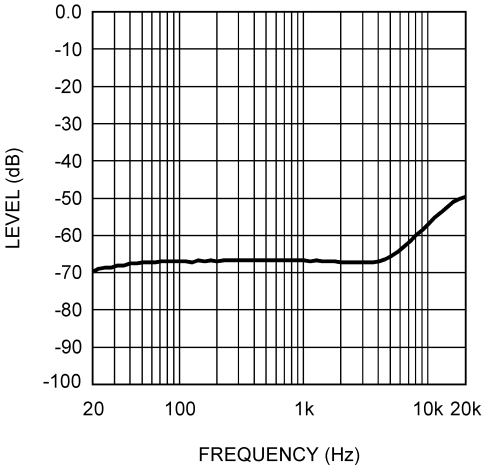


Figure 19.

THD+N vs Output Power
V_{DD} = 1.4V, R_L = 32Ω, f = 1kHz

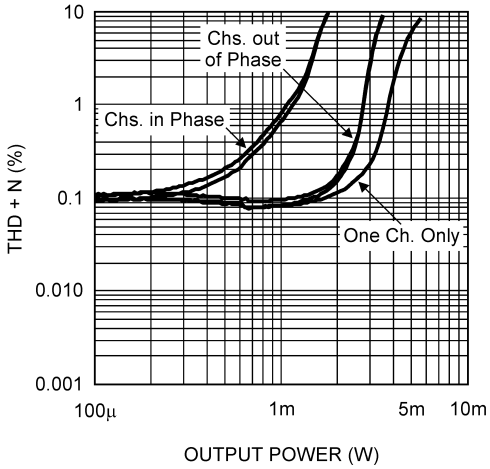


Figure 20.

Copyright © 2004–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

THD+N vs Output Power
V_{DD} = 1.8V, R_L = 16Ω, f = 1kHz

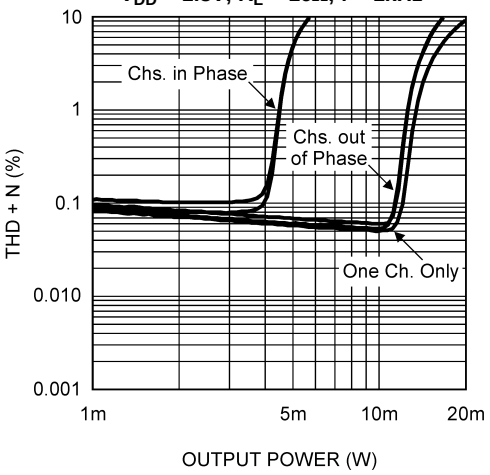


Figure 21.

THD+N vs Output Power
V_{DD} = 1.8V, R_L = 32Ω, f = 1kHz

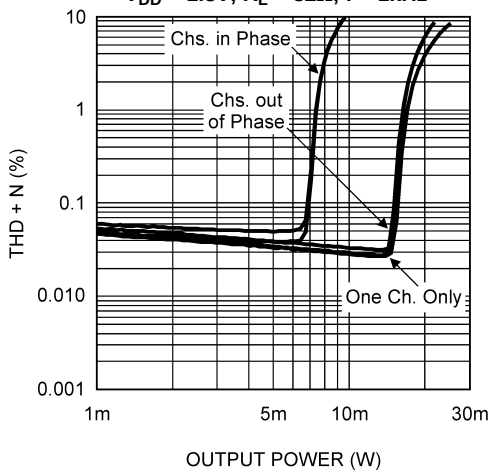


Figure 22.

THD+N vs Output Power
V_{DD} = 3.0V, R_L = 16Ω, f = 1kHz

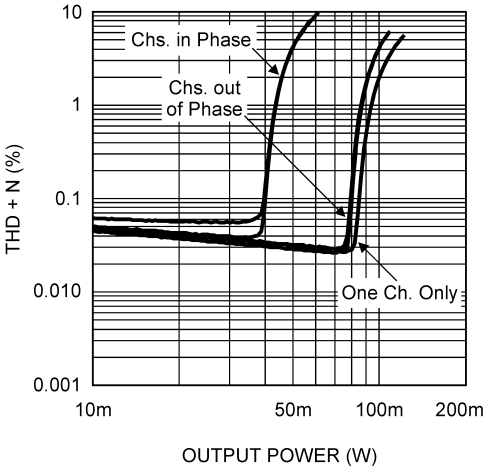


Figure 23.

THD+N vs Output Power
V_{DD} = 3.0V, R_L = 32Ω, f = 1kHz

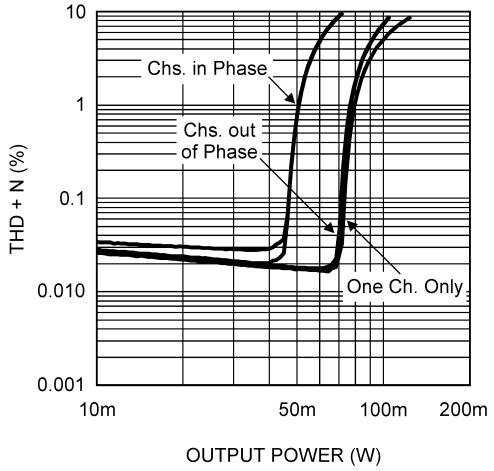


Figure 24.

Power Dissipation vs Output Power
V_{DD} = 1.8V, R_L = 16Ω

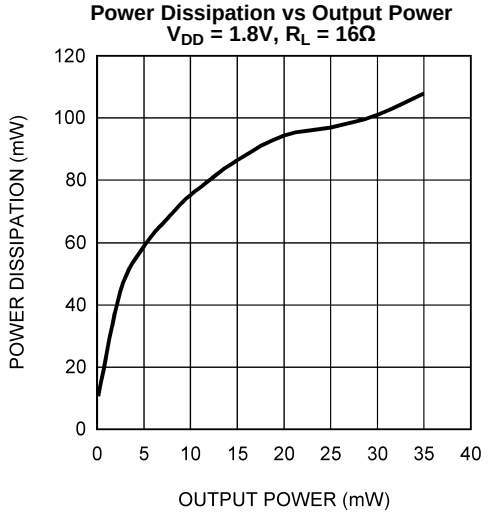


Figure 25.

Power Dissipation vs Output Power
V_{DD} = 1.8V, R_L = 32Ω

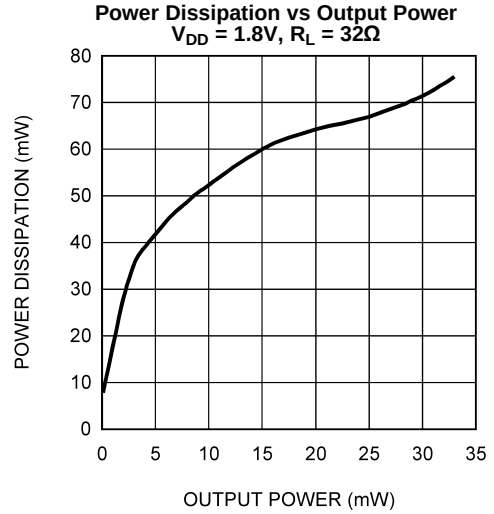


Figure 26.

Typical Performance Characteristics (continued)

Power Dissipation vs Output Power
V_{DD} = 3V, R_L = 16Ω

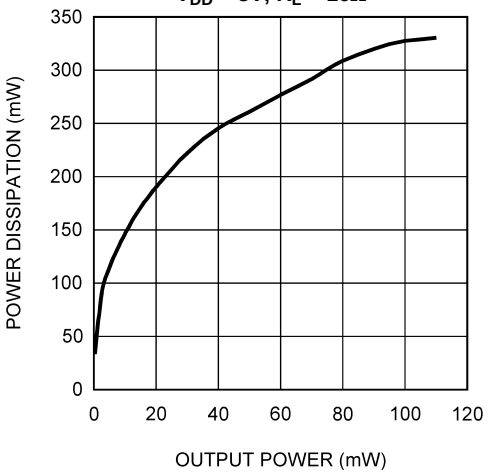


Figure 27.

Power Dissipation vs Output Power
V_{DD} = 3V, R_L = 32Ω

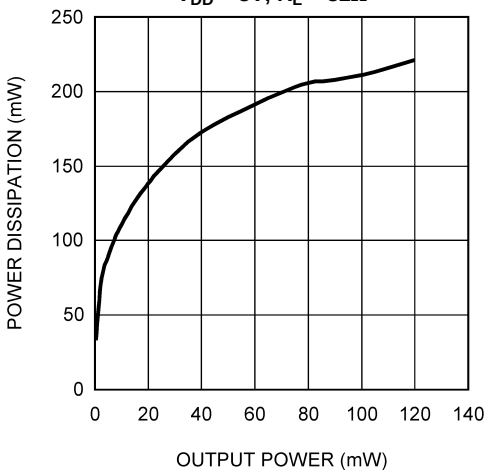


Figure 28.

Supply Current vs Supply Voltage

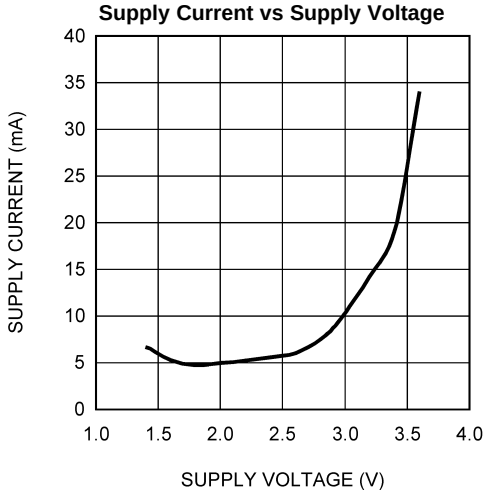


Figure 29.

Copyright © 2004–2013, Texas Instruments Incorporated

APPLICATION INFORMATION

ELIMINATING THE OUTPUT COUPLING CAPACITOR

The LM4917 features a low noise inverting charge pump that generates an internal negative supply voltage. This allows the outputs of the LM4917 to be biased about GND instead of a nominal DC voltage, like traditional headphone amplifiers. Because there is no DC component, the large DC blocking capacitors (typically 220µF) are not necessary. The coupling capacitors are replaced by two, small ceramic charge pump capacitors, saving board space and cost.

Eliminating the output coupling capacitors also improves low frequency response. The headphone impedance and the output capacitor form a high pass filter that not only blocks the DC component of the output, but also attenuates low frequencies, impacting the bass response. Because the LM4917 does not require the output coupling capacitors, the low frequency response of the device is not degraded by external components.

In addition to eliminating the output coupling capacitors, the ground referenced output nearly doubles the available dynamic range of the LM4917 when compared to a traditional headphone amplifier operating from the same supply voltage.

OUTPUT TRANSIENT ('CLICK AND POPS') ELIMINATED

The LM4917 contains advanced circuitry that virtually eliminates output transients ('clicks and pops'). This circuitry prevents all traces of transients when the supply voltage is first applied or when the part resumes operation after coming out of shutdown mode.

To ensure optimal click and pop performance under low gain configurations (less than 0dB), it is critical to minimize the RC combination of the feedback resistor R_F and stray input capacitance at the amplifier inputs. A more reliable way to lower gain or reduce power delivered to the load is to place a current limiting resistor in series with the load as explained in the **Minimizing Output Noise / Reducing Output Power** section.

AMPLIFIER CONFIGURATION EXPLANATION

As shown in Figure 2, the LM4917 has two operational amplifiers internally. The two amplifiers have externally configurable gain, and the closed loop gain is set by selecting the ratio of R_f to R_i. Consequently, the gain for each channel of the IC is

$$A_V = -(R_f / R_i) \quad (1)$$

Since this an output ground-referenced amplifier, by driving the headphone through R_{OUT} (Pin 11) and L_{OUT} (Pin 8), the LM4917 does not require output coupling capacitors. The typical single-ended amplifier configuration where one side of the load is connected to ground requires large, expensive output capacitors.

POWER DISSIPATION

Power dissipation is a major concern when using any power amplifier and must be thoroughly understood to ensure a successful design. Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \quad (2)$$

Since the LM4917 has two operational amplifiers in one package, the maximum internal power dissipation point is twice that of the number which results from Equation 2. Even with the large internal power dissipation, the LM4917 does not require heat sinking over a large range of ambient temperature. From Equation 2, assuming a 3V power supply and a 16Ω load, the maximum power dissipation point is 28mW per amplifier. Thus the maximum package dissipation point is 56mW. The maximum power dissipation point obtained must not be greater than the power dissipation that results from Equation 3:

$$P_{DMAX} = (T_{JMAX} - T_A) / (\theta_{JA}) \quad (3)$$

Copyright © 2004–2013, Texas Instruments Incorporated

For package TSSOP, θ_{JA} = 109°C/W. T_{JMAX} = 150°C for the LM4917. Depending on the ambient temperature, T_A, of the system surroundings, Equation 3 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 2 is greater than that of Equation 3, then either the supply voltage must be decreased, the load impedance increased or T_A reduced. For the typical application of a 3V power supply, with a 16Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 119.9°C provided that device operation is around the maximum power dissipation point. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature may be increased accordingly. Refer to the Typical Performance Characteristics curves for power dissipation information for lower output powers.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 3V power supply typically use a 4.7µF in parallel with a 0.1µF ceramic filter capacitors to stabilize the power supply's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 0.1µF supply bypass capacitor, C_S, connected between the LM4917's supply pins and ground. Keep the length of leads and traces that connect capacitors between the LM4917's power supply pin and ground as short as possible.

MICRO POWER SHUTDOWN

The voltage applied to the $\overline{\text{SD_LC}}$ (shutdown left channel) pin and the $\overline{\text{SD_RC}}$ (shutdown right channel) pin controls the LM4917's shutdown function. When active, the LM4917's micropower shutdown feature turns off the amplifiers' bias circuitry, reducing the supply current. The trigger point is 0.3*CPV_{DD} for a logic-low level, and 0.7 x CPV_{DD} for logic-high level. The low 0.01µA(typ) shutdown current is achieved by appling a voltage that is as near as ground a possible to the $\overline{\text{SD_LC}}$/$\overline{\text{SD_RC}}$ pins. A voltage that is higher than ground may increase the shutdown current.

There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 100kΩ pull-up resistor between the $\overline{\text{SD_LC}}$/$\overline{\text{SD_RC}}$ pins and V_{DD}. Connect the switch between the $\overline{\text{SD_LC}}$/$\overline{\text{SD_RC}}$ pins and ground. Select normal amplifier operation by opening the switch. Closing the switch connects the $\overline{\text{SD_LC}}$/$\overline{\text{SD_RC}}$ pins to ground, activating micro-power shutdown. The switch and resistor ensure that the $\overline{\text{SD_LC}}$/$\overline{\text{SD_RC}}$ pins will not float. This prevents unwanted state changes. In a system with a microprocessor or microcontroller, use a digital output to apply the control voltage to the $\overline{\text{SD_LC}}$/$\overline{\text{SD_RC}}$ pins. Driving the $\overline{\text{SD_LC}}$/$\overline{\text{SD_RC}}$ pins with active circuitry eliminates the pull-up resistor.

SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the LM4917's performance requires properly selecting external components. Though the LM4917 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The LM4917 is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of $1V_{RMS}$ ($2.83V_{P-P}$). Please refer to the AUDIO POWER AMPLIFIER DESIGN section for more information on selecting the proper gain.

Charge Pump Capacitor Selection

Choose low ESR (<100mΩ) ceramic capacitors for optimum performance. Low ESR capacitors keep the charge pump output impedance to a minimum, extending the headroom on the negative supply. Choose capacitors with an X7R dielectric for best performance over temperature.

Charge pump load regulation and output resistance is affected by the value of the flying capacitor (C1). A larger valued C1 improves load regulation and minimizes charge pump output resistance. The switch on-resistance and capacitor ESR dominates the output resistance for capacitor values above 2.2µF.

The output ripple is affected by the value and ESR of the output capacitor (C2). Larger valued capacitors reduce output ripple on the negative power supply. Lower ESR capacitors minimizes the output ripple and reduces the output resistance of the charge pump.

 Copyright © 2004–2013, Texas Instruments Incorporated

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor (C_i in Figure 2). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using high value input and output capacitors.

Besides affecting system cost and size, C_i has an effect on the LM4917's click and pop performance. The magnitude of the pop is directly proportional to the input capacitor's size. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired −3dB frequency.

As shown in Figure 2, the input resistor, R_i and the input capacitor, C_i, produce a -3dB high pass filter cutoff frequency that is found using Equation (3).

$$f_{i\text{-}3dB} = 1 / 2\pi R_i C_i \tag{4}$$

Also, careful consideration must be taken in selecting a certain type of capacitor to be used in the system. Different types of capacitors (tantalum, electrolytic, ceramic) have unique performance characteristics and may affect overall system performance.

AUDIO POWER AMPLIFIER DESIGN

Design a Dual 90mW/16Ω Audio Amplifier

Given:	
Power Output	90mW
Load Impedance	16Ω
Input Level	1Vrms (max)
Input Impedance	20kΩ
Bandwidth	100Hz–20kHz ± 0.50dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs Supply Voltage curve in the Typical Performance Characteristics section. Another way, using Equation 5, is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. For a single-ended application, the result is Equation 5.

$$V_{opeak} = \sqrt{(2R_L P_O)} \tag{5}$$

$$V_{DD} \geq [2V_{OPEAK} + (V_{DOTOP} + V_{DOBOT})] \tag{6}$$

The Output Power vs Supply Voltage graph for a 16Ω load indicates a minimum supply voltage of 3.1V. This is easily met by the commonly used 3.3V supply voltage. The additional voltage creates the benefit of headroom, allowing the LM4917 to produce peak output power in excess of 90mW without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates maximum power dissipation as explained above in the POWER DISSIPATION section. Remember that the maximum power dissipation point from Equation 2 must be multiplied by two since there are two independent amplifiers inside the package. Once the power dissipation equations have been addressed, the required gain can be determined from Equation 7.

$$A_V \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \tag{7}$$

Thus, a minimum gain of 1.2 allows the LM4917 to reach full output swing and maintain low noise and THD+N perfromance. For this example, let $A_V = 1.5$.

The amplifiers overall gain is set using the input (R_i) and feedback (R_f) resistors. With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation (7).

$$A_V = R_f / R_i$$

where

- The value of R_f is 30kΩ (8)

The last step in this design is setting the amplifier's −3db frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at lease one−fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are

$$f_L = 100Hz / 5 = 20Hz \quad (9)$$

and

$$f_H = 20kHz \times 5 = 100kHz \quad (10)$$

As stated in the External Components Description section, both R_i in conjunction with C_i, and R_L, create first order highpass filters. Thus to obtain the desired low frequency response of 100Hz within ±0.5dB, both poles must be taken into consideration. The combination of two single order filters at the same frequency forms a second order response. This results in a signal which is down 0.34dB at five times away from the single order filter −3dB point. Thus, a frequency of 20Hz is used in the following equations to ensure that the response is better than 0.5dB down at 100Hz.

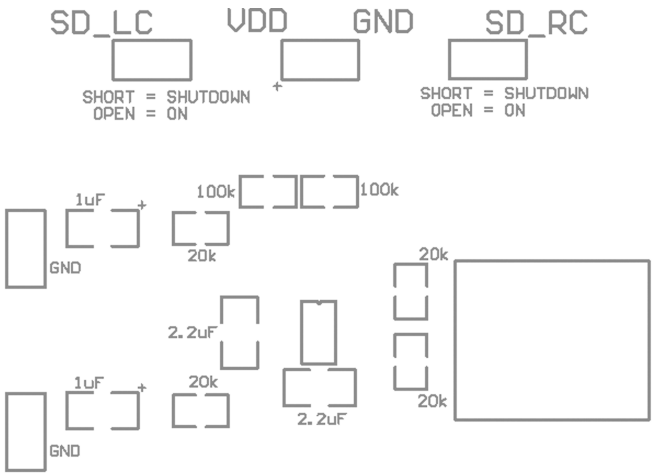
$$C_i \geq 1 / (2\pi*20k\Omega*20Hz) = 0.397\mu F; \text{ use } 0.39\mu F \quad (11)$$

The high frequency pole is determined by the product of the desired high frequency pole, f_H, and the closed-loop gain, A_V. With a closed-loop gain of 1.5 and f_H = 100kHz, the resulting GBWP = 150kHz which is much smaller than the LM4917's GBWP of 3MHz. This figure displays that if a designer has a need to design an amplifier with a higher gain, the LM4917 can still be used without running into bandwidth limitations.

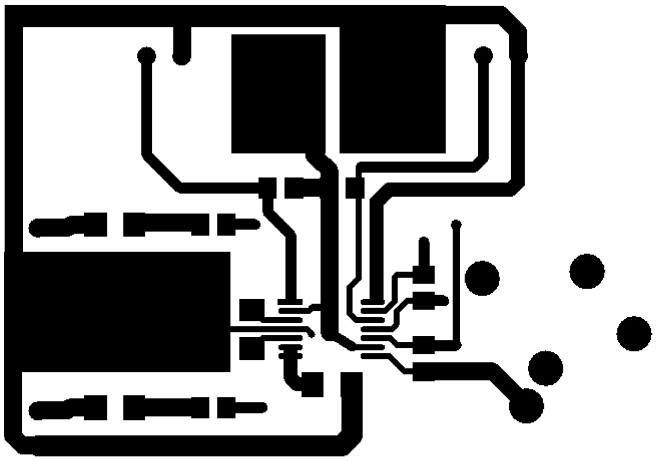
Copyright © 2004–2013, Texas Instruments Incorporated

LM4917 TSSOP Demo Board Artwork

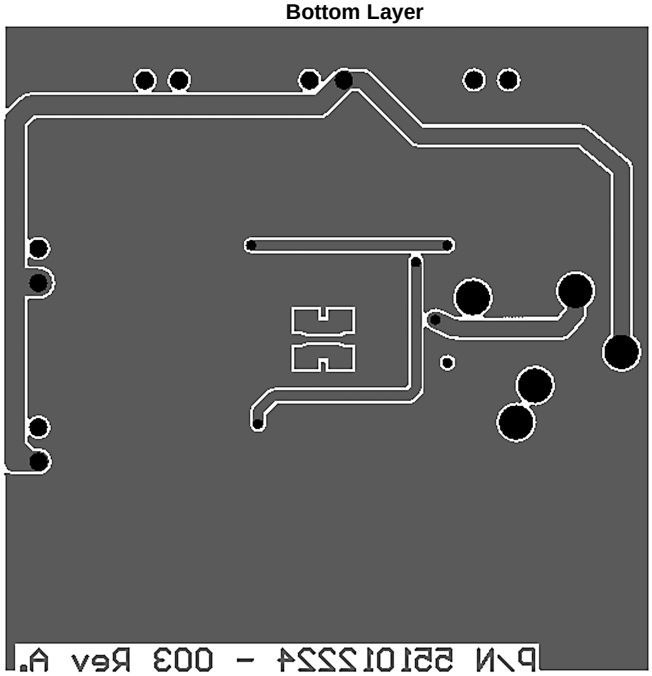
Top Overlay



Top Layer

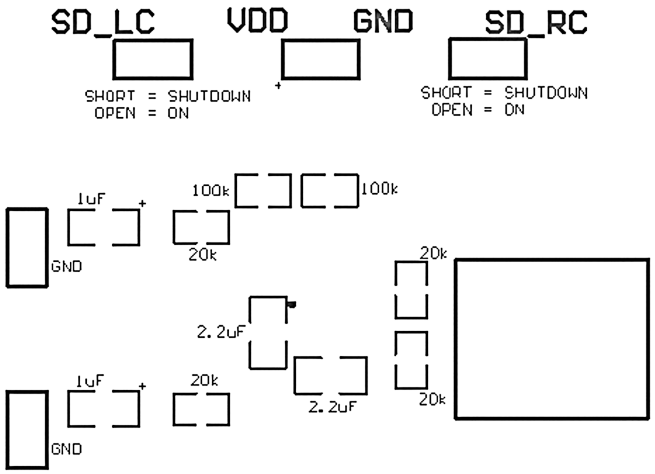


Bottom Layer

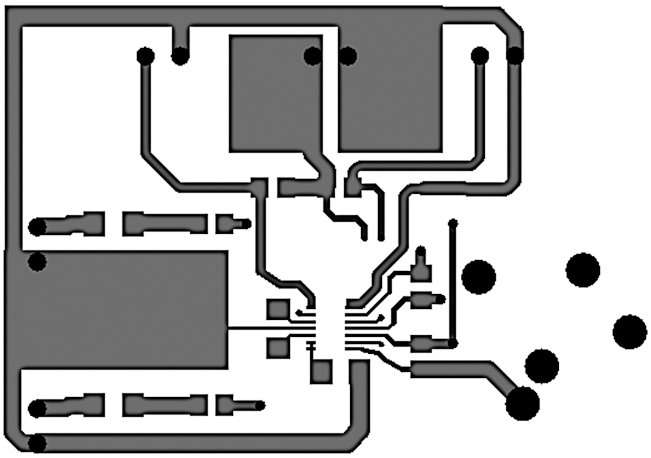


LM4917 WSON Demo Board Artwork

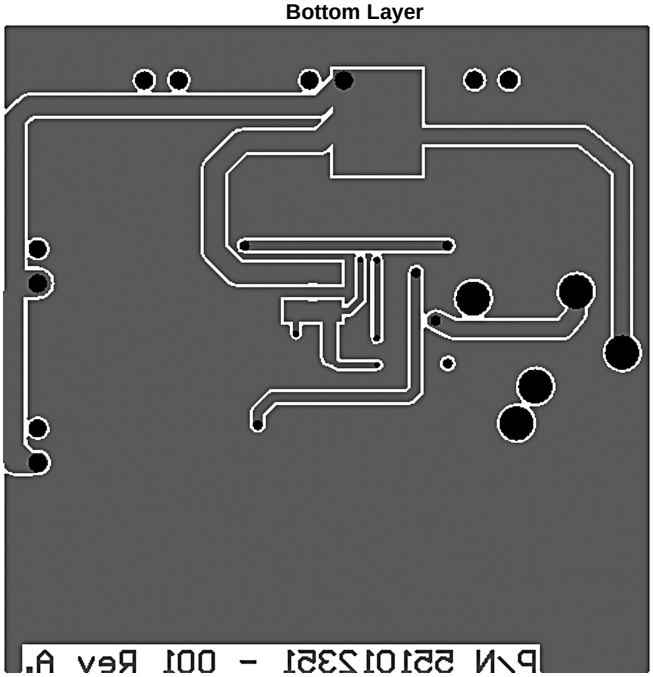
Top Overlay



Top Layer



Bottom Layer



Copyright © 2004–2013, Texas Instruments Incorporated

LM4917 Reference Design Boards Bill Of Materials

Part Description	Qty	Ref Designator
LM4917 Mono Reference Design Board	1	
LM4917 Audio AMP	1	U1
Tantalum Cap 1µF 16V 10	1	Cs
Ceramic Cap 0.39µF 50V Z50 20	2	Ci
Resistor 20kΩ 1/10W 5	4	Ri, Rf
Resistor 100kΩ 1/10W 5	1	Rpu
Jumper Header Vertical Mount 2X1, 0.100	1	J1

PCB Layout Guidelines

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results will depend heavily on the final layout.

Avoiding Shorts on the Charge Pump Outputs

For the LM4917SD package, the exposed dap is connected to the substrate of the device. Because LM4917's charge pump is powered by both a negative and positive supply the exposed dap must be left floating. This will avoid shorting the charge pump outputs.

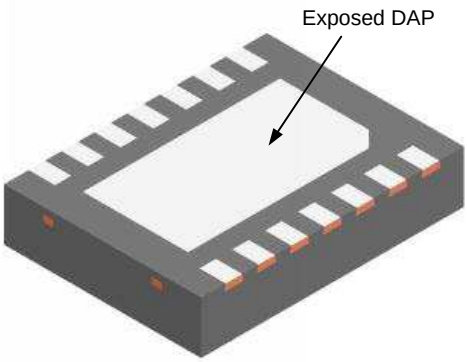


Figure 30. Bottom View of LM4917SD Package

Minimization of THD

PCB trace impedance on the power, ground, and all output traces should be minimized to achieve optimal THD performance. Therefore, use PCB traces that are as wide as possible for these connections. As the gain of the amplifier is increased, the trace impedance will have an ever increasing adverse affect on THD performance. At unity-gain (0dB) the parasitic trace impedance effect on THD performance is reduced but still a negative factor in the THD performance of the LM4917 in a given application.

General Mixed Signal Layout Recommendation

Power and Ground Circuits

For two layer mixed signal design, it is important to isolate the digital power and ground trace paths from the analog power and ground trace paths. Star trace routing techniques (bringing individual traces back to a central point rather than daisy chaining traces together in a serial manner) can greatly enhance low level signal performance. Star trace routing refers to using individual traces to feed power and ground to each circuit or even device. This technique will require a greater amount of design time, but will not increase the final price of the board. The only extra parts required may be some jumpers.

Copyright © 2004–2013, Texas Instruments Incorporated

Single-Point Power / Ground Connections

The analog power traces should be connected to the digital traces through a single point (link). A "PI-filter" can be helpful in minimizing high frequency noise coupling between the analog and digital sections. Further, place digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

Placement of Digital and Analog Components

All digital components and high-speed digital signal traces should be located as far away as possible from analog components and circuit traces.

Avoiding Typical Design / Layout Problems

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.

Copyright © 2004–2013, Texas Instruments Incorporated

REVISION HISTORY

Changes from Revision F (May 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM4917MT/NOPB	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	L4917 MT
LM4917MT/NOPB.A	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	L4917 MT
LM4917MTX/NOPB	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	L4917 MT
LM4917MTX/NOPB.A	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	L4917 MT
LM4917SD/NOPB	Active	Production	WSON (NHK) | 14	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	L4917
LM4917SD/NOPB.A	Active	Production	WSON (NHK) | 14	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	L4917

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

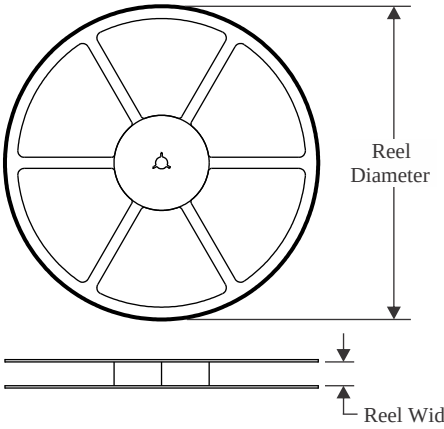
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

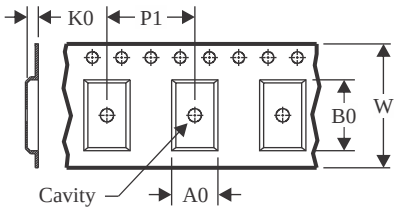
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

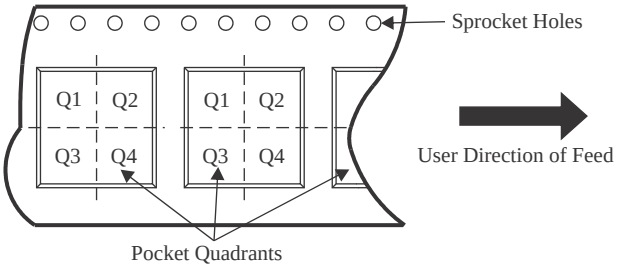


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

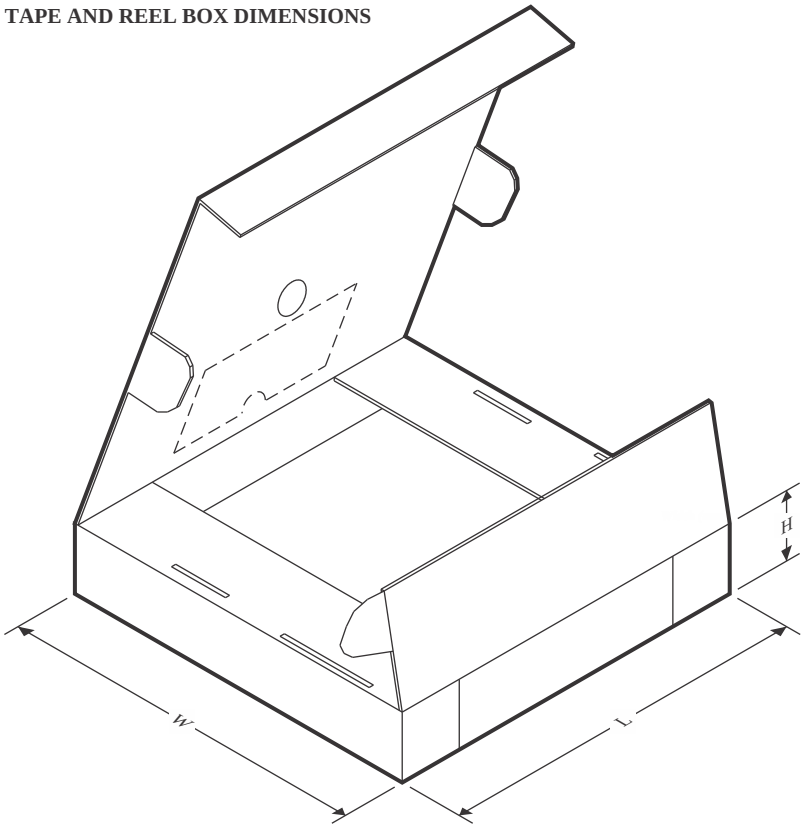
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4917MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM4917SD/NOPB	WSON	NHK	14	1000	177.8	12.4	3.3	4.3	1.0	8.0	12.0	Q1

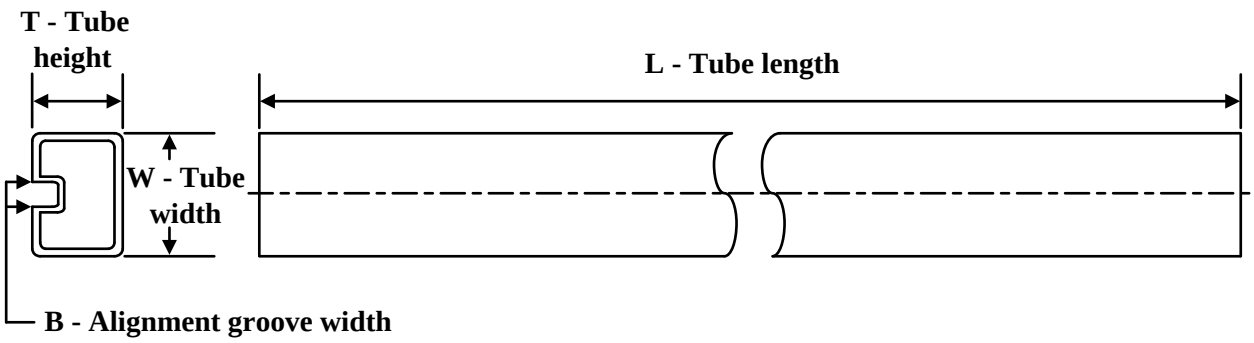
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4917MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LM4917SD/NOPB	WSON	NHK	14	1000	208.0	191.0	35.0

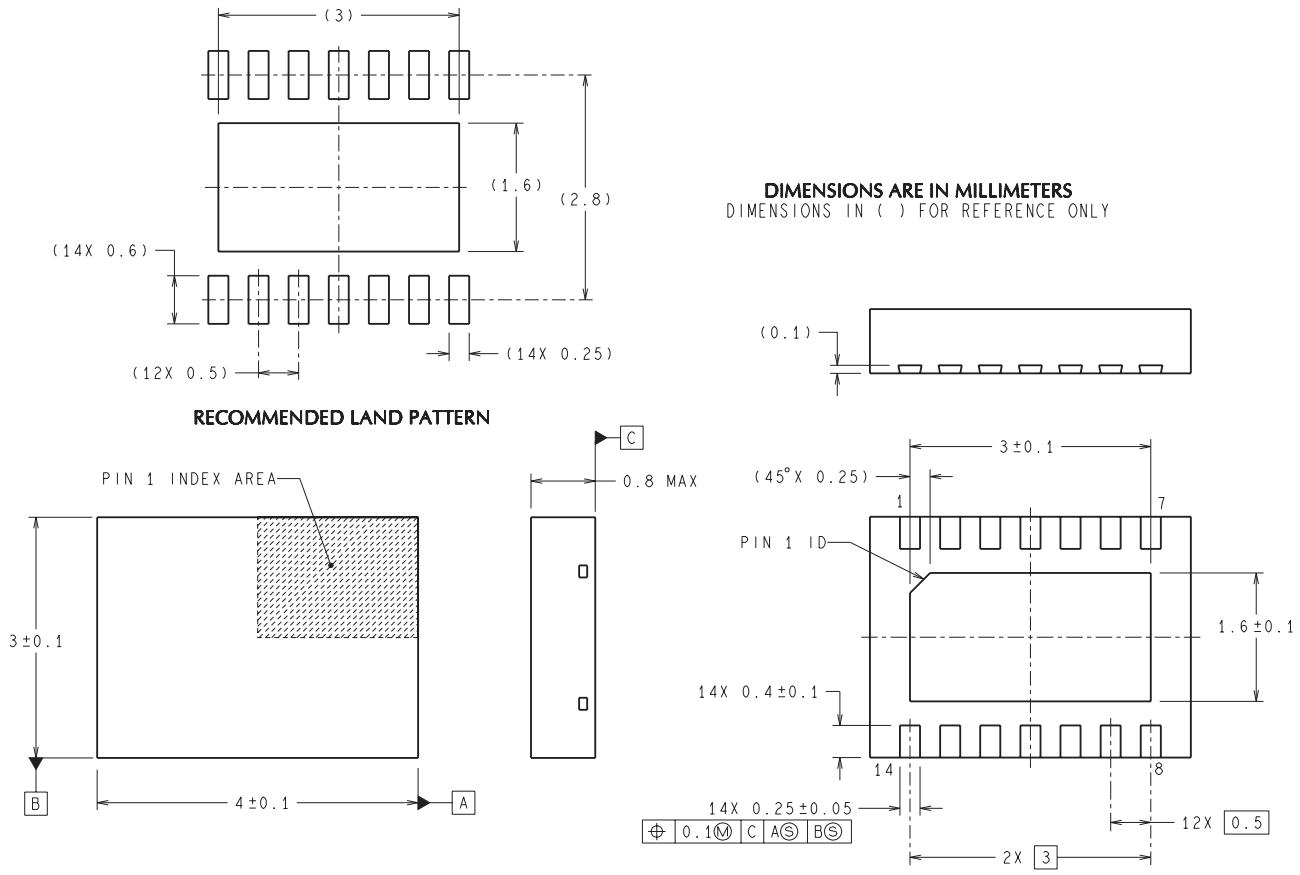
TUBE



*All dimensions are nominal

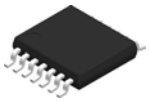
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM4917MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06
LM4917MT/NOPB.A	PW	TSSOP	14	94	495	8	2514.6	4.06

NHK0014A



SDA14A (Rev A)

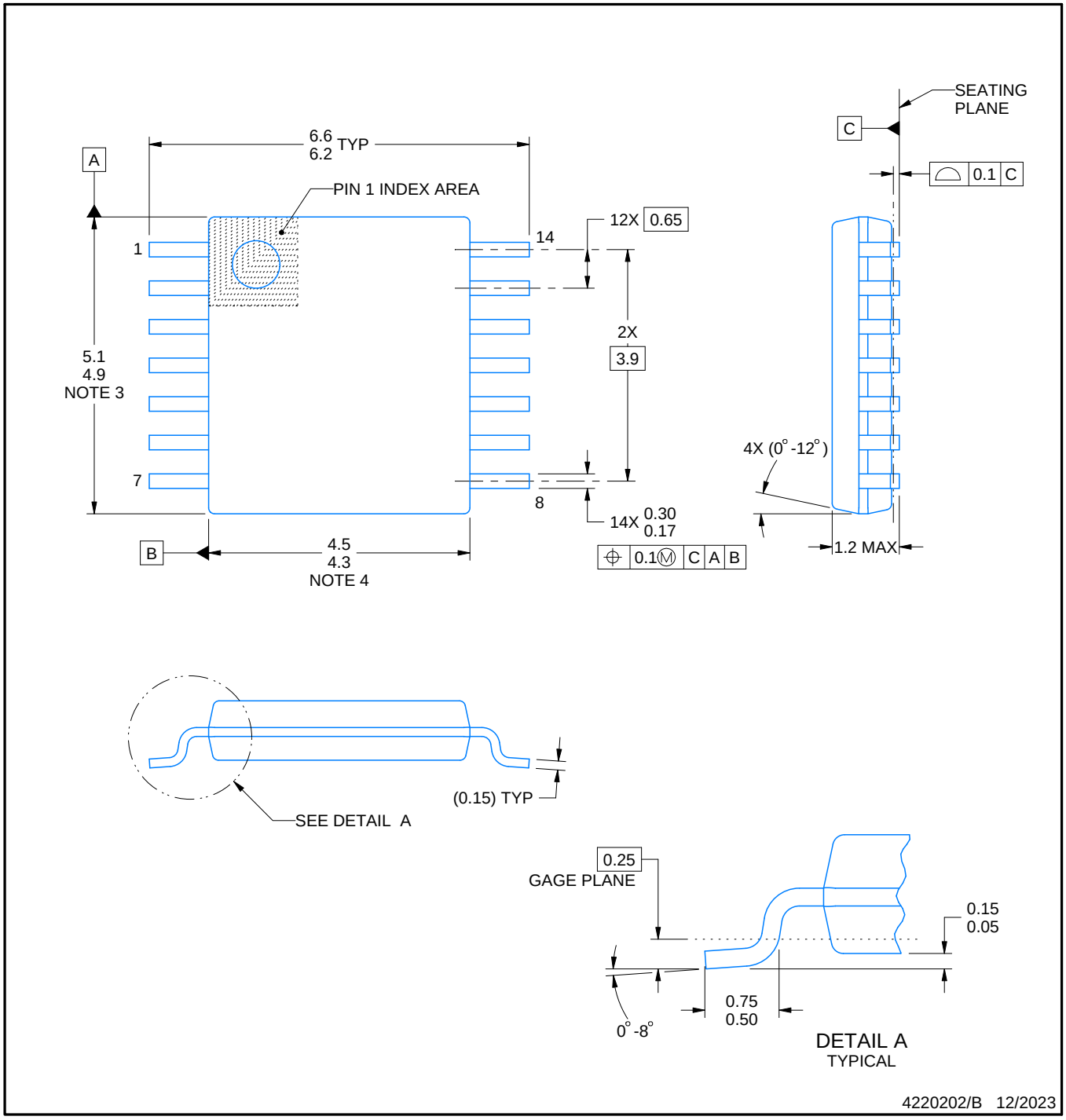
PW0014A



PACKAGE OUTLINE

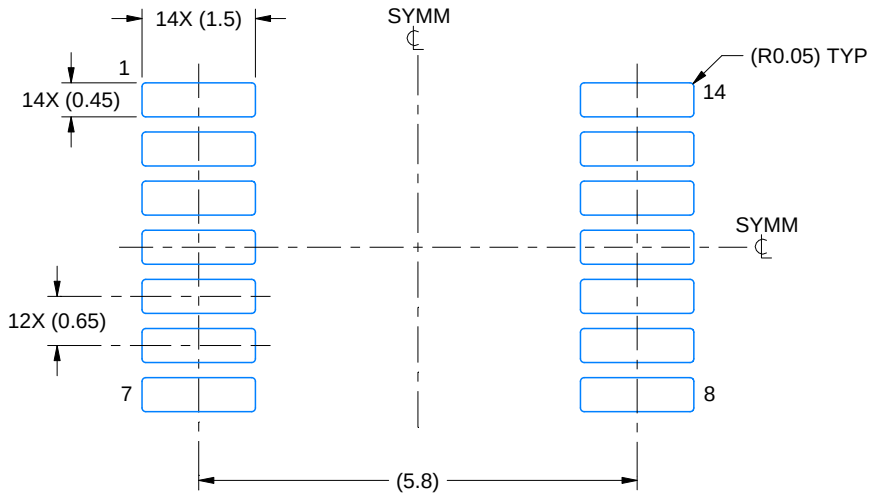
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

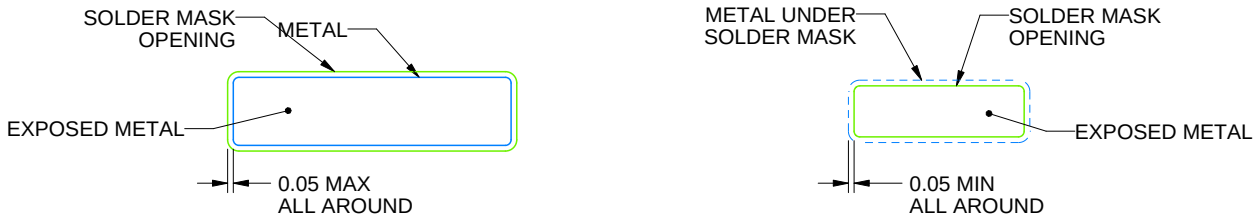


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

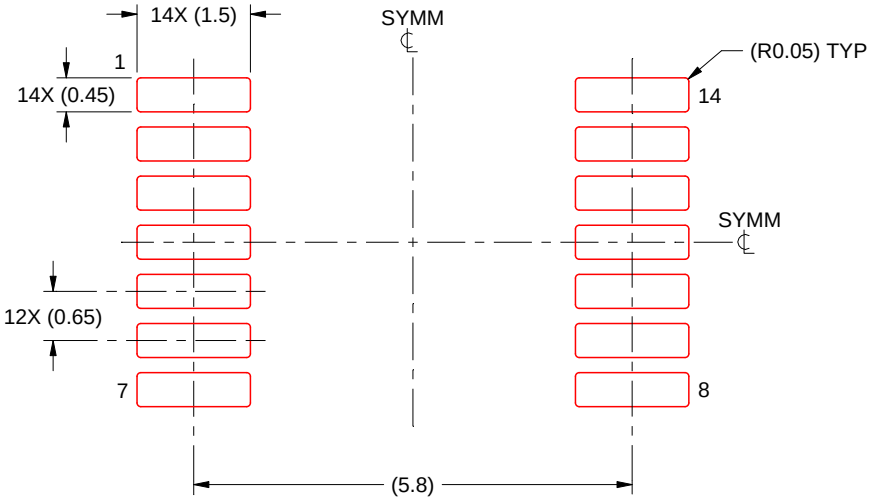
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025