LM5023 AC-DC Quasi-Resonant Current Mode PWM Controller

1 Features

- Critical conduction mode
- Peak-current mode control
- Skip-cycle mode for low-standby power
- Hiccup mode for continuous overload protection
- Cycle-by-cycle overcurrent protection maintains accuracy over the universal AC line
- Line-voltage feedforward
- OVP protection by sensing the auxiliary winding
- Integrated 0.7A peak gate driver
- Direct optocoupler interface
- Leading edge blanking of current sense signal
- Maximum frequency clamp 130kHz
- Programmable soft-start
- Thermal shutdown
- 8-pin VSSOP package
- Create a custom design using the LM5023 with the WEBENCH® Power Designer

2 Applications

- Universal input AC-to-DC notebook adapters from 10W to 65W
- High-efficiency housekeeping and auxiliary power supplies
- Battery chargers
- Consumer electronics (DVD players, set-top boxes, DTV, gaming, printers)

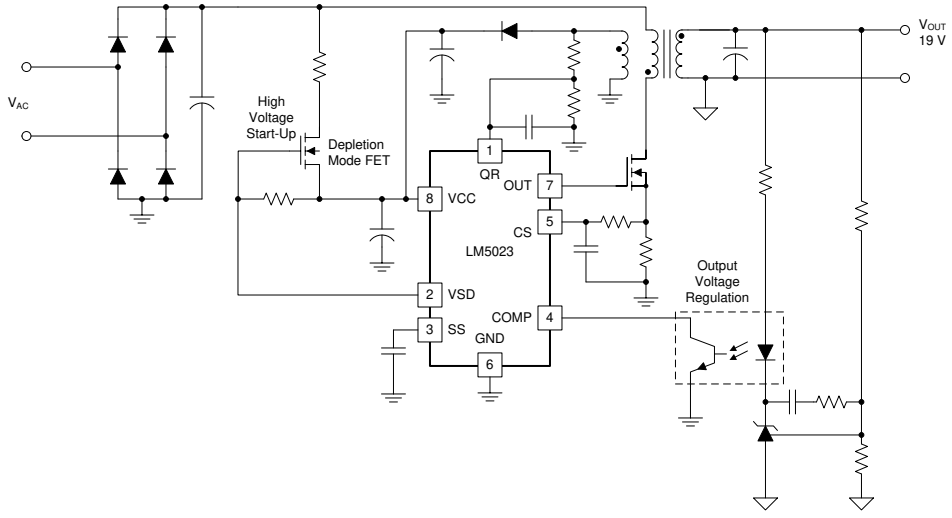
3 Description

The LM5023 is a quasi-resonant pulse width modulated (PWM) controller which contains all of the features needed to implement a highly efficient off-line power supply. The LM5023 uses the transformer auxiliary winding for demagnetization detection to establish critical conduction mode (CrCM) operation. The LM5023 features a hiccup mode for overcurrent protection with an auto restart to reduce the stress on the power components during an overload. A skip-cycle mode reduces power consumption at light loads for energy conservation applications (ENERGY STAR®, CEPCP, and so forth). The LM5023 also uses the transformer auxiliary winding for output overvoltage protection (OVP); if an OVP fault is detected the LM5023 latches off the controller.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LM5023	DGK (VSSOP, 8)	3.00mm × 3.00mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....3
5 Specifications....4
5.1 Absolute Maximum Ratings....4
5.2 ESD Ratings....4
5.3 Recommended Operating Conditions....4
5.4 Thermal Information....4
5.5 Electrical Characteristics....5
5.6 Typical Characteristics....7
6 Detailed Description....9
6.1 Overview....9
6.2 Functional Block Diagram....10
6.3 Feature Description....11
6.4 Device Functional Modes....17
7 Application and Implementation....19
7.1 Application Information....19
7.2 Typical Application....19
7.3 Power Supply Recommendations....28
7.4 Layout....28
8 Device and Documentation Support....30
8.1 Device Support....30
8.2 Documentation Support....30
8.3 Receiving Notification of Documentation Updates....30
8.4 Community Resources....30
8.5 Trademarks....30
9 Revision History....30
10 Mechanical, Packaging, and Orderable Information....31

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4 Pin Configuration and Functions

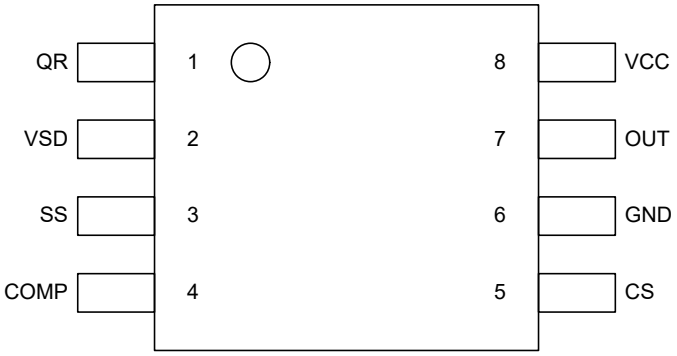


Figure 4-1. DGK Package8-Pin VSSOP Top View

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
COMP	4	I	Control input for the pulse width modulator and skip cycle comparators. COMP pullup is provided by an internal 42kΩ resistor which can be used to bias an optocoupler transistor.
CS	5	I	Current sense input for current-mode control and overcurrent protection. Current limiting is accomplished using a dedicated current sense comparator. If the CS comparator input exceeds 0.5V, the OUT pin switches low for cycle-by-cycle current limit. CS is held low for 130ns after OUT switches high to blank the leading edge current spike.
GND	6	G	Ground connection return for internal circuits.
OUT	7	O	High current output to the external MOSFET gate input with source/sink current capability of 0.3A and 0.7A respectively.
QR	1	I	The auxiliary flyback winding of the power transformer is monitored to detect the quasi-resonant operation. The peak-auxiliary voltage is sensed to detect an output overvoltage (OVP) fault and shuts down the controller.
SS	3	O	An external capacitor and an internal 22µA current source sets the soft-start ramp.
VSD	2	O	Connect this pin to the gate of the external start-up circuit FET; it disables the start-up FET after VCC is valid.
VCC	8	P	VCC provides bias to controller and gate drive sections of the LM5023. An external capacitor must connect from this pin to ground.

(1) I = input, O = output, P = power, G = ground

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
I_{QR}	Negative injection current when the QR pin is being driven below ground			4	mA
VSD	Maximum voltage		–0.3	45	V
I_{VSD}	VSD clamp continuous current			500	µA
V_{IN}	Voltage range	SS, COMP, QR	–0.3	7	V
		CS	–0.3	1.25	V
OUT	Gate-drive voltage at DRV		–0.3	Self-limiting	V
I_{OUT}	Peak OUT current, source			0.3	A
I_{OUT}	Peak OUT current sink			0.7	A
VCC	Bias supply voltage		–0.3	16	V
T_J	Operating junction temperature		–40	125	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
VCC	Bias supply voltage	8	14	V
I_{VSD}	VSD Current	2	100	µA
I_{QR}	QR pin current	1	4	mA
T_J	Junction temperature	–40	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		LM5023 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	168.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	88.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	87.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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5.5 Electrical Characteristics

Minimum and maximum apply over the junction temperature range of –40 to +125°C. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at +25°C, and are provided for reference purposes only. Unless otherwise specified, the following conditions apply:
VCC = 10V, F_{SW} = 100kHz 50% duty cycle, no load on OUT.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS SUPPLY INPUT						
VCC_{ON}	Controller enable threshold		12	12.8	13.5	V
VCC_{OFF}	Minimum operating voltage		7	7.5	8	V
V_{RST}	Internal logic reset (fault latch)	VCC falling < V_{RST}	4.5	5	5.5	V
ICC_{ST}	ICC current while in standby mode	COMP = 0.5V, CS = 0V, no switching		340	420	µA
ICC_{OP}	Operating supply current	COMP = 2.25V, OUT switching		800		µA
SHUTDOWN CONTROL (VSD PIN)						
$I_{VSD\ OFF}$	Off state leakage current			0.1		µA
$V_{VSD\ ON1}$	ON state pulldown voltage at 10 µA	After VCC_{ON} (I_{VSD} = 10 µA)		0.65		V
V_{VSD_ON2}	ON state pulldown voltage at 100 µA	After VCC_{ON} (I_{VSD} = 100 µA)		0.84		V
SKIP CYCLE MODE COMPARATOR						
V_{SKIP}	Skip cycle mode enable threshold	COMP falling	70	120	170	mV
V_{SK-HYS}	Skip cycle mode hysteresis			12		mV
QR DETECT						
V_{OVP}	Overvoltage comparator threshold		2.85	3	3.17	V
T_{OVP}	Sample delay for OVP		870	1050	1270	ns
V_{DEM}	VDEM demagnetization threshold			0.35		V
F_{MAX}	Maximum frequency		114	130	148	kHz
T_{RST}	$T_{RESTART}$		9.4	12	15.7	µs
PWM COMPARATORS						
T_{PPWM}	COMP to OUT propagation delay	COMP set to 2V, CS stepped 0 to 0.4V, time to OUT transition low, C_{LOAD} = 0		20		ns
D_{MIN}	Minimum duty cycle	COMP = 0V			0%	
G_{COMP}	COMP to PWM comparator gain			0.33		
V_{COMP-O}	COMP open circuit voltage	I_{COMP} = 20 µA	4.3	4.9	5.8	V
V_{COMP-H}	COMP at maximum VCS			2.25		V
I_{COMP}	COMP short circuit current	COMP = 0V		–132		µA
R_{COMP}	R pullup		41	45	49	kΩ
CURRENT LIMIT						
V_{CS}	Cycle-by-cycle sense voltage limit threshold		450	500	550	mV
T_{LEB}	Leading edge blanking time			130		ns
T_{PCS}	Current limit to OUT delay	CS step from 0 to 0.6V time to onset of OUT transition low, C_{LOAD} = 0		22		ns
R_{LEB}	CS blanking sinking impedance			15	35	Ω
G_{CM}	Current mirror gain	I_{QR} = 2mA		100		A/A
V_{FF}	Line-current feedforward	I_{QR} = 2mA		140		mV
HICCUP MODE						
T_{OL}_10	Over load detection timer	I_{VSD}= 10 µA		12		ms
T_{OL}_100	Over load detection timer	I_{VSD}= 100 µA		1.2		ms
OUTPUT GATE DRIVER						
V_{OH}	OUT high saturated	I_{OUT} = 50mA, VCC-OUT		0.3	1.1	V

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Minimum and maximum apply over the junction temperature range of –40 to +125°C. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at +25°C, and are provided for reference purposes only. Unless otherwise specified, the following conditions apply:
VCC = 10V, F_{SW} = 100kHz 50% duty cycle, no load on OUT.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	OUT low saturated	I_{OUT} = 100mA		0.3	1	V
I_{PH}	Peak OUT source current	OUT = VCC/2		0.3		A
I_{PL}	Peak OUT sink current	OUT = VCC/2		0.7		A
t_r	Rise time	C_{LOAD} = 1nF		25		ns
t_f	Fall time	C_{LOAD} = 1nF		15		ns
SOFT-START						
I_{SS}	Soft-start current		17	22	30	µA
THERMAL						
T_{SD}	Thermal shutdown temperature			165		°C

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5.6 Typical Characteristics

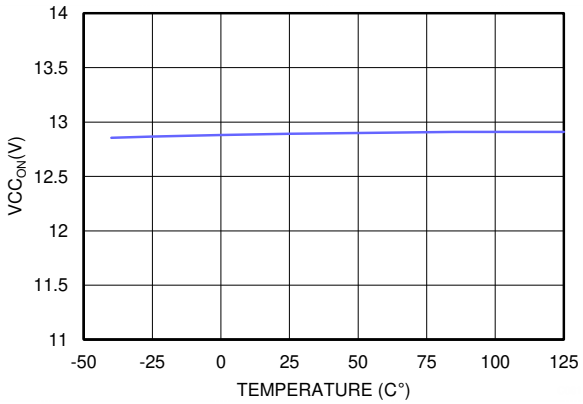


Figure 5-1. VCC_{ON} vs. Temperature

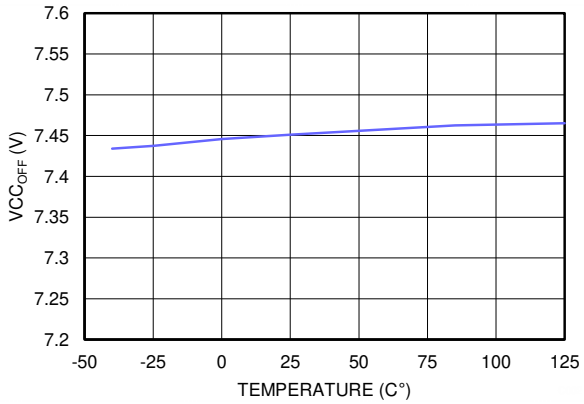


Figure 5-2. VCC_{OFF} vs. Temperature

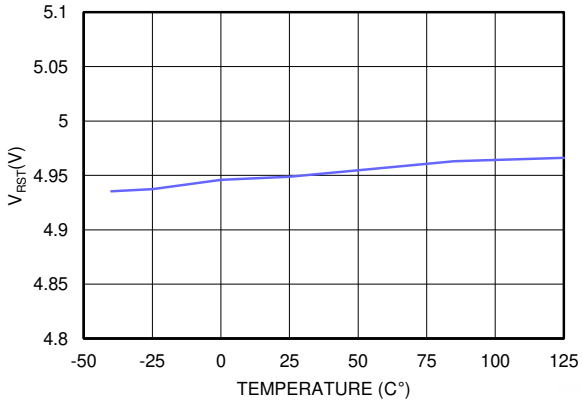


Figure 5-3. V_{RST} vs. Temperature

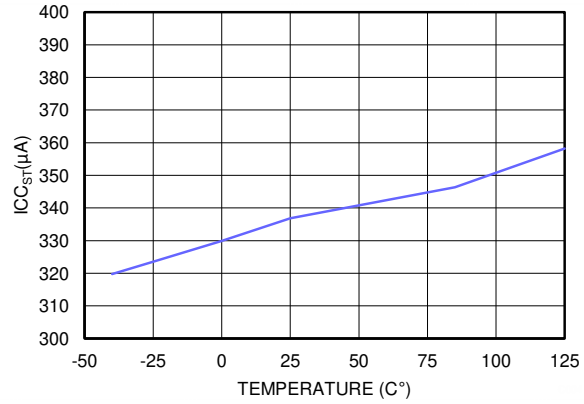


Figure 5-4. ICC_{ST} vs. Temperature

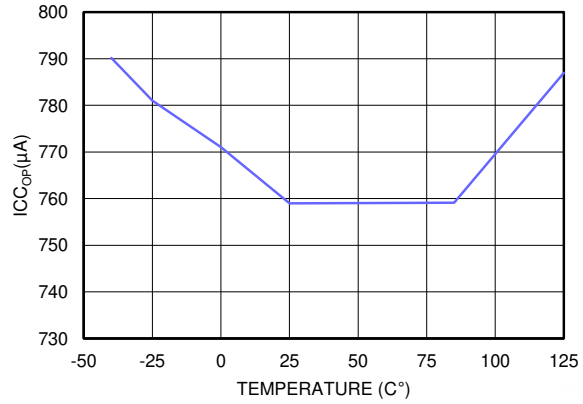


Figure 5-5. ICC_{OP} vs. Temperature

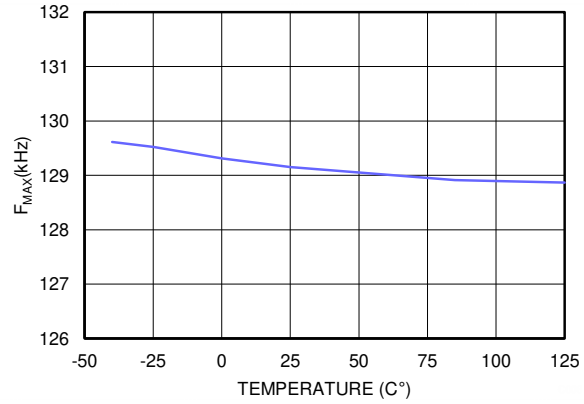


Figure 5-6. F_{MAX} vs. Temperature

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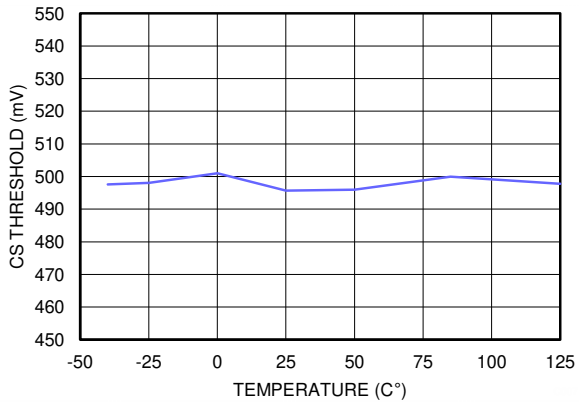


Figure 5-7. CS Threshold vs. Temperature

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6 Detailed Description

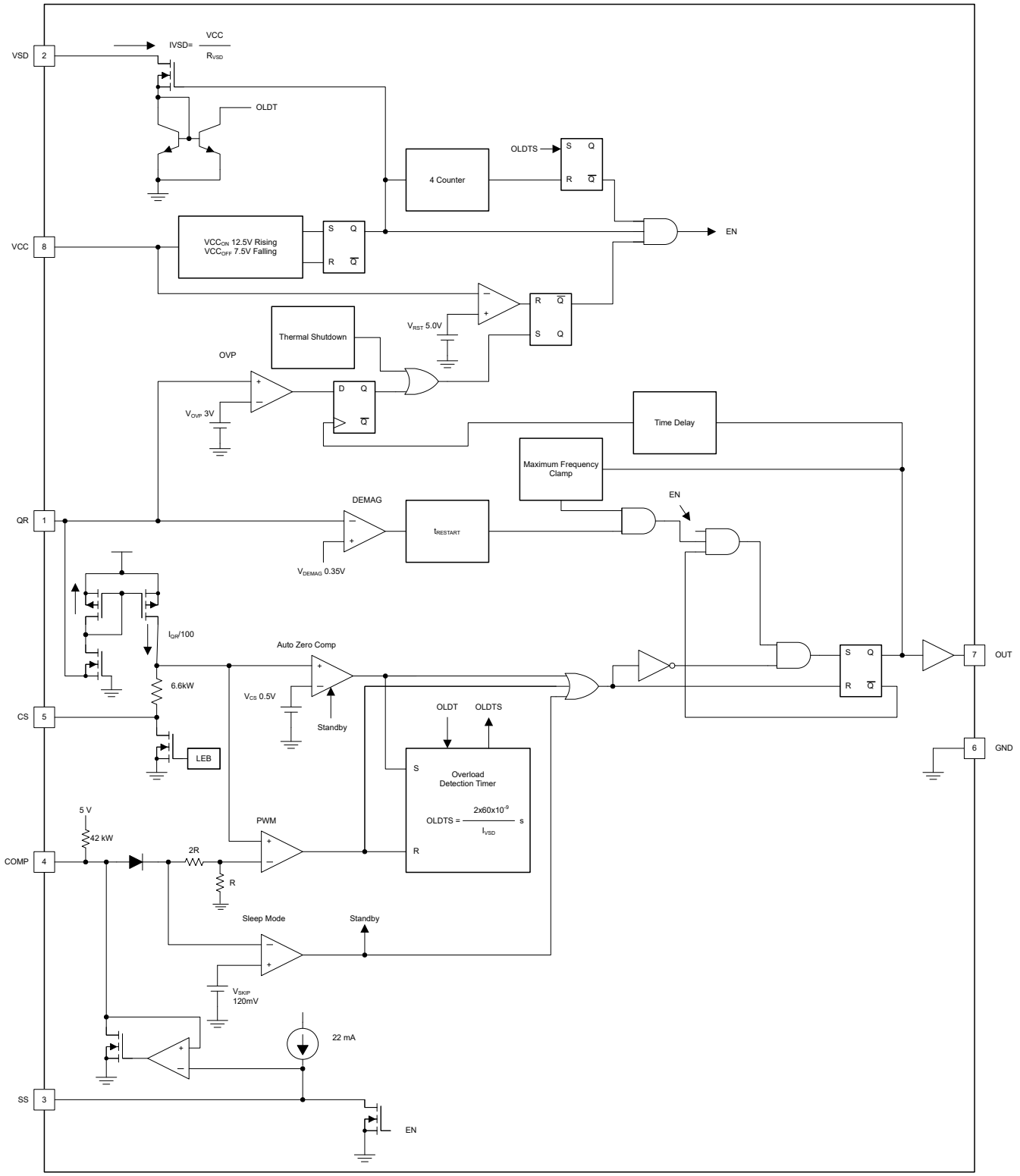
6.1 Overview

The LM5023 is a quasi-resonant PWM controller which contains all of the features needed to implement a highly efficient off-line power supply. The LM5023 uses the transformer auxiliary winding for demagnetization detection to confirm quasi-resonant operation (valley-switching) to minimize switching losses. For applications that need to meet the ENERGY STAR low standby power requirements, the LM5023 features an extremely low Iq current (346µA) and skip-cycle mode which reduces power consumption at light loads. The LM5023 uses a feedback signal from the output to provide a very accurate output-voltage regulation <1%. To reduce overheating and stress during a sustained overload conditions the LM5023 offers a hiccup mode for overcurrent protection and provides a current-limit restart timer to disable the outputs and forcing a delayed restart (hiccup mode).

For offline start-up, an external depletion mode N-channel MOSFET can be used. This method is recommended for applications where a very low standby power (<50mW) is required. For application where a low standby power is not as critical, an enhancement mode, N-channel MOSFET can be used. If an OV is detected on the auxiliary winding (QR pin), the device permanently latches off, requiring recycling of power to restart. VCC voltage must be brought lower than V_{RST} to reset the latch. Additional features include line-current feedforward, pulse-by-pulse current limit, and a maximum frequency clamp of 130kHz.

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6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Detailed Pin Description

6.3.1.1 QR Pin

The QR pin is connected to the auxiliary winding voltage divider and valley-switching delay capacitor which are also connected to GND. The auxiliary winding is monitored to detect quasi-resonant operation. The pin is also used to detect an output OV fault, which results in shutdown of the converter. Connect the capacitor and divider low-side resistor with short traces to the QR and GND pins. Avoid high dV/dt traces close to the QR pin connection and net.

6.3.1.2 VSD Pin

The VSD pin is connected to the gate of an external high-voltage start-up MOSFET. The VDS pin controls the gate of the external start-up MOSFET. When the V_{CC} exceeds $V_{CC(on)}$, the VSD pin is pulled low which turns off the start-up MOSFET. Avoid high frequency or high dV/dt traces close to this net.

6.3.1.3 SS Pin

The SS pin is connected to a capacitor selected to control the start-up soft-start time. Place a high quality ceramic capacitor with short traces to SS and GND.

6.3.1.4 COMP Pin

The COMP pin is the input to the pulse width modulator, and skip cycle comparators. There is an internal pull up resistance of 42kΩ on the COMP pin. Traces from the optocoupler to the COMP pin must have minimal loop area. It is recommended to shield the COMP trace with ground planes to minimize noise pick up. If a capacitor connects to COMP and GND, use short traces.

6.3.1.5 CS Pin

CS is the current sense input for current mode control, and peak current limit. Place a small ceramic filter capacitor on CS to GND with short traces, to filter any ringing present during the MOSFET turn-on. Return the current sense resistor current to the bulk capacitor ground terminal to minimize the primary high current loop area.

6.3.1.6 GND Pin

The GND pin is the signal and power reference for the controller. The GND pin must connect to the VCC capacitor with a short trace, and be kelvin connected to be the ground reference for components connected to the signal pins.

6.3.1.7 OUT Pin

The OUT pin connects to the primary MOSFET typically through a small resistance to limit switching speed of the MOSFET. This pin generates high dV/dt signals and must be routed as far away from the signal pins as possible.

6.3.1.8 VCC Pin

The VCC pin must be decoupled to GND with a good quality, low ESR, low ESL ceramic bypass capacitors with short traces to the VCC and GND pins. Additional bulk capacitance can be required to maintain VCC during start-up, but always use a ceramic bypass capacitor as well.

6.3.2 Start-Up

Referring to Figure 6-1, when the AC rectified line voltage is applied to the bulk-energy-storage capacitor; the N-channel depletion mode MOSFET is turned on and supplies the charging current to the VCC capacitor. When the voltage on the VCC pin reaches 12.5V typical, the PWM controller, soft-start circuit and gate driver are enabled.

When the LM5023 is enabled and the OUT drive signal starts switching the flyback MOSFET, energy is being stored and then transferred from the transformer primary to the secondary windings. A bias winding, shown in Figure 6-1, delivers energy to the VCC capacitor to sustain the voltage on the VCC pin. The voltage supplied

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from the auxiliary winding must be within the range from 10V to 14V (where 16V is the absolute maximum rating).

After reaching the VCC_{ON} threshold, the LM5023 VSD open-drain output, which is pulled up to VCC during start up, goes low. This applies a negative gate to source voltage on the depletion mode MOSFET turning it off. This disables the high-voltage start-up circuit. The high-voltage start-up circuit can be implemented in either of two ways; the first is shown in Figure 6-1, which uses an N-channel depletion mode FET, the second is shown in Figure 6-2, which uses an N-channel enhancement mode FET. The circuit using the depletion mode FET has the lowest standby power. The standby power consumption of the FET is the voltage across the start-up FET multiplied by the drain-to-source cutoff current with gate negatively biased, this is typically 0.1µA.

Standby power of the start-up FET calculation is shown in Equation 1 through Equation 5.

$$V_{IN} = 230V_{AC} \tag{1}$$

$$VCC = 10V \tag{2}$$

$$V_{DC(max)} = 230V_{AC} \times \sqrt{2} = 325V_{DC} \tag{3}$$

$$I_{D(off)} = 0.1\mu A \tag{4}$$

where

- $I_{D(off)}$ is the depletion mode FETs leakage current

$$Pd = I_{D(off)} \times V_{DC(max)} = 0.1\mu A \times 325V_{DC} = 32.5\mu W \tag{5}$$

When VCC < VCC_{ON} the standby current consumption of the IC = $I_{CC(st)}$, nominally 340µA.

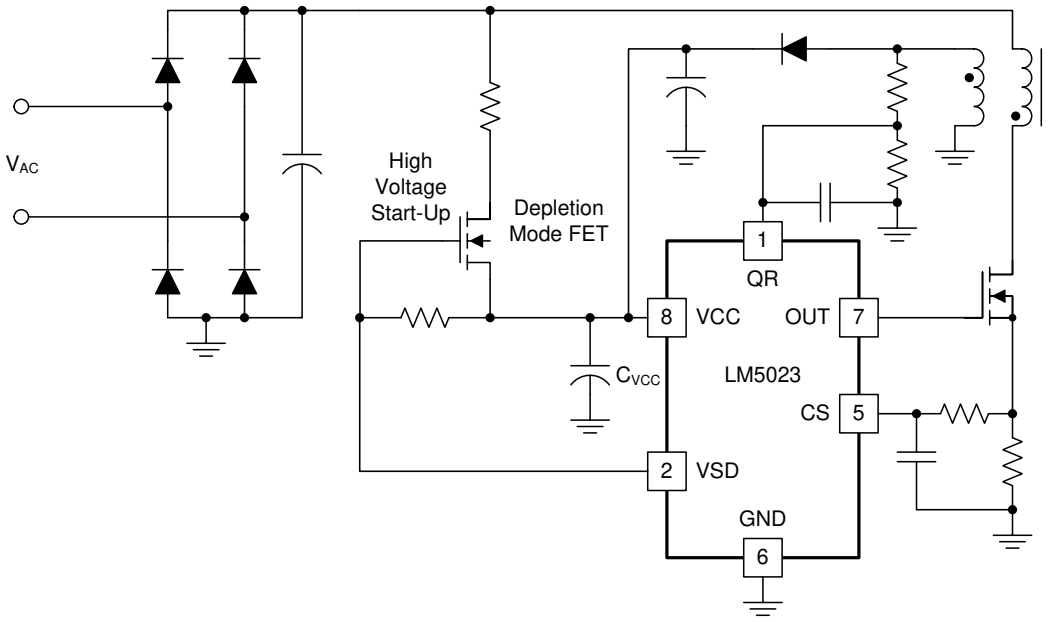


Figure 6-1. Start-Up With a Depletion Mode FET

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An alternative start-up circuit employs an enhancement mode FET with pull-up resistors connected from the rectified DC bus to the gate of the FET, Figure 6-2. After the input AC power is applied, the enhancement mode FET supplies the charging current to the VCC capacitor C_{VCC}. After reaching the VCC_{ON} threshold, the LM5023 VSD open-drain output, which is pulled up to VCC during start up, goes low. This grounds the gate of the start-up MOSFET, turning it off. The start-up resistors are always in the circuit, therefore the standby power consumed is higher than if using a depletion mode FET.

$$V_{IN} = 230V_{AC} \tag{6}$$

$$VCC = 10V \tag{7}$$

$$V_{DC(max)} = 230V_{AC} \times \sqrt{2} = 325V_{DC} \tag{8}$$

$$R_{START\text{-}UP} = 10M\Omega \tag{9}$$

$$P_{RESISTORS} = \frac{{V_{DC}}^2}{R_{START-UP}} = \frac{325^2}{10M\ \Omega} = 10.56mW \tag{10}$$

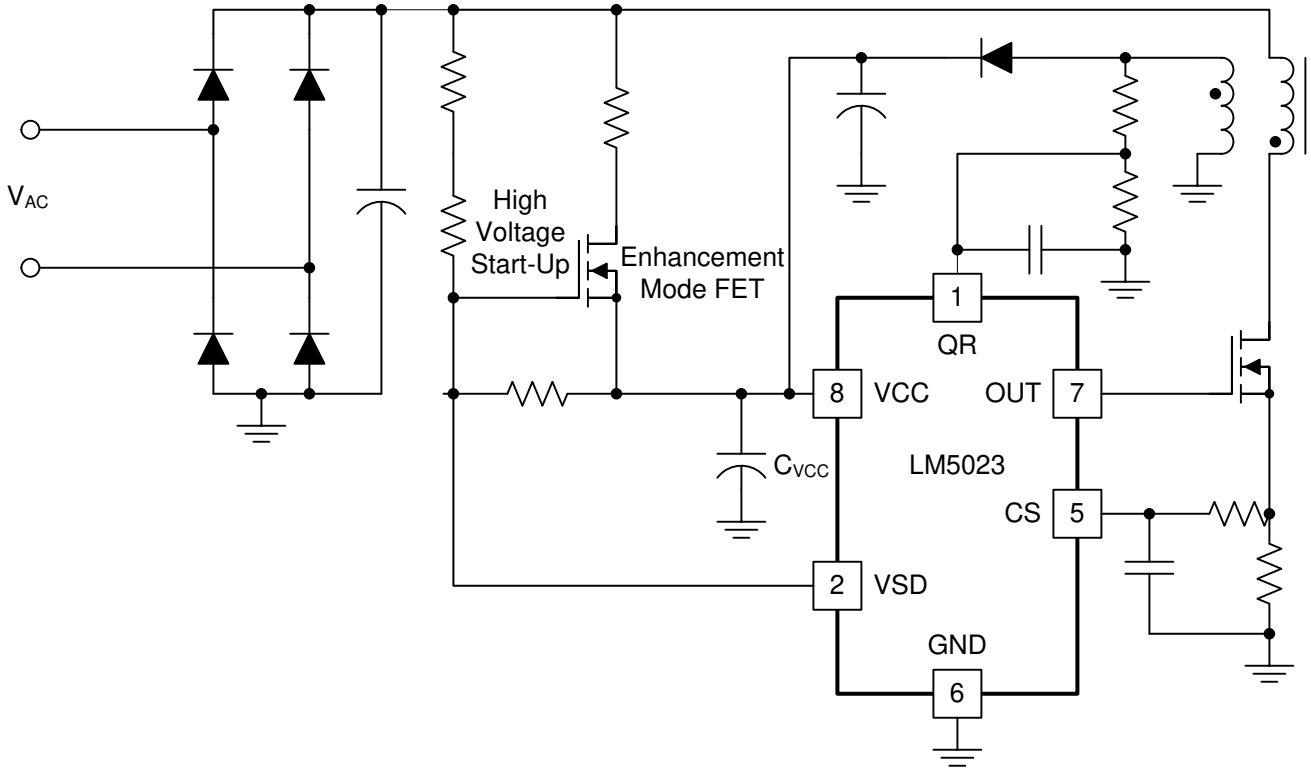


Figure 6-2. Start-Up With an Enhancement Mode FET

6.3.3 Quasi-Resonant Operation

A quasi-resonant controlled flyback converter operates by storing energy in the transformer's primary during the on-time of the MOSFET. During the on-time (t_{ON}) V_{IN} is applied across the primary of the transformer. The primary current starts out at zero and ramps toward a peak value (I_{PEAK}). When the peak-primary current reaches the feedback compensation error voltage the PWM comparator resets the output drive, turning off the MOSFET. Due to the phasing of the transformer, the output diode is reverse-biased during the MOSFET on-time.

During the off time of the MOSFET, the output diode is forward biased and the stored energy in the transformer primary inductor is transferred to the output. The voltage seen on the secondary winding is V_{OUT} plus the

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forward voltage drop of the output diode, V_F. The current in the secondary winding linearly decreases from I_{PEAK} × Np/Ns to zero, refer to Figure 6-4.

When the current in the secondary reaches zero, the transformer is demagnetized, and there is an open circuit on the secondary, and with the primary MOSFET also turned off, there is an open on the primary. A resonant circuit is formed between the transformers primary inductance and the MOSFET output capacitance. The resonant frequency is calculated by Equation 11.

$$FRES = \frac{1}{2 \times \pi \sqrt{Lp \times COSS}} \tag{11}$$

During the resonant period the drain voltage of the MOSFET rings down toward ground, refer to Figure 6-3. When the drain voltage is at its minimum the flyback MOSFET is turned back on. The point where the voltage is at its minimum is calculated by Equation 12.

$$td = \pi \times \sqrt{L_P \times COSS} \tag{12}$$

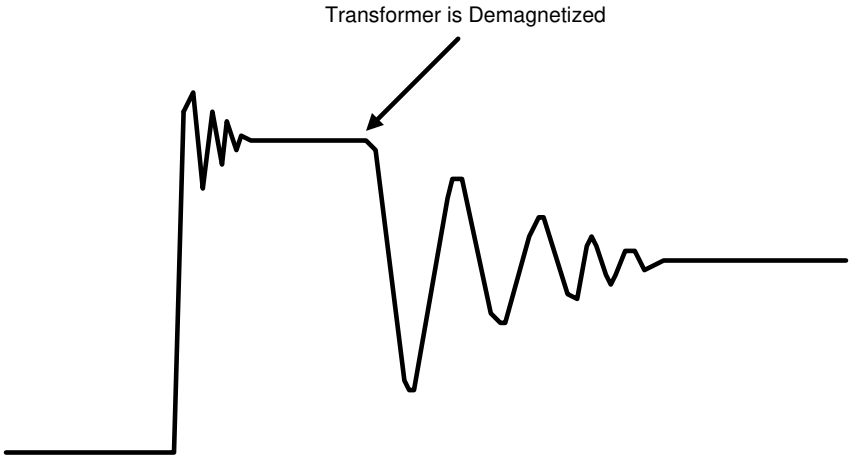


Figure 6-3. Flyback Drain Voltage Waveform

Transformer demagnetization is detected by sensing the transformers auxiliary winding. When the transformer is demagnetized the auxiliary winding voltage follows the drain of the MOSFET and changes from $V_{OUT} \times N_{AUX}/N_S$ to $-V_{IN} \times N_{AUX} / Np$. Internal to the LM5203 QR pin is a comparator with a 0.35V reference. As the auxiliary-winding voltage falls below 0.35V, the voltage is sensed and the comparator sets the PWM flip-flop turning on the flyback MOSFET. Figure 6-4 shows the QR converter typical waveforms; the auxiliary winding voltage, and primary and secondary current waveforms. It is possible to adjust the delay on the auxiliary winding with a resistor and external capacitor to confirms that the MOSFET switches when its drain voltage is at its minimum. Refer to the schematic in Figure 7-3 and the section on *Section 7.2.2.3* for details. The benefits of QR operation are reduced EMI, and reduced turn-on switching losses.

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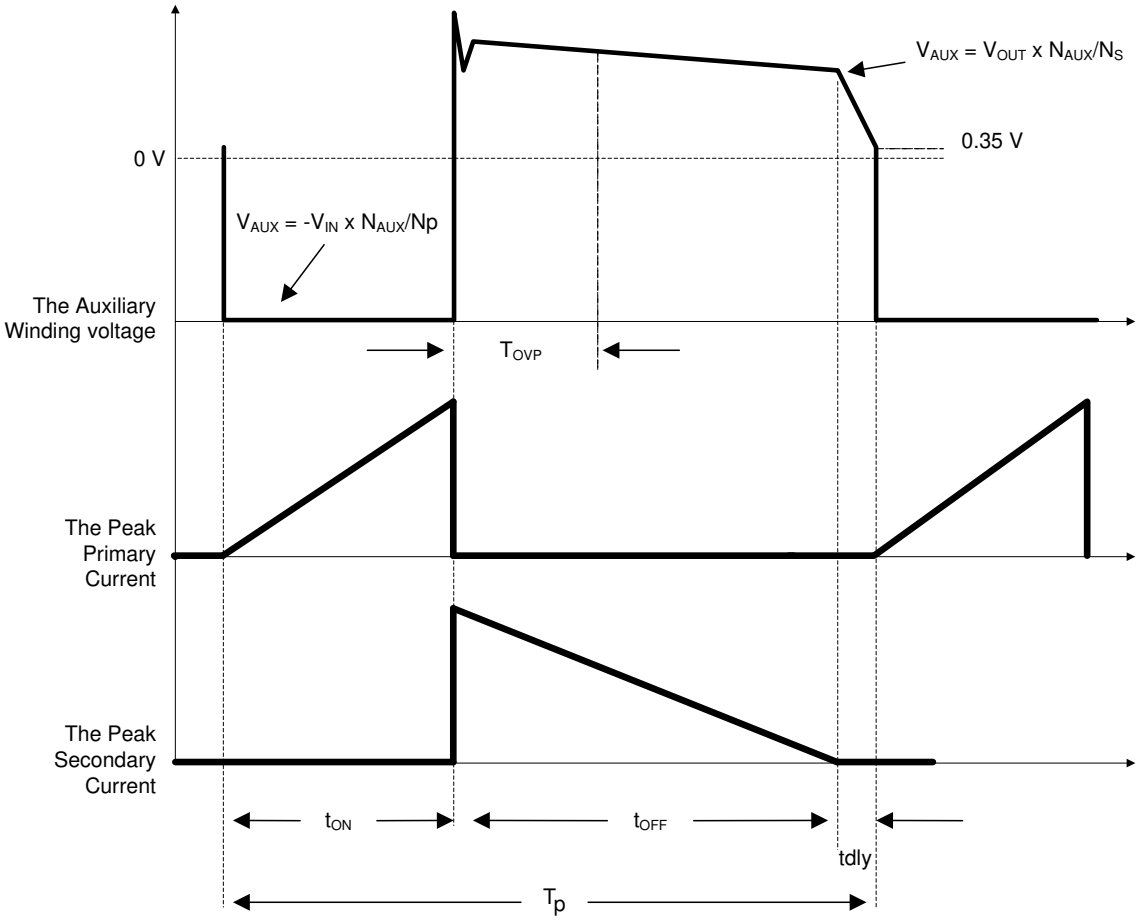


Figure 6-4. QR Converter Typical Waveforms

6.3.4 Quasi-Resonant Operating Frequency

When the primary-side flyback MOSFET turns on, the current ramps up until the peak-primary current exceeds the feedback compensation error voltage. When this occurs the PWM comparator resets the output drive, turning off the MOSFET. The current ramps up with a slope shown in Equation 13.

$$\frac{V_{IN}}{Lp} = \frac{di}{dt} \tag{13}$$

The t_{ON} time of the switch is calculated by Equation 14.

$$t_{ON} = \frac{Lp}{V_{IN}} \times I_{PK} \tag{14}$$

When the primary-side flyback MOSFET is turned off, the energy stored in the primary inductance is transfer to the secondary inductance, the off time to transfer all of the energy is shown in Equation 15.

$$t_{OFF} = I_{PK} \times \frac{N_{SP} \times Lp}{V_O + V_f} \tag{15}$$

where

$$N_{SP} = N_S / N_P \tag{16}$$

The total switching period is shown in Equation 15.

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$$tp = t_{ON} + t_{OFF} + t_{DLY} \quad (17)$$

The resonant circuit created by the transformer primary inductance and the MOSFETs switch node capacitance is the t_{DLY} time, refer to Figure 6-4.

$$t_{DLY} = \pi \times \sqrt{Lp \times C_{SWN}} \quad (18)$$

$$P_{OUT} = \frac{1}{2} \times Lp \times {I_{PK}}^2 \times FREQ \times \eta \quad (19)$$

Equation 20 represents the relationship of switching frequency, L_P, and N_{PS}.

$$FREQ = \frac{1}{\left(\frac{V_{IN} + (V_O + V_f) \times N_{PS}}{(V_O + Vf) \times N_{PS}}\right)^2 \times \frac{2 \times P_{OUT}}{\eta} \times \frac{Lp}{{V_{IN}}^2} + t_{DLY}} \quad (20)$$

The QR flyback converter does not operate at a fixed frequency. The frequency varies with the output load, input line voltage, or a combination of the two. To keep LM5023 frequency below the EMI starting limit of 150kHz per CISPR--22, the LM5023 has an internal timer which prevents the output drive from restarting within 7.69µs of the previous driver output (OUT) low-to-high transition. This timer clamps the maximum switching frequency at 130kHz (typical).

6.3.5 PWM Comparator

The PWM comparator compares the current sense signal with the loop error voltage from the COMP pin. The COMP pin voltage is reduced by a fixed 0.75V offset and then attenuated by a 3:1 resistor divider. The PWM comparator input offset voltage is designed such that less than 0.75V at the COMP pin results in a zero duty cycle at the controller output.

6.3.6 Soft-Start

The soft-start feature allows the power converter to gradually reach the initial steady state operating point, thereby reducing start-up stresses and current surges. At power on, after the VCC reaches the VCC_{ON} threshold, an internal 22µA current source charges an external capacitor connected to the SS pin. The capacitor voltage ramps up slowly and limits the COMP pin voltage and the duty cycle of the output pulses.

6.3.7 Gate Driver

The design of the LM5023 driver (OUT) is to drive the gate of an N-channel MOSFET and can source a peak current of 0.4A and sinking 0.7A.

6.3.7.1 Skip-Cycle Operation

During light-load conditions, the efficiency of the switching power supply typically drops as the losses associated with switching and operating bias currents of the converter become a significant percentage of the power delivered to the load. The largest component of the power loss is the switching loss associated with the gate driver and external MOSFET gate charge and the switched-node capacitance energy. Each PWM cycle consumes a finite amount of energy as the MOSFET is turned on and then turned off. These switching losses are proportional to the frequency of operation.

To improve the light-load efficiency the LM5023 enters a skip-cycle mode during light-load conditions. As the output load decreases, the COMP pin voltage is reduced by the voltage feedback loop to reduce the flyback converters peak-primary current. Referring to the *Section 6.2*, the PWM comparator input tracks the COMP pin voltage through a 0.75V level-shift circuit and a 3:1 resistor divider. As the COMP pin voltage falls, the input to the PWM comparator falls proportionately. When the PWM comparator input falls to 120mV, the skip cycle comparator detects the light-load condition and disables output pulses from the controller. The LM5023 also reduces all internal bias currents, while in skip mode, to further reduce quiescent power. The controller continues to skip switching cycles until the power supply output falls and the COMP pin voltage increases to demand more output current. The number of cycles skipped depends on the load and the response time of the

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frequency voltage loop compensation network. Eventually the COMP voltage increases when the voltage loop requires more current to sustain the regulated output voltage. When the PWM comparator input exceeds 155mV (30mV hysteresis), normal fixed-frequency switching resumes. Typical light-load operation power-supply designs produces a short burst of output pulses followed by a long skip-cycle interval (no drive pulses). The result is a large reduction in the average input power.

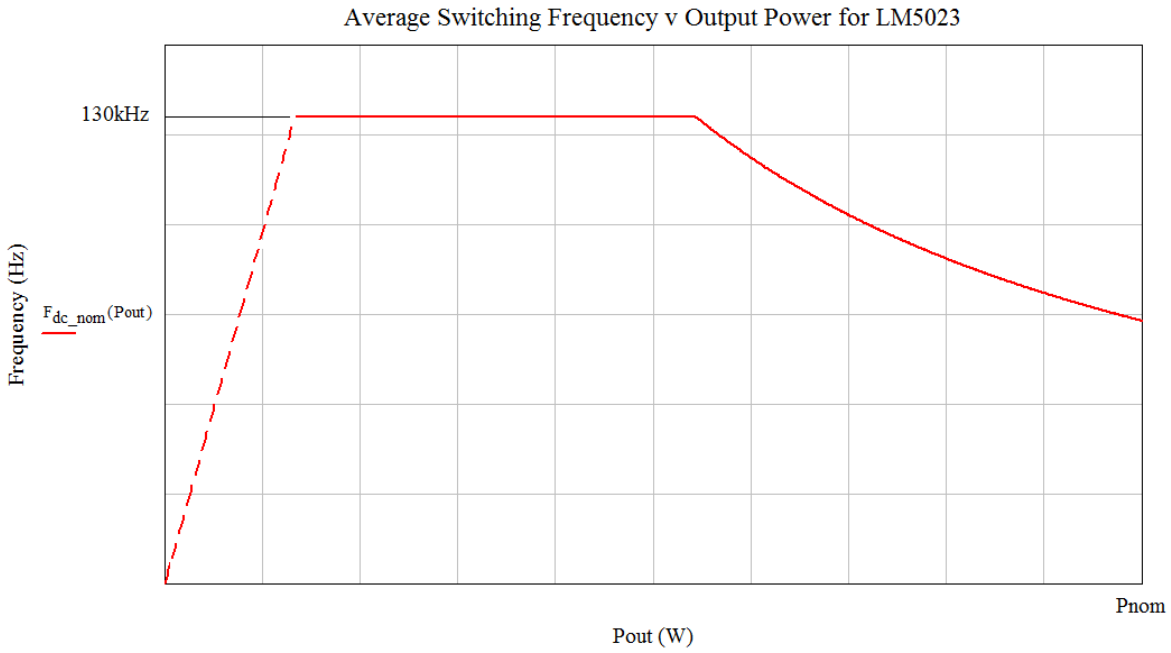


Figure 6-5. LM5023 Modulation Curve

6.3.8 Current Limit and Current Sense

The LM5023 provides a cycle-by-cycle overcurrent protection feature. Current limit is triggered by an internal current sense comparator with a threshold of 500mV. If the CS pin voltage plus the current limit feedforward signal voltage exceeds 500mV, the MOSFET drive signal (OUT) ends. An RC filter, located near the LM5023 CS pin is recommended to attenuate the noise coupled from the gate of the power FET to source switching. The CS pin capacitance is discharged at the end of each PWM cycle by an internal switch. The discharge switch remains on for an additional 130ns for leading edge blanking (LEB). LEB prevents the LM5023 current sense comparator from being falsely triggered due to the noise generated by the switch currents initial spike. The LM5023 current sense comparator is very fast and can respond to short-duration noise pulses. Layout considerations are critical for the current-sense filter and sense resistor. The capacitor associated with the CS filter must be placed very close to the device and connected directly to the pins of the device (CS and GND). If a current sense transformer is used, both leads of the transformer secondary must be routed to the sense resistor, which must also be located close to the device. If a current sense resistor located in the source of the power FET is used for current sense, a low inductance resistor is required. In this case, all of the noise-sensitive low-current grounds must connect in common near the device and then one connection must be made.

6.4 Device Functional Modes

According to the input voltage, the VCC voltage, and the output load conditions, the device can operate in different modes:

- At start-up, when VCC is less than the VCC_{ON} threshold, the VSD open drain output is pulled up to VCC which turns on the depletion mode MOSFET. The depletion mode MOSFET charges the VCC capacitor.
- When VCC exceeds the VCC_{ON} threshold, the VSC open drain output is pulled to ground which turns off the depletion mode MOSFET, disabling the high-voltage start-up circuit as long as VCC > $V_{CC(off)}$.

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- At power on, when VCC reaches the VCC_{ON} threshold, the device starts switching to deliver power to the converter output. On initial power up soft-start is initiated by a 22µA current source that charges a capacitor on the SS pin. The SS pin limits the voltage on the COMP pin voltage and the duty cycle of the OUT pulses.
- Soft-start ends based on the voltage required on the COMP pin to deliver the required power to achieve voltage regulation. Depending on the load condition, the converter operates in normal or skip-cycle mode.
  - Normal mode is the full-load to light-load condition where the controller output is enabled every cycle.
  - Skip-cycle mode occurs at light to no-load where the controller output is disabled based on the COMP pin voltage. The ICC current is reduced to ICC_{ST} when the output is disabled in skip cycle mode.
- The device operation can be stopped by the events listed below:
  - If VCC drops below VCC_{OFF} threshold, the device stops switching and the start-up sequence repeats.
  - If a fault is detected the driver is latched off until VCC reduces to VCC_{OFF}, and the start-up sequence is initiated.
  - If an overload condition exceeds the overload timer duration, the output is turned off until VCC reduces to VCC_{OFF}, and the start-up sequence is initiated.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The LM5023 is a quasi-resonant PWM controller optimized for isolated flyback converters with secondary-side regulation. The controller can be used with single or multiple output converters. Applications include notebook adapters and a variety of consumer and industrial applications. The skip-cycle operation, reduced device bias current and control for high-voltage start-up circuit facilitates achieving low-standby input power.

7.2 Typical Application

This AC-to-DC adapter, 19.2V, 65W design example describes the design of a 65W off-line flyback converter providing 19.2V at 3.43A maximum load and operating from a universal AC input. The design uses the LM5023 AC-to-DC quasi-resonant primary-side controller in a DCM type flyback converter and achieves 88% full load efficiency.

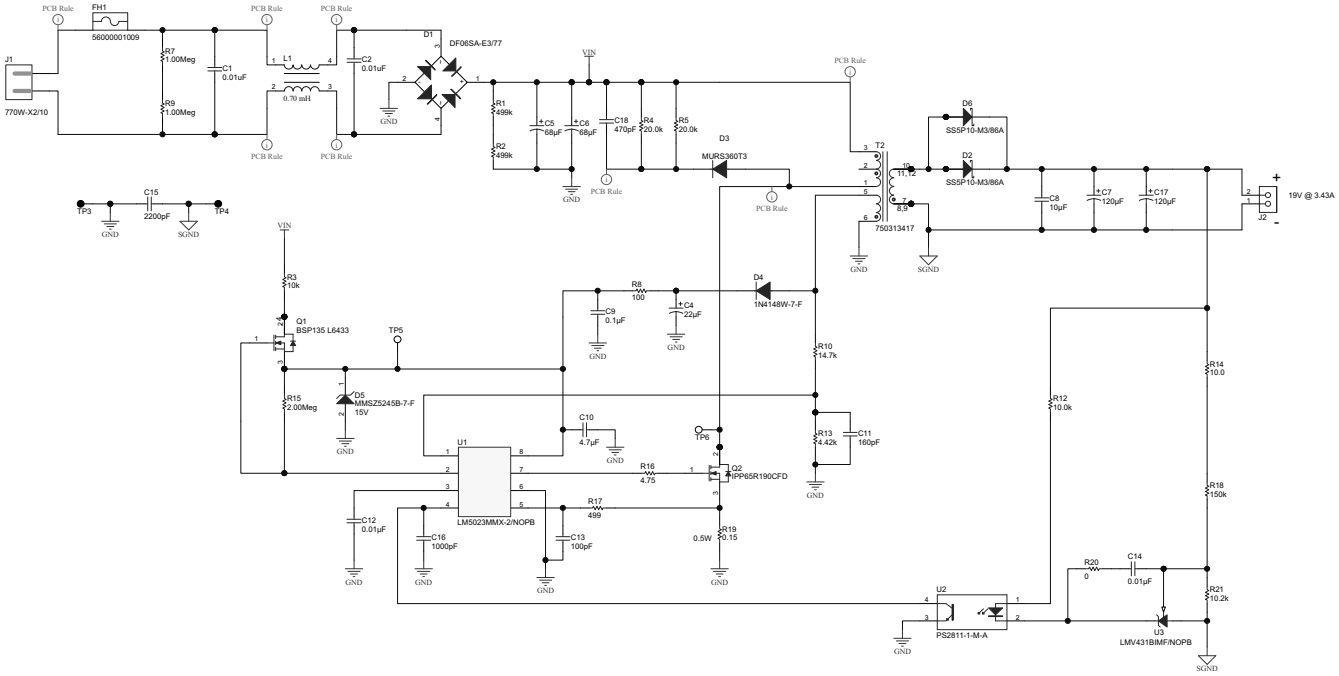


Figure 7-1. LM5023 Typical Application

7.2.1 Design Requirements

Table 7-1 lists the design requirements for the LM5023.

Table 7-1. LM5023 Performance Specifications

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
V_{IN}	Input voltage		90	115/230	264	V_{AC}
V_{IN}	No load input power	V_{IN} = 230V		30		mW
OUTPUT CHARACTERISTICS						

Table 7-1. LM5023 Performance Specifications (continued)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
V_{OUT}	Output voltage	V_{IN} = 115V, I_{OUT} = 3.43A	19.0	19.2	19.4	V
V_{OUT}	Line regulation	V_{IN} = min to max, I_{OUT} = max			1.0%	
V_{OUT}	Load regulation	V_{IN} = nom, I_{OUT} = no load to maximum load			1.0%	
V_{OUT}	Output voltage ripple	V_{IN} = nom, I_{OUT} = max load	100			mV_{PP}
I_{OUT}	Output current				3.43	A
V_{OVP}	Output OVP		24			V
M	Load step response	I_{OUT} = 0.343A to 3.09A, 3.09A to 0.343A	18.7		19.6	V
SYSTEMS CHARACTERISTICS						
	Switching frequency		130			kHz
η	Full load	V_{IN} = 115/230V, I_{OUT} = 3.43A	88%			

7.2.2 Detailed Design Procedure

7.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5023 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.2.2 Line Current-Limit Feedforward

In a peak-current mode controlled when the power supply is in an overload, the peak current (measured across the current sense resistor VCS) is compared to a voltage reference for overload protection. If the peak current exceeds the reference the LM5023 controller will turn off the primary-side flyback MOSFET on a cycle-by-cycle basis. However, the primary switch can't be turned off instantly, as there are several unavoidable delays. The first delay is caused by the LEB circuit which provides leading-edge blanking. The second delay is caused by the propagation delay between the detecting point of VCS and the actual turn off of the power MOSFET. The total delay time (t_{PROP}) refer to Figure 7-2, includes the current limit comparator, the logic, the gate driver, and the power MOSFET turning off.

The propagation delay causes the peak-primary current to overshoot, the overshoot increase the maximum peak current beyond the calculated value. The peak-current overshoot increase as the AC line voltage increase because of the increase in the slope of the primary current, shown in Equation 21.

$$\frac{V_{IN}}{Lp} = \frac{di}{t_{PROP}} \tag{21}$$

This increase in the peak-input-current overshoot causes a wide variation of overpower limit in a flyback converter. In Equation 22, the overpower limit increases with the input line voltage because of $I_{PK(max)}$ increase shown in Equation 22 through Equation 24.

$$I_{PK(max)} = \sqrt{\frac{P_{OUT} \times 2}{Lp \times FREQ \times \eta}} + \frac{V_{IN}}{Lp} \times t_{PROP} \tag{22}$$

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$$P_{IN} = \frac{1}{2} \times I_{PK(max)}^{2} \times L_P \times FREQ \quad (23)$$

$$P_{OUT} = P_{IN} \times \eta \quad (24)$$

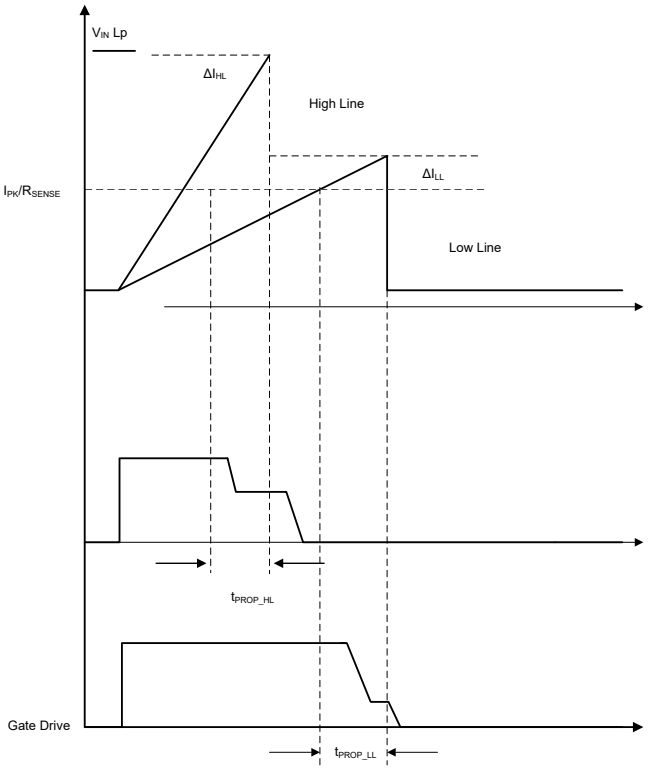


Figure 7-2. Line-Current Feedforward

To improve the overpower limit accuracy over the full universal input line, the LM5023 integrates line current limit feedforward. Line current limit feedforward improve the overpower limit by summing a current proportional to the input rectified line into the current sense resistor (R_{SENSE}), refer to Figure 7-3. The current proportional to the input line biases up the CS pin, this turns off the flyback MOSFET earlier at high input line. This feature compensates for the propagation delays creating a overpower protection that is nearly constant over the universal input line.

To implement line current limit feedforward, the first step is to calculate the QR switching frequency at low line and then at high line when the power supply is operating in current limit.

For this example:

- Lp = 400µH
- R_{SENSE} = 0.15Ω
- $V_{DC(min)}$ = 127V
- $V_{DC(max)}$ = 325V
- T_{PROP} = 160ns
- V_{CS} = 0.5V
- N_{AUX} = 10.9
- $N_{PS} = N_P/N_S$ = 6
- t_{DLY} = 580ns

$$FREQ_LL = \frac{1}{\left(\frac{V_{CS}}{R_{SENSE}}\right) \times Lp \times \left[\left(\frac{1}{V_{DC(min)}}\right) + \frac{1}{(V_{OUT} + Vf) \times N_{PS}}\right] + t_{DLY}} \quad (25)$$

$$FREQ_LL = \frac{1}{\left(\frac{0.5\ V}{0.15\ \Omega}\right) \times 400\ \mu H \times \left[\left(\frac{1}{127\ V}\right) + \frac{1}{(19\ V + 0.7\ V) \times 6}\right] + 580\ ns} = 44.7 kHz \quad (26)$$

$$FREQ_HL = \frac{1}{\left(\frac{V_{CS}}{R_{SENSE}}\right) \times Lp \times \left[\left(\frac{1}{V_{DC(max)}}\right) + \frac{1}{(V_{OUT} + Vf) \times N_{PS}}\right] + t_{DLY}} \quad (27)$$

$$FREQ_HL = \frac{1}{\left(\frac{0.5\ V}{0.15\ \Omega}\right) \times 400\ \mu H \times \left[\left(\frac{1}{325\ V}\right) + \frac{1}{(19\ V + 0.7\ V) \times 6}\right] + 580\ ns} = 62.6 kHz \quad (28)$$

The next step is to calculate the uncompensated output power at the minimum and maximum input line voltage while in current limit.

$$P_{OUT}_LL = \frac{1}{2} \times Lp \times \left(\frac{VCS}{R_{SENSE}}\right)^2 \times FREQ_LL \times \eta \quad (29)$$

$$P_{OUT_}LL = \frac{1}{2} \times 400\ \mu H \times \left(\frac{0.5}{0.15}\right)^2 \times 44.7\ kHz \times 0.86 = 85.4\ W \quad (30)$$

$$P_{OUT}_HL = \frac{1}{2} \times Lp \times \left(\frac{VCS}{R_{SENSE}}\right)^2 \times FREQ_HL \times \eta \quad (31)$$

$$P_{OUT_}HL = \frac{1}{2} \times 400\ \mu H \times \left(\frac{0.5}{0.15}\right)^2 \times 62.6\ kHz \times 0.86 = 120\ W \quad (32)$$

Step three is to calculate the peak current at high line so it does not deliver more power than while it is operating at low line (85.4W). One thing that complicates the line current limit feedforward calculation is that with quasi-resonant operation the switching frequency changes with line and load. There are two equations and two unknowns, the peak-primary current and the QR frequency.

$$N_{SP} = \frac{N_S}{N_P} \quad (33)$$

$$FREQ_COMP = \frac{4}{\left[\left(\sqrt{4 \times t_{DLY} + \frac{2 \times Lp \times P_{OUT_LL} \times \left(V_{OUT} + Vf + N_{SP} \times V_{DC(max)}\right)^2}{\eta \times V_{DC(max)}^2 \times (V_{OUT} + Vf)^2}}\right) + \frac{\sqrt{2} \times Lp \times \left(V_{OUT} + Vf + N_{SP} \times V_{DC(max)}\right) \times \sqrt{\frac{P_{OUT_LL}}{\eta \times Lp}}}{V_{DC(max)} \times (V_{OUT} + Vf)}\right]^2} \quad (34)$$

$$FREQ_COMP = \frac{4}{\left[\left(\sqrt{4 \times 580ns + \frac{2 \times 400\mu H \times 85.4W \times (19V + 0.7V + 0.167 \times 325V)^2}{0.86 \times (325V)^2 \times (19V + 0.7V)}}\right) + \frac{\sqrt{2} \times 400\mu H \times (19V + 0.7V + 0.167 \times 325) \times \sqrt{\frac{85.4W}{0.86 \times 400\mu H}}}{325V \times (19V + 0.7V)}\right]^2} \quad (35)$$

$= 85.2kHz$

Step four is to calculate the peak current.

$$I_{L(max)_LL} = \sqrt{\frac{2 \times P_{OUT_LL}}{\eta \times Lp \times FREQ_COMP}} \quad (36)$$

$$I_{L(max)_LL} = \sqrt{\frac{2 \times 85.4\ W}{0.86 \times 400\ \mu H \times 85.2\ kHz}} = 2.41\ A \quad (37)$$

$$VCS_CL = R_{SENSE} \times \left[I_{L(max)_CL} - \left(\frac{V_{DC(max)}}{Lp}\right) \times t_{PROP}\right] \quad (38)$$

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$$\text{VCS_CL} = 0.5\ \Omega \times \left[2.41\ \text{A} - \left(\frac{325\ \text{V}}{400\ \mu\text{H}}\right) \times 160\ \text{ns}\right] = 0.342\ \text{V} \quad (39)$$

For the power supply to go into pulse-by-pulse current limit the voltage across the current sense resistor must be 0.5V.

$$\text{VCS_OFFSET}: = V_{CS} - \text{VCS_CL} \quad (40)$$

VCS_OFFSET is the required voltage offset that must be injected across the current sense resistor, R_{SENSE}.

$$\text{VCS_OFFSET} = V_{CS} - \text{VCS_CL} = 0.5\ \text{V} - 0.342\ \text{V} = 0.158\ \text{V} \quad (41)$$

After calculating the required offset voltage, use Equation 42 and Equation 43 to calculate the required current feedforward.

While the main flyback switch is on, Q1, the voltage on the auxiliary winding is negative and proportional to the rectified line.

$$-V_{AUX} = \frac{V_{DC}}{N_{AUX}} \quad (42)$$

$$IQR = \frac{-V_{AUX}}{R1} \quad (43)$$

Select IQR in the range from 1mA to 4mA. Calculate the demagnetization circuit impedance to limit the maximum current flowing through QR pin to less than 4mA.

$$R_{OFFSET} = 6.6\text{k}\Omega + R_{EXTERNAL} \quad (44)$$

where

- N_{AUX} is the number of turns on the Flyback primary (Np) divided by the number of turns on the transformer Auxiliary (N_{AUX}) winding

The 6.6kΩ resistance is internal to the LM5023.

The current mirror in the QR pin input has a gain of 100; this offsets the voltage on the current sense pin shown in Equation 45.

$$V_{CS(offset)} = \frac{IQR}{100} \times \left(6.6\ \text{k}\Omega + R_{EXTERNAL}\right) \quad (45)$$

Set IQR = 1.75mA

$$R_1 = \frac{\frac{V_{DC(max)}}{N_{AUX}}}{IQR} = \frac{\frac{325\ \text{V}}{10.9}}{1.75\ \text{mA}} = 17.0\ \text{k}\Omega \quad (46)$$

$$R_{OFFSET} = \frac{V_{OFFSET}}{IQR} \times 100 = \frac{0.158\ \text{V}}{1.75\ \text{mA}} \times 100 = 9030\ \Omega \quad (47)$$

$$R_{OFFSET} = R_{INTERNAL} + R_{EXTERNAL} \quad (48)$$

$$R_{EXTERNAL} = R_{OFFSET} - 6.6\ \text{k}\Omega = 9030\ \Omega - 6.6\ \text{K}\Omega = 2.43\ \text{K}\Omega \quad (49)$$

No external resistor is required based on the applications describe above, so a 499Ω resistor and 100pF capacitor are installed in the CS pin input as a noise filter.

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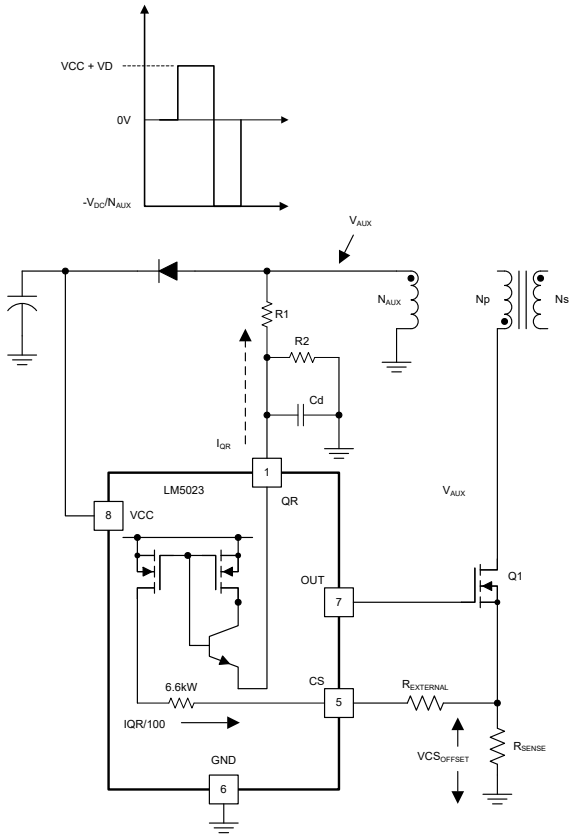


Figure 7-3. Current Feedforward

7.2.2.2.1 Overvoltage Protection

Output overvoltage protection is implemented with the LM5023 by monitoring the QR pin during the time when the main flyback MOSFET is off and the energy stored in the transformer primary is being transferred to the secondary. There is a delay before sampling the QR pin during the MOSFETs off time, T_{OVP}. There are two reasons for the delay, the first is to blank the voltage spike which is a result of the transformers leakage inductance. The second is to improve the accuracy of the output voltage sensing, referring to the transformer auxiliary winding voltage shown in Figure 6-4. It is clear there is a down slope in the voltage which represents the decreasing V_F of the output rectifier and resistance voltage drop (IS × RS) as the secondary current decreases to zero, so by delaying the sampling of the QR voltage a more accurate representation of the output voltage is achieved.

Connected to the QR pin is a comparator with a 3.0V reference. The transformers auxiliary voltage is proportional to V_{OUT} by the transformers turns ratio:

$$V_{AUX} = (V_O + V_F) \times \frac{N_{AUX}}{N_S} \tag{50}$$

To set the OVP, a voltage divider connects to the transformers auxiliary winding, refer to Figure 7-2. In Section 7.2.2.2 equations are developed to improve the power limit. Resistor R1 is calculated for line current limit feedforward; to implement OVP, calculate R2.

$$V_{OVP} = V_{AUX_OVP} \times \frac{R2}{R1 + R2} \tag{51}$$

$$R2 = 3.0V \times \frac{R1}{V_{AUX_OVP} - 3V} \tag{52}$$

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When an OVP fault has been detected, the LM5023 OUT driver is latched-off. VCC discharges to VCC_{MIN} and the VSD pin is asserted high, allowing the depletion mode FET to turn-on and charge up the VCC capacitor to VCC_{ON}. The VSD pin is toggled on-off-on to maintain VCC to the controller. The only way to clear the fault is to removed the input power and allow the controllers VCC voltage to drop below V_{RST}, 5.0V.

7.2.2.3 Valley Switching

For QR operation the flyback MOSFET is turned on with the minimum drain voltage. The delay on the auxiliary winding can be adjusted with an external resistor and capacitor to improve valley switching. The delay-time, t_{DLY}, must equal half of the natural oscillation in Equation 53

$$t_{DLYQR} = \frac{\pi}{2} \times \sqrt{Lp \times COSS} \tag{53}$$

By substituting Equation 54.

$$t_{DLYQR} = RFF \times Cd \tag{54}$$

Calculate the RC time constant to achieve the minimum drain voltage when the LM5023 turns on the Flyback MOSFET.

$$Cd := \frac{\left[\left(\frac{\pi}{2}\right) \times \sqrt{Lp_{USED} \times COSS}\right]}{RFF} \tag{55}$$

The LM5023 QR pin capacitance is approximately 20pF, so Cd_{USED} = Cd –20pF.

$$RFF := \frac{(R1 \times R2)}{(R1 + R2)} \tag{56}$$

R1 and R2 are previously calculated to set the line current limit feedforward and overvoltage protection.

7.2.2.4 Hiccup Mode

Hiccup Mode is a method to prevent the power supply from over-heating during and extended overload condition. In an overload fault, the current limit comparator turns off the driver output on pulse-by-pulse basis. This starts the over load detection timer, after the over load detection timer (OLDT) times out, the current limit comparator is rechecked, if the power supply is still in an overload condition, the OUT drive is latched-off and VCC is allowed to drop to VCC_{OFF} (7.5V).

When VCC reaches VCC_{OFF}, the VSD open-drain output is disabled allowing the depletion mode start-up FET to turn-on, charging up the VCC capacitor to VCC_{ON} (12.5V). When VCC reaches VCC_{ON}, the VSD output goes low turning-off the depletion mode FET. The VCC capacitor is discharged from VCC_{ON} to VCC_{OFF} at a rate proportional to the VCC capacitor and the ICC_{ST} current (340µA typical). The charging and discharging of the VCC capacitor is repeated four times (refer to Figure 7-4) use Equation 57 to figure the total Hiccup time.

$$t_{HICCUP} = t_{CHARGE} \times 4 + t_{DISCHARGE} \times 4 \tag{57}$$

After allowing VCC to charge and discharge four times, the LM5023 goes through an auto restart sequence, enabling the LM5023 soft start and driver output. It is important to set the over load detection timer long enough so that under low input-line and full-load conditions that the power supply has enough time to start-up.

The over load detection timer can be set with the resister in series with the VSD pin$_{VSD}$), refer to Figure 6-1.

$$IVSD = \frac{VCC}{RVSD} = \frac{10V}{1M\Omega} = 10\ \mu A \tag{58}$$

$$OVER_LOAD_DETECTION_TIMER = \frac{2 \times 60nA}{I_{VSD}} = \frac{2 \times 60nA}{10\ \mu\ A} = 12ms \tag{59}$$

Normally it is recommended that R_{VSD} > 1MΩ, if a lower value is used then the standby power is higher.

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Assuming the depletion mode FET charges the VCC capacitor with 2mA, VCC capacitor is 10µF.

$$t_{CHARGE} = \frac{(VCC_{ON} - VCC_{OFF})}{ICHARGE} \times C_{VCC} = \frac{12.5V - 7.5V}{2mA} \times 10\mu F = 25ms \quad (60)$$

$$t_{DISCHARGE} = \frac{(VCC_{ON} - VCC_{OFF})}{ICC_{ST}} \times C_{VCC} = \frac{12.5V - 7.5V}{340\ \mu A} \times 10\mu F = 145ms \quad (61)$$

$$t_{HICCUP} = 25ms \times 4 + 145ms \times 4 = 680ms \quad (62)$$

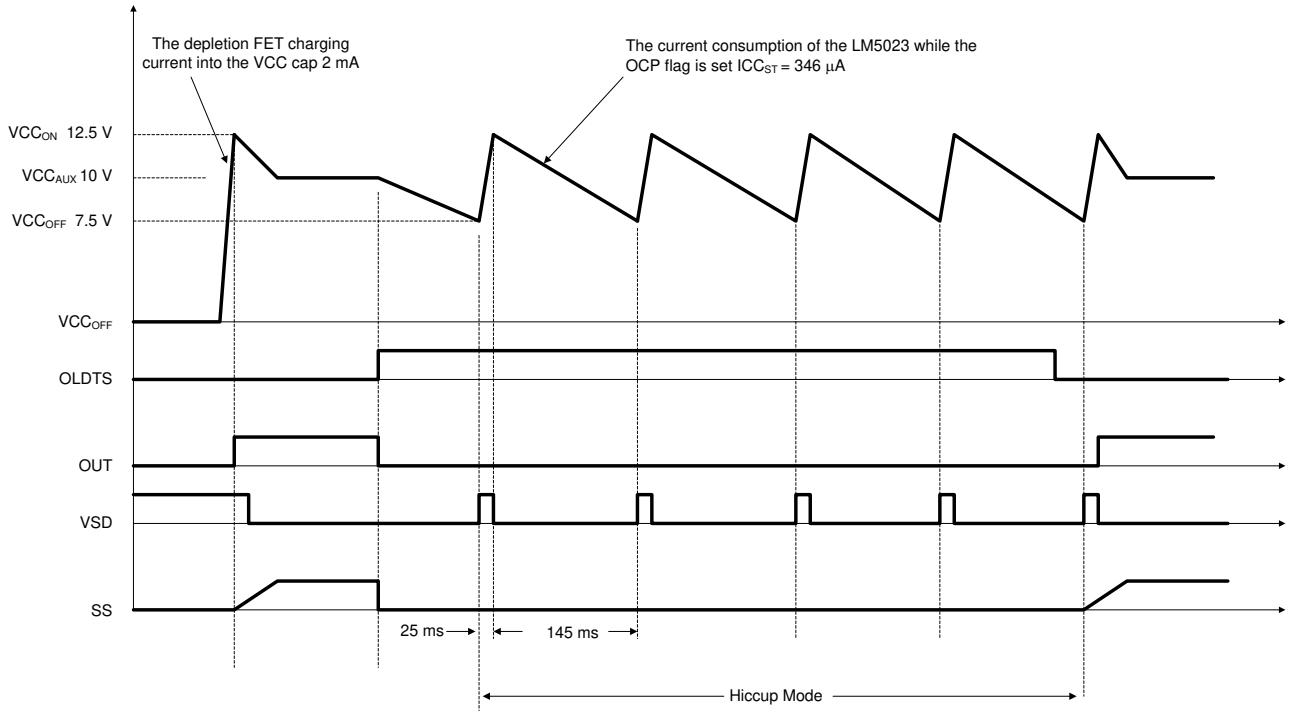


Figure 7-4. Hiccup Mode Timing

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7.2.3 Application Curves

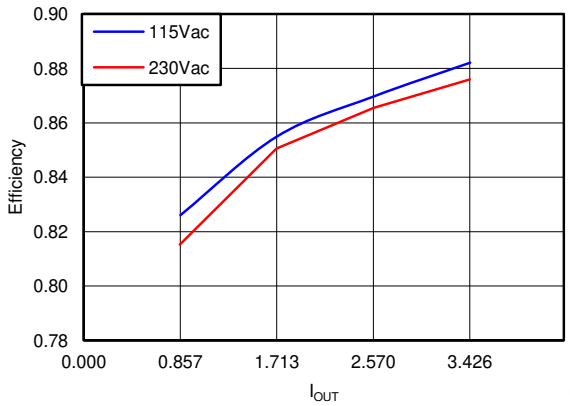
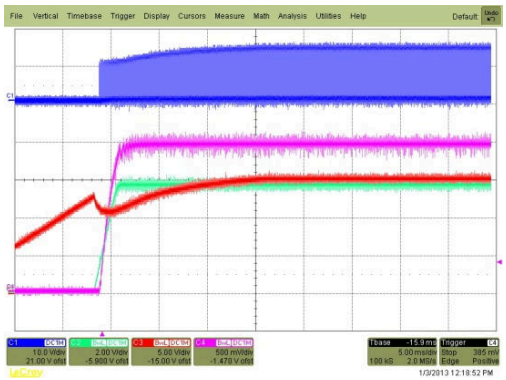
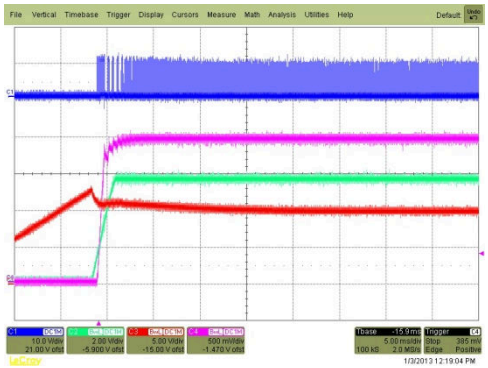


Figure 7-5. LM5023 EVM Efficiency



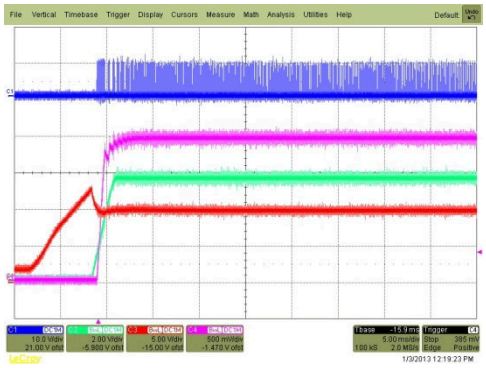
CH1: OUT, 10V/div
CH2: SS, 2V/div
CH3: VCC, 5V/div
CH4: VOUT, 5V/div

Figure 7-6. 115V Start-Up, 3.43A Load



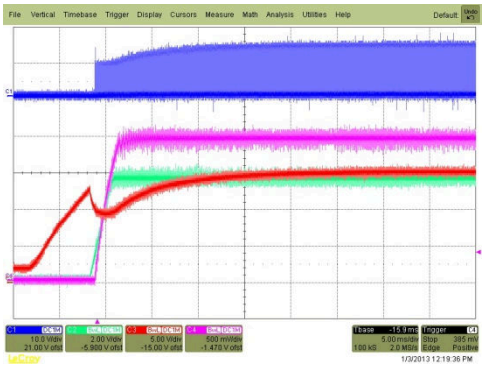
CH1: OUT, 10V/div
CH2: SS, 2V/div
CH3: VCC, 5V/div
CH4: VOUT, 5V/div

Figure 7-7. 115V Start-Up, 0.1A Load



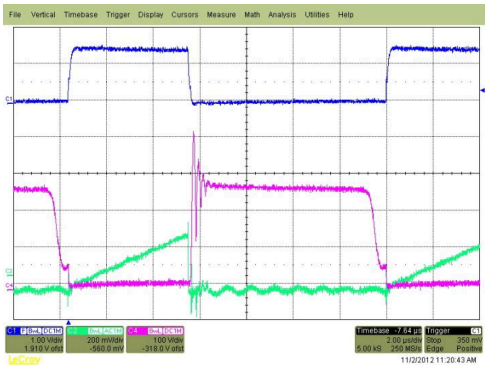
CH1: OUT, 10V/div
CH2: SS, 2V/div
CH3: VCC, 5V/div
CH4: VOUT, 5V/div

Figure 7-8. 230V Start-Up, 0.1A Load



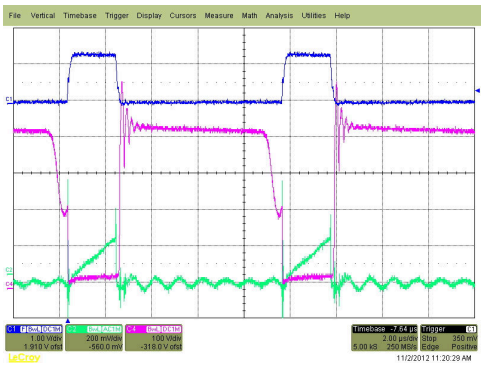
CH1: OUT, 10V/div
CH2: SS, 2V/div
CH3: VCC, 5V/div
CH4: VOUT, 5V/div

Figure 7-9. 230V Start-Up, 3.43A Load



CH1: OUT, 10V/div
CH2: CS, 200mV/div
CH4: VDS, 100V/div

Figure 7-10. QR Waveforms VIN 115V_{AC}, I_{OUT} 3.43A



CH1: OUT, 10V/div CH2: CS, 200mV/div
CH4: VDS, 100V/div

Figure 7-11. QR Waveforms V_{IN} 230V_{AC}, I_{OUT} 3.43A

7.3 Power Supply Recommendations

The LM5023 device is intended for AC-to-DC adapters and power supplies with input voltage range from 85$V_{AC(rms)}$ to 265$V_{AC(rms)}$ using the flyback topology. It can also be used in other applications and convertor topologies with different input voltages. Be sure that all voltages and currents are within the recommended operating conditions and absolute maximum ratings of the device.

7.4 Layout

7.4.1 Layout Guidelines

TI recommends all high-current loops be kept as short as possible. Keep all high-current and high-frequency traces away from other traces in the design. If necessary, high-frequency and high-current traces must be perpendicular to signal traces, not parallel to them. It is good practice to shield signal traces with ground traces to help reduce noise pick up. The ground reference for components connected to the signal pins must be a kelvin connection to the VCC bypass capacitor and GND pin. Always consider appropriate clearances between high-voltage nets and low-voltage nets.

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7.4.2 Layout Example

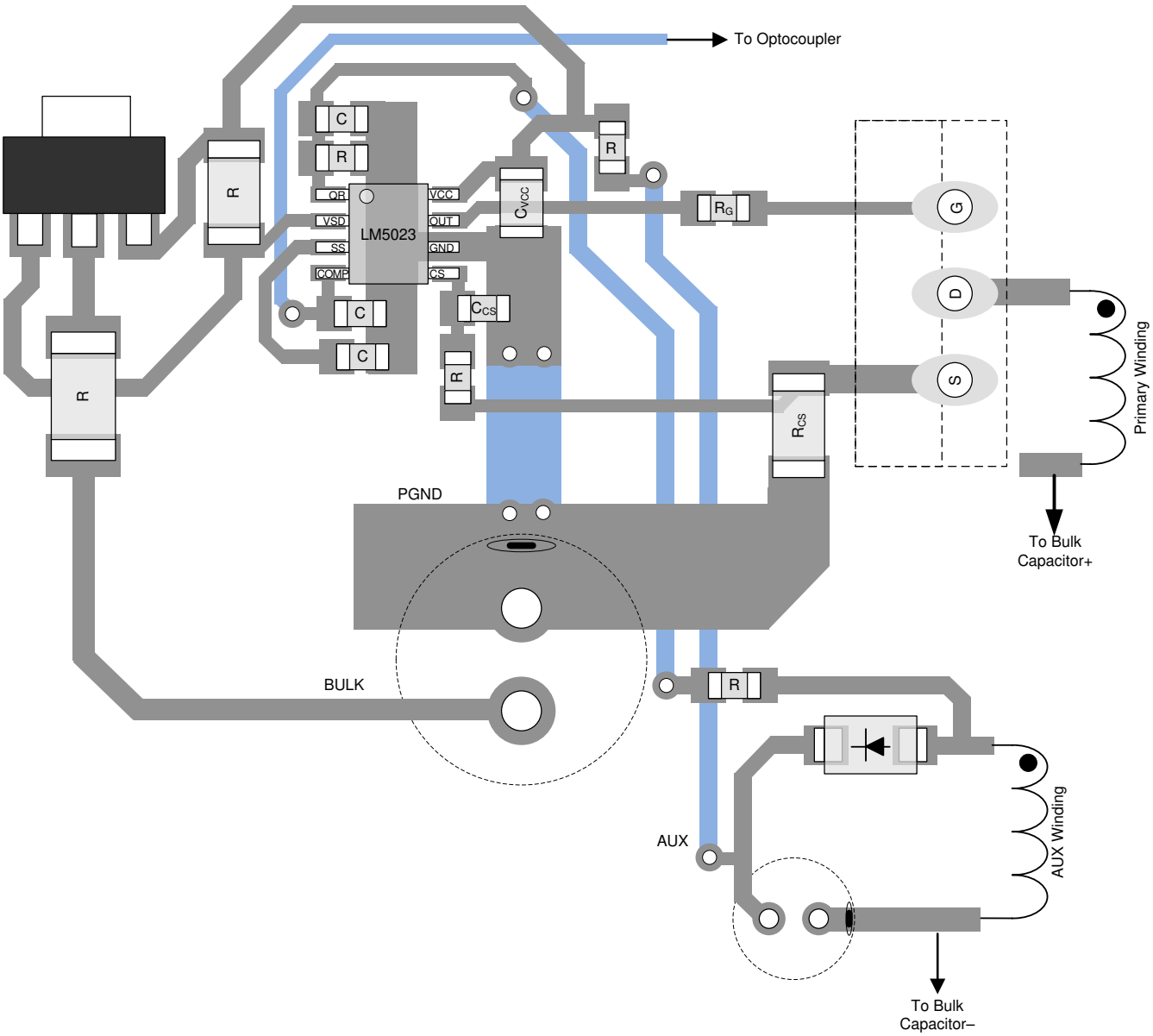


Figure 7-12. LM5023 Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

For design tools see the LM5023 PSpice Transient Model and the LM5023 TINA-TI Transient Spice Model.

8.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5023 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

-
- *LM5023-2EVM Notebook Adapter*
- *Using the UCC24630EVM-636 65W AC-to-DC Adapter*

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Community Resources

8.5 Trademarks

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ENERGY STAR® is a registered trademark of EPA.
All trademarks are the property of their respective owners.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (July 2014) to Revision F (October 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision D (January 2014) to Revision E (July 2014)	Page
• Added *Pin Configuration and Functions* section, *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout*	

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section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5023MM-2/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SK9B
LM5023MM-2/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SK9B
LM5023MMX-2/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SK9B
LM5023MMX-2/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SK9B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

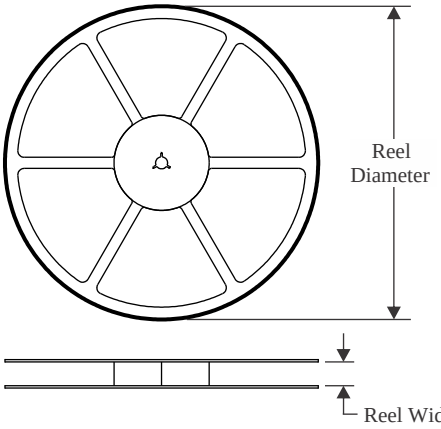
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

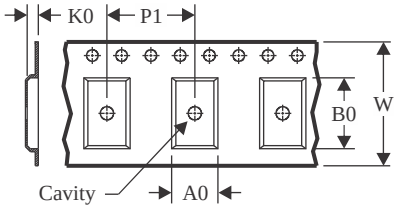
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

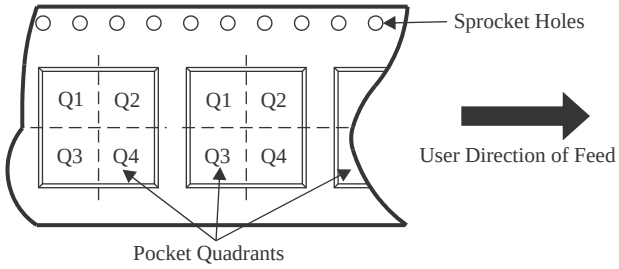


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

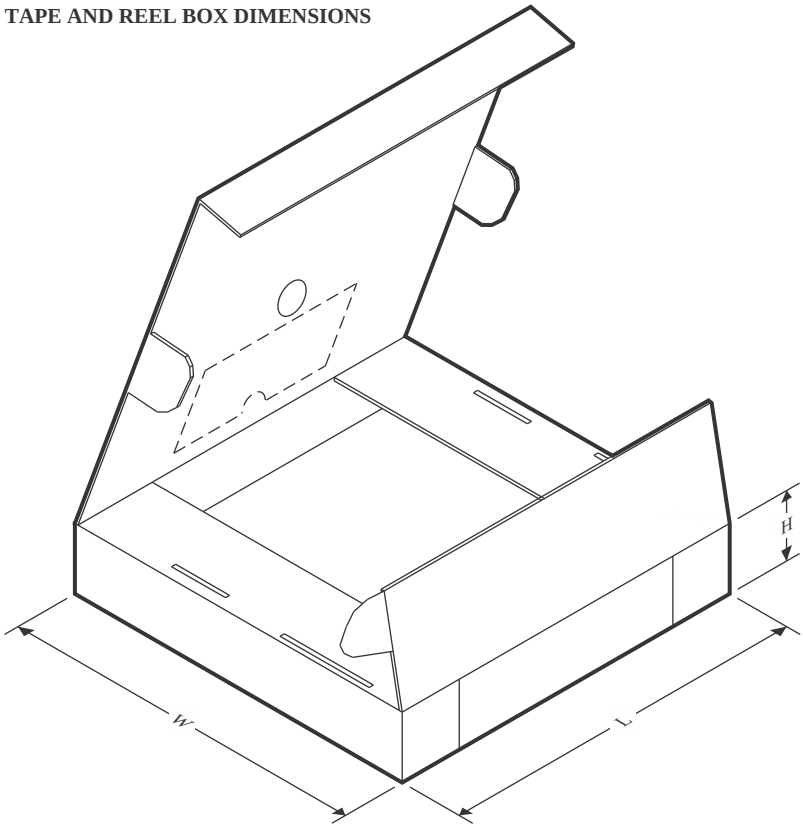
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5023MM-2/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5023MMX-2/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

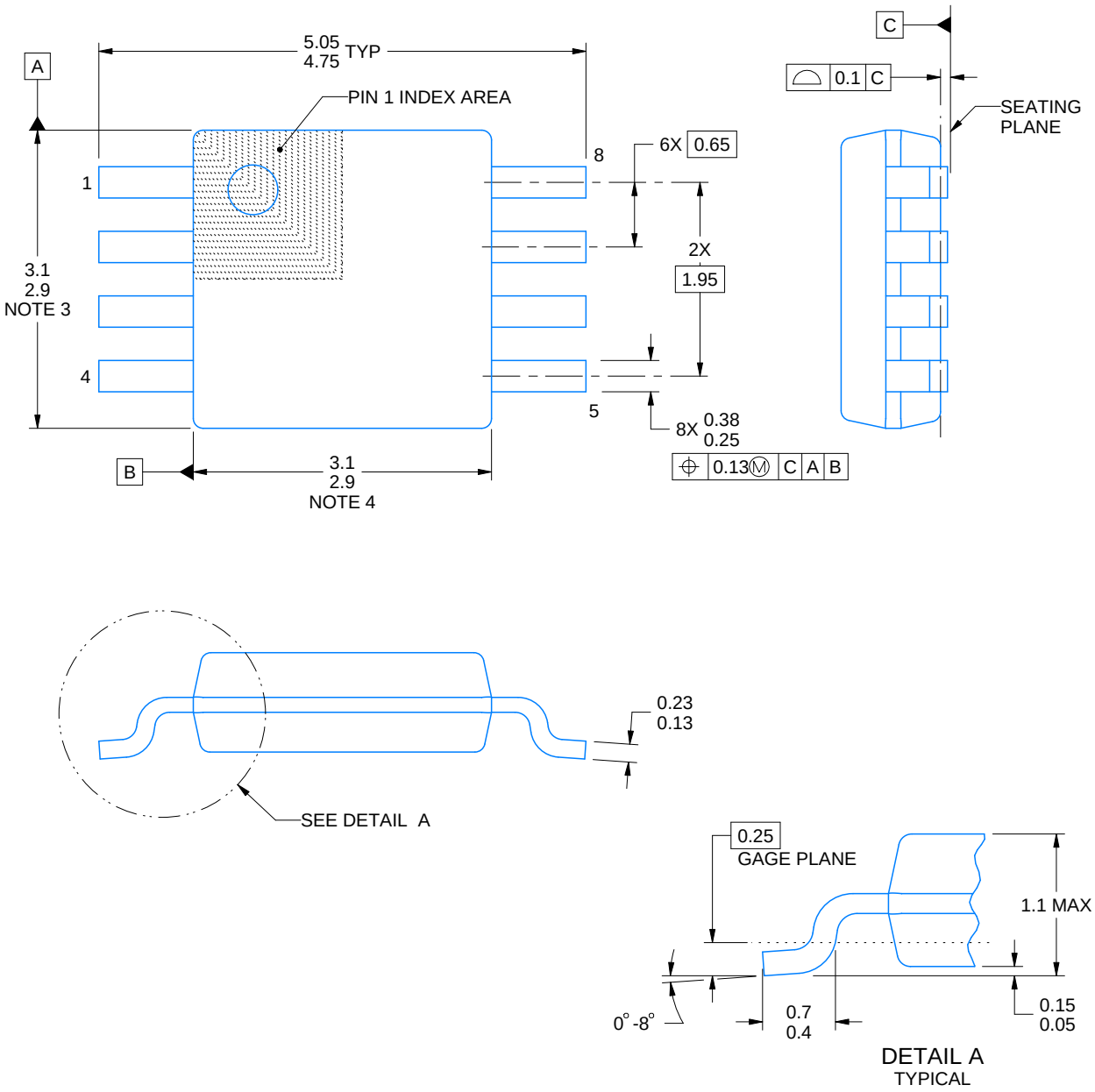
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5023MM-2/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM5023MMX-2/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

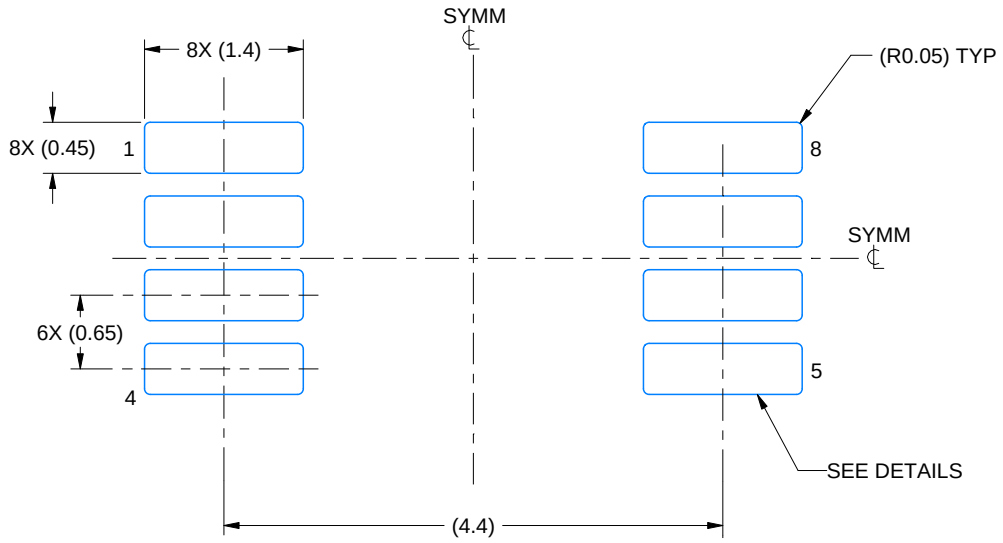
SMALL OUTLINE PACKAGE



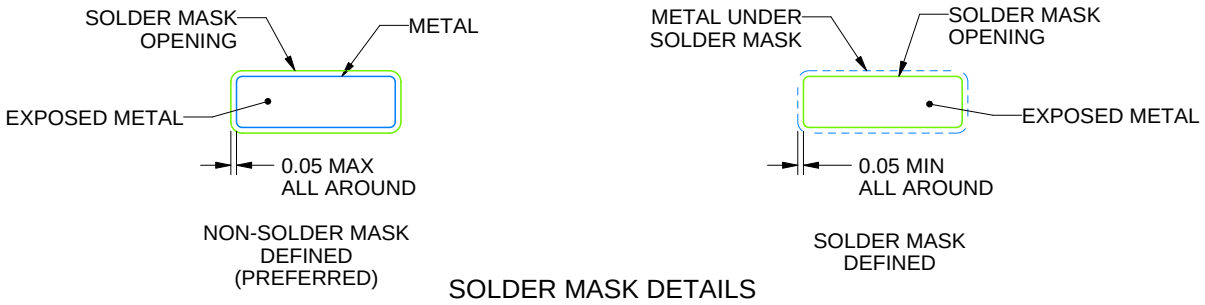
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

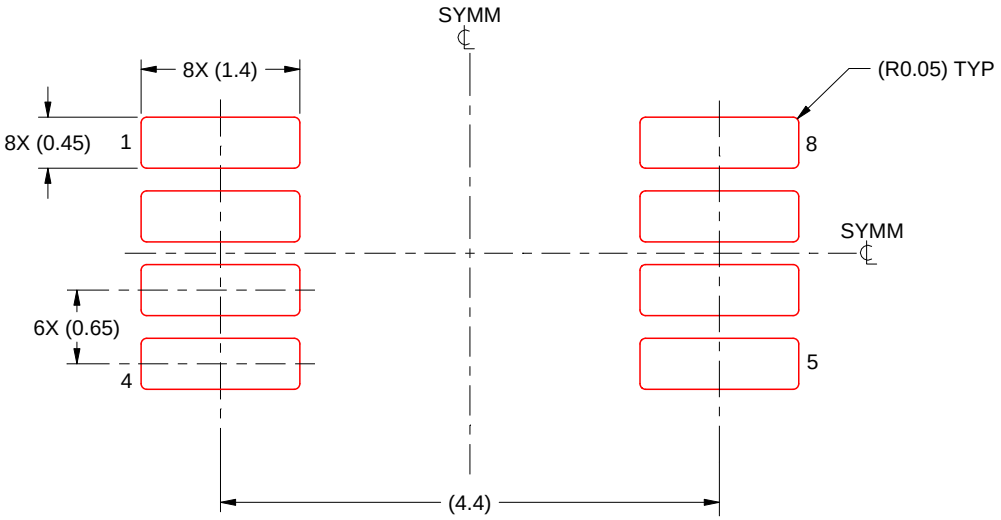


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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