LM555QML Timer

Check for Samples: LM555QML

FEATURES

- **Direct Replacement for SE555/NE555**
- **Timing from Microseconds through Hours**
- **Operates in Both Astable and Monostable Modes**
- **Adjustable Duty Cycle**
- **Output can Source or Sink 200 mA**
- **Output and Supply TTL Compatible**
- **Temperature Stability Better than 0.005% per °C**
- **Normally On and Normally Off Output**

APPLICATIONS

- **Precision Timing**
- **Pulse Generation**
- **Sequential Timing**
- **Time Delay Generation**
- **Pulse Width Modulation**
- **Pulse Position Modulation**
- **Linear Ramp Generator**

DESCRIPTION

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

CONNECTION DIAGRAM

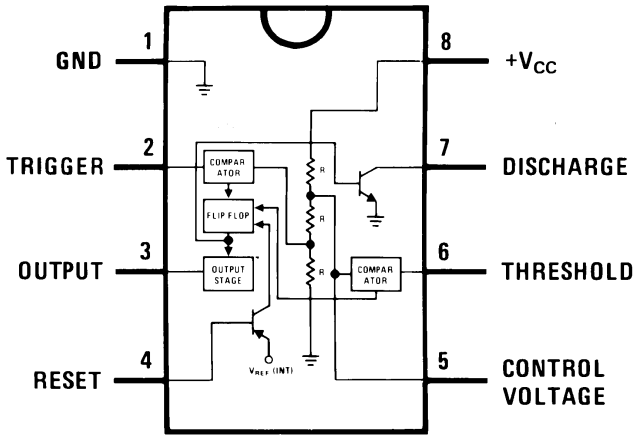


Figure 1. Dual-In-Line Package

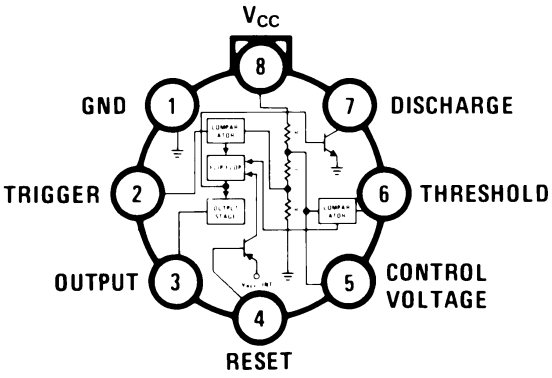


Figure 2. Metal Can Package

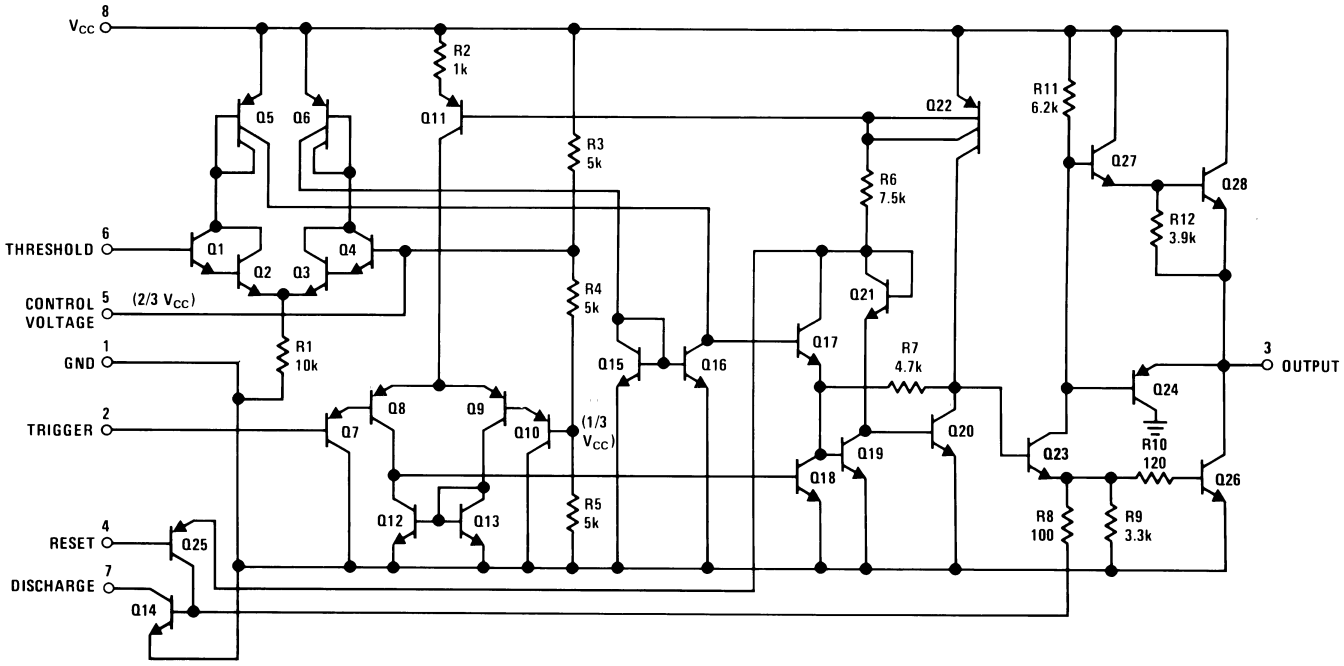
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SCHEMATIC DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage			+18V
Power Dissipation (2)	Metal Can		760 mW
	CDIP		1180 mW
Operating Temperature Range			$-55°C \le T_A \le +125°C$
Maximum Junction Temperature (T_{Jmax})			+150°C
Storage Temperature Range			$-65°C \le T_A \le +150°C$
Soldering Information (Soldering 10 Seconds)			260°C
Thermal Resistance	θ_{JA}	CDIP Still Air	125°C/W
		CDIP 500LF / Min Air Flow	71°C/W
		Metal Can Still Air	176°C/W
		Metal Can 500LF / Min Air Flow	96°C/W
	θ_{JC}	CDIP	20°C/W
		Metal Can	42°C/W
ESD Tolerance (3)			500V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

(3) Human body model, 1.5KΩ in series with 100pF.

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Table 1. QUALITY CONFORMANCE INSPECTION

Subgroup	Description	Temp °C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

ELECTRICAL CHARACTERISTICS- DC PARAMETERS

The following conditions apply to all the following parameters, unless otherwise specified.
DC: $+5V \le V_{CC} \le +15V$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CCL}	Supply Current Low State	V_{CC} = 5V, $R_L = \infty$			5.0	mA	1
		V_{CC} = 15V, $R_L = \infty$			12.0	mA	1
		V_{CC} = 18V, $R_L = \infty$, $V_2 = V_6$ = 18V			18.5	mA	1
I_{L7}	Leakage Current Pin 7	V_{CC} = 18V, V_7 = 18V, $V_2 = V_6$ = 0			100	nA	1
V_{Sat}	Saturation Voltage Pin 7	V_{CC} = 15V, I_7 = 15mA, $V_2 = V_6$ = 12V	See (1)		240	mV	1
		V_{CC} = 4.5V, I_7 = 4.5mA	See (1)		80	mV	1
V_{CO}	Control Voltage	V_{CC} = 5V, $V_2 = V_6$ = 4V		2.9	3.8	V	1, 2, 3
		V_{CC} = 15V, $V_2 = V_6$ = 12V		9.6	10.4	V	1, 2, 3
V_{Th}	Threshold Voltage			9.5	10.5	V	1
I_{Th}	Threshold Current	$V_6 = V_{Th}$, V_2 = 7.5V, $V_{Th} = V_{Th}$ Test Measured Value	See (2)		250	nA	1
I_{Trig}	Trigger Current	V_2 = 0			500	nA	1
V_{Trig}	Trigger Voltage	V_{CC} = 15V		4.8	5.2	V	1
				3.0	6.0	V	2, 3
		V_{CC} = 5V	See (3)	1.45	1.9	V	1, 2, 3
I_{Reset}	Reset Current	$V_2 = V_6$ = Gnd			0.4	mA	1
V_{Reset}	Reset Voltage			0.4	1.0	V	1

(1) No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.
(2) This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20MΩ.
(3) Ensured by tests at V_{CC} = 15V.

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ELECTRICAL CHARACTERISTICS- DC PARAMETERS (continued)

The following conditions apply to all the following parameters, unless otherwise specified.
DC: $+5V \le V_{CC} \le +15V$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{OL}	Output Voltage Drop Low	V_{CC} = 5V, I_{Sink} = +8mA, V_7 = 5V, V_6 = 5V			250	mV	1, 2, 3
		V_{CC} = 15V, I_{Sink} = +10mA, $V_2 = V_6$ = 15V			150	mV	1
					250	mV	2, 3
		V_{CC} = 15V, I_{Sink} = +50mA, $V_2 = V_6$ = 15V			500	mV	1
					800	mV	2, 3
		V_{CC} = 15V, I_{Sink} = +85mA, $V_2 = V_6$ = 15V			2.2	V	1, 2, 3
V_{OH}	Output Voltage Drop High	V_{CC} = 15V, I_{Source}= 85mA		13		V	1
				12.75		V	2, 3
		V_{CC} = 5V, I_{Source} = 85mA		3		V	1
				2.75		V	2, 3
A*f*	A Stable Frequency		See (4)	45	51	KHz	1
tE	Timing Error	V_{CC} = 5V	See (4)		±2	%	1, 2, 3
		V_{CC} = 15V, 1KΩ ≤ R_A ≤ 100KΩ, Timing error decreases with an increase in V_{CC}	See (4)		±2	%	1, 2, 3
$\Delta tE / \Delta V_{CC}$	Timing Drift with Supply	$5V \le V_{CC} \le 15V$	See (4)		0.2	% / V	1, 2, 3

(4) Ensured parameter, not tested.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

The following conditions apply to all the following parameters, unless otherwise specified.
AC: $+5V \le V_{CC} \le +15V$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
tR	Rise Time	V_{Trig} = 5V	See (1)		250	nS	9, 10
			See (1)		400	nS	11
tF	Fall Time	V_{Trig} = 5V	See (1)		250	nS	9, 10
			See (1)		400	nS	11

(1) Ensured parameter, not tested.

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TYPICAL PERFORMANCE CHARACTERISTICS

Minimum Pulse Width Required for Triggering

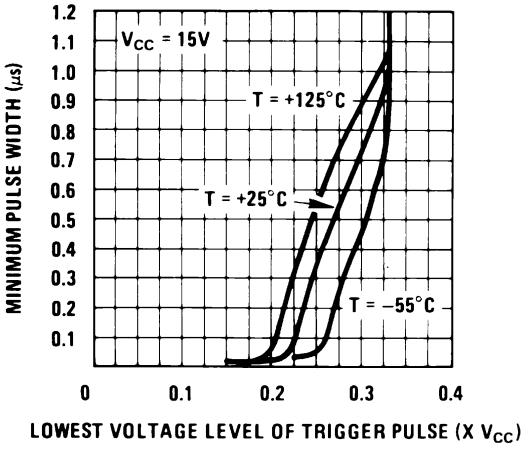


Figure 3.

Supply Current vs. Supply Voltage

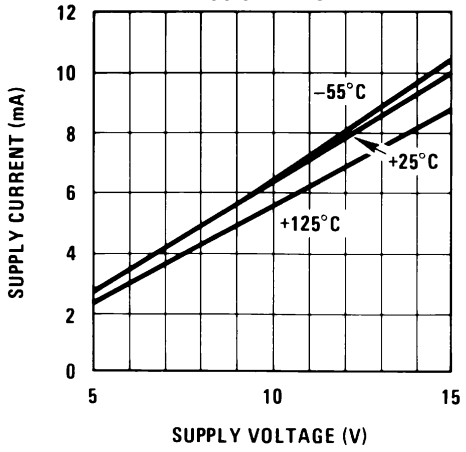


Figure 4.

High Output Voltage vs. Output Source Current

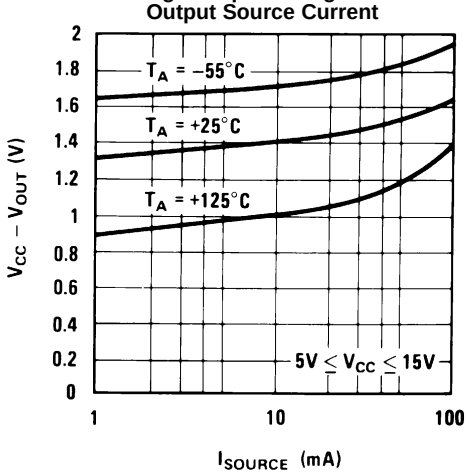


Figure 5.

Low Output Voltage vs. Output Sink Current

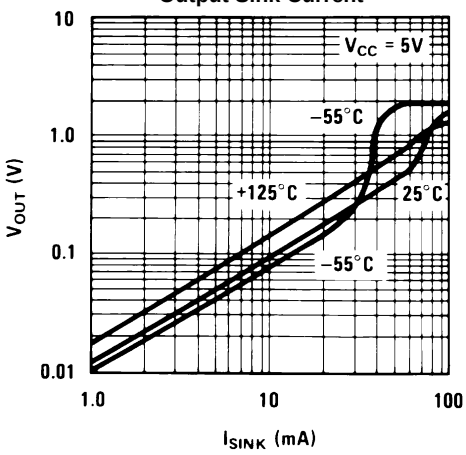


Figure 6.

Low Output Voltage vs. Output Sink Current

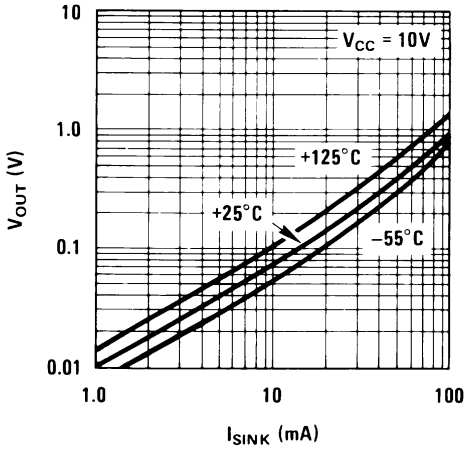


Figure 7.

Low Output Voltage vs. Output Sink Current

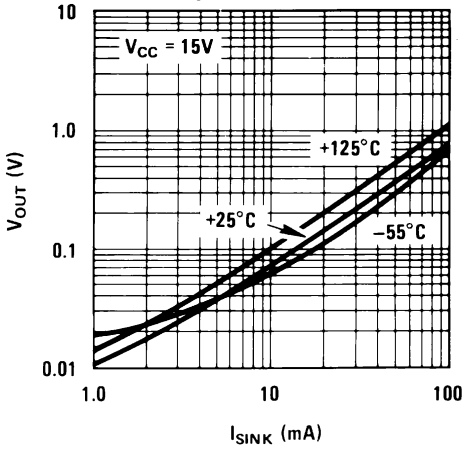


Figure 8.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Output Propagation Delay vs. Voltage Level of Trigger Pulse

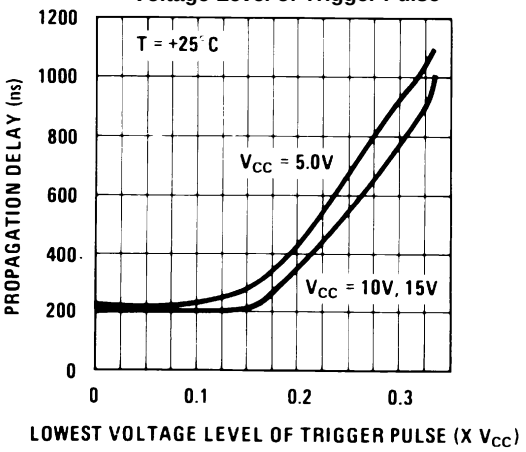


Figure 9.

Output Propagation Delay vs. Voltage Level of Trigger Pulse

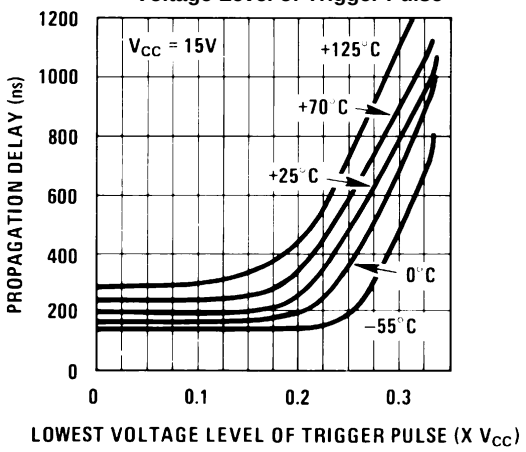


Figure 10.

Discharge Transistor (Pin 7) Voltage vs. Sink Current

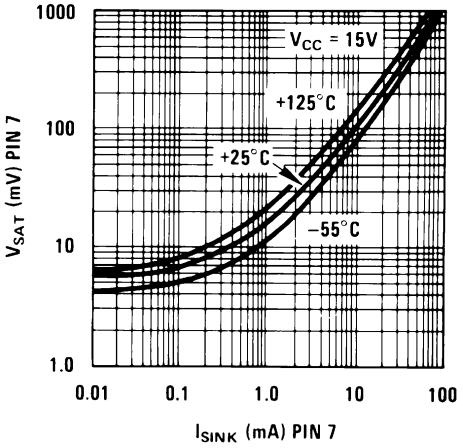


Figure 11.

Discharge Transistor (Pin 7) Voltage vs. Sink Current

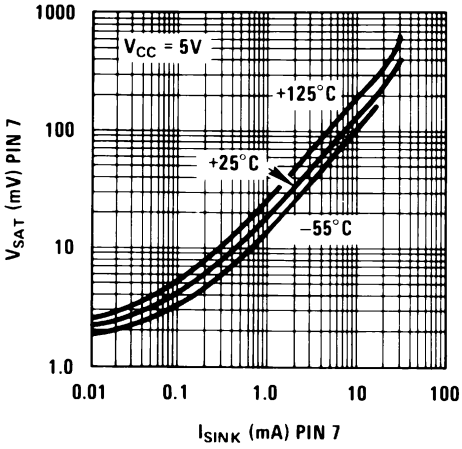


Figure 12.

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APPLICATIONS INFORMATION

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (Figure 13). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

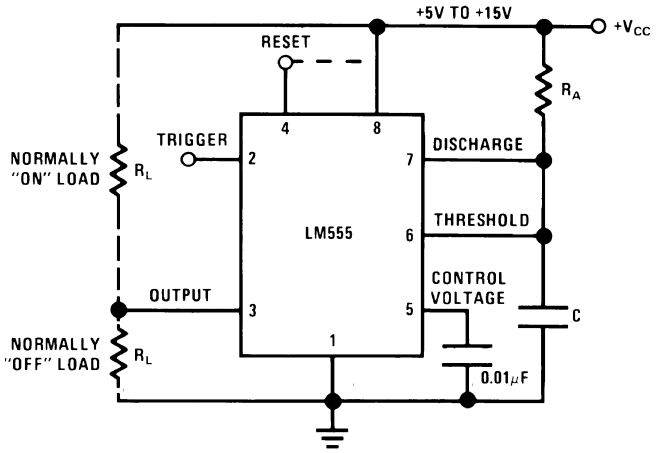
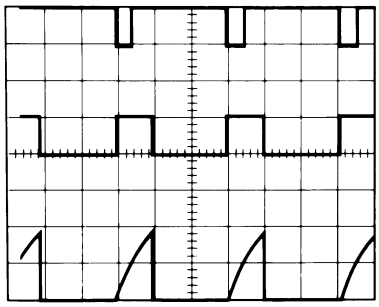


Figure 13. Monostable

The voltage across the capacitor then increases exponentially for a period of t = 1.1 R_A C, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. Figure 14 shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.



V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 9.1kΩ
C = 0.01μF

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

Figure 14. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

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Figure 15 is a nomograph for easy determination of R, C values for various time delays.

NOTE

In monostable operation, the trigger should be driven high before the end of timing cycle.

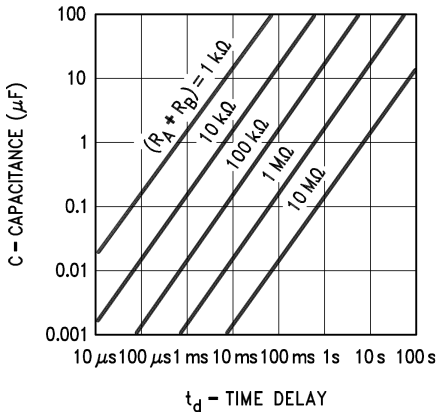


Figure 15. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in Figure 16 (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

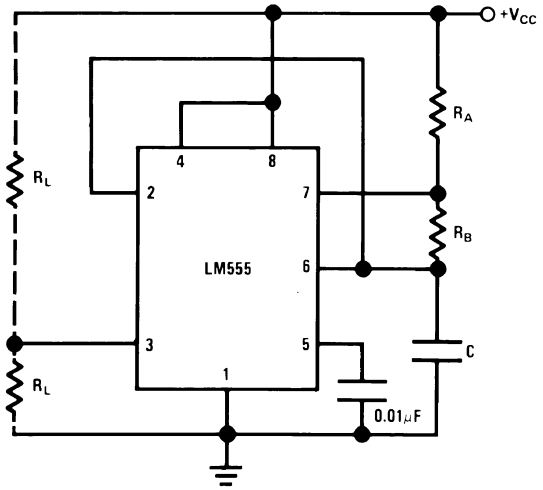
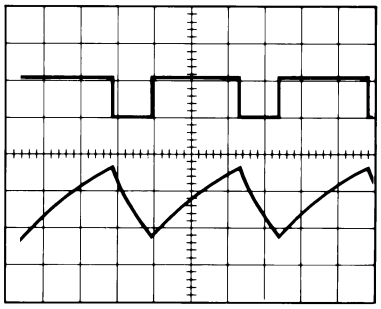


Figure 16. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 17 shows the waveforms generated in this mode of operation.

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V_{CC} = 5V Top Trace: Output 5V/Div.
TIME = 20µs/DIV. Bottom Trace: Capacitor Voltage 1V/Div.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

Figure 17. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C \quad (1)$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C \quad (2)$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C \quad (3)$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2\,R_B)\,C} \quad (4)$$

Figure 18 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B} \quad (5)$$

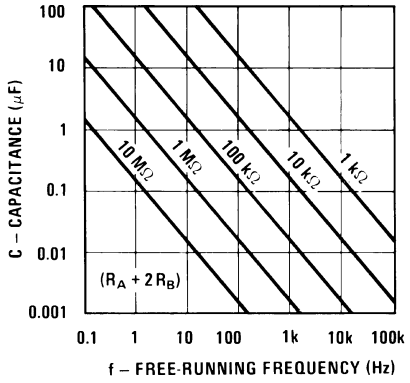
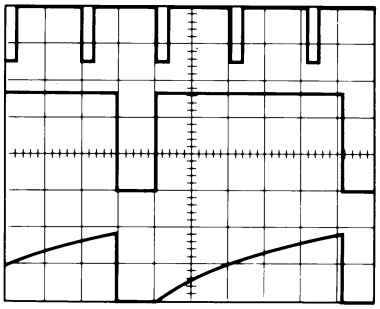


Figure 18. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of Figure 13 can be used as a frequency divider by adjusting the length of the timing cycle. Figure 19 shows the waveforms generated in a divide by three circuit.



V_{CC} = 5V
TIME = 20µs/DIV.
R_A = 9.1kΩ
C = 0.01µF

Top Trace: Input 4V/Div.
Middle Trace: Output 2V/Div.
Bottom Trace: Capacitor 2V/Div.

Figure 19. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. Figure 20 shows the circuit, and in Figure 21 are some waveform examples.

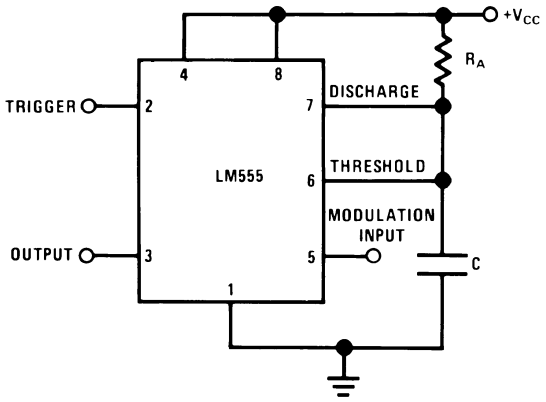
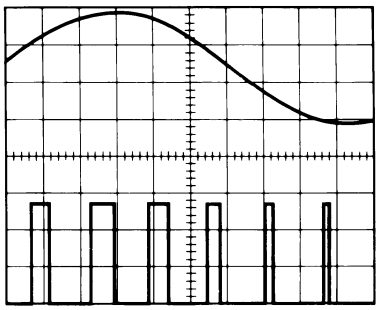


Figure 20. Pulse Width Modulator

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V_{CC} = 5V Top Trace: Modulation 1V/Div.
TIME = 0.2 ms/DIV. Bottom Trace: Output Voltage 2V/Div.
R_A = 9.1kΩ
C = 0.01µF

Figure 21. Pulse Width Modulator

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in Figure 22, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 23 shows the waveforms generated for a triangle wave modulation signal.

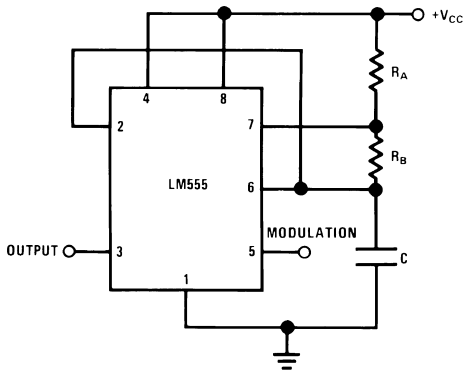
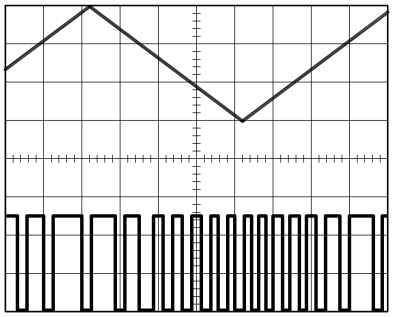


Figure 22. Pulse Position Modulator



V_{CC} = 5V Top Trace: Modulation Input 1V/Div.
TIME = 0.1 ms/DIV. Bottom Trace: Output 2V/Div.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

Figure 23. Pulse Position Modulator

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LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. Figure 24 shows a circuit configuration that will perform this function.

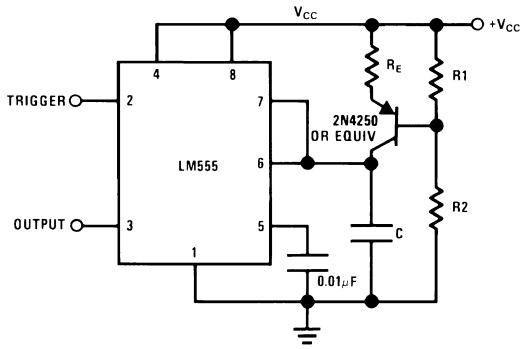


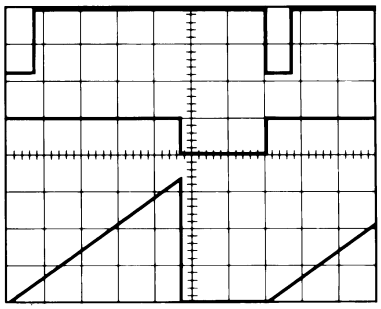
Figure 24. Linear Ramp Circuit Configuration

Figure 25 shows waveforms generated by the linear ramp.

The time interval is given by:

$$T = \frac{2/3\ V_{CC}\ R_E\ (R_1 + R_2)\ C}{R_1\ V_{CC} - V_{BE}\ (R_1 + R_2)} \qquad V_{BE} \cong 0.6V \tag{6}$$

$$V_{BE} \simeq 0.6V \tag{7}$$



V_{CC} = 5V Top Trace: Input 3V/Div.
TIME = 20μs/DIV. Middle Trace: Output 5V/Div.
R_1 = 47kΩ Bottom Trace: Capacitor Voltage 1V/Div.
R_2 = 100kΩ
R_E = 2.7 kΩ
C = 0.01 μF

Figure 25. Linear Ramp

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in Figure 26. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is t_2 =

$$\left[(R_A\ R_B)/(R_A + R_B)\right] C\ \ell n \left[\frac{R_B - 2R_A}{2R_B - R_A}\right] \tag{8}$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2} \tag{9}$$

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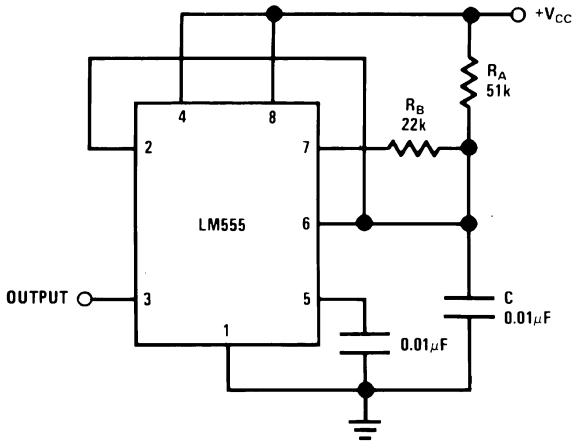


Figure 26. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1μF in parallel with 1μF electrolytic.

Lower comparator storage time can be as long as 10μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10μs minimum.

Delay time reset to output is 0.47μs typical. Minimum reset pulse width must be 0.3μs, typical.

Pin 7 current switches within 30ns of the output (pin 3) voltage.

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Table 2. REVISION HISTORY

Date Released	Revision	Section	Originator	Changes
08/04/05	A	New Release to corporate format	L. Lytle	1 MDS datasheet converted into once datasheet in the corporate format. Removed drift endpoints since not performed on 883 product. MNLM555-X Rev 0B0 to be archived
04/10/06	B	Ordering Information Table	R. Malone	NS Package Number and Description was referenced incorrectly. Revision A will be Archived.
07/25/06	C	APPLICATIONS INFORMATION	R. Malone	Correct a typo in the paragraph after Figure 13(change the word internal to interval) to reflect same change made to Commercial data sheet. Revision B will be Archived.
04/01/13	C	All		Changed layout of National Data Sheet to TI format.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM555H/883	Active	Production	TO-99 (LMC) | 8	20 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LM555H/883 Q ACO LM555H/883 Q >T
LM555J/883	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM555J /883 Q ACO /883 Q >T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

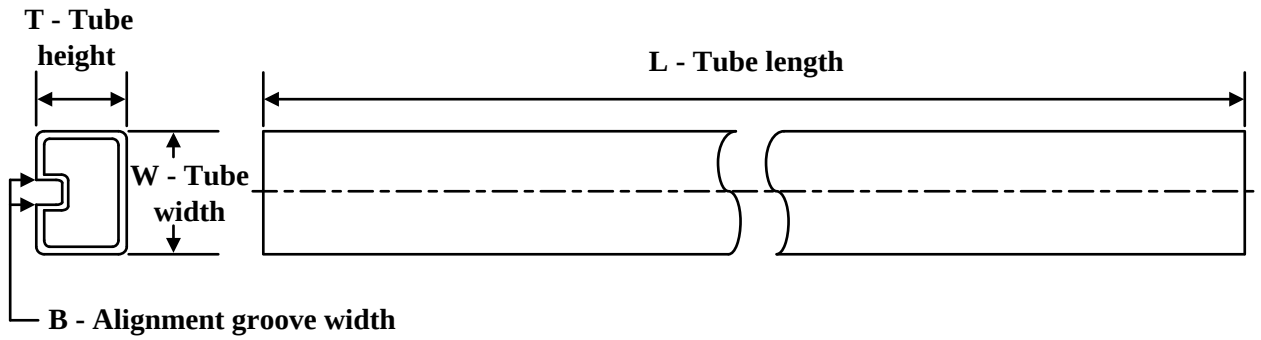
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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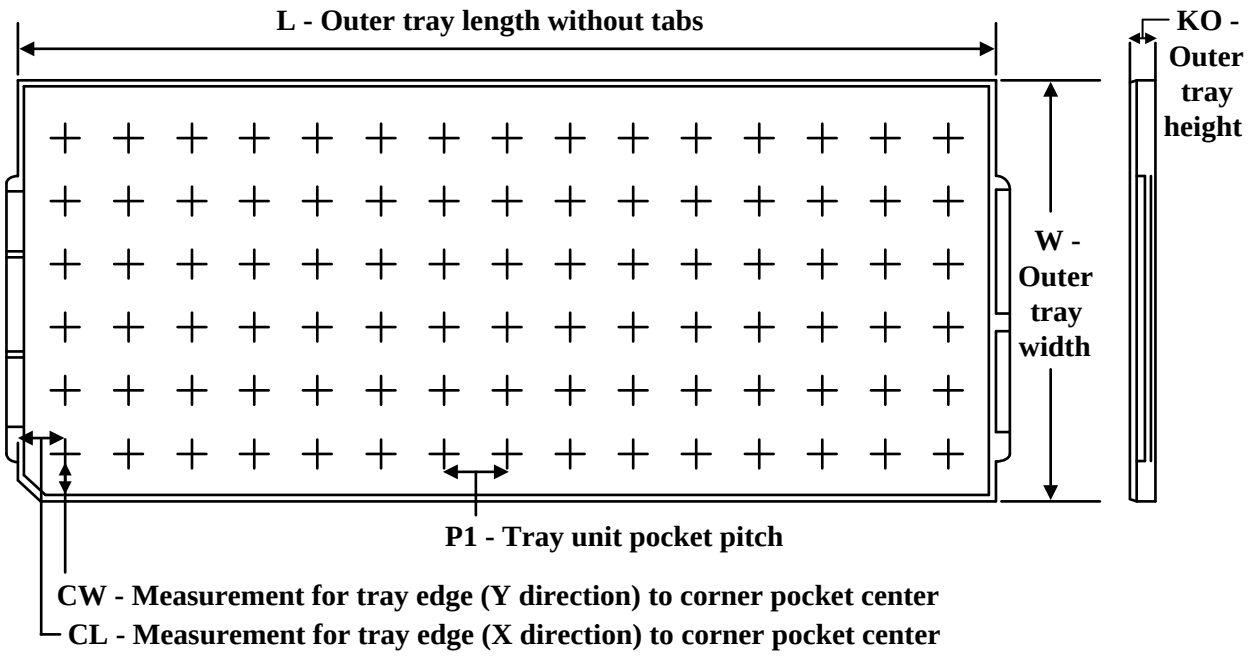
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM555J/883	NAB	CDIP	8	40	506.98	15.24	13440	NA

TRAY

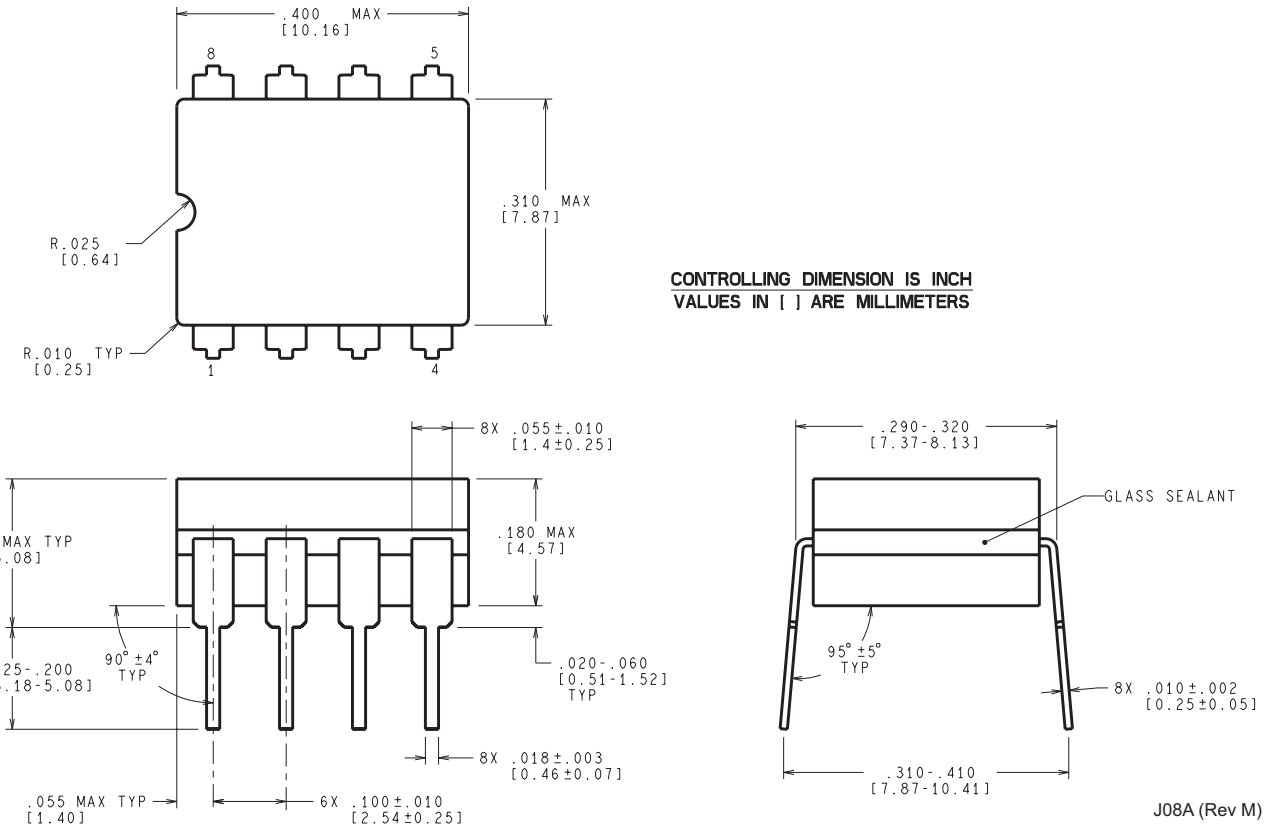


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
LM555H/883	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54

NAB0008A

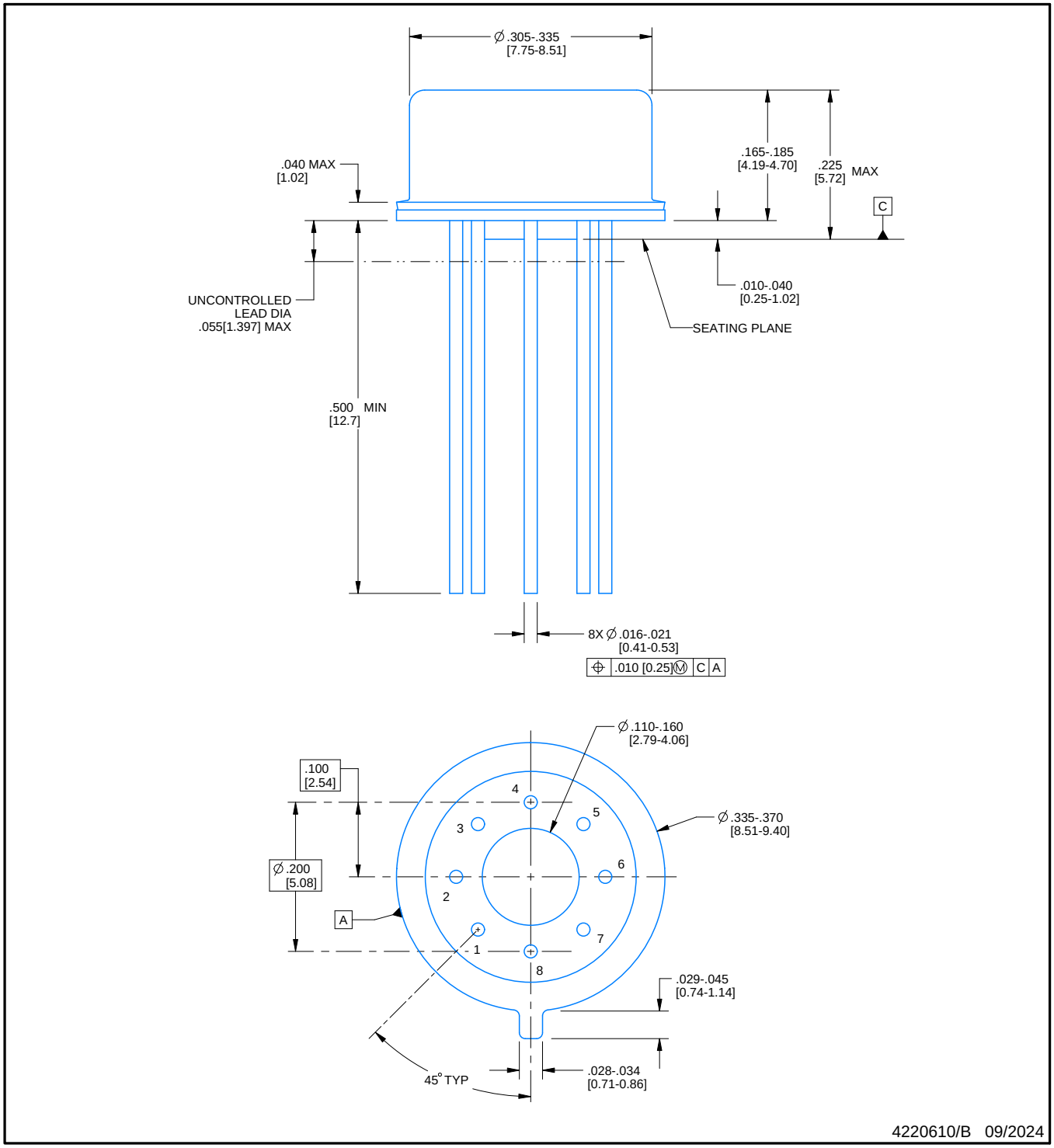

.400 MAX
[10.16]
8
5
.310 MAX
[7.87]
R.025
[0.64]
R.010 TYP
[0.25]
1
4
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
8X .055±.010
[1.4±0.25]
.200 MAX TYP
[5.08]
.180 MAX
[4.57]
8X .125-.200
[3.18-5.08]
90° ±4°
TYP
.020-.060
[0.51-1.52]
TYP
8X .018±.003
[0.46±0.07]
.055 MAX TYP
[1.40]
6X .100±.010
[2.54±0.25]
.290-.320
[7.37-8.13]
GLASS SEALANT
95° ±5°
TYP
8X .010±.002
[0.25±0.05]
.310-.410
[7.87-10.41]
J08A (Rev M)

PACKAGE OUTLINE

LMC0008A

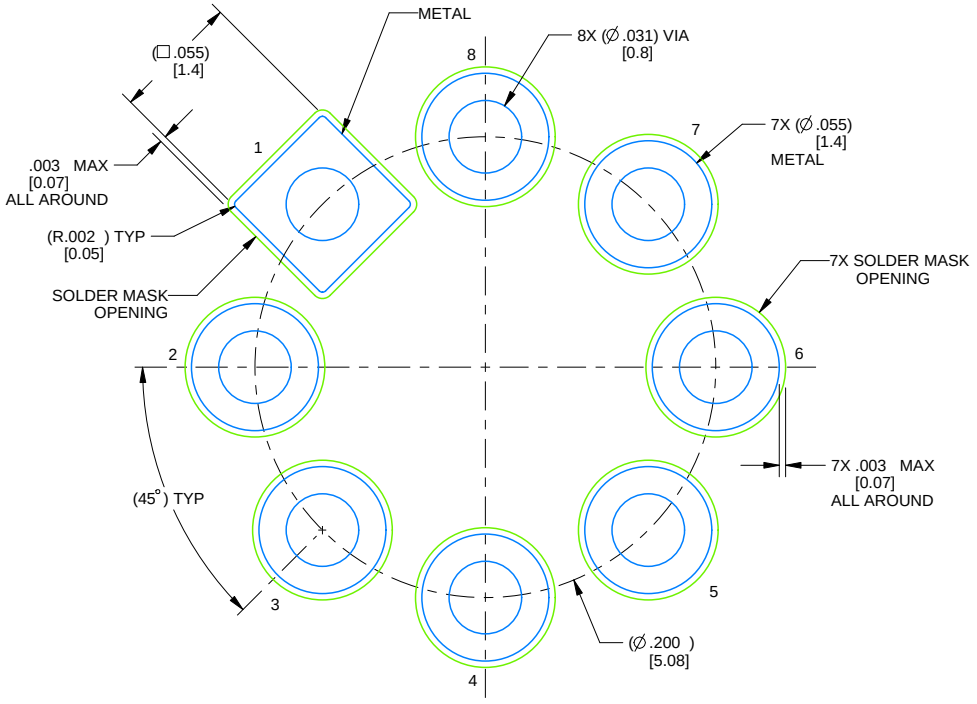
TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

4220610/B 09/2024

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