

LM614x 17MHz Rail-to-Rail Input-Output Operational Amplifiers

1 Features

At $V_S = 5V$. Typ Unless Noted.

- Rail-to-rail Input CMVR $-0.25V$ to $5.25V$
- Rail-to-Rail Output
- Wide Gain-Bandwidth: 17MHz at 50kHz (typ)
- Slew Rate: 30V/ μs
- Low Supply Current 650 μA /Amplifier
- Wide Supply Range 2.7V to 24V
- CMRR 107dB
- Gain 108dB with $R_L = 10k$
- PSRR 87dB

2 Applications

- Battery Operated Instrumentation
- Depth Sounders/Fish Finders
- Barcode Scanners
- Wireless Communications
- Rail-to-Rail in-out Instrumentation Amps

3 Description

Using patent pending new circuit topologies, the LM6142/LM6144 provides new levels of performance in applications where low voltage supplies or power limitations previously made compromise necessary. Operating on supplies of 2.7V to over 24V, the LM6142/LM6144 is an excellent choice for battery operated systems, portable instrumentation and others.

The greater than rail-to-rail input voltage range eliminates concern over exceeding the common-mode voltage range. The rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

High gain-bandwidth with 650 μA /Amplifier supply current opens new battery powered applications where previous higher power consumption reduced battery life to unacceptable levels. The ability to drive large capacitive loads without oscillating functionally removes this common problem.

Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE ⁽¹⁾	BODY SIZE
LM6142	Dual	D (SOIC, 8)	4.90mm × 3.91mm
		P (PDIP, 8)	9.81mm × 6.35mm
LM6144	Quad	D (SOIC, 14)	8.65mm × 3.91mm
		NFF (PDIP, 14)	19.177mm × 6.35mm



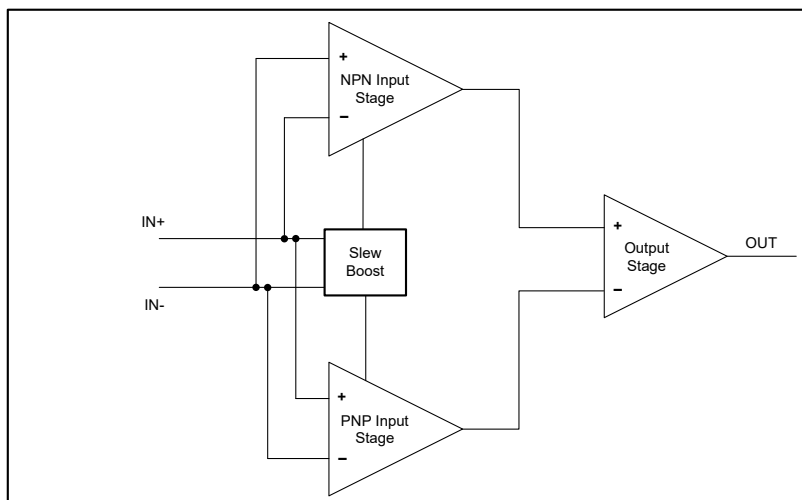
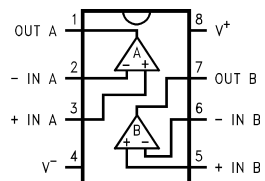
**Functional Block Diagram**

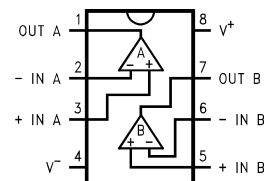
Table of Contents

1 Features	1	5.9 Typical Characteristics.....	11
2 Applications	1	5.10 Old Versus New Die Comparison.....	16
3 Description	1	6 Application and Implementation	17
4 Connection Diagrams	4	6.1 Application Information.....	17
5 Specifications	5	6.2 Typical Applications.....	17
5.1 Absolute Maximum Ratings.....	5	7 Device and Documentation Support	19
5.2 ESD Ratings.....	5	7.1 Receiving Notification of Documentation Updates....	19
5.3 Recommended Operating Conditions.....	5	7.2 Support Resources.....	19
5.4 Thermal Information LM6142.....	6	7.3 Electrostatic Discharge Caution.....	19
5.5 Thermal Information LM6144.....	6	7.4 Glossary.....	19
5.6 Electrical Characteristics: $V_S = 5V$	7	8 Revision History	20
5.7 Electrical Characteristics: $V_S = 2.7V$	9	9 Mechanical, Packaging, and Orderable Information ..	22
5.8 Electrical Characteristics: $V_S = 24V$	10		

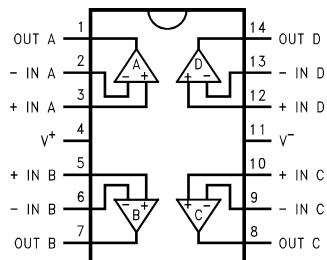
4 Connection Diagrams



**Figure 4-1. 8-Pin CDIP
Top View**



**Figure 4-2. 8-Pin PDIP/SOIC
Top View**



**Figure 4-3. 14-Pin PDIP/SOIC
Top View**

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$		0	33	V
Signal input pins	Common-mode voltage ⁽³⁾	$(V-) - 0.5$	$(V+) + 0.5$	V
	Differential voltage ⁽⁴⁾		± 15	V
	Current ⁽³⁾		± 10	mA
Output short-circuit ⁽²⁾		Continuous		
Operating ambient temperature, T_A		-55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		-65	150	°C

- (1) Operating the device beyond the ratings listed under *Absolute Maximum Ratings* will cause permanent damage to the device. These are stress ratings only, based on process and design limitations, and this device has not been designed to function outside the conditions indicated under *Recommended Operating Conditions*. Exposure to any condition outside *Recommended Operating Conditions* for extended periods, including absolute-maximum-rated conditions, may affect device reliability and performance.
- (2) Short-circuit to ground, one amplifier per package. Extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual destruction.
- (3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
- (4) Input pins are connected by back-to-back diodes for input protection. If the differential input voltage may exceed 0.5 V, limit the input current to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 4000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	± 1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, $(V+) - (V-)$	2.7	32	V
T_A	Specified temperature	-40	85	°C

5.4 Thermal Information LM6142

THERMAL METRIC ⁽¹⁾		LM6142		UNIT
		D (SOIC) ⁽¹⁾	P (PDIP) ⁽¹⁾	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	127.10	84.45	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.27	58.07	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.20	50.90	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.91	30.43	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	70.54	50.44	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Thermal Information LM6144

THERMAL METRIC ⁽¹⁾		LM6144		Unit
		D (SOIC) ⁽¹⁾	NFF (PDIP) ⁽¹⁾	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	82.48	81	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.77	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.86	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.66	N/A	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	37.51	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.6 Electrical Characteristics: $V_S = 5V$

For $V^+ = 5.0V$, $V^- = 0V$, $R_L > 1M\Omega$ connected to $V_S / 2$, $V_{CM} = V^+ / 2$, and $V_O = V^+ / 2$, at $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage	LM6142AI, LM6144AI		0.3		1	mV
			T _A = −40°C to 85°C	2.2			
		LM6142BI, LM6144BI		0.3		2.5	
			T _A = −40°C to 85°C	3.3			
dV _{OS} /dT	Input offset voltage drift	T _A = −40°C to 85°C		3			μV/°C
PSRR	Input offset voltage versus power supply	2.5V ≤ V _S ≤ 12V, LM6132AI, LM6134AI		78	82	dB	
			T _A = −40°C to 85°C	75			
		2.5V ≤ V _S ≤ 12V, LM6132BI, LM6134BI		78	82		
			T _A = −40°C to 85°C	75			
	Amp-to-amp isolation			130			dB
INPUT BIAS CURRENT							
I _B	Input bias current	LM6142AI, LM6144AI		170	250	nA	
		LM6142BI, LM6144BI		170	300		
		0V ≤ V _{CM} ≤ 5V, LM6142AI, LM6144AI		180	280		
			T _A = −40°C to 85°C	526			
		0V ≤ V _{CM} ≤ 5V, LM6142BI, LM6144BI		180			
			T _A = −40°C to 85°C	526			
I _{OS}	Input offset current	LM6142AI, LM6144AI		3	30	nA	
			T _A = −40°C to 85°C	80			
		LM6142BI, LM6144BI		3	30		
			T _A = −40°C to 85°C	80			
			INPUT VOLTAGE				
V _{CM}	Common-mode input voltage range			− 0.25	5.25	V	
		T _A = −40°C to 85°C		0	5	V	
CMRR	Common-mode rejection ratio	0V ≤ V _{CM} ≤ 4V, LM6142AI, LM6144AI		84	107	dB	
			T _A = −40°C to 85°C	78			
		0V ≤ V _{CM} ≤ 4V, LM6142BI, LM6144BI		84	107		
			T _A = −40°C to 85°C	78			
		0V ≤ V _{CM} ≤ 5V, LM6142AI, LM6144AI		66	82		
			T _A = −40°C to 85°C	64	79		
		0V ≤ V _{CM} ≤ 5V, LM6142BI, LM6144BI		66	82		
			T _A = −40°C to 85°C	64	79		
INPUT IMPEDANCE							
R _{IN}	Common-mode input resistance			126			MΩ
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	R _L = 10kΩ, LM6142AI, LM6144AI		100	270	V/mV	
			T _A = −40°C to 85°C	33	70		
		R _L = 10kΩ, LM6142BI, LM6144BI		80	270		
			T _A = −40°C to 85°C	25	70		
NOISE							
e _N	Input voltage noise density	f = 1kHz		16			nV/√Hz
i _N	Input current noise density	f = 1kHz		0.22			pA/√Hz
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	f = 50kHz		10	17	MHz	
			T _A = −40°C to 85°C	6			

For $V^+ = 5.0\text{V}$, $V^- = 0\text{V}$, $R_L > 1\text{M}\Omega$ connected to $V_S / 2$, $V_{CM} = V^+ / 2$, and $V_O = V^+ / 2$, at $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT		
SR	Slew rate	$V_S = 12\text{V}$, $V_{\text{STEP}} = 8\text{V}$, $R_S > 1\text{k}\Omega$	LM6142AI, LM6144AI	15	25	V/ μs			
			LM6142AI, LM6144AI, $T_A = -40^\circ\text{C}$ to 85°C	13					
			LM6142AI, LM6144AI	13	25				
			LM6142AI, LM6144AI, $T_A = -40^\circ\text{C}$ to 85°C	11					
PM	Phase margin				38		°		
THD+N	Total harmonic distortion + noise	$f = 10\text{kHz}$, $R_L = 10\text{k}\Omega$			0.003		%		
OUTPUT									
V_O	Voltage output swing	$R_L = 100\text{k}\Omega$, From positive rail			30	40	mV		
			$T_A = -40^\circ\text{C}$ to 85°C			70			
		$R_L = 100\text{k}\Omega$, From negative rail			45	50			
			$T_A = -40^\circ\text{C}$ to 85°C			60			
		$R_L = 10\text{k}\Omega$, From positive rail				40			
		$R_L = 10\text{k}\Omega$, From negative rail				50			
		$R_L = 2\text{k}\Omega$, From positive rail			100	140			
			$T_A = -40^\circ\text{C}$ to 85°C			200			
I_{SC}	Short-circuit current	Sourcing, LM6142A		10	13	mA			
			$T_A = -40^\circ\text{C}$ to 85°C	4.9			35		
		Sourcing, LM6142B		8	13				
			$T_A = -40^\circ\text{C}$ to 85°C	4			35		
		Sinking, LM6142A		10	24				
			$T_A = -40^\circ\text{C}$ to 85°C	5.3			35		
		Sinking, LM6142B		10	24				
			$T_A = -40^\circ\text{C}$ to 85°C	5.3			35		
I_Q	Quiescent current per amplifier	LM6142AI, LM6144AI			650	800	μA		
			$T_A = -40^\circ\text{C}$ to 85°C			880			
		LM6142BI, LM6144BI			650	800	μA		
			$T_A = -40^\circ\text{C}$ to 85°C			880			
		POWER SUPPLY							

5.7 Electrical Characteristics: $V_S = 2.7V$

For $V^+ = 2.7V$, $V^- = 0V$, $R_L > 1M\Omega$ connected to $V_S / 2$, $V_{CM} = V^+ / 2$, and $V_O = V^+ / 2$, at $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage	LM6142AI, LM6144AI		0.4	1.8	mV	
			T _A = −40°C to 85°C	4.3			
		LM6142BI, LM6144BI		0.4	2.5		
			T _A = −40°C to 85°C	5			
PSRR	Input offset voltage versus power supply	3V ≤ V* ≤ 5V		79		dB	
INPUT BIAS CURRENT							
I _B	Input bias current	LM6142AI, LM6144AI		150	250	nA	
			T _A = −40°C to 85°C	526			
		LM6142BI, LM6144BI		150	300		
			T _A = −40°C to 85°C	526			
I _{OS}	Input offset current	LM6142AI, LM6144AI		4	30	nA	
			T _A = −40°C to 85°C	80			
		LM6142BI, LM6144BI		4	30		
			T _A = −40°C to 85°C	80			
INPUT VOLTAGE							
V _{CM}	Common-mode input voltage range			0	2.7	V	
CMRR	Common-mode rejection ratio	0V ≤ V _{CM} ≤ 1.8V		90		dB	
		0V ≤ V _{CM} ≤ 2.7V		76			
INPUT IMPEDANCE							
R _{IN}	Common-mode input resistance			128		MΩ	
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	R _L = 10kΩ		55		V/mV	
NOISE							
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	f = 50kHz		9		MHz	
PM	Phase margin			36		°	
GM	Gain margin			6		dB	
OUTPUT							
V _O	Voltage output swing	R _L = 100kΩ, From positive rail		30	75	mV	
			T _A = −40°C to 85°C	450			
		R _L = 100kΩ, From negative rail		19	80		
			T _A = −40°C to 85°C	112			
POWER SUPPLY							
I _Q	Quiescent current per amplifier	LM6142AI, LM6144AI		510	800	μA	
			T _A = −40°C to 85°C	880			
		LM6142BI, LM6144BI		510	800	μA	
			T _A = −40°C to 85°C	880			

5.8 Electrical Characteristics: $V_S = 24V$

For $V^+ = 24V$, $V^- = 0V$, $R_L > 1M\Omega$ connected to $V_S / 2$, $V_{CM} = V^+ / 2$, and $V_O = V^+ / 2$, at $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage	LM6142AI, LM6144AI		1.3	2	mV	
			T _A = −40°C to 85°C	4.8			
		LM6142BI, LM6144BI		1.3	3.8		
			T _A = −40°C to 85°C	4.8			
PSRR	Input offset voltage versus power supply	0V ≤ V _S ≤ 24V		87		dB	
INPUT BIAS CURRENT							
I _B	Input bias current			174		nA	
I _{OS}	Input offset current			5		nA	
INPUT VOLTAGE							
V _{CM}	Common-mode input voltage range			0	24	V	
CMRR	Common-mode rejection ratio	0V ≤ V _{CM} ≤ 23V		114		dB	
		0V ≤ V _{CM} ≤ 24V		100			
INPUT IMPEDANCE							
R _{IN}	Common-mode input resistance			288		MΩ	
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	R _L = 10kΩ		500		V/mV	
NOISE							
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	f = 50kHz		18		MHz	
OUTPUT							
V _O	Voltage output swing	R _L = 10kΩ, From positive rail		150	190	mV	
			T _A = −40°C to 85°C	380			
		R _L = 10kΩ, From negative rail		70	150		
			T _A = −40°C to 85°C	185			
POWER SUPPLY							
I _Q	Quiescent current per amplifier	LM6142AI, LM6144AI		750	1100	μA	
			T _A = −40°C to 85°C	1150			
		LM6142BI, LM6144BI		750	1100	μA	
			T _A = −40°C to 85°C	1150			

5.9 Typical Characteristics

at $T_A = 25^\circ\text{C}$ and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

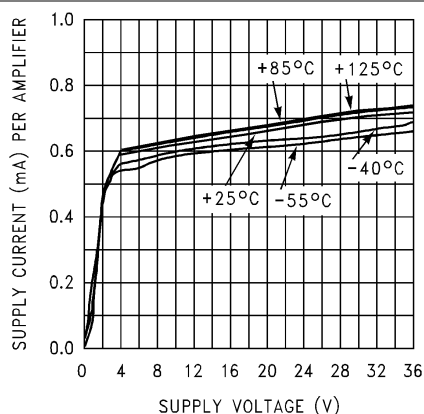


Figure 5-1. Supply Current vs Supply Voltage

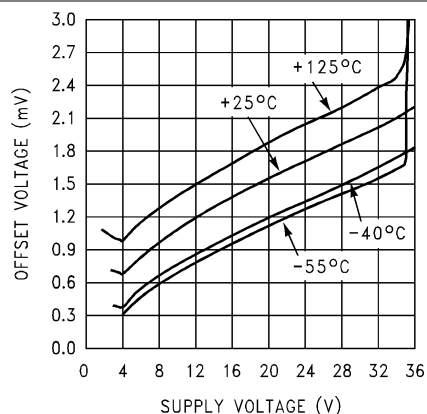


Figure 5-2. Offset Voltage vs Supply Voltage

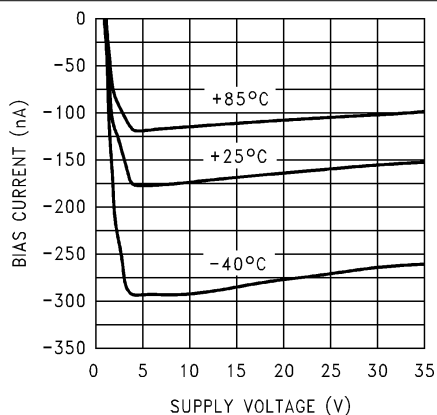


Figure 5-3. Bias Current vs Supply Voltage

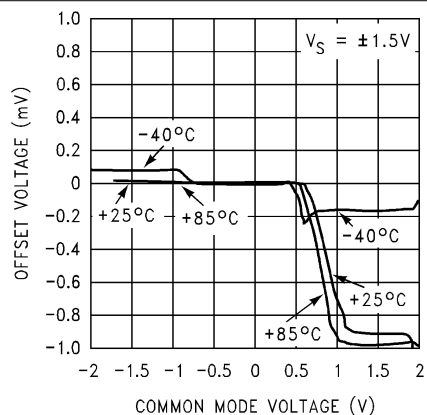


Figure 5-4. Offset Voltage vs V_{CM}

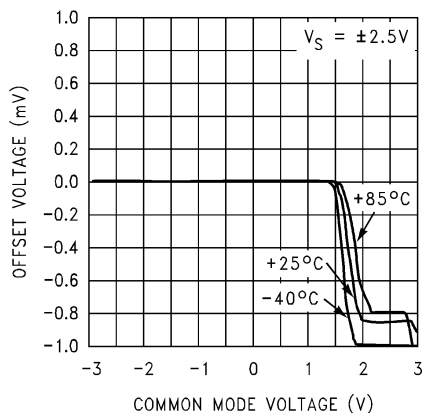


Figure 5-5. Offset Voltage vs V_{CM}

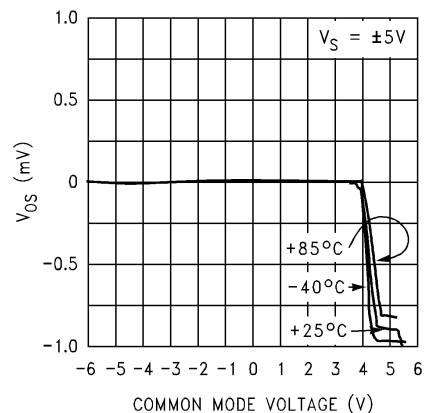


Figure 5-6. Offset Voltage vs V_{CM}

5.9 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$ and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

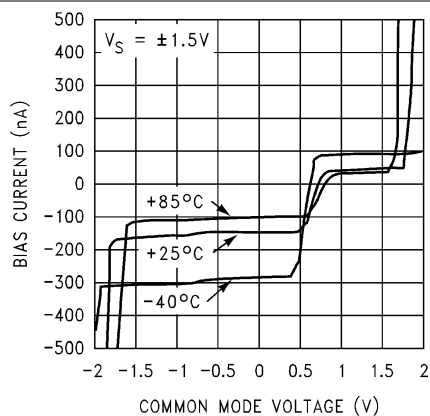


Figure 5-7. Bias Current vs V_{CM}

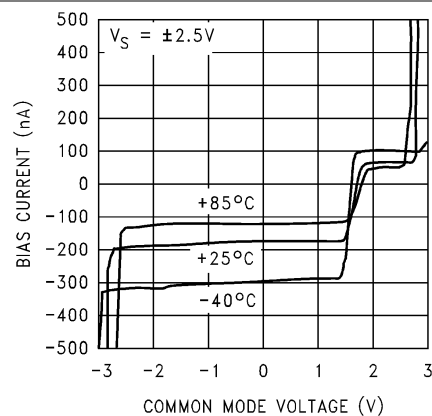


Figure 5-8. Bias Current vs V_{CM}

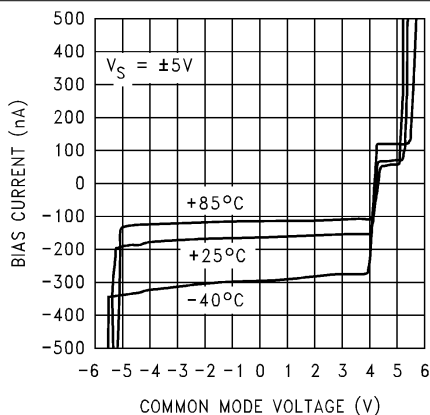


Figure 5-9. Bias Current vs V_{CM}

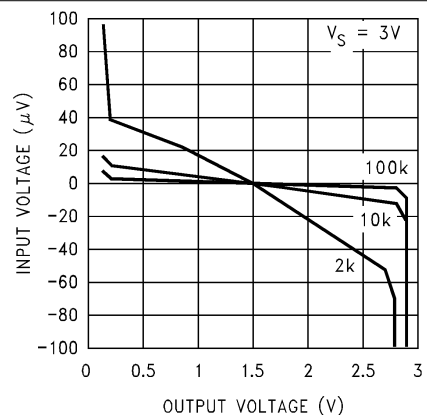


Figure 5-10. Open-Loop Transfer Function

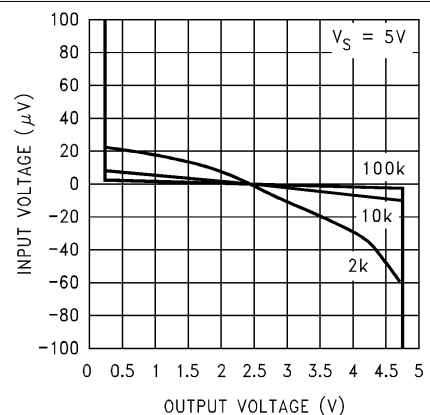


Figure 5-11. Open-Loop Transfer Function

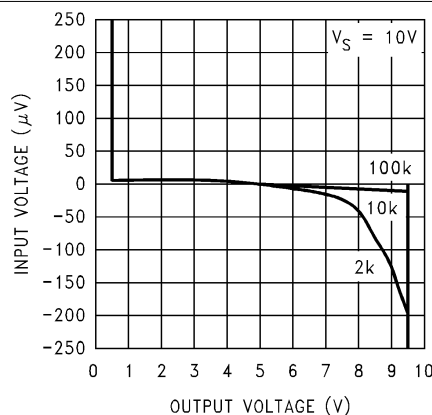


Figure 5-12. Open-Loop Transfer Function

5.9 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$ and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

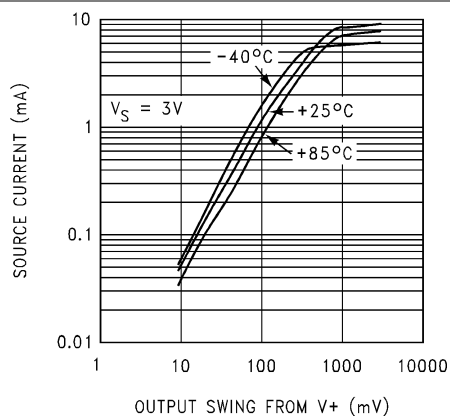


Figure 5-13. Output Voltage vs Source Current

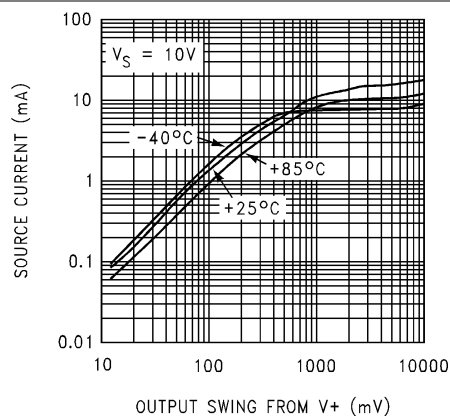


Figure 5-14. Output Voltage vs Source Current

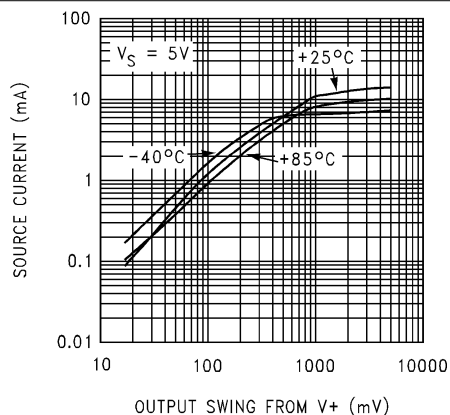


Figure 5-15. Output Voltage vs Source Current

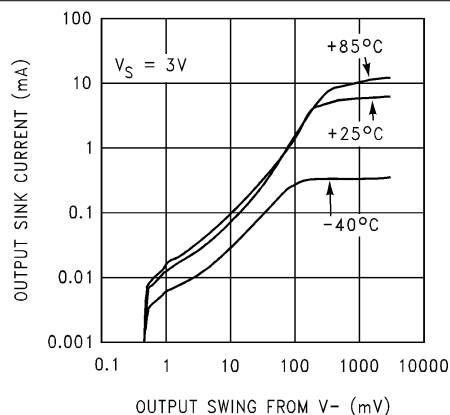


Figure 5-16. Output Voltage vs Sink Current

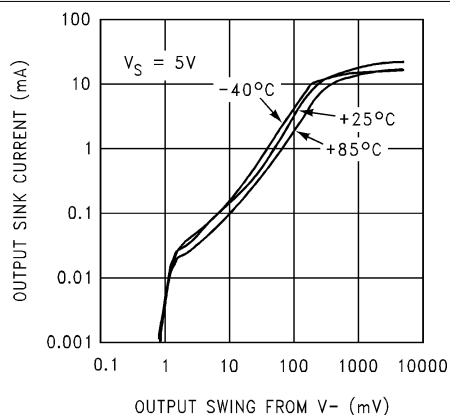


Figure 5-17. Output Voltage vs Sink Current

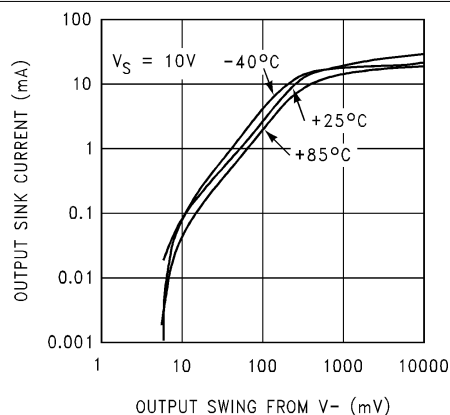


Figure 5-18. Output Voltage vs Sink Current

5.9 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$ and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

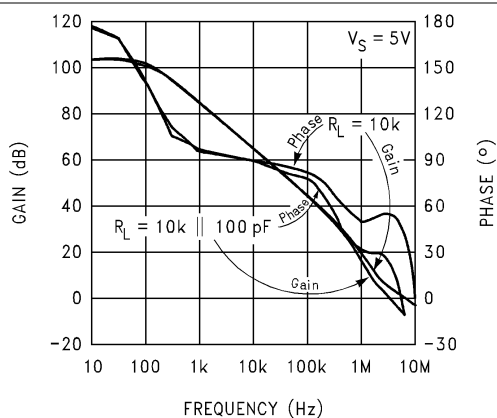


Figure 5-19. Gain and Phase vs Load

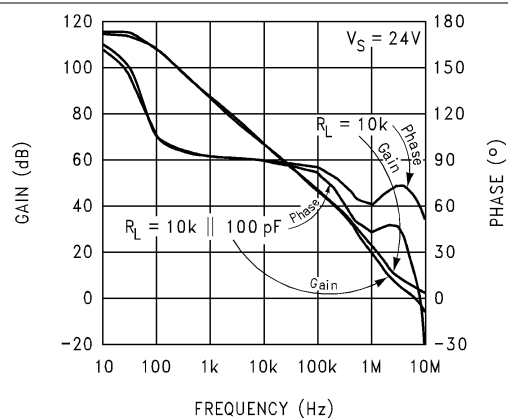


Figure 5-20. Gain and Phase vs Load

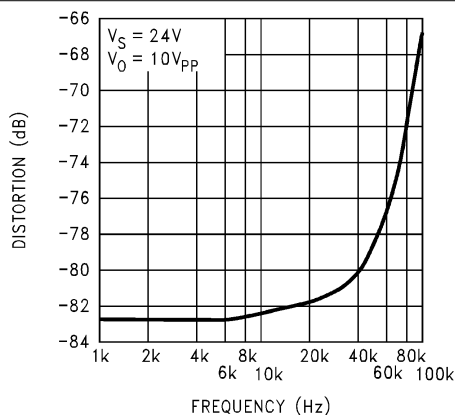


Figure 5-21. Distortion + Noise vs Frequency

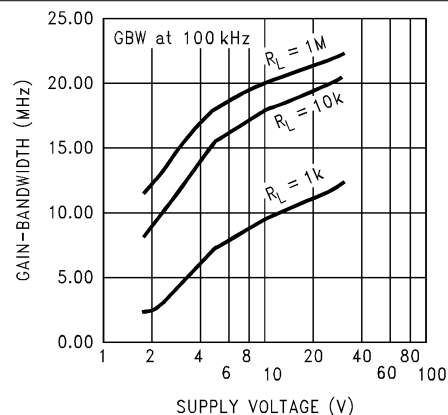


Figure 5-22. GBW vs Supply

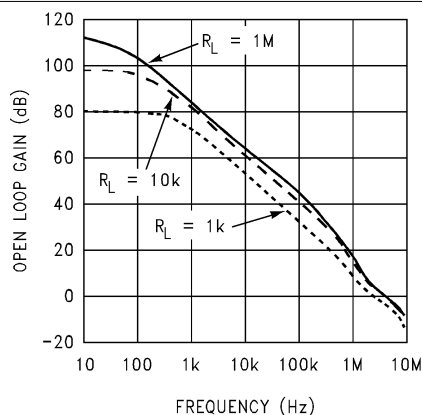


Figure 5-23. Open Loop Gain vs Load, 3V Supply, Old Die

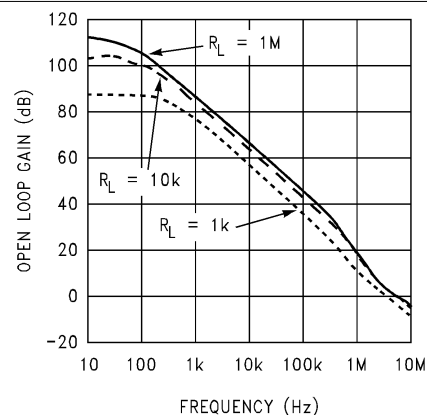


Figure 5-24. Open Loop Gain vs Load, 5V Supply, Old Die

5.9 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$ and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

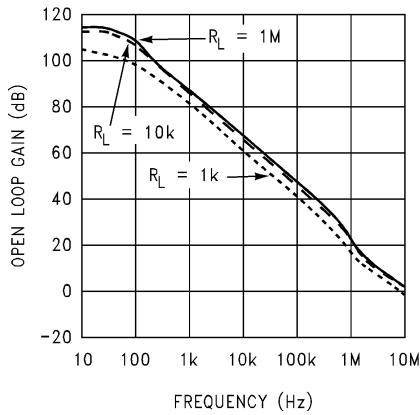


Figure 5-25. Open Loop Gain vs Load, 24V Supply, Old Die

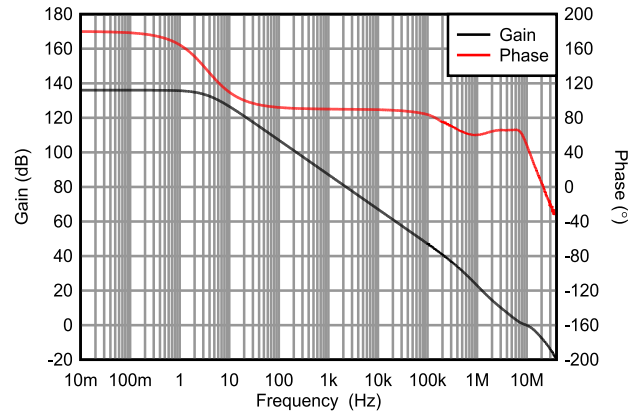


Figure 5-26. Open Loop Gain vs Load, 5V Supply, New Die

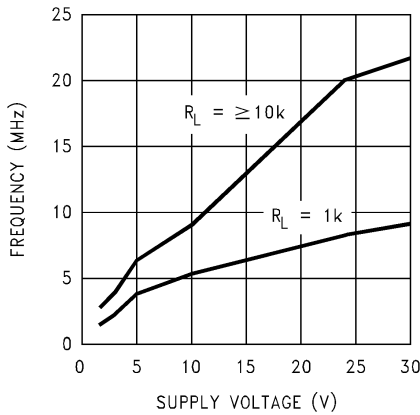


Figure 5-27. Unity Gain Frequency vs V_S

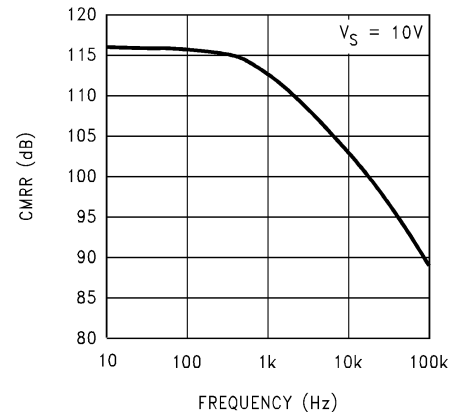


Figure 5-28. CMRR vs Frequency, Old Die

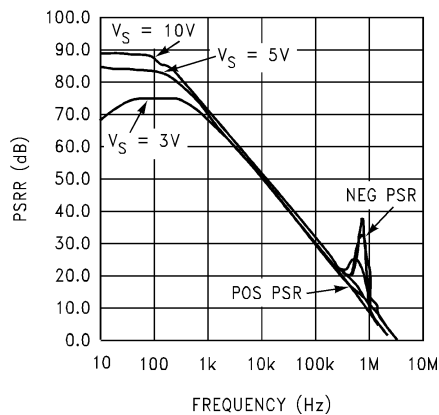


Figure 5-29. PSRR vs Frequency, Old Die

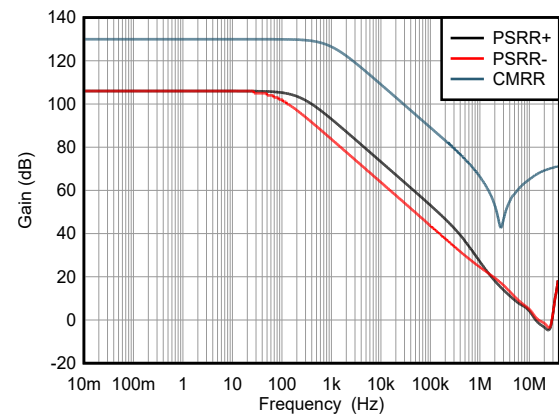


Figure 5-30. CMRR and PSRR vs Frequency, New Die

5.9 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$ and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

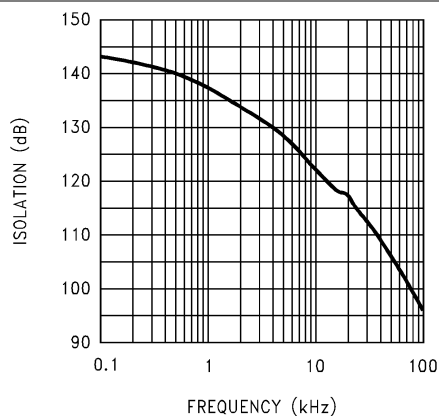


Figure 5-31. Crosstalk vs Frequency

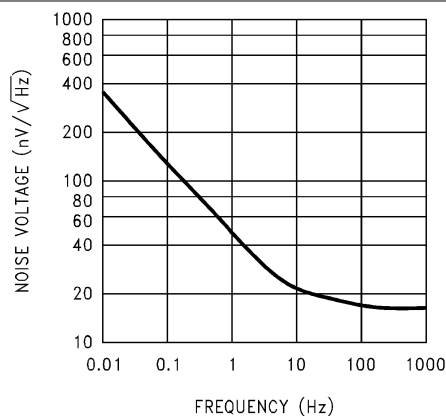


Figure 5-32. Noise Voltage vs Frequency

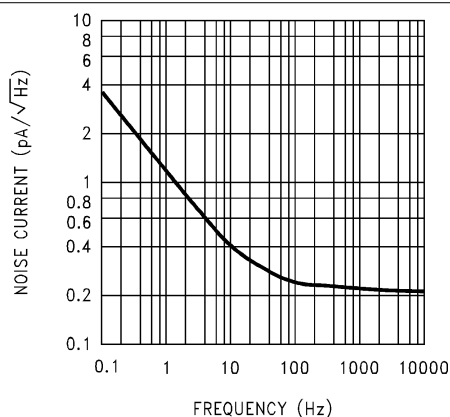


Figure 5-33. Noise Current vs Frequency

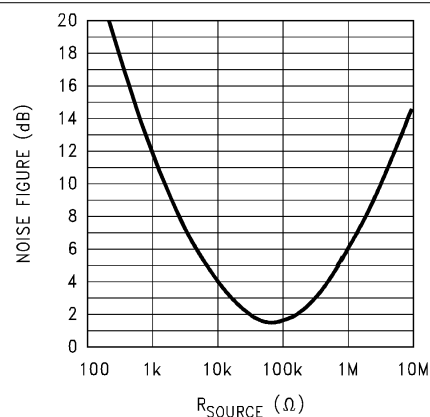


Figure 5-34. NF vs R_{SOURCE}

5.10 Old Versus New Die Comparison

As of the publication of revision F of this data sheet, Texas Instruments has moved manufacturing of the die for LM6142 and LM6144 to a modern fabrication site. The two different die are referred to in this document as “old” (previous fabrication site) and “new” die. The die origin can be separated from the “Chip Source Origin” (CSO) parameter in the shipping information. The old die CSO is “GF6”, for the new die CSO is “RFB”. The old die information is maintained in this data sheet for comparison purposes, but all new manufacturing has moved to the new die.

Table 5-1. Old Versus New Die Comparison

Description	Old Die	New Die
Absolute maximum supply voltage	35V	33V
Minimum supply voltage	1.8V	2.7V
Typical/Minimum output voltage range for 100k Ω load ($V_S = 5V$)	0.005V - 4.995V / 0.01V - 4.98V	0.045V - 4.97V / 0.05V - 4.96V
Typical output voltage range for 10k Ω load ($V_S = 5V$)	0.02V - 4.97V	0.05V - 4.96V
Output voltage slew architecture	Standard slew architecture	Slew-boosted architecture

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The LM6142 brings a new level of ease of use to op amp system design.

With greater than rail-to-rail input voltage range concern over exceeding the common-mode voltage range is eliminated.

Rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The high gain-bandwidth with low supply current opens new battery-powered applications, where high power consumption, previously reduced battery life to unacceptable levels.

To take advantage of these features, keep some ideas in mind.

6.2 Typical Applications

6.2.1 FISH FINDER/ DEPTH SOUNDER.

The LM6142/LM6144 is an excellent choice for battery operated fish finders. The low supply current, high gain-bandwidth and full rail to rail output swing of the LM6142 provides an ideal combination for use in this and similar applications.

6.2.2 ANALOG TO DIGITAL CONVERTER BUFFER

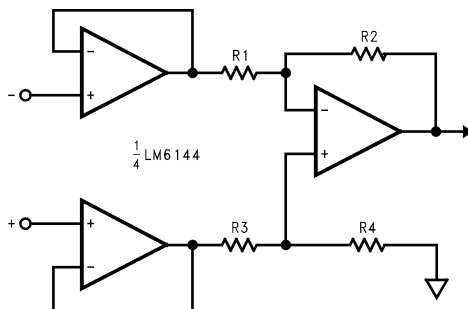
The high capacitive load driving ability, rail-to-rail input and output range with the excellent CMR of 82 dB, make the LM6142/LM6144 a good choice for buffering the inputs of A to D converters.

6.2.3 3 OP AMP INSTRUMENTATION AMP WITH RAIL-TO-RAIL INPUT AND OUTPUT

Using the LM6144, a 3 op amp instrumentation amplifier with rail-to-rail inputs and rail to rail output can be made. These features make these instrumentation amplifiers an excellent choice for single supply systems.

Some manufacturers use a precision voltage divider array of 5 resistors to divide the common-mode voltage to get an input range of rail-to-rail or greater. The problem with this method is that the method also divides the signal, so to even get unity gain, the amplifier must be run at high closed loop gains. This raises the noise and drift by the internal gain factor and lowers the input impedance. Any mismatch in these precision resistors reduces the CMR as well. Using the LM6144, all of these problems are eliminated.

In this example, amplifiers A and B act as buffers to the differential stage ([Figure 6-1](#)). These buffers maintain that the input impedance is over 100M Ω and the buffers eliminate the requirement for precision matched resistors in the input stage. The buffers also maintain that the difference amp is driven from a voltage source. This is necessary to maintain the CMR set by the matching of R1–R2 with R3–R4.

**Figure 6-1.**

The gain is set by the ratio of $R2/R1$ and $R3$ equals $R1$ and $R4$ equal $R2$. Making $R4$ slightly smaller than $R2$ and adding a trim pot equal to twice the difference between $R2$ and $R4$ allows the CMR to be adjusted for optimum.

With both rail to rail input and output ranges, the inputs and outputs are only limited by the supply voltages. Remember that even with rail-to-rail output, the output cannot swing past the supplies so the combined common mode voltage plus the signal must not be greater than the supplies or limiting occurs.

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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All trademarks are the property of their respective owners.

7.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.4 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E (May 2026)	Page
• Deleted "Swing 0.005V to 4.995V" in <i>Features</i>	1
• Deleted "Small Signal, 5V/μs" in <i>Features</i>	1
• Deleted "Large Signal, 30V/μs" in <i>Features</i>	1
• Changed Slew Rate to Slew Rate: 30V/μs in <i>Features</i>	1
• Changed supply range from 1.8V to 2.7V in <i>Features</i>	1
• Changed from "Operating on supplies of 1.8V" to "Operating on supplies of 2.7V"	1
• Updated table note 1 of <i>Absolute Maximum Ratings</i>	5
• Changed absolute maximum rating for supply voltage from 35V to 33V	5
• Deleted absolute maximum rating for current at power supply pin	5
• Updated table note 3 of <i>Absolute Maximum Ratings</i>	5
• Changed absolute maximum rating for input (common-mode) voltage from (V±) ± 0.3V to (V±) ± 0.5V	5
• Updated table note 4 of <i>Absolute Maximum Ratings</i>	5
• Changed absolute maximum rating for differential input voltage from 15V to ±15V	5
• Updated table note 2 of <i>Absolute Maximum Ratings</i>	5
• Changed absolute maximum rating for output current from ±25mA to Continuous	5
• Added absolute maximum rating for operating ambient temperature	5
• Deleted absolute maximum rating for lead temperature	5
• Added <i>ESD Ratings</i> table	5
• Changed HBM ESD rating from 2500V to ±4000V	5
• Changed minimum operating voltage from 1.8V to 2.7V	5
• Deleted table note 1 on Operating Ratings	5
• Added <i>Thermal Information</i> table for LM6142	6
• Changed junction-to-ambient thermal resistance for LM6142D from 193°C/w to 127.1°C/W	6
• Changed junction-to-ambient thermal resistance for LM6142P from 115°C/w to 84.45°C/W	6
• Added junction-to-case thermal resistance for LM6142	6
• Added junction-to-board thermal resistance for LM6142	6
• Added junction-to-top characterization parameter for LM6142	6
• Added junction-to-board characterization parameter for LM6142	6
• Added <i>Thermal Information</i> table for LM6144	6
• Changed junction-to-ambient thermal resistance for LM6144D from 126°C/W to 82.48°C/W	6
• Added junction-to-case (top) thermal resistance for LM6144	6
• Added junction-to-board thermal resistance for LM6144	6
• Added junction-to-top characterization parameter for LM6144	6
• Added junction-to-board characterization parameter for LM6144	6
• Updated all <i>Electrical Characteristics</i> tables to latest format	7
• Updated Output Swing format to refer to rails	7
• Changed typical voltage output swing for 100kΩ load from 4.995V to 30mV from positive rail	7
• Changed maximum voltage output swing for 100kΩ load from 4.98V to 40mV from positive rail	7
• Changed typical voltage output swing for 100kΩ load from 0.005V to 45mV from negative rail	7
• Changed maximum voltage output swing for 100kΩ load from 0.01V to 50mV from negative rail	7
• Changed maximum voltage output swing for 100kΩ load over temp range from 0.013V to 60mV from negative rail	7
• Changed typical voltage output swing for 10kΩ load from 4.97V to 40mV from positive rail	7
• Changed typical voltage output swing for 10kΩ load from 0.02V to 50mV from negative rail	7
• Deleted table notes for <i>Electrical Characteristics</i> tables	7
• Updated Output Swing format to refer to rails	9
• Changed maximum voltage output swing for 100kΩ load from 2.66V to 75mV from positive rail	9
• Updated Output Swing format to refer to rails	10

• Added Open Loop Gain vs Load, for New Die.....	11
• Added CMRR and PSRR vs Frequency, for New Die.....	11
• Added a new sub-section <i>Old Versus New Die Comparison</i>	16
• Deleted sub-section <i>Enhanced Slew Rate</i>	17

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM6142AIMX/NOPB	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM614 2AIM
LM6142AIMX/NOPB.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM614 2AIM
LM6142AIMX/NOPB.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM614 2AIM
LM6142BIM/NOPB	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	LM614 2BIM
LM6142BIMX/NOPB	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM614 2BIM
LM6142BIMX/NOPB.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM614 2BIM
LM6142BIMX/NOPB.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM614 2BIM
LM6142BIN/NOPB	Active	Production	PDIP (P) 8	40 TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM6142 BIN
LM6142BIN/NOPB.A	Active	Production	PDIP (P) 8	40 TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM6142 BIN
LM6142BIN/NOPB.B	Active	Production	PDIP (P) 8	40 TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM6142 BIN
LM6144AIM/NOPB	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 85	LM6144 AIM
LM6144AIMX/NOPB	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM6144 AIM
LM6144AIMX/NOPB.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM6144 AIM
LM6144BIM/NOPB	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 85	LM6144 BIM
LM6144BIMX/NOPB	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM6144 BIM
LM6144BIMX/NOPB.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM6144 BIM
LM6144BIN/NOPB	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM6144BIN

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM6144BIN/NOPB.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM6144BIN

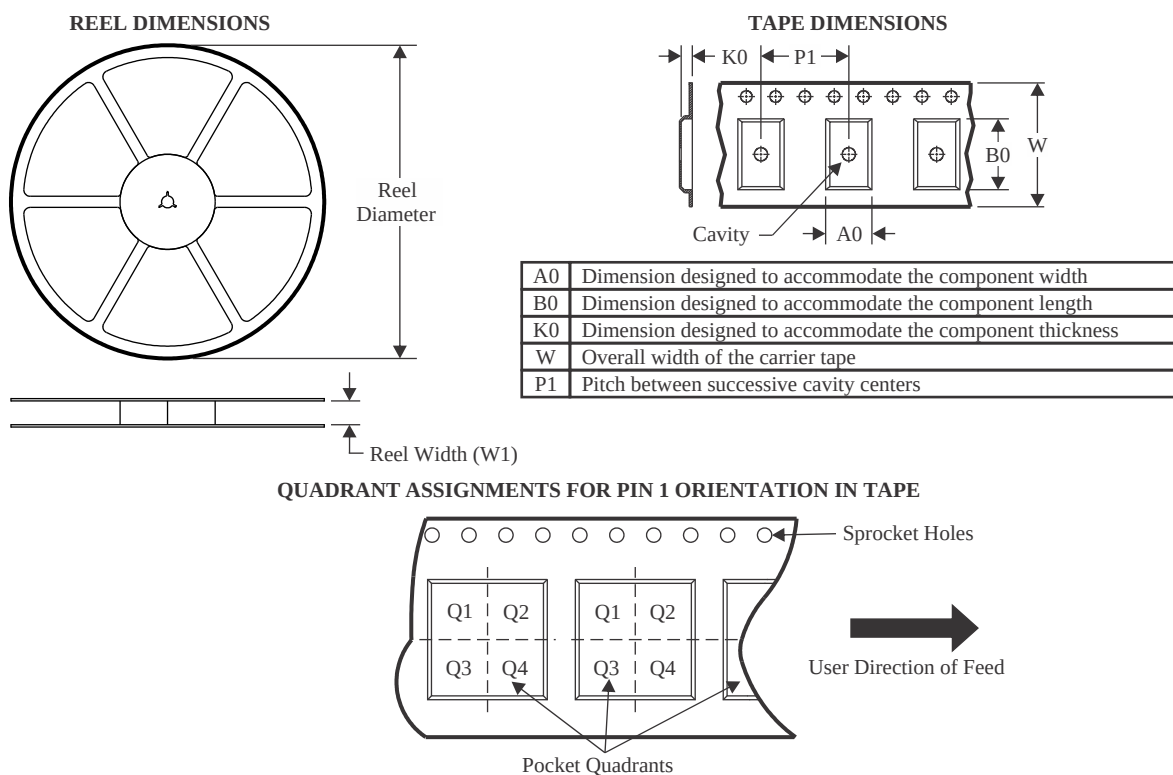
- ⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).
- ⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- ⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- ⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- ⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- ⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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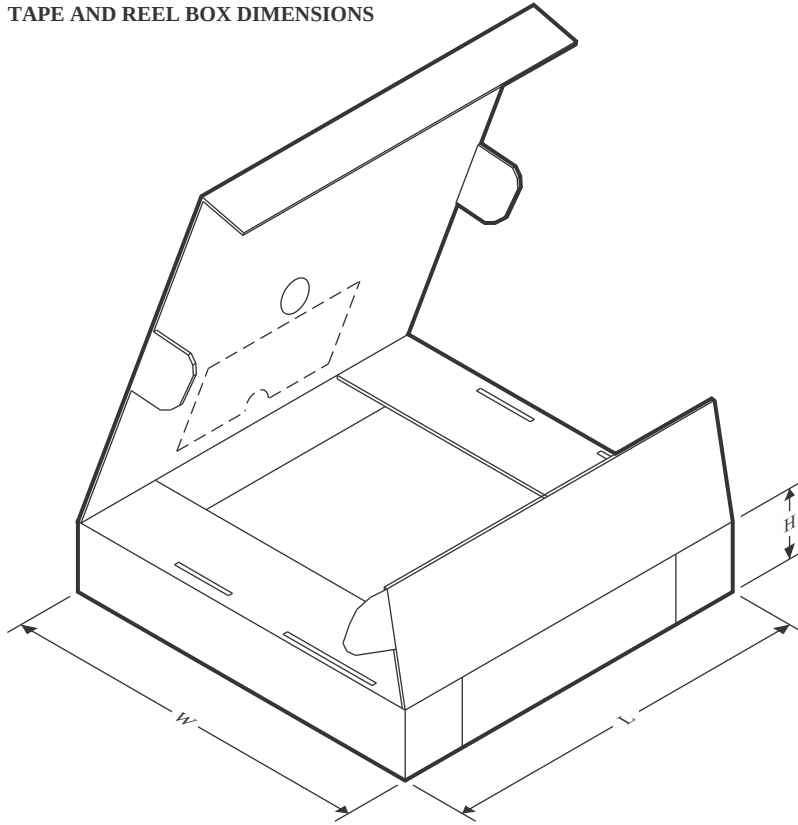
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM6142AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6142BIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6144AIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM6144BIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

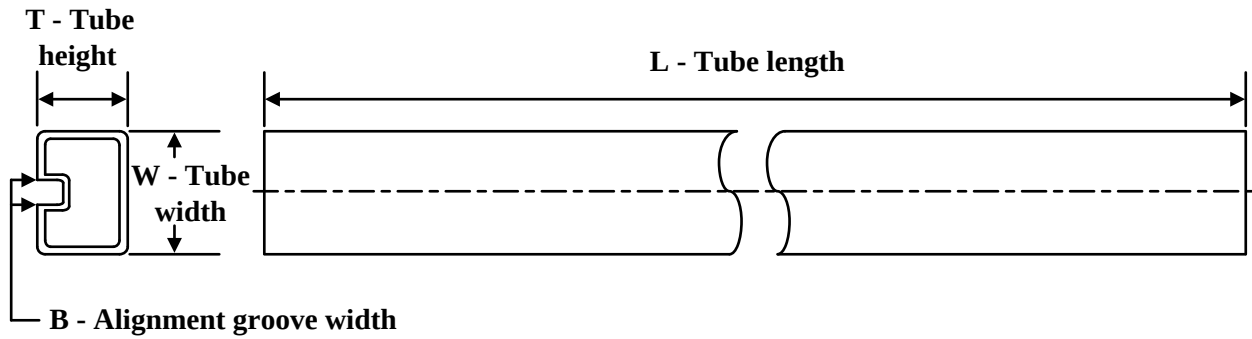
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

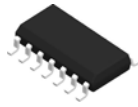
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM6142AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM6142BIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM6144AIMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LM6144BIMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

TUBE

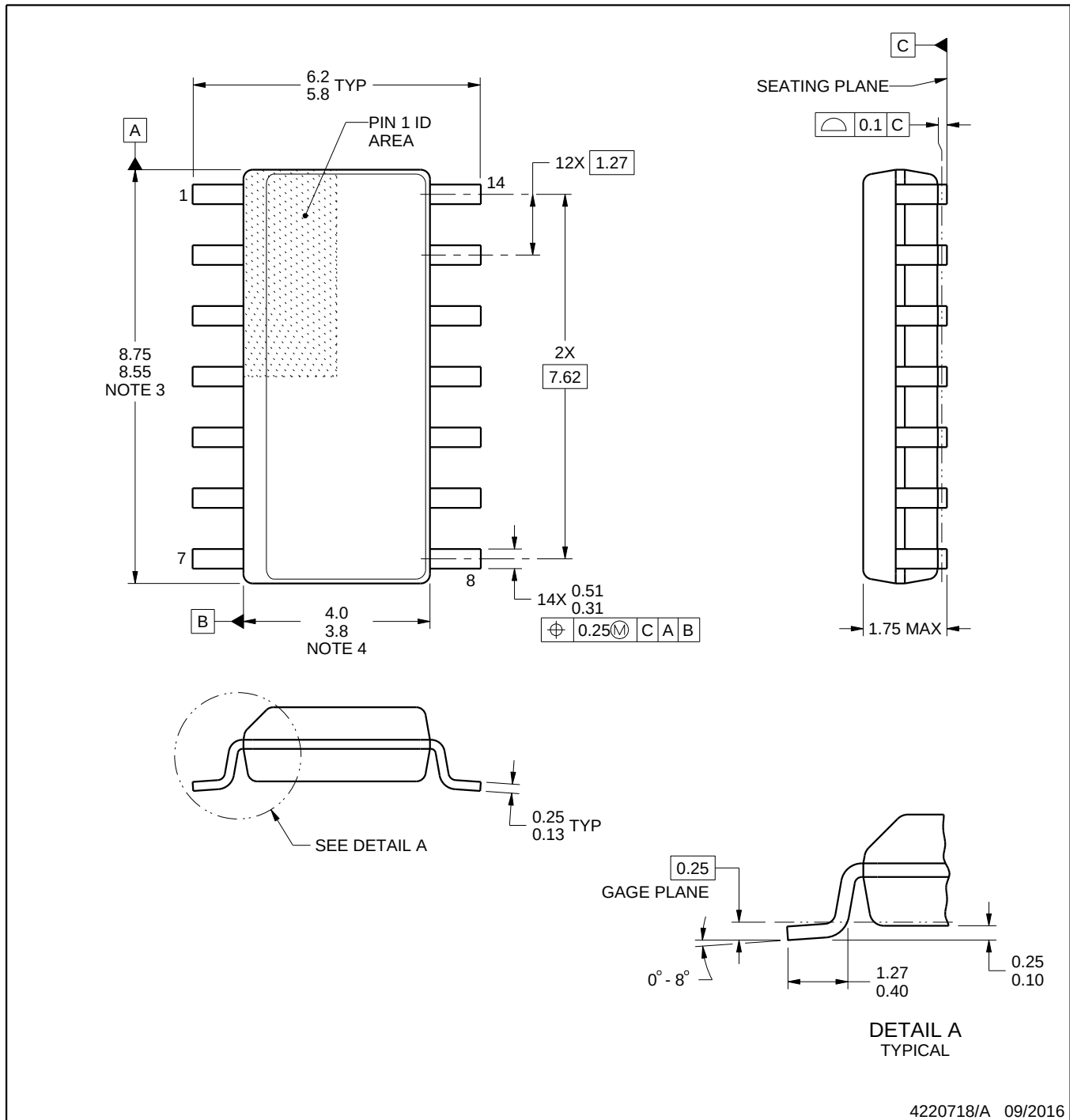


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LM6142BIN/NOPB	P	PDIP	8	40	502	14	11938	4.32
LM6142BIN/NOPB.A	P	PDIP	8	40	502	14	11938	4.32
LM6142BIN/NOPB.B	P	PDIP	8	40	502	14	11938	4.32
LM6144BIN/NOPB	N	PDIP	14	25	502	14	11938	4.32
LM6144BIN/NOPB.A	N	PDIP	14	25	502	14	11938	4.32

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

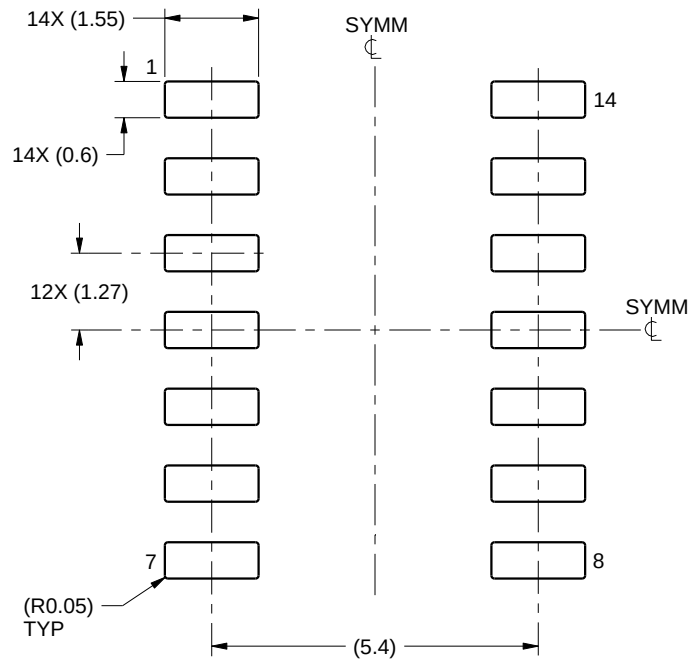
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

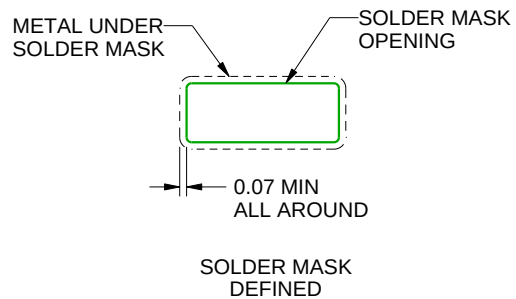
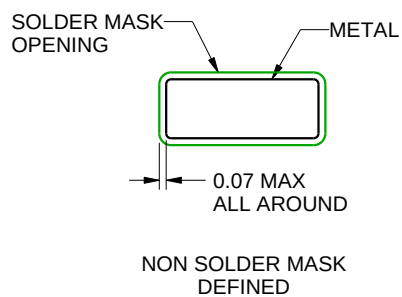
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

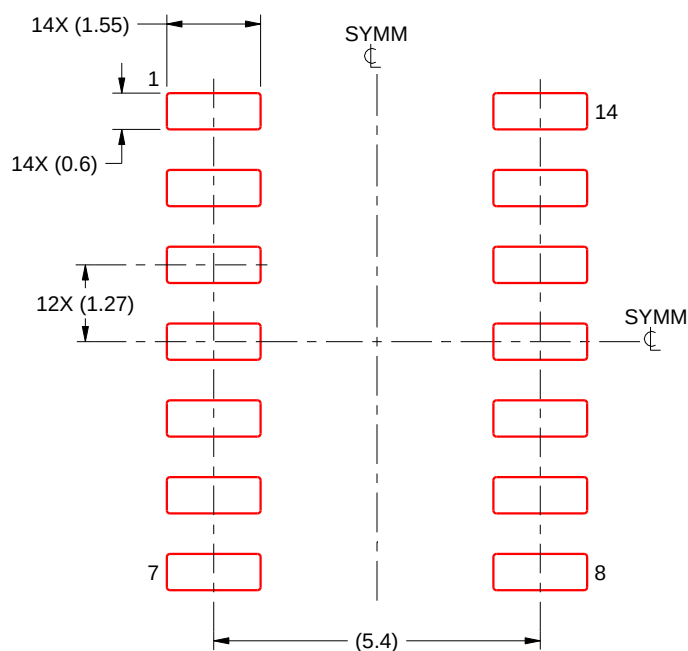
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

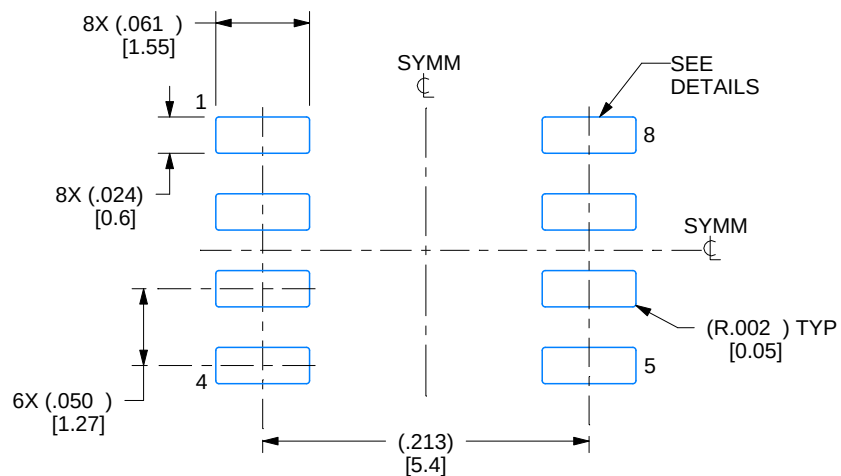


1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

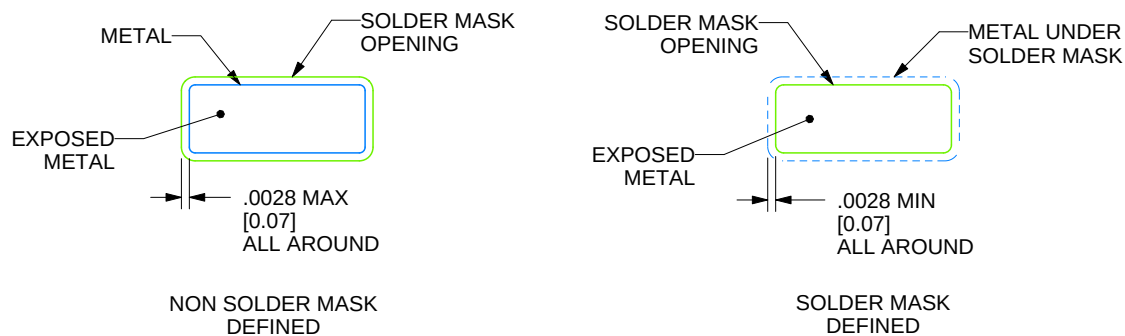
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

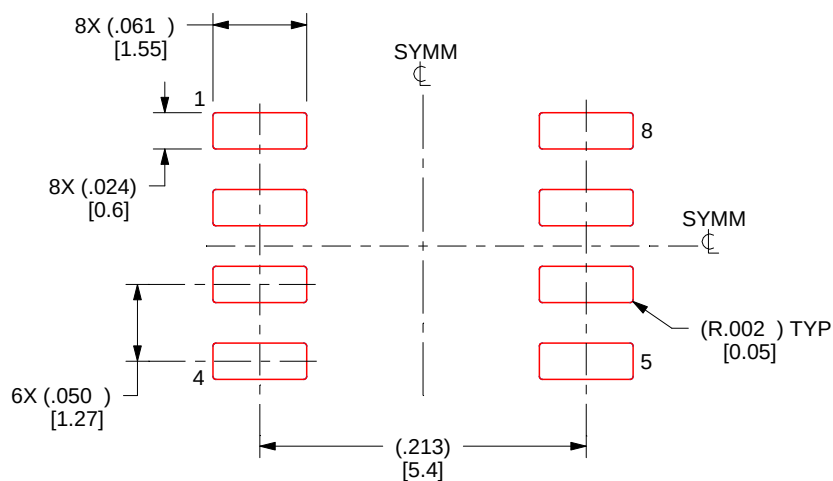
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

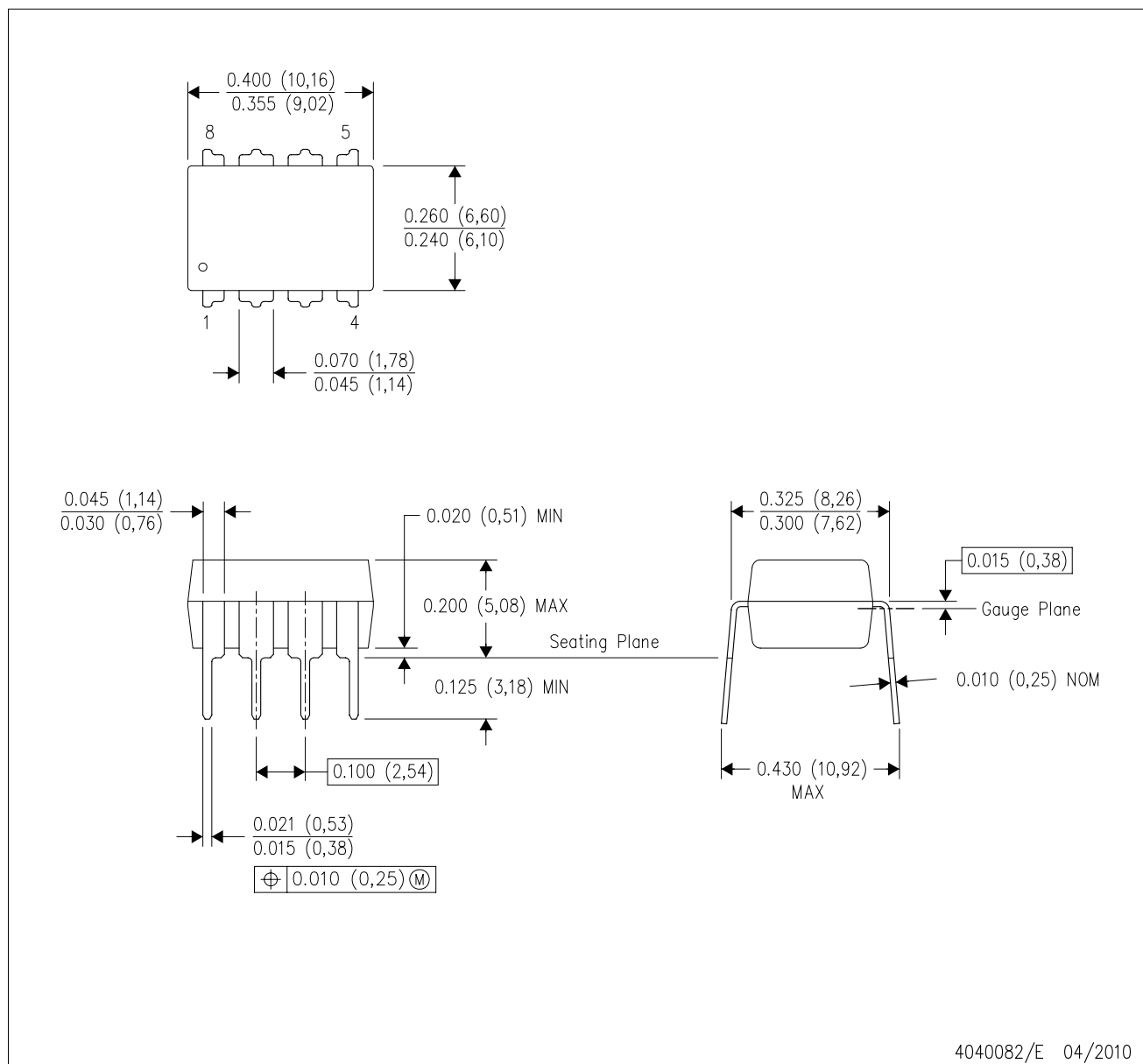
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

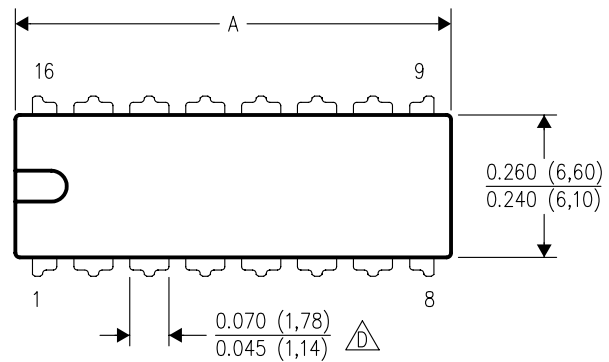


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

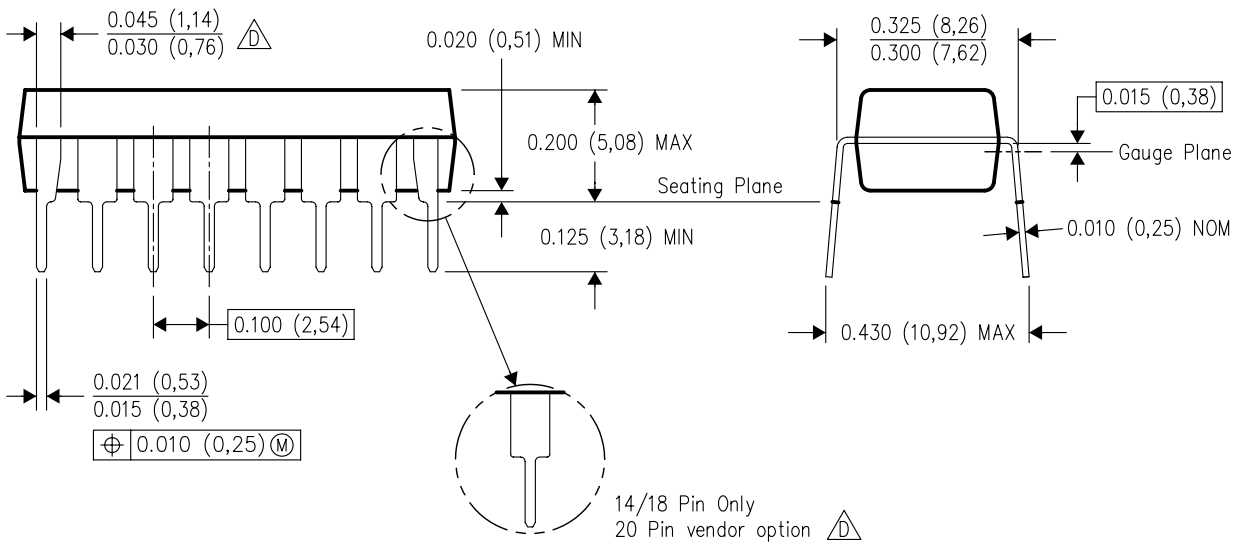
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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