LM6172 Dual, High-Speed, Low-Power, Low-Distortion, Voltage-Feedback Amplifier

1 Features

- Typical values unless otherwise noted
- Easy-to-use voltage-feedback topology
- High slew rate: 3000V/µs
- Wide unity-gain bandwidth: 100MHz
- Low supply current: 2.3mA/channel
- High output current: 50mA/channel
- Specified operation: ±15V and ±5V

2 Applications

- Scanner I-to-V converters
- ADSL/HDSL drivers
- Multimedia broadcast systems
- Video amplifiers
- NTSC, PAL and SECAM systems
- ADC/DAC buffers
- Pulse amplifiers and peak detectors

3 Description

The LM6172 is a dual, high-speed voltage-feedback amplifier. The device is unity-gain stable and provides excellent dc and ac performance. With a 100MHz unity-gain bandwidth, 3000V/µs slew rate, and 50mA of output current per channel, the LM6172 offers high performance in dual amplifiers, yet only consumes 2.3mA of supply current per channel.

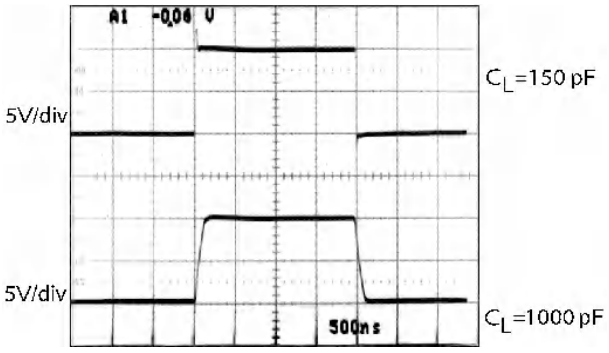
The LM6172 operates on ±15V power supplies for systems requiring large voltage swings, such as ADSL, scanners and ultrasound equipment. The device is also specified for ±5-V power supplies for low-voltage applications, such as portable video systems.

The LM6172 is built with TI's advanced complementary bipolar process. See the LM6171 data sheet for a single amplifier with these same features.

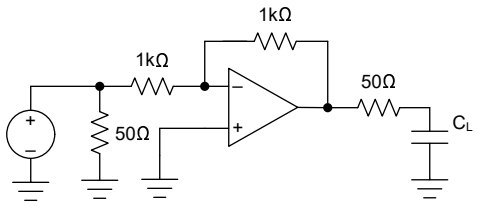
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LM6172	D (SOIC, 8)	4.9mm × 6mm
	P (PDIP, 8)	9.81mm × 9.43mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



LM6172 Driving a Capacitive Load



LM6172 Driving Capacitive Load

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4 Pin Configuration and Functions

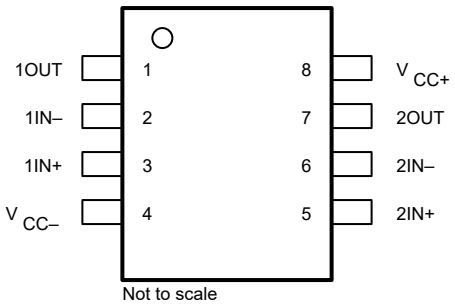


Figure 4-1. D Package, 8-Pin SOIC and P Package, 8-Pin PDIP (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN–	2	Input	Channel 1 inverting input
1IN+	3	Input	Channel 1 noninverting input
1OUT	1	Output	Channel 1 output
2IN–	6	Input	Channel 2 inverting input
2IN+	5	Input	Channel 2 noninverting input
2OUT	7	Output	Channel 2 output
$V_{CC–}$	4	—	Negative power supply
V_{CC+}	8	—	Positive power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_S	Supply voltage (V_{CC+} – $V_{CC–}$)		36	V
V_I	Differential input voltage		±10	V
V_{CM}	Common-mode voltage	$V_{CC–}$ – 0.3	V_{CC+} + 0.3	V
I_{IN}	Input current		±10	mA
I_{SC}	Output current short to ground(3)		Continuous	A
T_J	Junction temperature(4)		150	°C
T_{stg}	Storage temperature	–65	150	°C
T_{SOLDER}	Infrared or convection reflow (20 seconds)		235	°C
	Wave soldering lead temp (10 seconds)		260	

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(2) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(3) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly into a PC board.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Machine model(2)	±300	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) Machine model, 200Ω in series with 100pF.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_S	Supply voltage	5.5		36	
T_A	Ambient temperature	−40		85	°C

5.4 Thermal Information

THERMAL METRIC(1)		LM6172		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	172	108	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.4	52.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.7	51.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.5	6.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	55.1	51.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics ±15V

at T_J = 25°C, V_{CC+} = 15V, $V_{CC–}$ = −15V, V_{CM} = 0V, and R_L = 1kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN[2]	TYP[1]	MAX[2]	UNIT
V_{OS}	Input offset voltage				0.4	3	mV
		T_A = –40°C to +85°C				4	
TCV_{OS}	Input offset voltage average drift				6		µV/°C
I_B	Input bias current				1.2	3	µA
		T_A = –40°C to +85°C				4	
I_{OS}	Input offset current				0.02	2	µA
		T_A = –40°C to +85°C				3	
R_{IN}	Input resistance	Common-mode			40		MΩ
		Differential-mode			4.9		
R_O	Open-loop output resistance				14		Ω
CMRR	Common-mode rejection ratio	V_{CM} = ±10V		70	110		dB
			T_A = –40°C to +85°C	65			
PSRR	Power supply rejection ratio	V_S = ±15V to ±5V		75	95		dB
			T_A = –40°C to +85°C	70			
V_{CM}	Input common-mode voltage	CMRR > 60dB			±13.5		V
A_V	Large-signal voltage gain[3]	R_L = 1kΩ, V_{OUT} = ±5V		80	86		dB
			T_A = –40°C to +85°C	75			
		R_L = 100Ω, V_{OUT} = ±5V		65	78		
			T_A = –40°C to +85°C	60			
V_O	Output swing	R_L = 1kΩ, sourcing		12.5	13.2		V
			T_A = –40°C to +85°C	12			
		R_L = 1kΩ, sinking			−13.1	−12.5	
			T_A = –40°C to +85°C			−12	
		R_L = 100Ω, sourcing		6	9		
			T_A = –40°C to +85°C	5			
		R_L = 100Ω, sinking			−8.5	−6	
			T_A = –40°C to +85°C			−5	
	Continuous output current (open loop)[4]	Sourcing, R_L = 100Ω		60	90		mA
			T_A = –40°C to +85°C	50			
		Sinking, R_L = 100Ω			−85	−60	
			T_A = –40°C to +85°C			−50	
I_{SC}	Output short-circuit current	D package	Sourcing		173		mA
			Sinking		−183		
		P package	Sourcing		107		
			Sinking		−105		
I_S	Supply current				4.6	8	mA
		T_A = –40°C to +85°C				9	
SR	Slew rate[5]	A_V = +2, V_{IN} = 13V_{PP}			3000		V/µs
		A_V = +2, V_{IN} = 10V_{PP}			2500		
	Unity-gain bandwidth	D package			80		MHz
		P package			100		
	−3dB frequency	A_V = +1			160		MHz
		A_V = +2			62		MHz
φ_m	Phase margin				40		Deg

5.5 Electrical Characteristics ±15V (continued)

at T_J = 25°C, V_{CC+} = 15V, $V_{CC–}$ = −15V, V_{CM} = 0V, and R_L = 1kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(1)	MAX(2)	UNIT
	Bandwidth matching between channels				2		MHz
t_s	Settling time (0.1%)	A_V = −1, V_{OUT} = ±5V, R_L = 500Ω			65		ns
A_D	Differential gain(6)				0.28		%
φ_D	Differential phase(6)				0.6		°
e_n	Input-referred voltage noise	f = 10kHz			12		nV/√Hz
i_n	Input-referred current noise	f = 10kHz			1		pA/√Hz
HD2	Second harmonic distortion	D package	f_{IN} = 10kHz		−88		dBc
			f_{IN} = 5MHz		−50		
		P package	f_{IN} = 10kHz		−110		
			f_{IN} = 5MHz		−50		
HD3	Third harmonic distortion	D package	f_{IN} = 10kHz		−93		dBc
			f_{IN} = 5MHz		−41		
		P package	f_{IN} = 10kHz		−105		
			f_{IN} = 5MHz		−50		

(1) Typical values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Large-signal voltage gain is the total output swing divided by the input signal required to produce that swing. For V_S = ±15V, V_{OUT} = ±5V. For V_S = 5V, V_{OUT} = ±1V.
(4) The open-loop output current is the output swing with the 100Ω load resistor divided by that resistor.
(5) Slew rate is the average of the rising and falling slew rates.
(6) Differential gain and phase are measured with A_V = +2, V_{IN} = $1V_{PP}$ at 3.58MHz and both input and output 75Ω terminated.

5.6 Electrical Characteristics ±5V

at T_J = 25°C, V_{CC+} = 5V, $V_{CC–}$ = −5V, V_{CM} = 0V, and R_L = 1kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN[2]	TYP[1]	MAX[2]	UNIT
V_{OS}	Input offset voltage				0.1	3	mV
		T_A = –40°C to +85°C				4	
TCV_{OS}	Input offset voltage average drift				4		µV/°C
I_B	Input bias current				1.4	2.5	µA
		T_A = –40°C to +85°C				3.5	
I_{OS}	Input offset current				0.02	1.5	µA
		T_A = –40°C to +85°C				2.2	
R_{IN}	Input resistance	Common-mode			40		MΩ
		Differential-mode			4.9		
R_O	Open loop output resistance				14		Ω
CMRR	Common-mode rejection ratio	V_{CM} = ±2.5V		70	105		dB
			T_A = –40°C to +85°C	65			
PSRR	Power supply rejection ratio	V_S = ±15V to ±5V		75	95		dB
			T_A = –40°C to +85°C	70			
V_{CM}	Input common-mode voltage	CMRR > 60dB			±3.7		V
A_V	Large-signal voltage gain[3]	R_L = 1 kΩ, V_{OUT} = ±1V		70	82		dB
			T_A = –40°C to +85°C	65			
		R_L = 100Ω, V_{OUT} = ±1V		65	78		
			T_A = –40°C to +85°C	60			
V_O	Output swing	R_L = 1kΩ, sourcing		3.1	3.4		V
			T_A = –40°C to +85°C	3			
		R_L = 1kΩ, sinking			−3.3	−3.1	
			T_A = –40°C to +85°C			−3	
		R_L = 100Ω, sourcing		2.5	2.9		
			T_A = –40°C to +85°C	2.4			
		R_L = 100Ω, sinking			−2.7	−2.4	
			T_A = –40°C to +85°C			−2.3	
	Continuous output current (open loop)[4]	Sourcing, R_L = 100Ω		25	29		mA
			T_A = –40°C to +85°C	24			
		Sinking, R_L = 100Ω			−27	−24	
			T_A = –40°C to +85°C			−23	
I_{SC}	Output short-circuit current	D package	Sourcing		155		mA
			Sinking		−158		
		P package	Sourcing		93		
			Sinking		−72		
I_S	Supply current				4.4	6	mA
		TA = –40°C to +85°C				7	
SR	Slew rate[5]	A_V = +2, V_{IN} = 3.5V_{PP}			750		V/µs
	Unity-gain bandwidth				70		MHz
	−3dB frequency	A_V = +1			130		MHz
		A_V = +2	D package		75		
			P package		45		
φ_m	Phase margin	D Package			41		Deg
		P package			57		

5.6 Electrical Characteristics ±5V (continued)

at T_J = 25°C, V_{CC+} = 5V, $V_{CC–}$ = −5V, V_{CM} = 0V, and R_L = 1kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(1)	MAX(2)	UNIT
t_s	Settling time (0.1%)	A_V = −1, V_{OUT} = ±1V, R_L = 500Ω			72		ns
A_D	Differential gain(6)				0.4		%
φ_D	Differential phase(6)				0.7		°
e_n	Input-referred voltage noise	f = 10kHz			11		nV/√Hz
i_n	Input-referred current noise	f = 10kHz			1		pA/√Hz
HD2	Second harmonic distortion	D package	f_{IN} = 10kHz		−89		dBc
			f_{IN} = 5MHz		−48		
		P package	f_{IN} = 10kHz		−110		
			f_{IN} = 5MHz		−48		
HD3	Third harmonic distortion	D package	f_{IN} = 10kHz		−93		dBc
			f_{IN} = 5MHz		−42		
		P package	f_{IN} = 10kHz		−105		
			f_{IN} = 5MHz		−50		

(1) Typical values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Large-signal voltage gain is the total output swing divided by the input signal required to produce that swing. For V_S = ±15V, V_{OUT} = ±5V. For V_S = 5V, V_{OUT} = ±1V.
(4) The open-loop output current is the output swing with the 100Ω load resistor divided by that resistor.
(5) Slew rate is the average of the rising and falling slew rates.
(6) Differential gain and phase are measured with A_V = +2, V_{IN} = 1V_{PP} at 3.58MHz and both input and output 75Ω terminated.

5.7 Typical Characteristics: D (SOIC, 8) Package

at T_A = 25°C (unless otherwise noted)

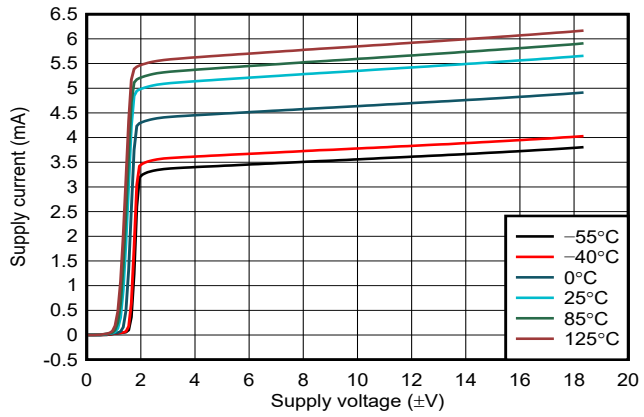


Figure 5-1. Supply Voltage vs Supply Current

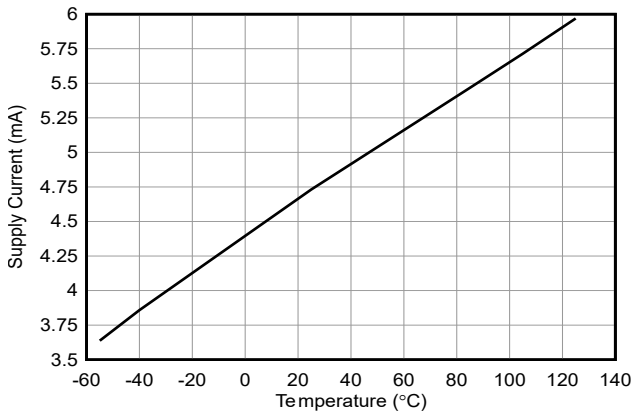


Figure 5-2. Supply Current vs Temperature

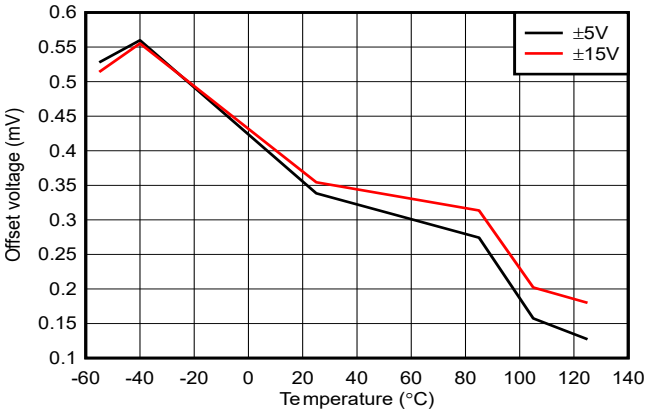


Figure 5-3. Input Offset Voltage vs Temperature

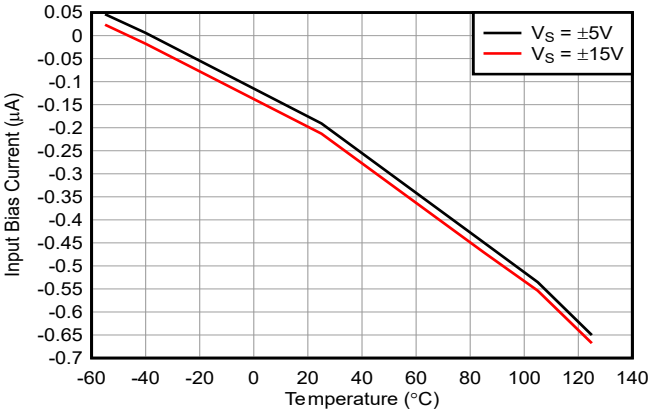


Figure 5-4. Input Bias Current vs Temperature

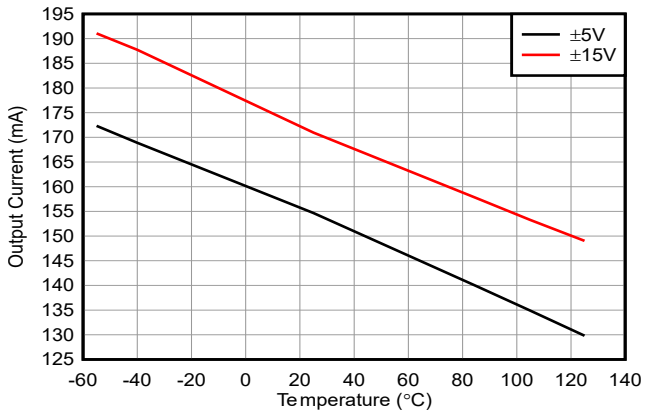


Figure 5-5. Short Circuit Current vs Temperature (Sourcing)

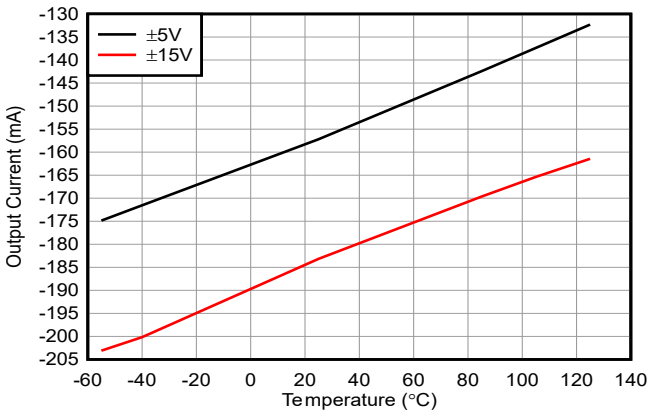
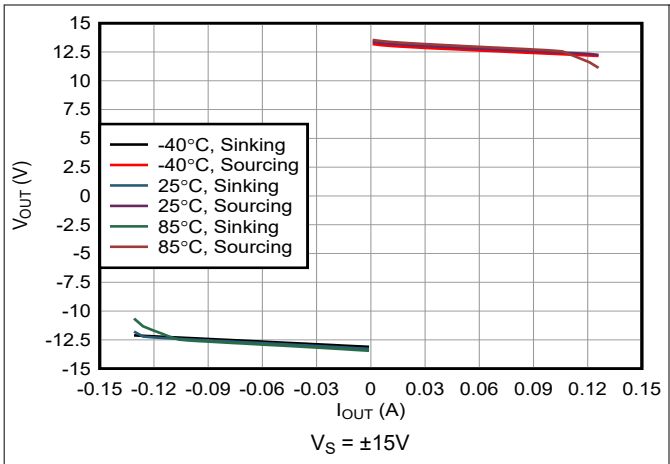


Figure 5-6. Short Circuit Current vs Temperature (Sinking)

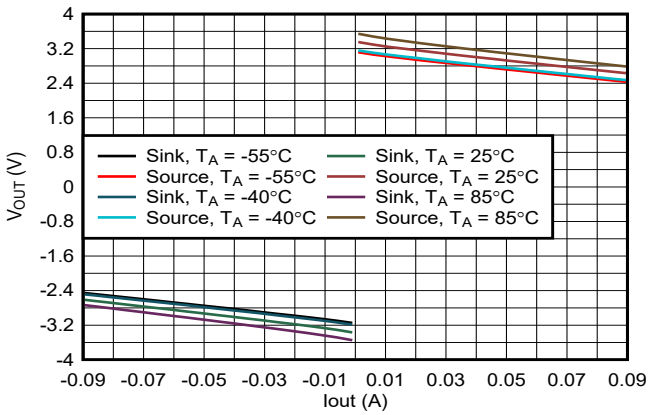
5.7 Typical Characteristics: D (SOIC, 8) Package (continued)

at T_A = 25°C (unless otherwise noted)



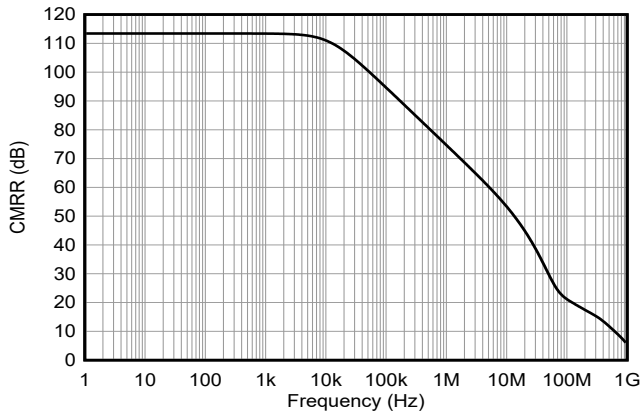
V_S = ±15V

Figure 5-7. Output Voltage vs Output Current



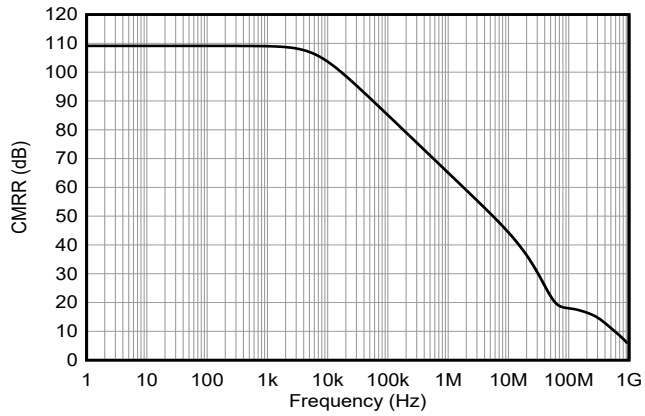
V_S = ±5V

Figure 5-8. Output Voltage vs Output Current



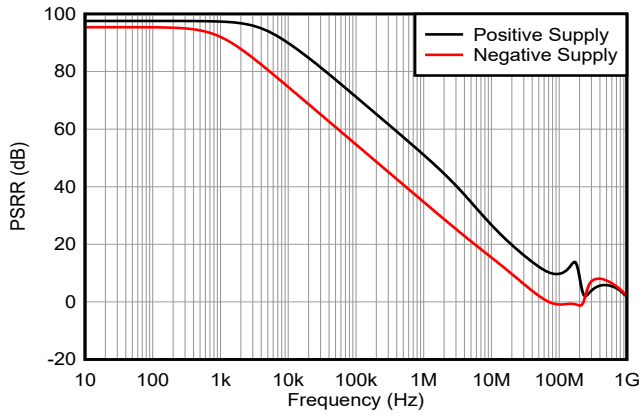
V_S = ±15V

Figure 5-9. Common-Mode Rejection Ratio vs Frequency



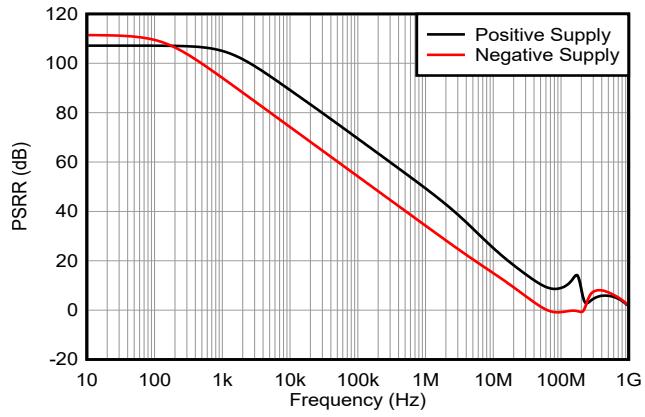
V_S = ±5V

Figure 5-10. Common-Mode Rejection Ratio vs Frequency



V_S = ±15V

Figure 5-11. Power-Supply Rejection Ratio vs Frequency

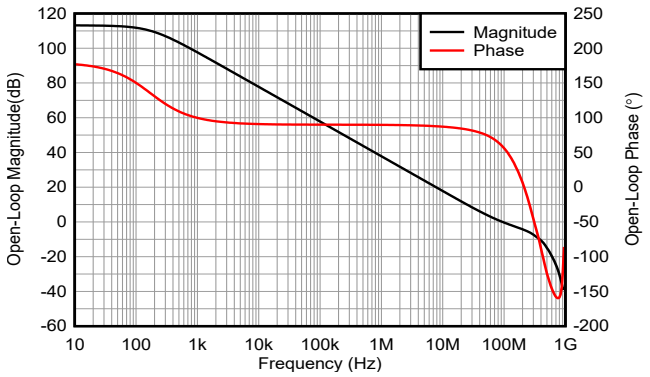


V_S = ±5V

Figure 5-12. Power-Supply Rejection Ratio vs Frequency

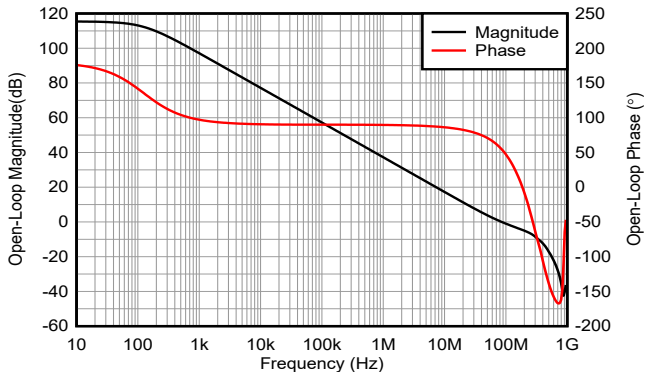
5.7 Typical Characteristics: D (SOIC, 8) Package (continued)

at T_A = 25°C (unless otherwise noted)



V_S = ±15V

Figure 5-13. Open-Loop Frequency Response



V_S = ±5V

Figure 5-14. Open-Loop Frequency Response

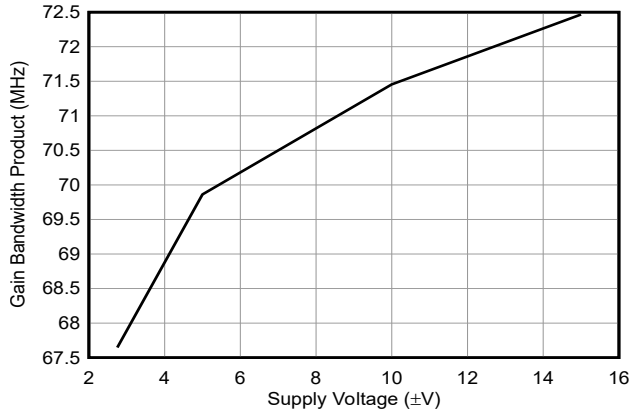
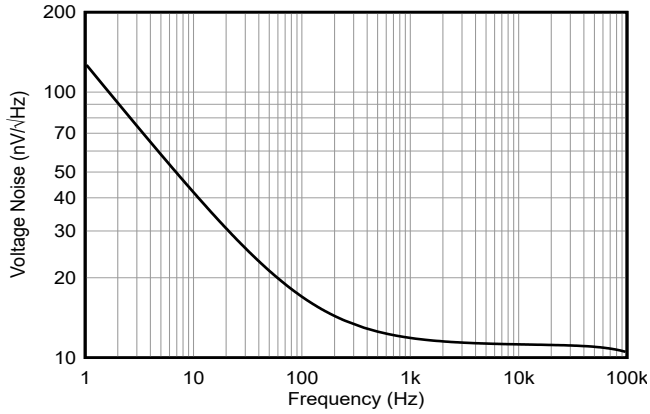
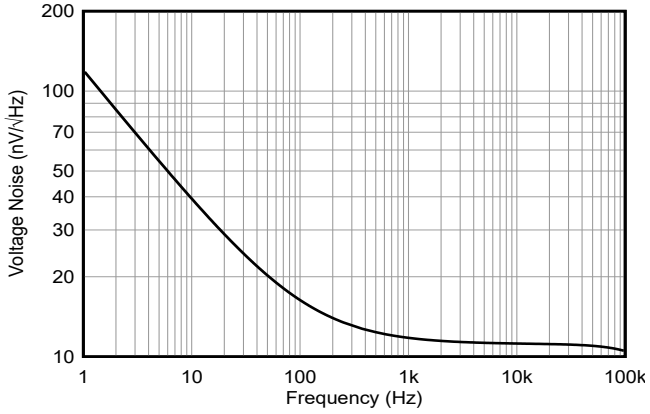


Figure 5-15. Gain-Bandwidth Product vs Supply Voltage at Different Temperature



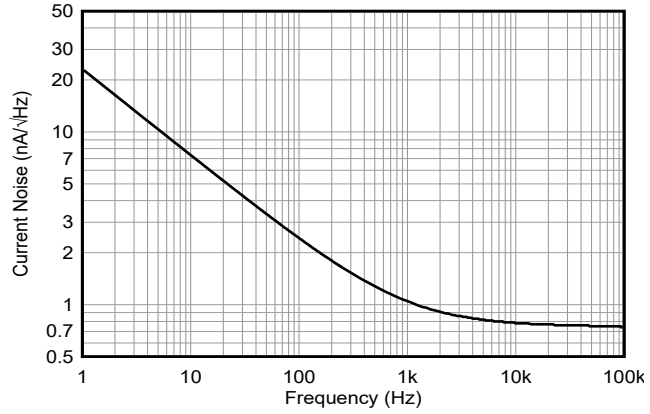
V_S = ±15V

Figure 5-16. Input Voltage Noise vs Frequency



V_S = ±5V

Figure 5-17. Input Voltage Noise vs Frequency

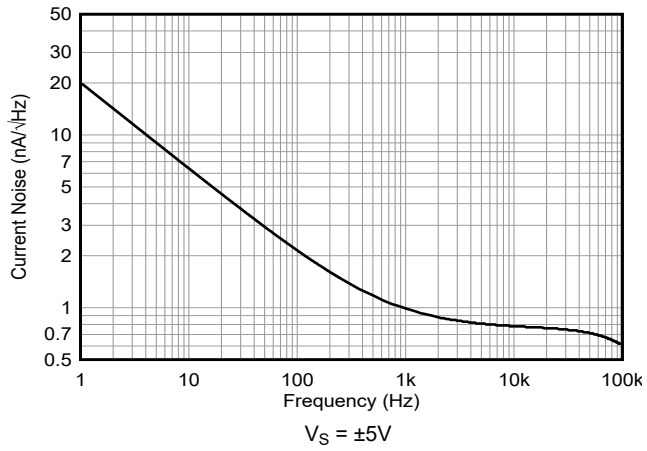


V_S = ±15V

Figure 5-18. Input Current Noise vs Frequency

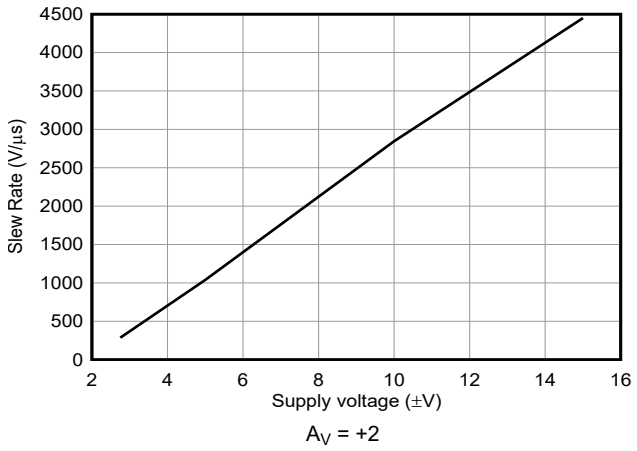
5.7 Typical Characteristics: D (SOIC, 8) Package (continued)

at T_A = 25°C (unless otherwise noted)



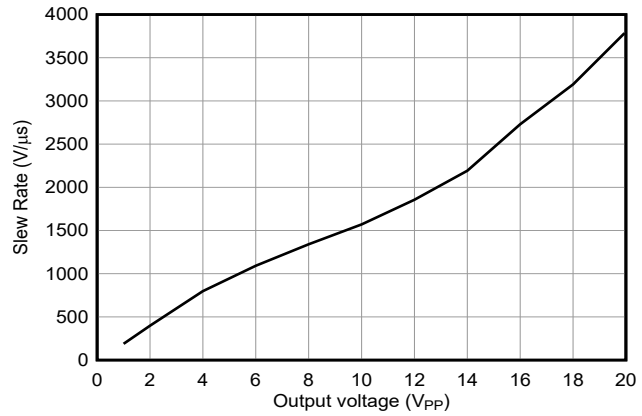
V_S = ±5V

Figure 5-19. Input Current Noise vs Frequency



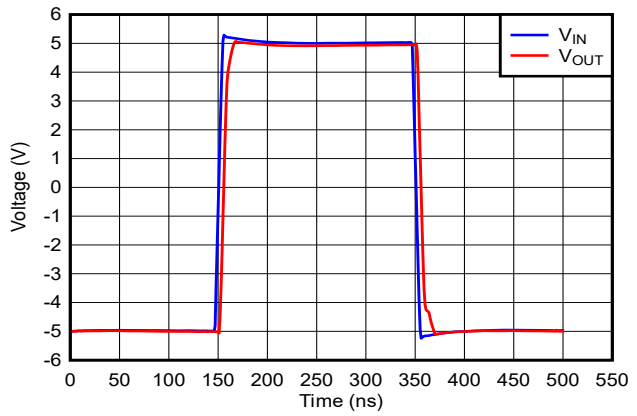
A_V = +2

Figure 5-20. Slew Rate vs Supply Voltage



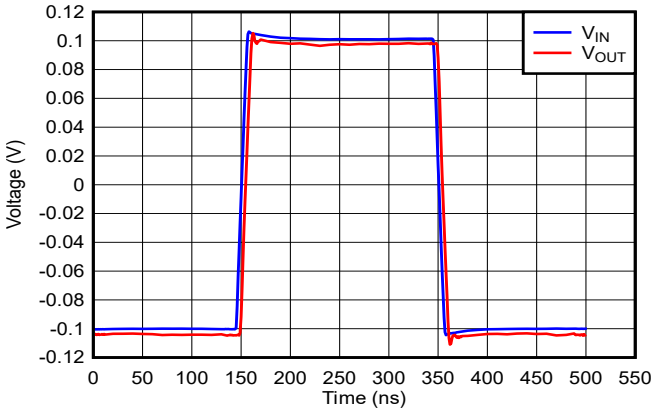
A_V = +2

Figure 5-21. Slew Rate vs Output Voltage



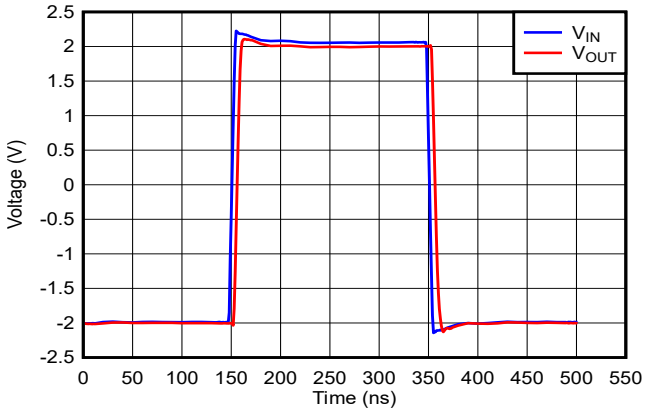
A_V = +1, V_S = ±15V

Figure 5-22. Large-Signal Pulse Response



A_V = +1, V_S = ±15V

Figure 5-23. Small-Signal Pulse Response

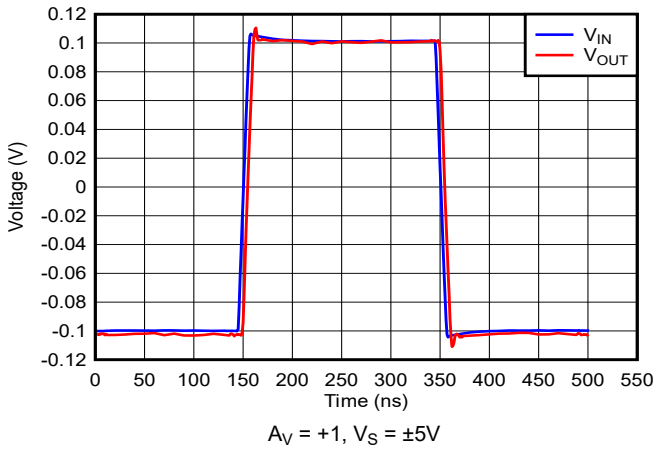


A_V = +1, V_S = ±5V

Figure 5-24. Large-Signal Pulse Response

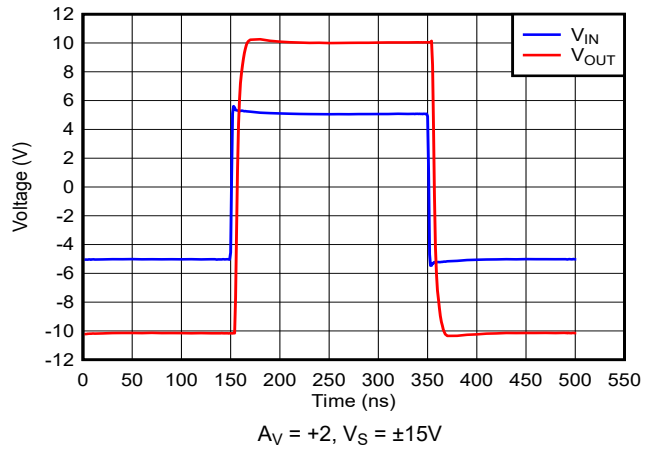
5.7 Typical Characteristics: D (SOIC, 8) Package (continued)

at T_A = 25°C (unless otherwise noted)



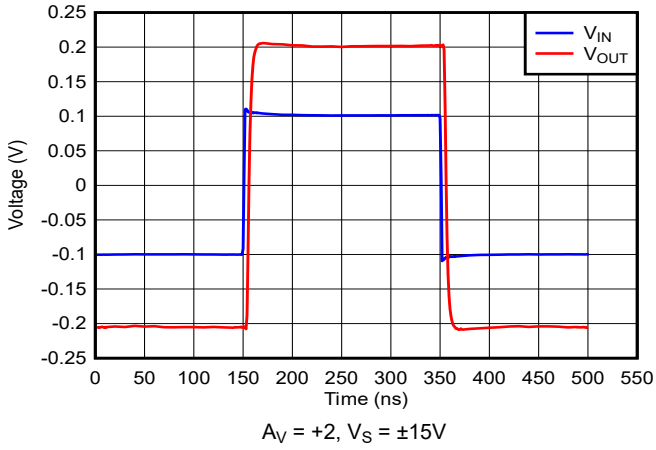
A_V = +1, V_S = ±5V

Figure 5-25. Small-Signal Pulse Response



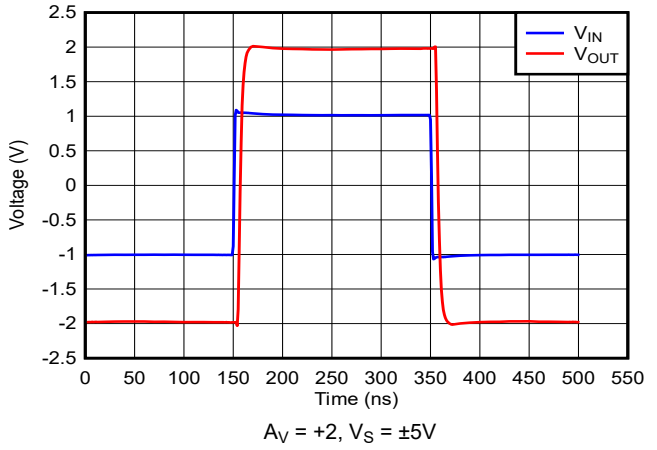
A_V = +2, V_S = ±15V

Figure 5-26. Large-Signal Pulse Response



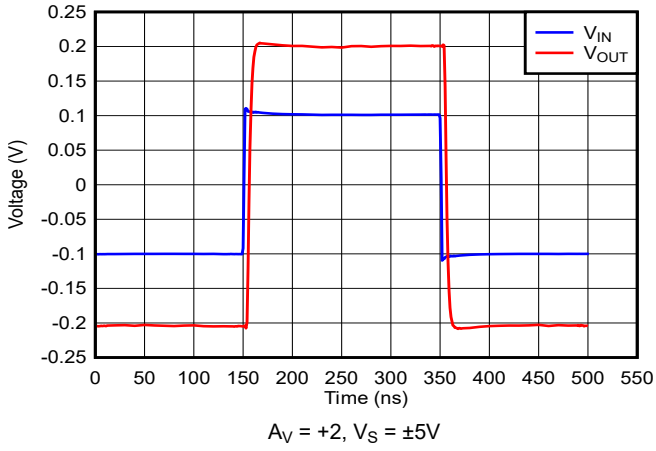
A_V = +2, V_S = ±15V

Figure 5-27. Small-Signal Pulse Response



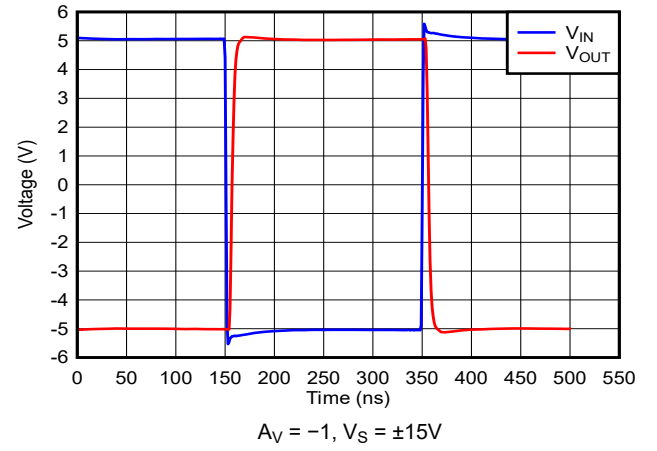
A_V = +2, V_S = ±5V

Figure 5-28. Large-Signal Pulse Response



A_V = +2, V_S = ±5V

Figure 5-29. Small-Signal Pulse Response

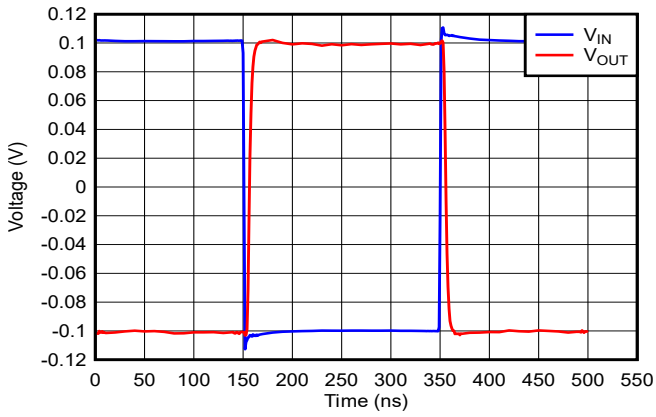


A_V = −1, V_S = ±15V

Figure 5-30. Large-Signal Pulse Response

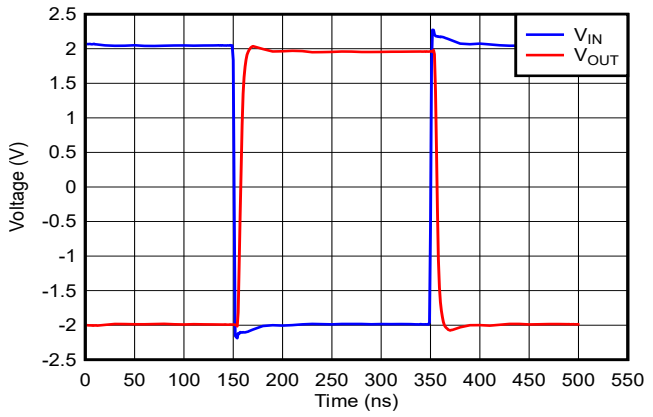
5.7 Typical Characteristics: D (SOIC, 8) Package (continued)

at T_A = 25°C (unless otherwise noted)



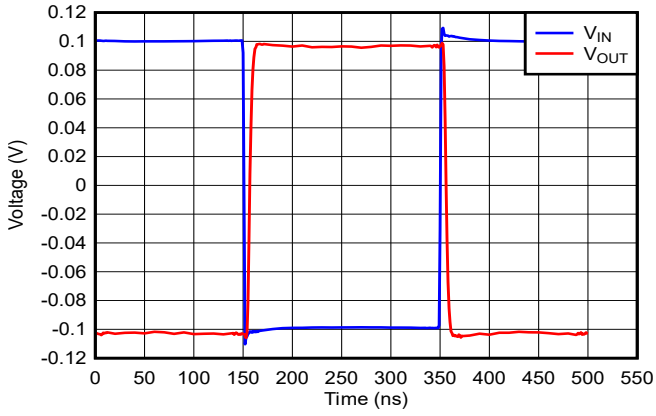
A_V = −1, V_S = ±15V

Figure 5-31. Small-Signal Pulse Response



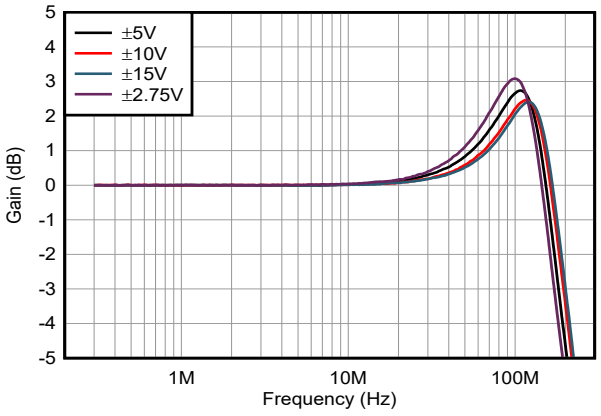
A_V = −1, V_S = ±5V

Figure 5-32. Large-Signal Pulse Response



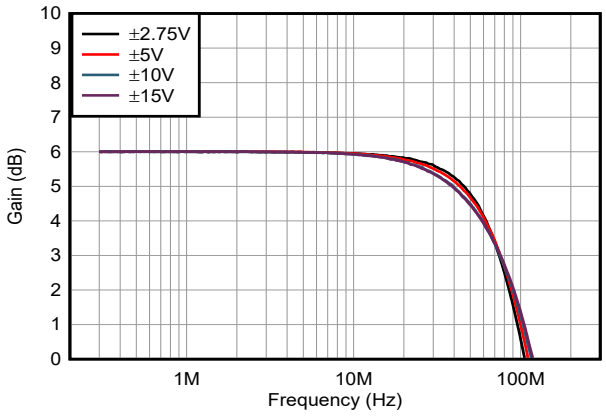
A_V = −1, V_S = ±5V

Figure 5-33. Small-Signal Pulse Response



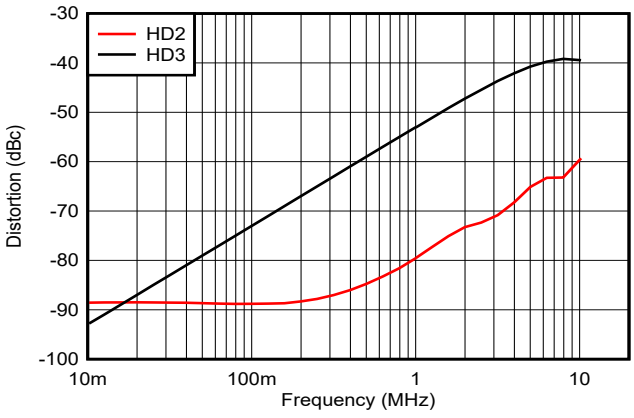
A_V = +1

Figure 5-34. Closed-Loop Frequency Response vs Supply Voltage



A_V = +2

Figure 5-35. Closed-Loop Frequency Response vs Supply Voltage



V_S = ±15V

Figure 5-36. Harmonic Distortion vs Frequency

5.7 Typical Characteristics: D (SOIC, 8) Package (continued)

at T_A = 25°C (unless otherwise noted)

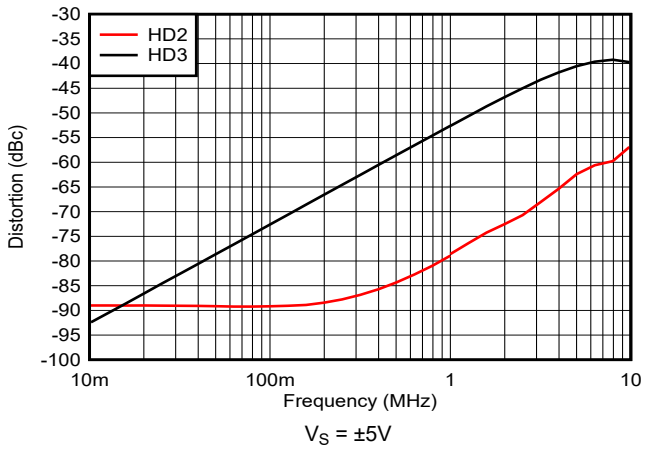


Figure 5-37. Harmonic Distortion vs Frequency

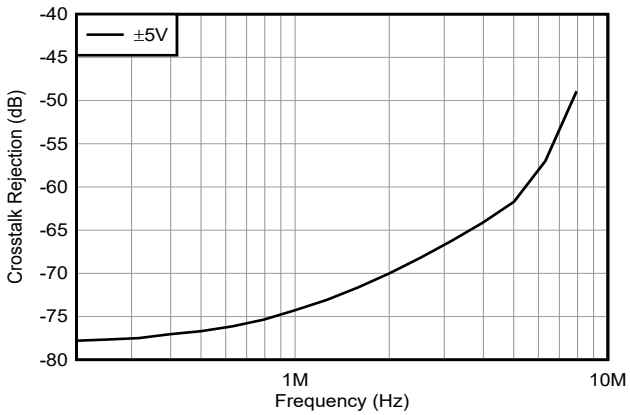


Figure 5-38. Crosstalk Rejection vs Frequency

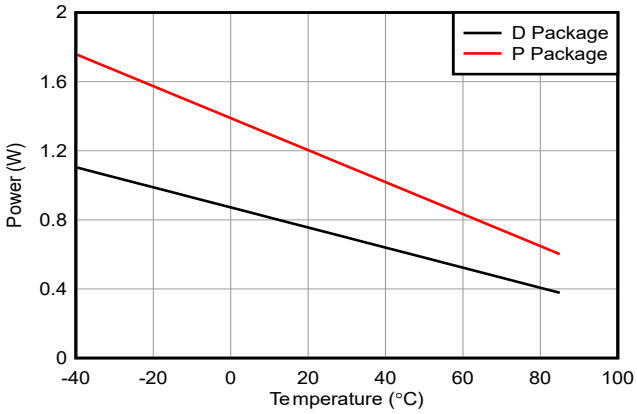


Figure 5-39. Maximum Power Dissipation vs Ambient Temperature

5.8 Typical Characteristics: P (PDIP, 8) Package

at T_A = 25°C (unless otherwise noted)

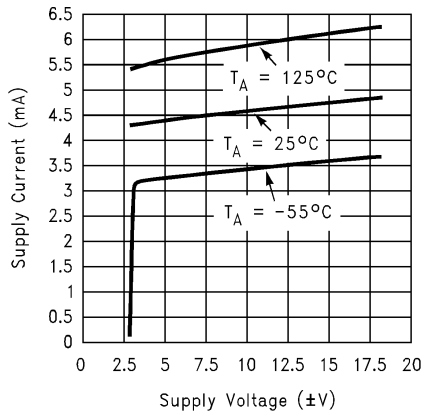


Figure 5-40. Supply Voltage vs. Supply Current

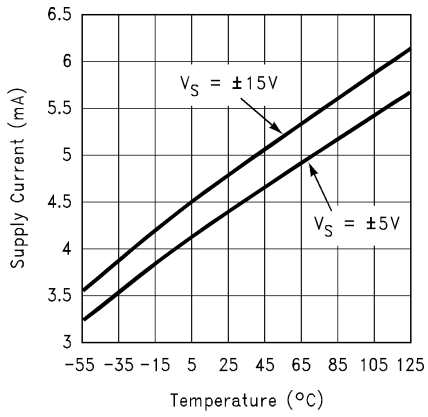


Figure 5-41. Supply Current vs Temperature

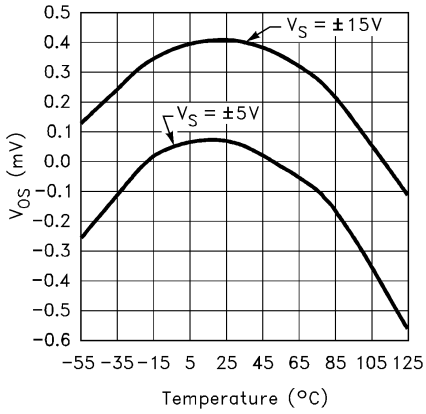


Figure 5-42. Input Offset Voltage vs Temperature

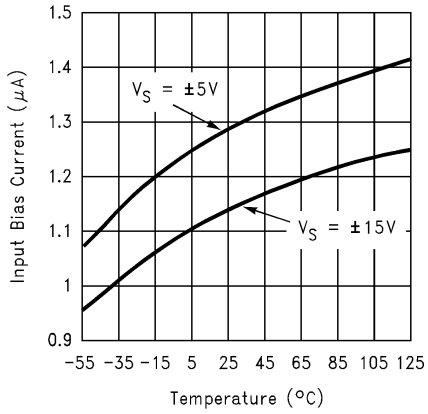


Figure 5-43. Input Bias Current vs Temperature

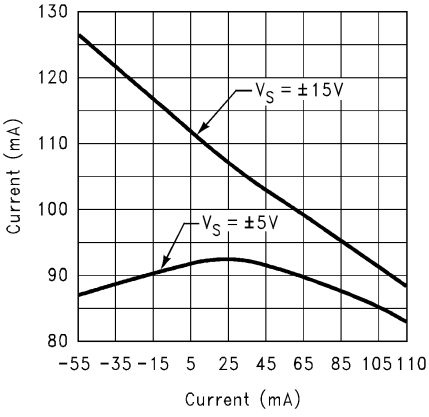


Figure 5-44. Short Circuit Current vs Temperature (Sourcing)

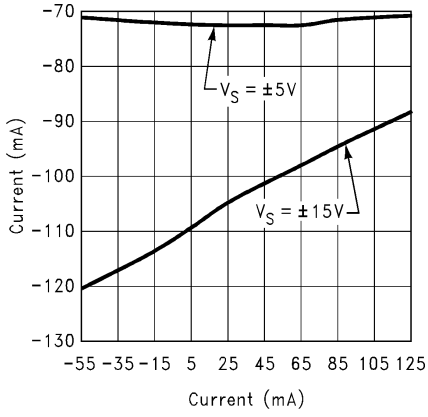
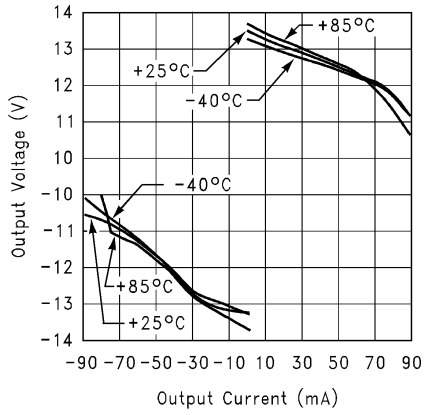


Figure 5-45. Short Circuit Current vs Temperature (Sinking)

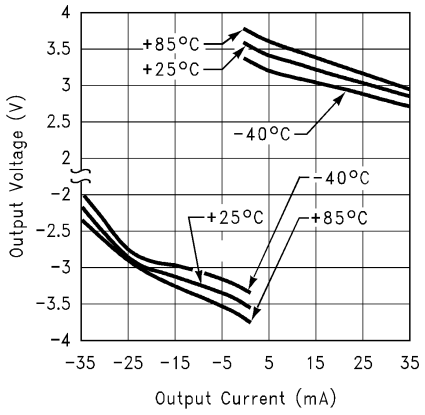
5.8 Typical Characteristics: P (PDIP, 8) Package (continued)

at T_A = 25°C (unless otherwise noted)



V_S = ±15V

Figure 5-46. Output Voltage vs Output Current



V_S = ±5V

Figure 5-47. Output Voltage vs Output Current

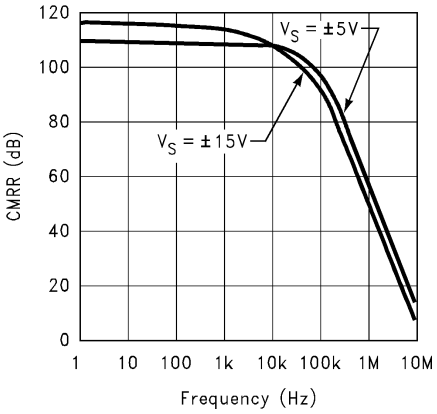


Figure 5-48. Common-Mode Rejection Ratio vs Frequency

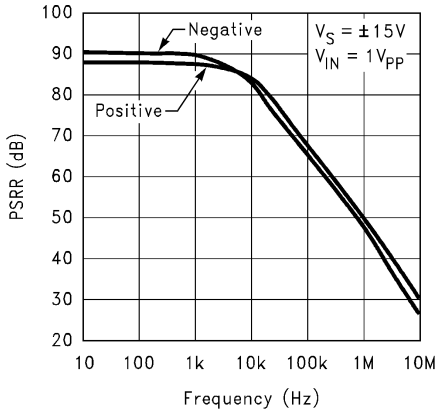


Figure 5-49. PSRR vs Frequency

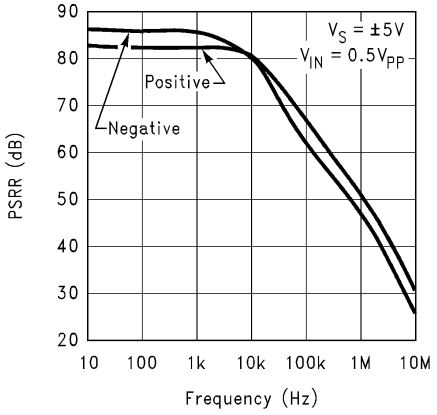


Figure 5-50. PSRR vs Frequency

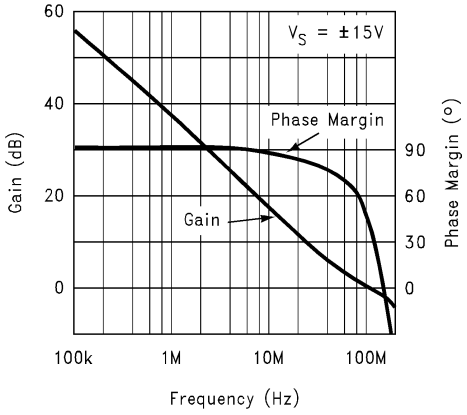


Figure 5-51. Open-Loop Frequency Response

5.8 Typical Characteristics: P (PDIP, 8) Package (continued)

at T_A = 25°C (unless otherwise noted)

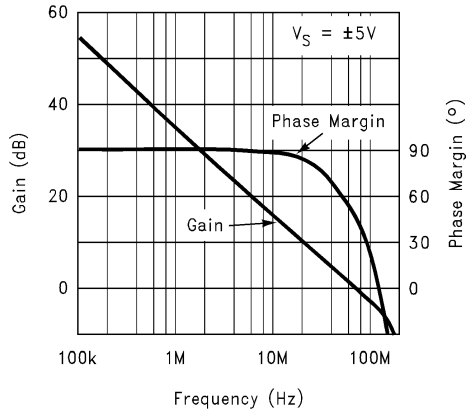


Figure 5-52. Open-Loop Frequency Response

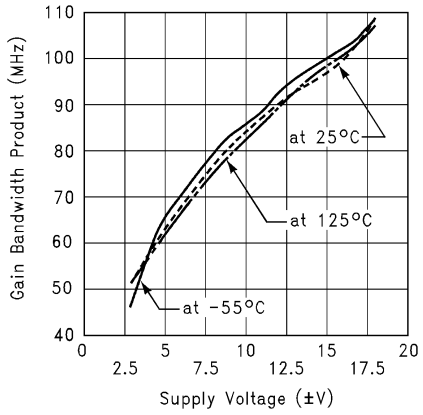


Figure 5-53. Gain-Bandwidth Product vs Supply Voltage at Different Temperature

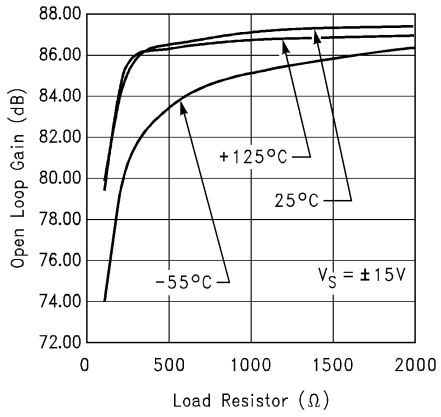


Figure 5-54. Large-Signal Voltage Gain vs Load

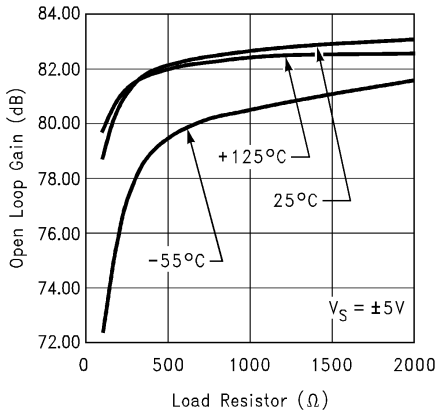


Figure 5-55. Large-Signal Voltage Gain vs Load

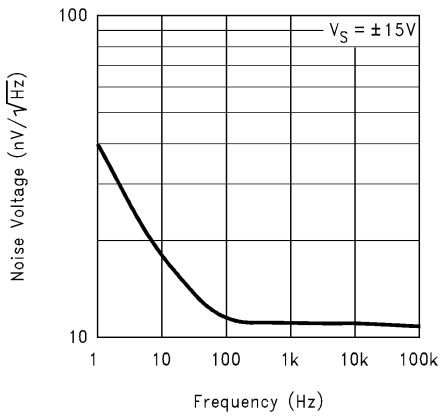


Figure 5-56. Input Voltage Noise vs Frequency

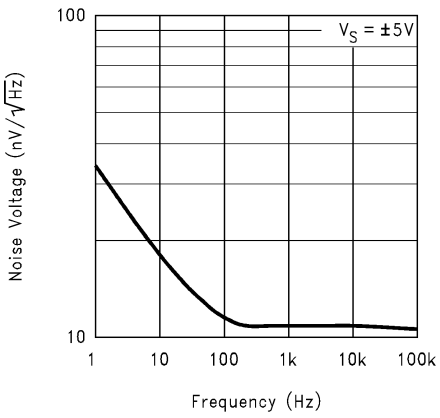


Figure 5-57. Input Voltage Noise vs Frequency

5.8 Typical Characteristics: P (PDIP, 8) Package (continued)

at T_A = 25°C (unless otherwise noted)

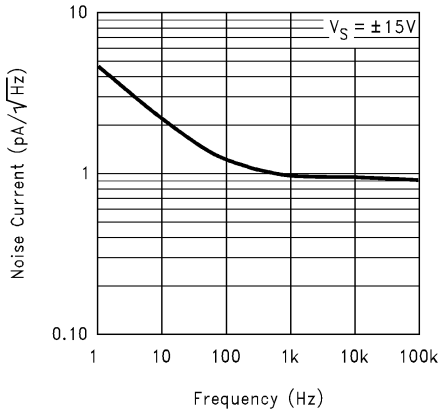


Figure 5-58. Input Current Noise vs Frequency

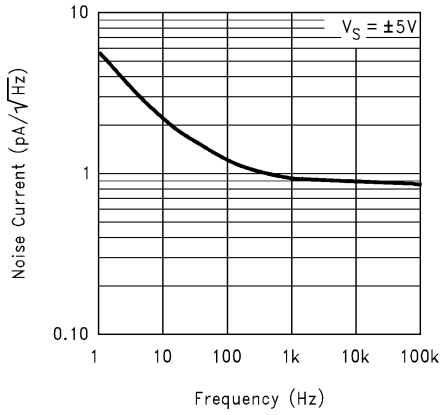


Figure 5-59. Input Current Noise vs Frequency

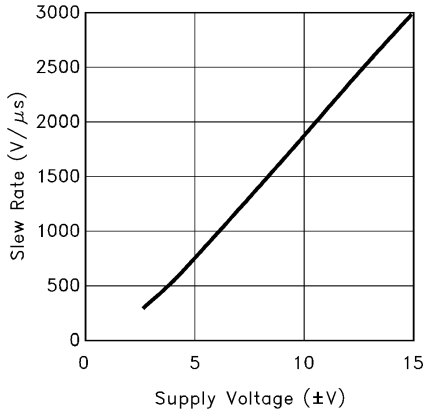


Figure 5-60. Slew Rate vs Supply Voltage

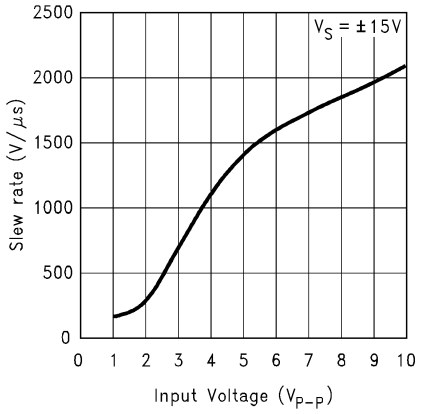
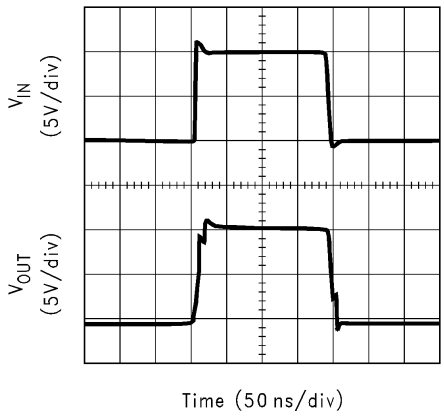
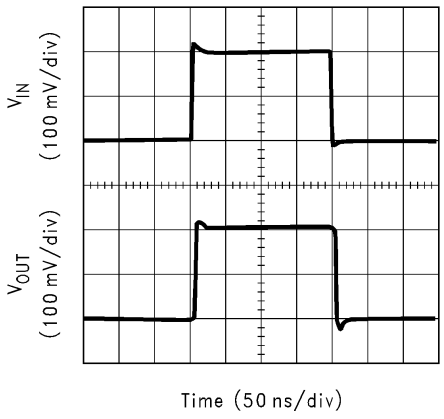


Figure 5-61. Slew Rate vs Input Voltage



A_V = +1, V_S = ±15V

Figure 5-62. Large-Signal Pulse Response

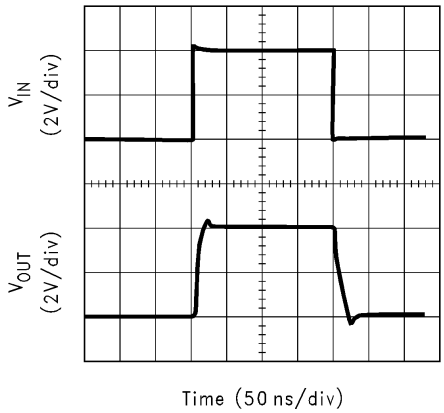


A_V = +1, V_S = ±15V

Figure 5-63. Small-Signal Pulse Response

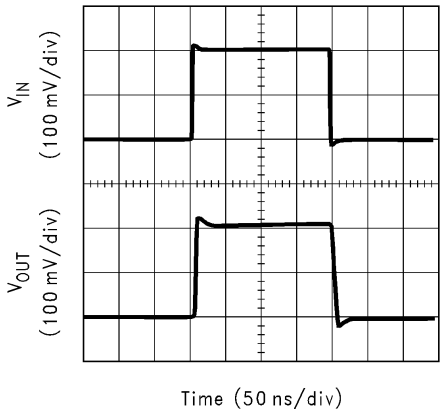
5.8 Typical Characteristics: P (PDIP, 8) Package (continued)

at T_A = 25°C (unless otherwise noted)



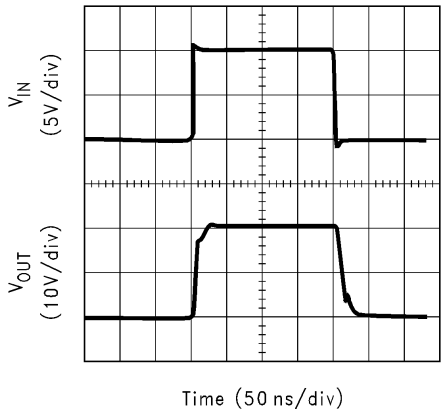
A_V = +1, V_S = ±5V

Figure 5-64. Large-Signal Pulse Response



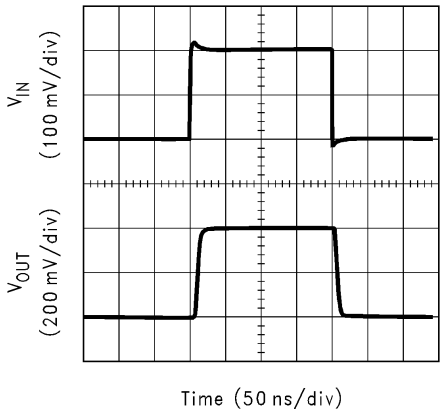
A_V = +1, V_S = ±5V

Figure 5-65. Small-Signal Pulse Response



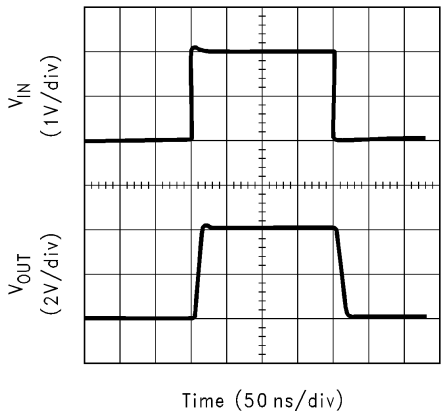
A_V = +2, V_S = ±15V

Figure 5-66. Large-Signal Pulse Response



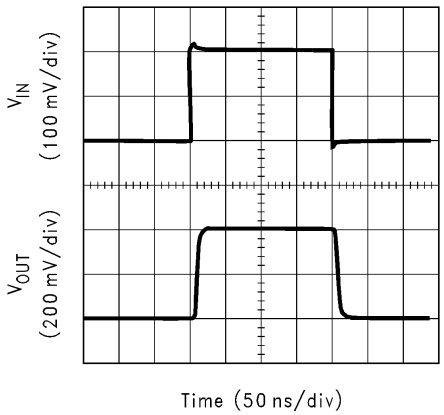
A_V = +2, V_S = ±15V

Figure 5-67. Small-Signal Pulse Response



A_V = +2, V_S = ±5V

Figure 5-68. Large-Signal Pulse Response

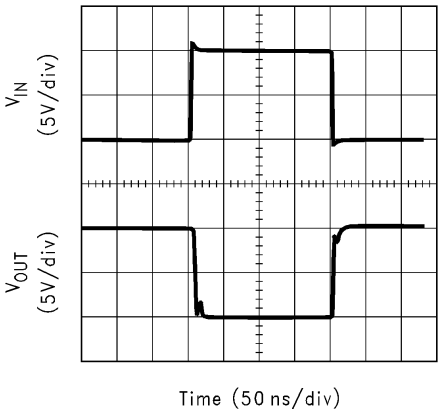


A_V = +2, V_S = ±5V

Figure 5-69. Small-Signal Pulse Response

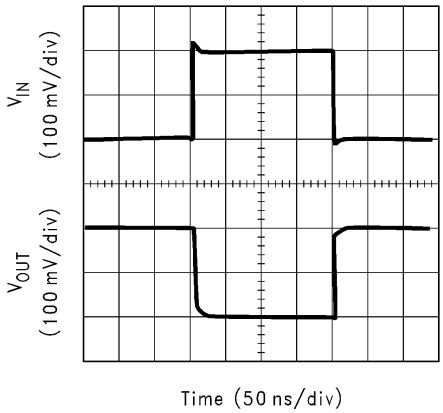
5.8 Typical Characteristics: P (PDIP, 8) Package (continued)

at T_A = 25°C (unless otherwise noted)



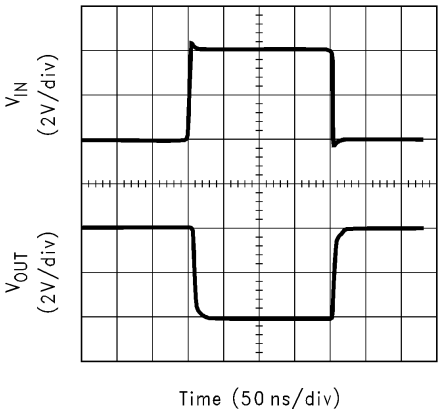
A_V = −1, V_S = ±15V

Figure 5-70. Large-Signal Pulse Response



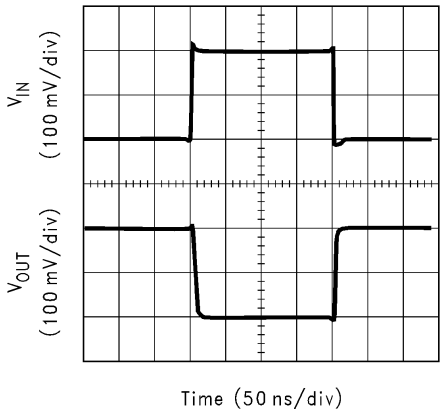
A_V = −1, V_S = ±15V

Figure 5-71. Small-Signal Pulse Response



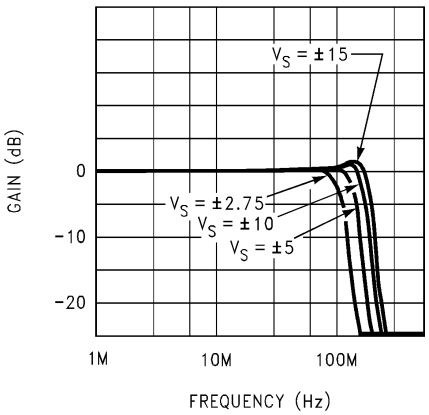
A_V = −1, V_S = ±5V

Figure 5-72. Large-Signal Pulse Response



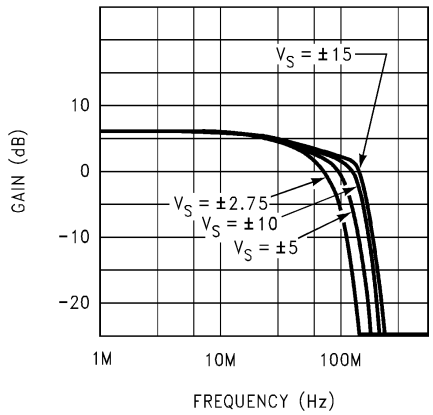
A_V = −1, V_S = ±5V

Figure 5-73. Small-Signal Pulse Response



A_V = +1

Figure 5-74. Closed-Loop Frequency Response vs Supply Voltage

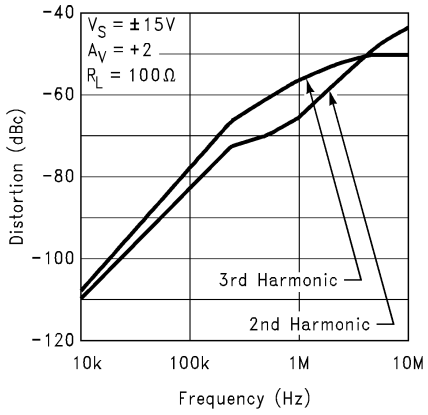


A_V = +2

Figure 5-75. Closed-Loop Frequency Response vs Supply Voltage

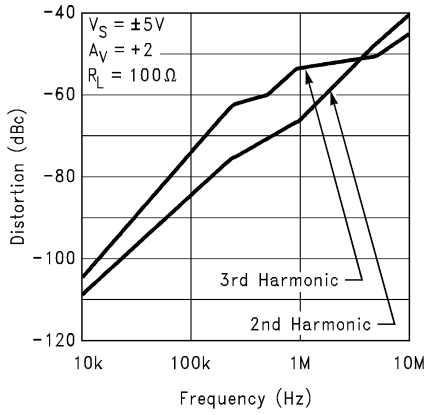
5.8 Typical Characteristics: P (PDIP, 8) Package (continued)

at T_A = 25°C (unless otherwise noted)



V_S = ±15V

Figure 5-76. Harmonic Distortion vs Frequency



V_S = ±5V

Figure 5-77. Harmonic Distortion vs Frequency

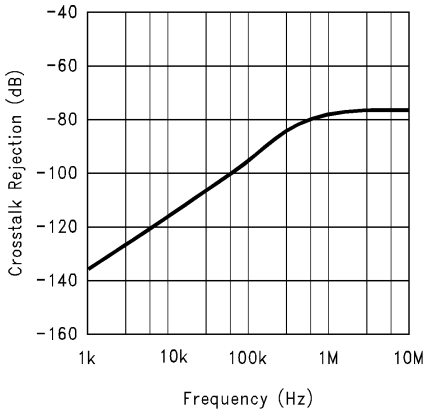


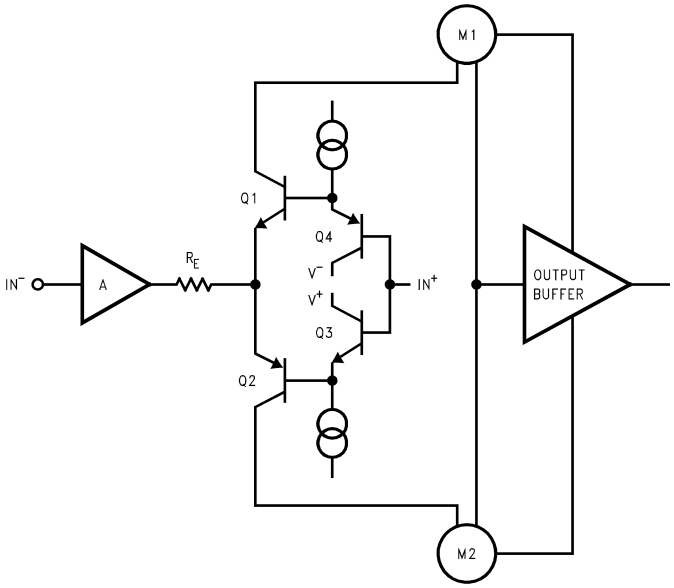
Figure 5-78. Crosstalk Rejection vs Frequency

6 Detailed Description

6.1 Overview

The LM6172 is a dual, high-speed, low-power, voltage-feedback amplifier. The device is unity-gain stable and offers outstanding performance with only 2.3mA of supply current per channel. The combination of 100MHz unity-gain bandwidth, 3000V/µs slew rate, 50mA per channel output current, and other attractive features makes the LM6172 easy to implement in various applications. The quiescent power of the LM6172 is 138mW operating at a ±15V supply and 46mW at a ±5V supply.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Slew Rate

The slew rate of LM6172 is determined by the current available to charge and discharge an internal high impedance node capacitor. This current is the differential input voltage divided by the total degeneration resistor R_E. Therefore, the slew rate is proportional to the input voltage level, and the higher slew rates are achievable in the lower gain configurations.

When a very fast, large signal pulse is applied to the input of an amplifier, some overshoot or undershoot occurs. By placing an external series resistor (such as 1kΩ) to the input of LM6172, the slew rate is reduced to help lower the overshoot, which reduces settling time.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Circuit Operation

The class AB input stage in LM6172 is fully symmetrical and has a similar slewing characteristic to the current feedback amplifiers. In the functional block diagram of Section 6.2, Q1 through Q4 form the equivalent of the current feedback input buffer, R_E the equivalent of the feedback resistor, and stage A buffers the inverting input. The triple-buffered output stage isolates the gain stage from the load to provide low output impedance.

7.1.2 Reduce Settling Time

The LM6172 has a very fast slew rate that causes overshoot and undershoot. To reduce settling time on LM6172, a 1kΩ resistor can be placed in series with the input signal to decrease slew rate. A feedback capacitor can also be used to reduce overshoot and undershoot. This feedback capacitor serves as a zero to increase the stability of the amplifier circuit. A 2pF feedback capacitor is recommended for initial evaluation. When the LM6172 is configured as a buffer, a feedback resistor of 1kΩ must be added in parallel to the feedback capacitor.

Another possible source of overshoot and undershoot comes from capacitive load at the output. See also Section 7.1.3.

7.1.3 Drive Capacitive Loads

Amplifiers that drive capacitive loads can oscillate or ring at the output. To eliminate oscillation or reduce ringing, place an isolation resistor as shown in Figure 7-1. The combination of the isolation resistor and the load capacitor forms a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of the isolation resistor; the bigger the isolation resistor, the more damped (slow) the pulse response becomes. For the LM6172, a 50Ω isolation resistor is recommended for initial evaluation.

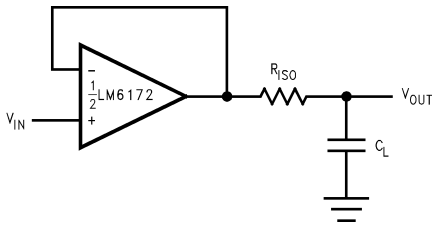


Figure 7-1. Isolation Resistor Used to Drive Capacitive Load

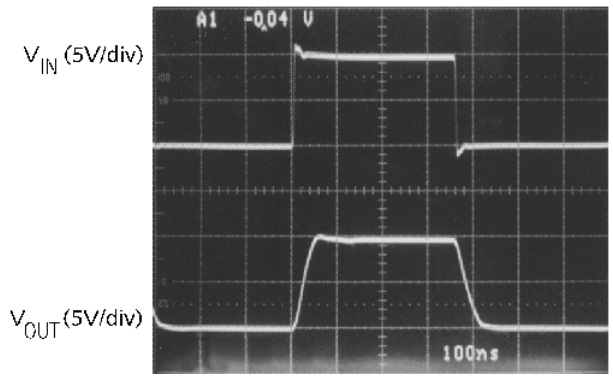


Figure 7-2. The LM6172 Driving a 510pF Load With a 30Ω Isolation Resistor

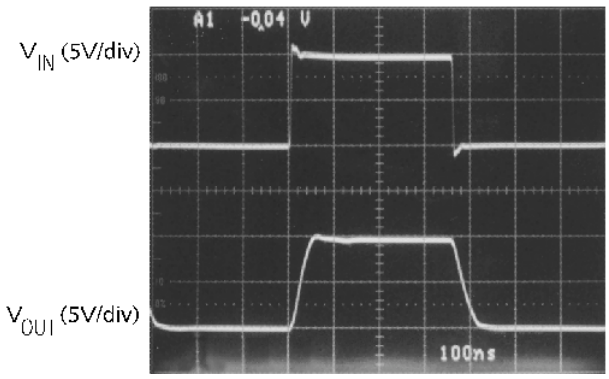


Figure 7-3. The LM6172 Driving a 220pF Load With a 50Ω Isolation Resistor

7.1.4 Compensation for Input Capacitance

The combination of an amplifier input capacitance with gain-setting resistors adds a pole that can cause peaking or oscillation. To solve this problem, a feedback capacitor with the following value can be used to cancel that pole:

$$C_F > (R_G \times C_{IN}) / R_F \quad (1)$$

For the LM6172, a feedback capacitor of 2pF is recommended. Figure 7-4 illustrates the compensation circuit.

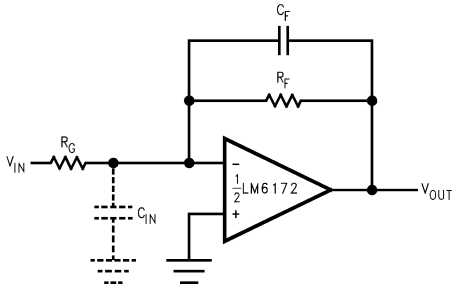


Figure 7-4. Compensating for Input Capacitance

7.1.5 Termination

In high-frequency applications, reflections occur if signals are not properly terminated. Figure 7-5 shows a properly terminated signal while Figure 7-6 shows an improperly terminated signal.

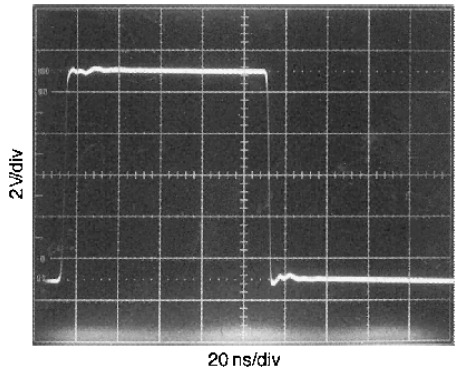


Figure 7-5. Properly Terminated Signal

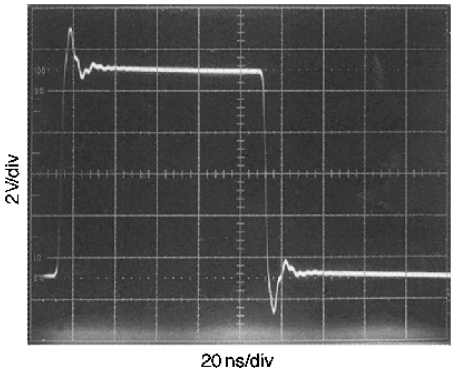


Figure 7-6. Improperly Terminated Signal

To minimize reflection, use coaxial cable with matching characteristic impedance to the signal source. Terminate the other end of the cable with the same value terminator or resistor. For commonly used cables, RG59 has a 75Ω characteristic impedance, and RG58 has a 50Ω characteristic impedance.

7.2 Typical Application

7.2.1 Application Circuits

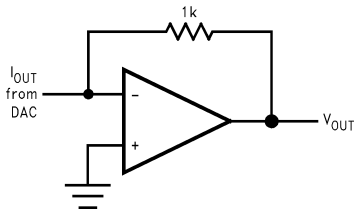


Figure 7-7. I-to-V Converters

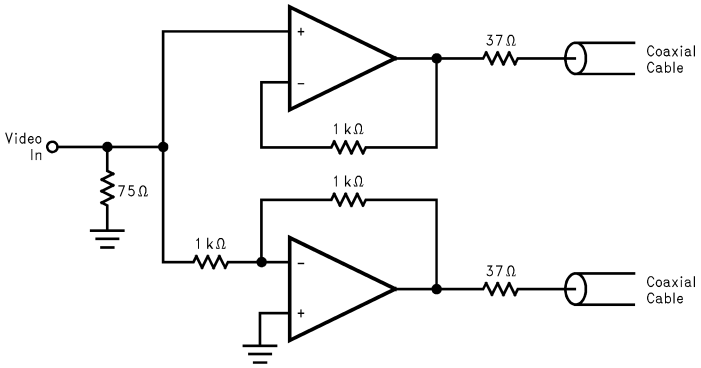


Figure 7-8. Differential Line Driver

7.3 Power Supply Recommendations

7.3.1 Power Supply Bypassing

Bypassing the power supply is necessary to maintain low power supply impedance across frequency. Bypass both positive and negative power supplies individually by placing 0.01µF ceramic capacitors directly to the power supply pins and 2.2µF tantalum capacitors close to the power-supply pins.

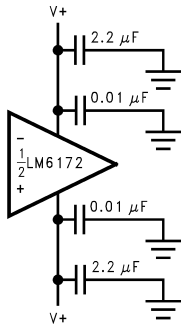


Figure 7-9. Power Supply Bypassing

7.3.2 Power Dissipation

The maximum power allowed to dissipate in a device is defined as:

$$P_D = (T_{J(max)} - T_A) / \theta_{JA} \quad (2)$$

where

- P_D is the power dissipation in a device
- $T_{J(max)}$ is the maximum junction temperature
- T_A is the ambient temperature
- θ_{JA} is the thermal resistance of a particular package

For example, for the LM6172 in a SOIC-8 package, the maximum power dissipation at 25°C ambient temperature is 726mW.

Thermal resistance, θ_{JA}, depends on parameters such as die size, package size, and package material. The smaller the die size and package, the higher the θ_{JA}. The 8-pin PDIP package has lower thermal resistance (108°C/W) than that of the 8-pin SOIC (172°C/W). Therefore, for higher dissipation capability, use an 8-pin PDIP.

The total power dissipated in a device can also be calculated as:

$$P_D = P_Q + P_L \quad (3)$$

where

- P_Q is quiescent power dissipated in a device with no load connected at the output.
- P_L is power dissipated in the device with a load connected at the output, not power dissipated by the load.

Furthermore,

- P_Q = supply current × total supply voltage with no load
- P_L = output current × (voltage difference between supply voltage and output voltage of the same supply)

For example, use Equation 3 to solve the total power dissipated by the LM6172 with V_S = ±15V and both channels swinging output voltage of 10V into 1kΩ:

- = 2[(2.3mA)(30V)] + 2[(10mA)(15V − 10V)]
- = 138mW + 100mW
- = 238mW

7.4 Layout

7.4.1 Layout Guidelines

7.4.1.1 Printed Circuit Boards and High-Speed Op Amps

There are many things to consider when designing printed circuit boards (PCBs) for high-speed op amps. Without proper caution, excessive ringing, oscillation and other degraded ac performance in high-speed circuits can occur. As a rule, use short and wide the signal traces to provide low inductance and low impedance paths. Ground any unused board space to reduce stray signal pickup. Also ground critical components at a common point to eliminate voltage drop. Sockets add capacitance to the board and can affect frequency performance. Best practice is to solder the amplifier directly into the PCB without using a socket.

7.4.1.2 Using Probes

Active (FET) probes are an excellent choice for taking high-frequency measurements because these probes have wide bandwidth, high input impedance, and low input capacitance. However, the probe ground leads provide a long ground loop that produces errors in measurement. Instead, ground the probes directly by removing the ground leads and probe jackets and using scope probe jacks.

7.4.1.3 Components Selection and Feedback Resistor

In high-speed applications, keep all component leads short because wires are inductive at high frequency. For discrete components, choose carbon composition-type resistors and mica-type capacitors. Surface-mount components are preferred over discrete components for minimum inductive effect.

Large values of feedback resistors can couple with parasitic capacitance and cause undesirable effects such as ringing or oscillation in high-speed amplifiers. For the LM6172, a feedback resistor less than 1kΩ gives optimized performance.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E (December 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added *Package Information* table and *Pin Configuration and Functions*, *Specifications*, *ESD Ratings*, *Recommended Operating Conditions*, *Thermal Information*, *Detailed Description*, *Overview*, *Functional Block Diagram*, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Typical Applications*, *Power Supply Recommendations*, *Layout*, *Layout Guidelines*, *Layout Example*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections	1
• Changed pin names and updated pinout diagram to reflect new naming convention	3
• Updated *Thermal Information* for the D (SOIC-8) and P (PDIP-8) packages	4
• Moved *DC and AC Electrical Characteristics* into one table for both ±15V and ±5V specifications	5
• Changed output short-circuit current for D package	5
• Updated unity-gain bandwidth from 100MHz to 80MHz for D package	5
• Updated second harmonic distortion for D package	5
• Updated third harmonic distortion for D package	5
• Changed output short-circuit current for D package	7
• Updated –3dB frequency for D package	7
• Updated phase margin for D package	7
• Updated second harmonic distortion for D package	7
• Updated third harmonic distortion for D package	7
• Deleted *Maximum Power Dissipation vs Ambient Temperature*	16

- Changed thermal values in *Power Dissipation* to match *Thermal Information* table..... 27

Changes from Revision C (March 2013) to Revision D (March 2013) **Page**

- Deleted ESD information and footnote from *Absolute Maximum Ratings* and moved to *ESD Ratings*.....4
- Deleted footnote from *Recommended Operating Conditions*.....4
- Changed layout of National Data Sheet to TI format.....26

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM6172IM/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	LM61 72IM
LM6172IMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 85	LM61 72IM
LM6172IMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LM61 72IM
LM6172IMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LM61 72IM
LM6172IN/NOPB	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM6172IN
LM6172IN/NOPB.A	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM6172IN
LM6172IN/NOPB.B	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM6172IN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

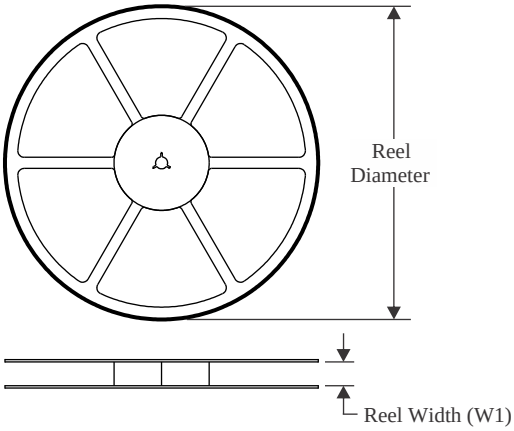
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

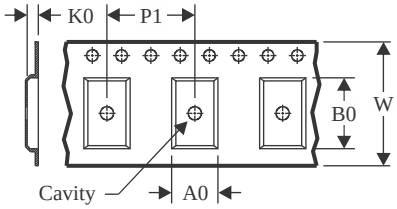
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

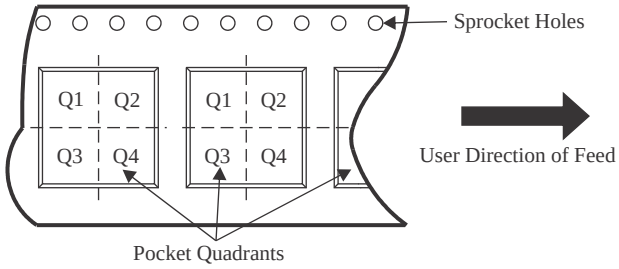


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

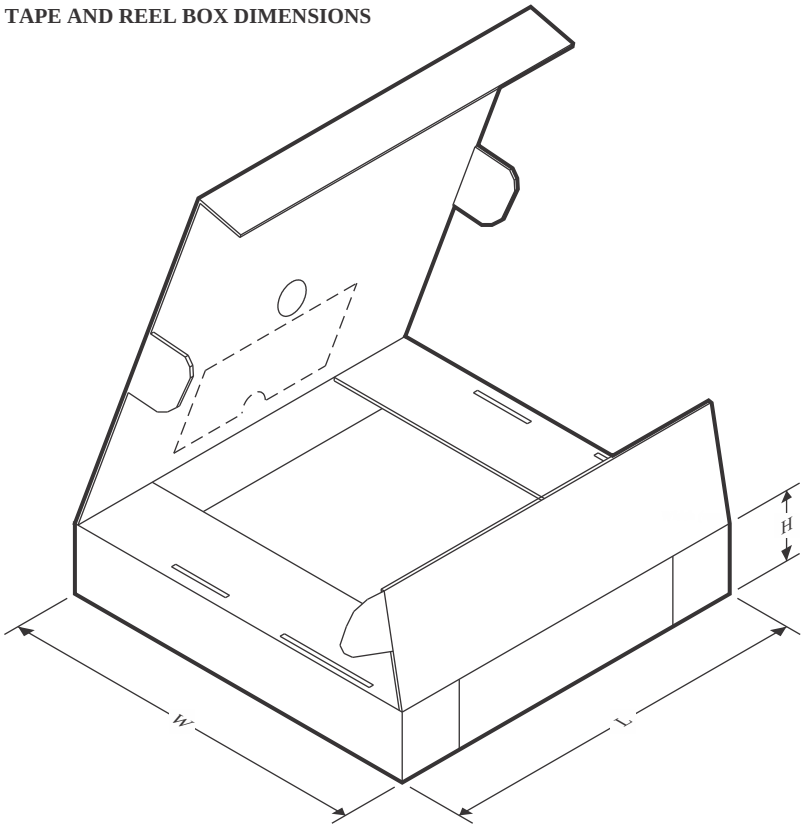
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM6172IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

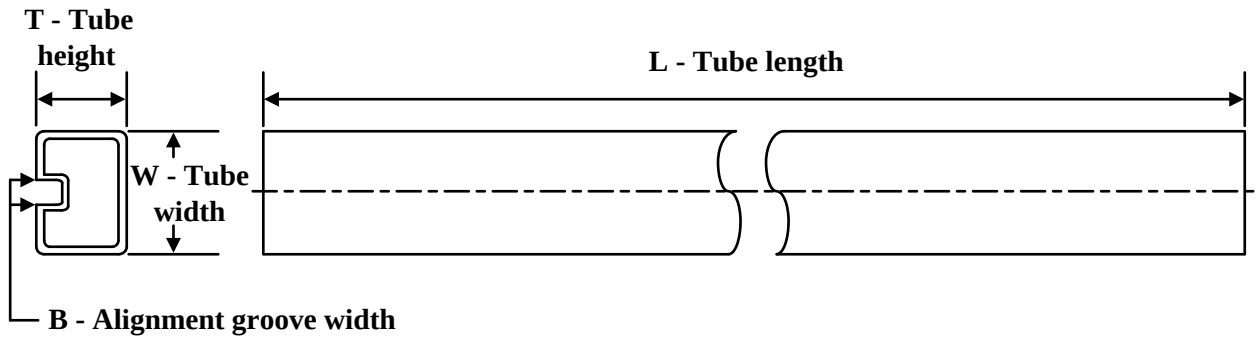
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

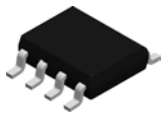
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM6172IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM6172IN/NOPB	P	PDIP	8	40	502	14	11938	4.32
LM6172IN/NOPB.A	P	PDIP	8	40	502	14	11938	4.32
LM6172IN/NOPB.B	P	PDIP	8	40	502	14	11938	4.32

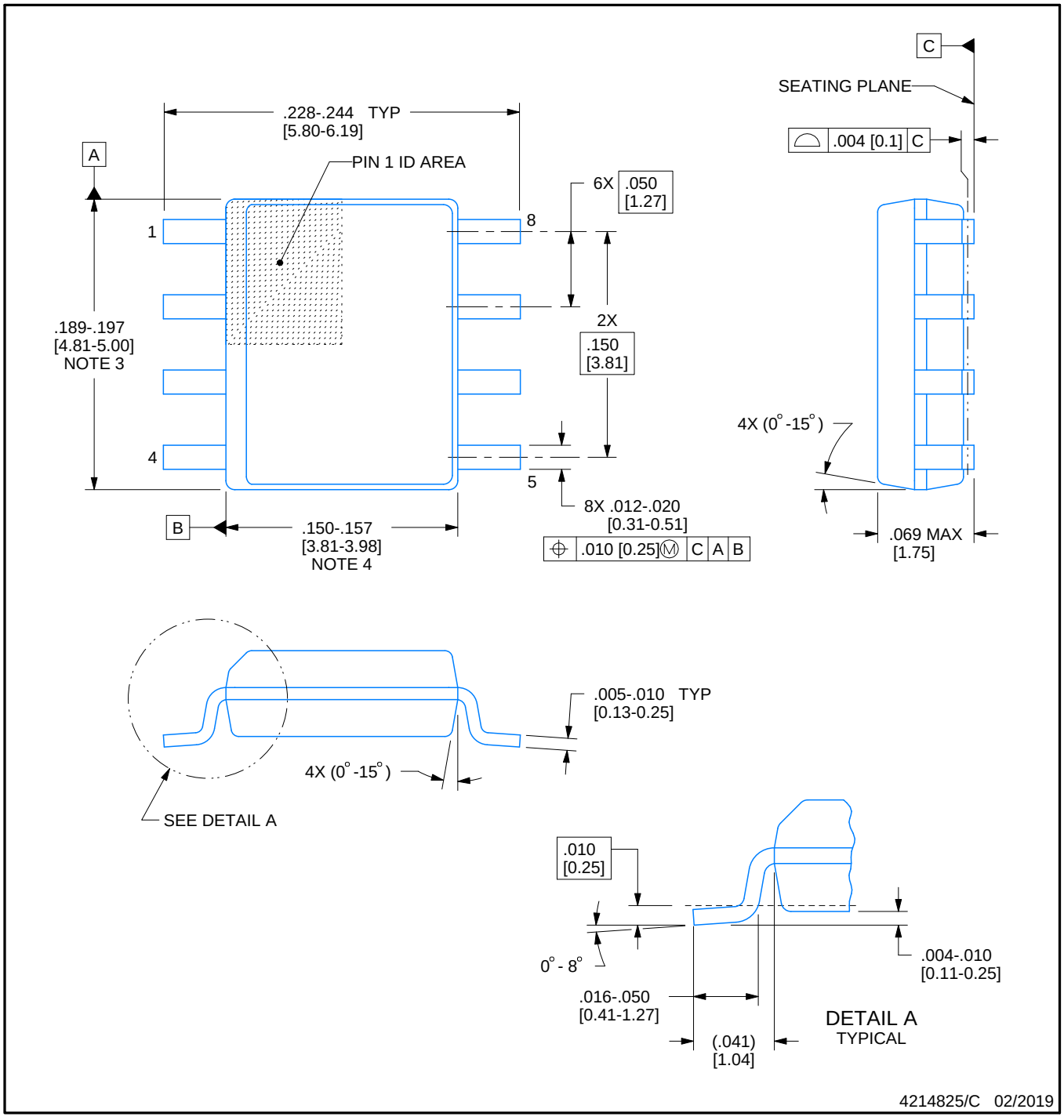


PACKAGE OUTLINE

D0008A

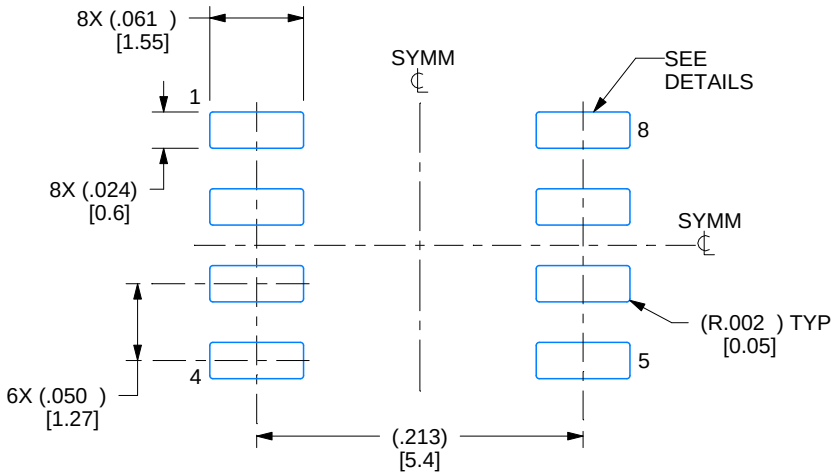
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

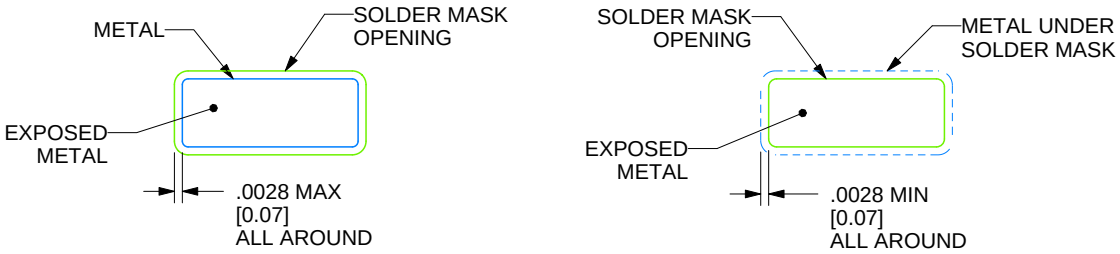


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

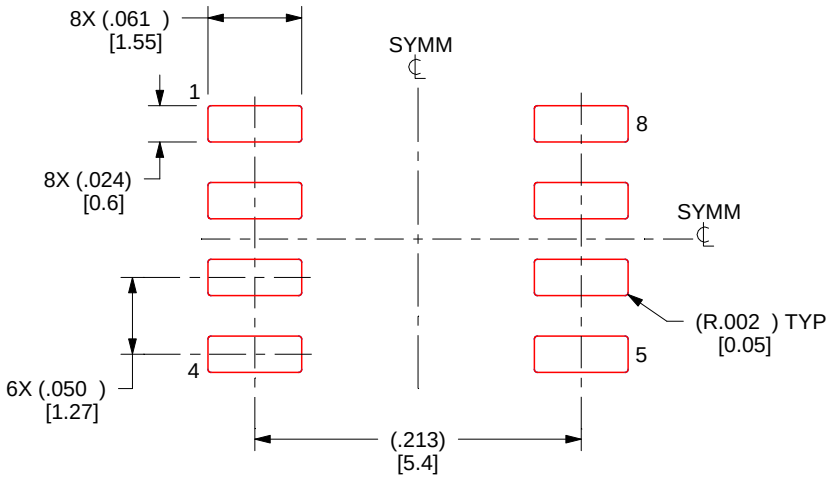
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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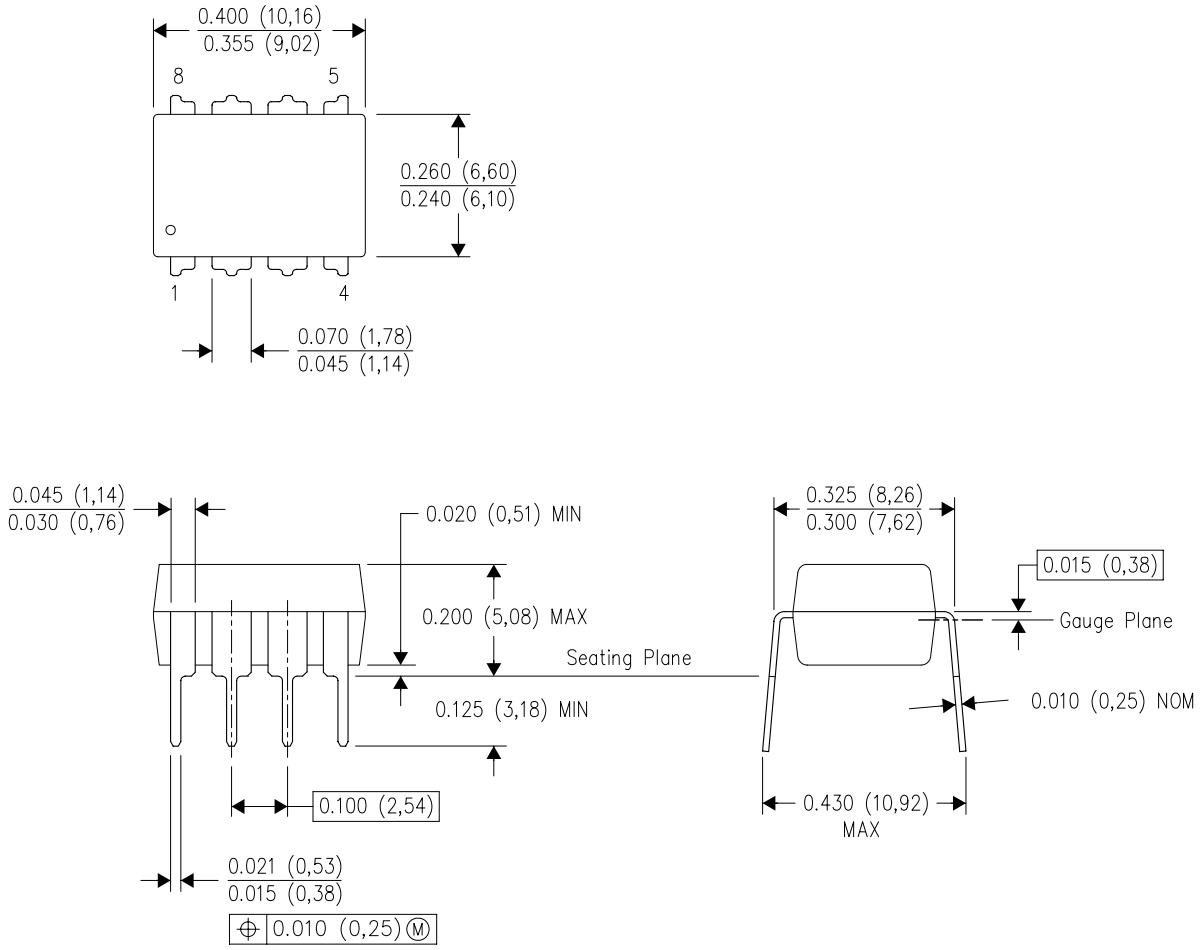
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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Last updated 10/2025