LM7311 3.5V–23V, 33mΩ, 5A eFuse With True Reverse Current blocking

1 Features

- Wide operating input voltage range: 3.5V to 23V
  - 28V absolute maximum
  - Output negative voltage support up to -1V
- Integrated back-to-back FETs with low ON-resistance: R_{ON} = 33mΩ (typ)
- 5A continuous current
- 15A peak current for 10ms with 2% duty cycle
- Active High Enable input with adjustable undervoltage Lockout (UVLO)
- Ideal diode operation with true reverse current blocking (RCB)
- Fixed Overvoltage (OVLO) protection with debounce time
- Short Circuit protection at startup and steady state
- Adjustable output slew rate control (dVdt)
- Overtemperature protection
- Digital output: Fault Indication ($\overline{FLT}$)
- Small footprint: DFN 3mm × 3mm

2 Applications

- Adapter and charger input protection
- USB PD protection:smartphone, tablet, PC, notebook, monitor, dock
- Power MUXing and ORing

3 Description

The LM7311x family is a highly integrated, circuit-protection and power-management device in a small package. The devices provide multiple protection modes that use few external components and are a robust defense against overloads, short-circuits, voltage surges and excessive inrush current. With integrated back-to-back FETs, reverse current flow from output to input is blocked at all times, making the devices designed for power MUX and ORing applications, as well as systems that need load side energy hold up storage if input power supply fails. The devices use a linear ORing based scheme to maintain almost zero DC reverse current and emulate ideal diode behavior with minimum forward voltage drop and power dissipation.

Output slew rate and inrush current can be adjusted using a single external capacitor. Loads are protected from input overvoltage conditions by cutting off the output if input exceeds an adjustable overvoltage threshold.

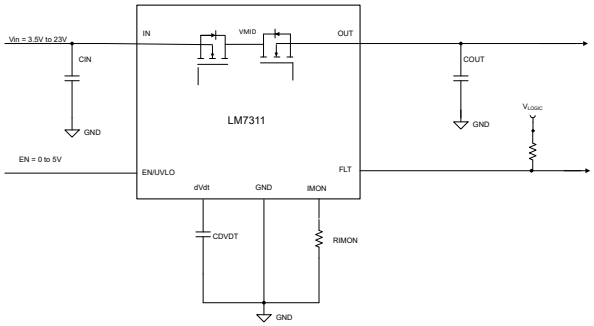
The devices are available in a 3mm × 3mm, for improved thermal performance and reduced system footprint.

The devices are characterized for operation over a junction temperature range of –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LM7311x	(DFN, 12)	3mm × 3mm

(1) For all available variants, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Device Comparison Table

Part Number	Response to TSD Fault
LM7311L	Latch-Off
LM7311A	Auto-retry

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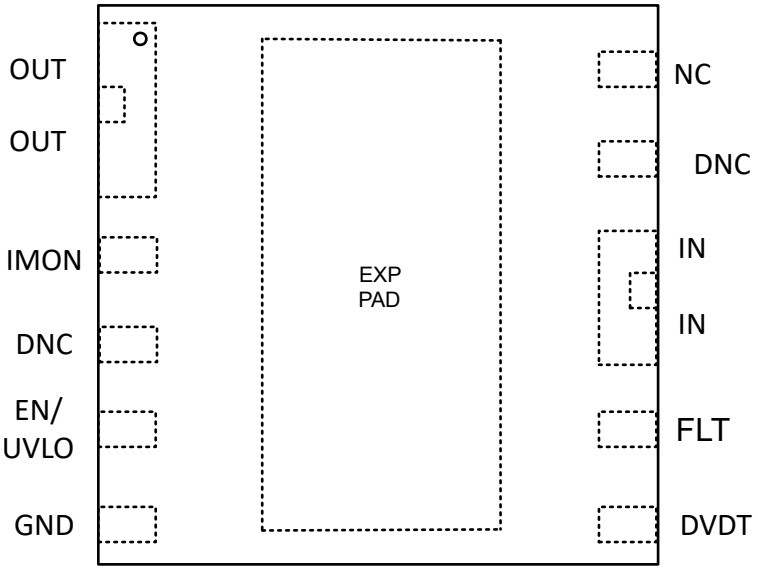
5 Pin Configuration and Functions



LM7311

Figure 5-1. LM7311 Package, 12- DFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
OUT	1,2	Power	Power Output. Must be soldered to the output power plane uniformly for power heat dissipation
IMON	3	Input	Pin acts as a accurate analog output load current monitor signal if a resistor to GND is connected. Can be left floating if unused. Connecting to EXP PAD has no effect on device performance.
DNC	4	-	Do not connect. Connecting a passive component has no effect on device performance.
EN/UVLO	5	Input	Active High Enable input. Connect a resistor divider or voltage source to enable the device. This pin has a weak pullup to internal supply to support floating for auto turn on.
GND	6	Ground	Device Ground Reference Pin. Connect to system Ground
DVDT	7	Input/ Output	Start up output slew rate control pin from IN to OUT. Leave the pin open to allow fastest startup. Connect a capacitor to GND to slow down the slew rate to manage inrush
$\overline{\text{FLT}}$	8	Input/ Output	Fault Output. Connect a External pullup resistor. Pulled down during fault event. This pin as a weak pullup to internal supply.
IN	9,10	Power	Power Input. Must be soldered to the input power plane uniformly for proper heat dissipation
DNC	11	-	Do not Connect
NC	12	-	No connect
EXP PAD	EXP PAD	-	Thermal pad for power dissipation. Must be connected to a floating copper plan on the board through multipl vias for best thermal performance and must be electrically isolated.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Pin	MIN	MAX	UNIT
VIN	Maximum Input Voltage Range, -40 ℃ ≤ T_J ≤ 125 ℃	IN	-0.3	28	V
VOUT	Maximum Output Voltage Range, -40 ℃ ≤ T_J ≤ 125 ℃	OUT	–1	28	
VEN/UVLO	Maximum Enable Pin Voltage Range	EN/UVLO	–0.3	6.5	V
VdVdT	Maximum dVdT Pin Voltage Range	dVdt	–0.3	6.5	V
VFLTB	Maximum FLTb Pin Voltage Range	FLTB	–0.3	6.5	V
VIMON	Maximum IMON Pin Voltage Range	IMON	6.5		V
IMAX	Maximum Continuous Switch Current	IN to OUT	5		A
T_J	Junction temperature		–40	125	°C
TLEAD	Maximum Lead Temperature			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. [Following sentence optional; see the wiki.] Manufacturing with less than 250-V CDM is possible with the necessary precautions. [Following sentence optional; see the wiki.] Pins listed as ±YYY V and/or ±ZZZ V can actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
VIN	Input Voltage Range	IN	3.5	23	V
VOUT	Output Voltage Range	OUT	3.5	23	V
VEN/UVLO	Enable Pin Voltage Range	EN/UVLO		5	V
VdVdT	dVdT Capacitor Voltage Rating	dVdt		Internally limited	V
VFLTB	FLTB Pin Voltage Range	FLTB		5	V
RIMON	IMON Pin Resistance	IMON	420	3360	Ω
IMAX	Continuous Switch Current, , T_J ≤ 125 ℃	IN to OUT		5	A
T_J	Junction temperature		–40	125	°C

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6.4 Thermal Information

THERMAL METRIC(1)		LM7311x DRR(QFN) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

VIN = 20V, EN = 5V, CIN = 10uF, CDVDT = 5.6nF unless otherwise noted.
Over operating free-air temperature range (unless otherwise noted)

Test Parameter	Description	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)					
IQ(ON)	IN Supply Quiescent Current powered from VIN		460		uA
IQ(OFF,UVLO)	IN OFF State Current (VSD<EN<VUVLO)		93		uA
ISD	IN Shutdown Current (EN <VSD)		10		uA
VUVP(R)	IN Supply UVP Rising threshold VIN		3.42		V
VUVP(F)	IN Supply UVP Falling threshold VIN		3.32		V
VUVPHYS	IN Supply UVP Hysteresis VIN		100		mV
ON RESISTANCE (IN - OUT)					
RON	ON Resistance at VIN = 12V, Iout = 5A, TJ =25C		33		mΩ
RON	ON Resistance at VIN = 12V, Iout = 5A, TJ =-40 <=TJ<=125C		33		mΩ
ENABLE/UNDERVOLTAGE LOCKOUT (EN/UVLO)					
VUVLO(R)	UVLO Rising threshold		1.2		V
VUVLO(F)	UVLO Falling threshold		1.09		V
VUVLOHYS	UVLO Hysteresis		100		mV
VSD(F)	VSD Threshold Falling		0.77		V
VSD(R)	VSD Threshold Rising		0.78		V
IENLKG	EN leakage current			1	uA
OVERVOLTAGE LOCKOUT (OVLO)					
POVP	OVP Threshold		24		
REVERSE CURRENT BLOCKING (IN - OUT)					
VFWD	VIN - VOUT Forward regulation voltage		12		mV
VREVTH	VOUT - VIN threshold for fast BFET turn off (enter reverse current blocking).		50		mV
IREVLKG	Reverse leakage current during RCB		0.5		µA
VFWDTH	VIN - VOUT threshold for BFET turn on (exit reverse current blocking)		100		mV
OUTPUT LOAD CURRENT MONITOR (IMON)					
GIMON	Current Monitor Gain (IMON:IOUT) IOUT = 1A		142		uA/A
GIMON	Current Monitor Gain (IMON:IOUT) IOUT = 3A		142		uA/A
GIMON	Current Monitor Gain (IMON:IOUT) IOUT = 5A		142.5		uA/A
SHORT CIRCUIT PROTECTION (OUT)					
ILIM	Startup ILIM VOUT>VFB		6.5		A
ISFT	Scalable Fast Trip Threshold (ISFT): ILIM Ratio (Startup)		200		%

VIN = 20V, EN = 5V, CIN = 10uF, CDVDT = 5.6nF unless otherwise noted.
Over operating free-air temperature range (unless otherwise noted)

Test Parameter	Description	MIN	TYP	MAX	UNITS
IFFT	Fixed Fast Trip Threshold (FFT)		18		A
VFB	I_{HOLD} Foldback Voltage		2.78		V
FAULT INDICATION (FLTB)					
IFLTLKG	FLT leakage current vs. VIN			1	uA
RFLT	FLTB Internal Pull down resistance		13.5		Ω
OVERTEMPERATURE PROTECTION (OTP)					
TSD	Thermal Shutdown Rising Threshold		152		°C
TSDHYS	Thermal Shutdown Hysteresis		12		°C
DVDT					
Gdvdt	dVdt Gain		22		V/V
Idvdt	dVdt Pin Charging Current		2.5		uA
VDSCLAMP					
VDSCLAMP activation	VDS CLAMP activation voltage		25.4		V
VOCLAMP	Output voltage post VDS CLAMP		12		V

6.6 Timing Requirements

VIN = 20V, EN = 5V, CIN = 10uF, CDVDT = 5.6nF unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
td_on	Insertion Delay when EN>UVLO	EN>UVLO to VOUT rising		8		ms
tOVLOdeb	Overvoltage protection debounce time	VIN>OV		512		us
tSC	Short circuit response time during startup	IOUT > 3 × ILIMto Output current cut off		500		ns
tSC	Short circuit response time during steady state	IOUT > IFFT to Output current cut off		500		ns
tREV	Reverse Current Blocking comparator response time	(VOUT - VIN) > V_{REVTH} + 30% to BFET OFF		1		µs
tSWRCB	Reverse Current Blocking comparator recovery time	(VIN- VOUT) > V_{FWDTH} to VOUT rising		50		µs
tTSD,RST	Thermal Shutdown Auto-Retry Interval	Device Enabled and TJ < TSD - TSDHYS		64		ms

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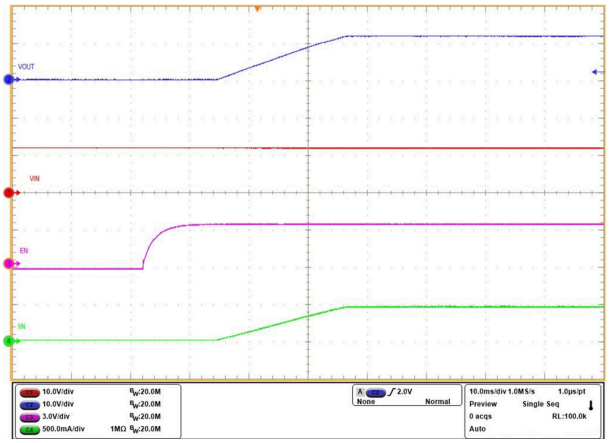
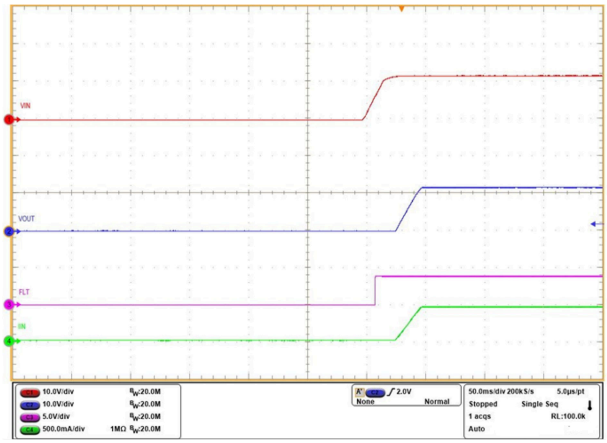
6.7 Typical Characteristics



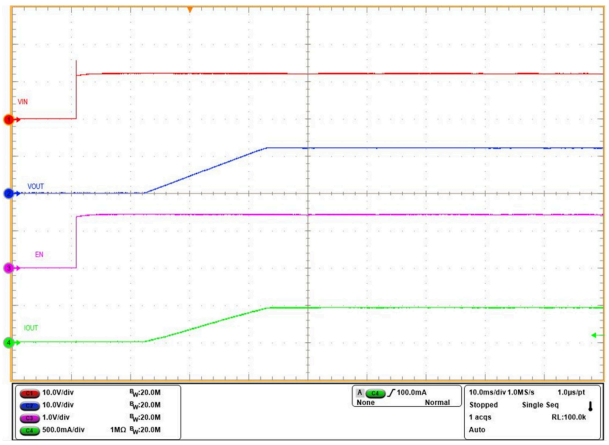
V_{IN} = 12V, C_{OUT} = 11µF, R_{OUT} = 23Ω, C_{dVdt} =100nF , $V_{EN/UVLO}$ stepped up to 3.5V

Figure 6-1. Start Up With Enable



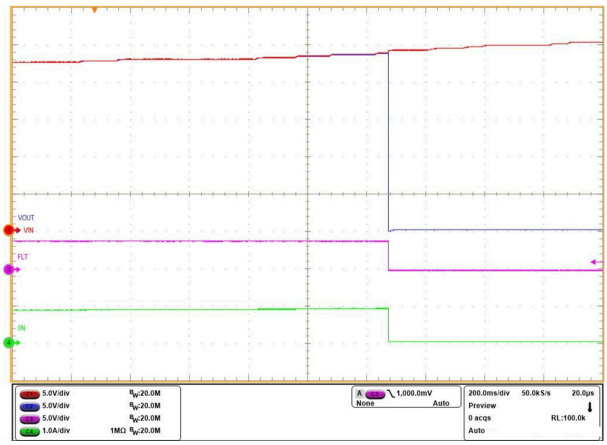
$V_{EN/UVLO}$ = 10.7V via Resitive divider of R_1=1MΩ(from V_{EN} to GND), R_2=124k Ω(VIN to V_{EN}) from VIN to GND, C_{OUT} = 11µF, R_{OUT}= 23Ω, C_{dVdt} = 100nF, V_{IN} ramped up to 12V

Figure 6-2. Start Up With Supply and EN tied via resistive divider



C_{IN} = 0.1 µF, C_{OUT} = 11µF, R_{OUT}= 23Ω, C_{dVdt} = 100nF, EN/UVLO connected to IN through resistor ladder, 12 V hot-plugged to IN

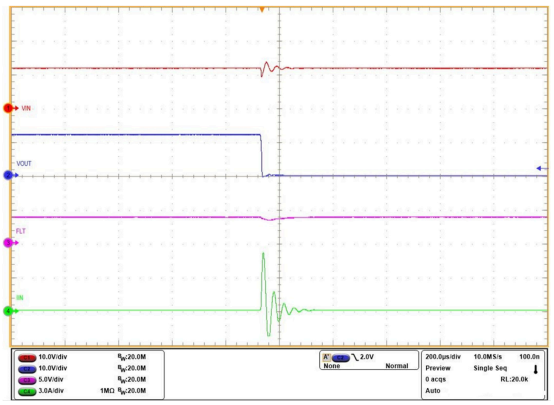
Figure 6-3. Input Hot-Plug



V_{IN} Overvoltage threshold is internally fixed to 24V, V_{IN} ramped up from 23V to 25V

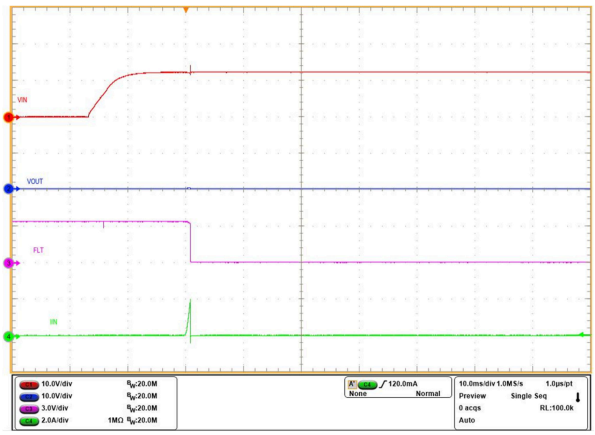
Figure 6-4. Overvoltage Lockout Response

6.7 Typical Characteristics (continued)



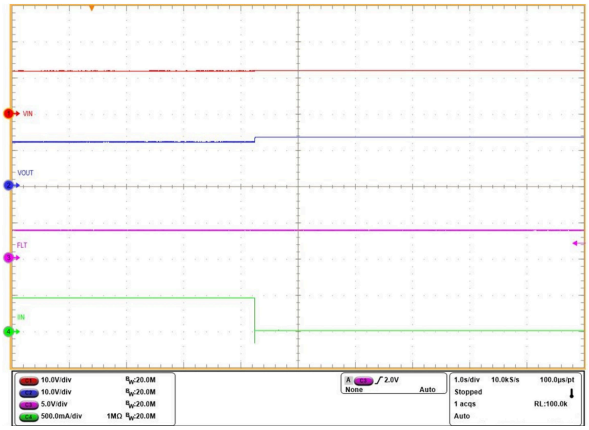
V_{IN} = V, $V_{EN/UVLO}$ = 3V, OUT stepped from Open → Short-circuit to GND

Figure 6-5. Output Short-Circuit During Steady State



V_{IN} = 12V, OUT short-circuit to GND, I_{LIM} internally set at 6.5A

Figure 6-6. Power Up Into Short-Circuit



V_{IN} = 12V, OUT taken to 13V. I_{LOAD}=500mA before the RCB

Figure 6-7. Reverse Current Blocking

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7 Detailed Description

7.1 Overview

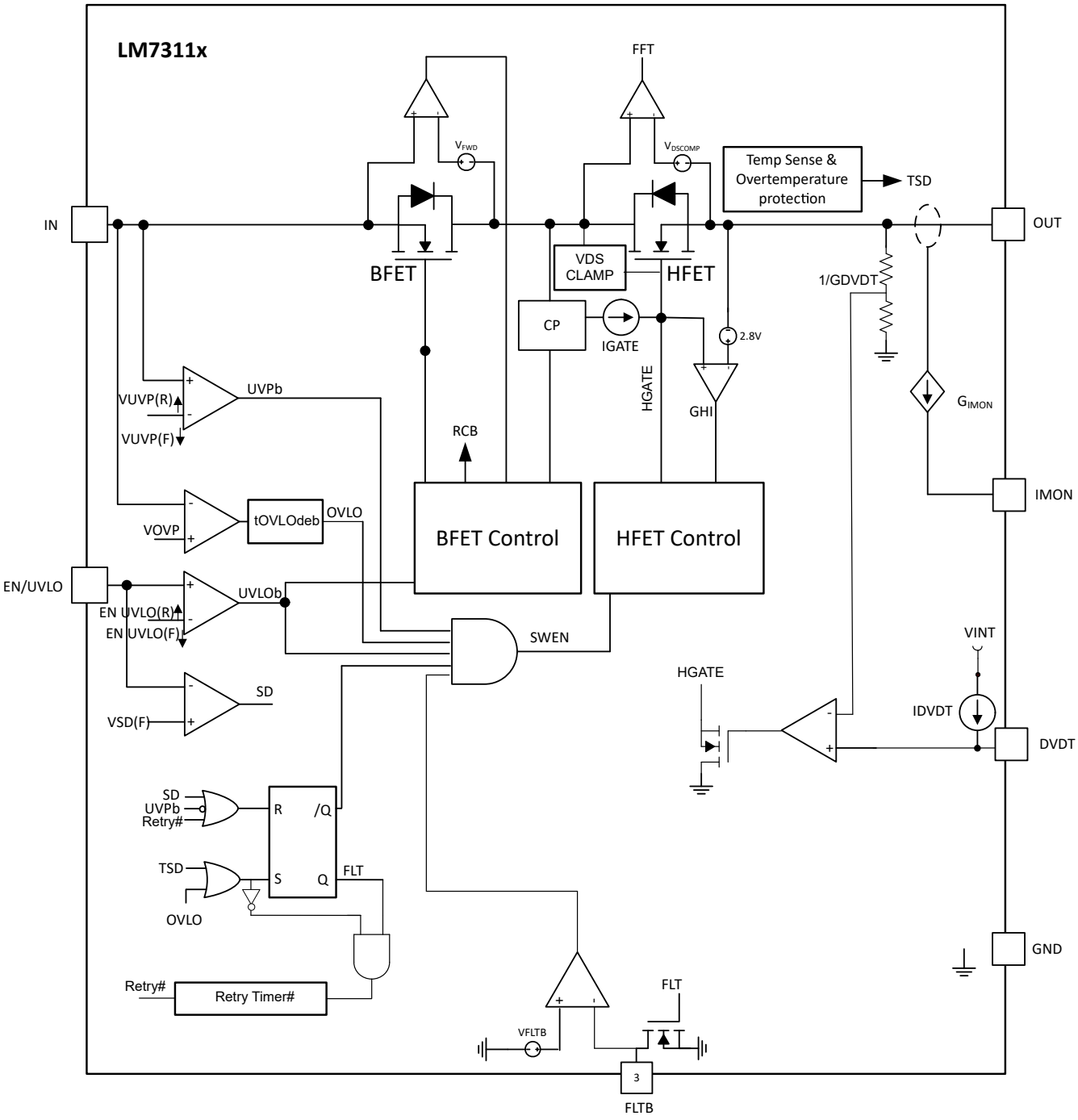
The LM7311 is an eFuse that is used to maintain safe power delivery in a system. The device starts operation by monitoring the IN bus. When the input supply voltage (VIN) exceeds the undervoltage protection threshold (VUVP), the device samples the EN/UVLO pin. A high level (> VUVLO(R)) on this pin enables the internal power path (BFET+HFET) to start conducting and allow current to flow from IN to OUT. When EN/ UVLO pin is held low (< VUVLO(F)), the internal power path is turned off.

After a successful start-up sequence, the device now actively monitors load current and input voltage, and controls the internal HFET to maintain that the fast-trip threshold (IFT) is not exceeded and overvoltage spikes are cut-off once they cross the user adjustable overvoltage lockout threshold (VOVLO). This helps to keep the system safe from harmful levels of voltage and current.

The device has integrated reverse current blocking FET (BFET) which operates like an ideal diode. The BFET is linearly regulated to maintain a small constant forward drop (VFWD) in forward conduction mode and turned off completely to block reverse current from OUT to IN if output voltage exceeds the input voltage

The device also has a built-in thermal sensor based shutdown mechanism to protect itself in case the device temperature (T_J) exceeds the recommended operating conditions.

7.2 Functional Block Diagram



only in LM7311A (Auto-Retry Variant)

Figure 7-1. LM7311x Block Diagram

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7.3 Feature Description

The LM7311 eFuse is a compact, feature rich power management device that provides detection, protection and indication in the event of system faults. .

7.3.1 Undervoltage Lockout (UVLO and UVP)

The LM7311 implements undervoltage protection on IN in case the applied voltage becomes too low for the system or device to properly operate. The undervoltage protection has a default lockout threshold of VUVP which is fixed internally. Apart from that, the UVLO comparator on the EN/UVLO pin allows the undervoltage Protection threshold to be externally adjusted to a user defined value. The Figure 7-1 and Equation 1 below show how a resistor divider can be used to set the UVLO set point for a given voltage supply

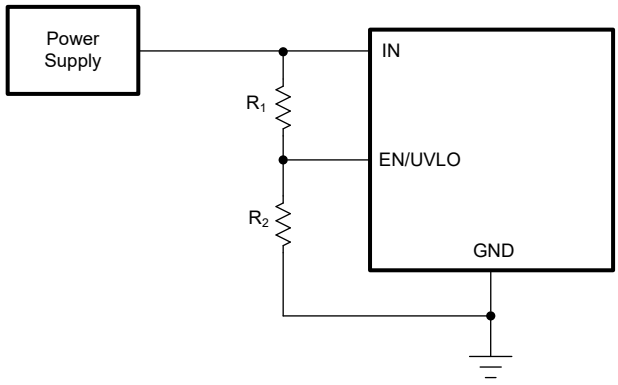

Figure 7-2. Adjustable Undervoltage Protection

$$\mathrm{VIN(UV)} = \mathrm{VUVLO(F)} \times \frac{\mathrm{R1} + \mathrm{R2}}{\mathrm{R2}} \quad (1)$$

7.3.2 Overvoltage Lockout (OVLO)

The LM7311 implements a fixed overvoltage lockout to protect the load from input overvoltage conditions. Once the voltage at the VIN pin crosses the OVLO rising threshold VOV(R), the device turns off the power to the output after tOVLOdeb debounce time.

Once the device turns off its latched off till a EN cycle is applied for it to start again

The device employs additional protection mechanism of VDS CLAMP in the event of the device VIN voltage exceeding the VDSCLAMP activation threshold. Here the device partially turns on to protect itself from VDS (VIN-VOUT) absmax violation by charging the output to VOCLAMP voltage. This protection helps the device self-protect during transient surges if the TVS diode is unable to clamp the surge below the device VDS absmax.

7.3.3 Inrush Current, Overcurrent, and Short Circuit Protection

LM7311 incorporates four mechanisms to handle overcurrent:

1. Adjustable slew rate (dVdt) for inrush current control durint start-up.
2. Fixed Current limit (I_{LIM}) during overcurrent in start-up.
3. Fixed threshold (I_{SFT}) for fast-trip response to quickly protect against hard output short-circuits during startup.
4. Fixed threshold (I_{FFT}) for fast-trip response to quickly protect against hard output short-circuits during steady-state.

7.3.3.1 Slew Rate (dVdt) and Inrush Current Control

During hot-plug events or while trying to charge a large output capacitance at start-up, there can be a large inrush current. If the inrush current is not managed properly, it can damage the input connectors and/or cause the system power supply to droop leading to unexpected restarts elsewhere in the system. The inrush current during turn on is directly proportional to the load capacitance and rising slew rate.

Equation 2 can be used to find the slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{OUT}):

$$\text{IINRUSH (mA)} = \text{COUT (µF)} \times \text{SRON (V/ms)} \quad (2)$$

A capacitor can be connected to the dVdt pin to control the rising slew rate and lower the inrush current during turn on. The required C_{dVdt} capacitance to produce a given slew rate can be calculated using the equation:

$$\text{SRON(V/ms)} = \text{GDVDT(V/V)x}\frac{\text{IDVDT(uA)}}{\text{CDVDT(uF)}} \quad (3)$$

The fastest output slew rate is achieved by leaving the dVdt pin open.

7.3.3.2 Short-Circuit Protection

During certain system faults, the current through the device can increase very rapidly. In such events, the device provides fast-trip response with a fixed thresholds I_{FFT} during steady state and I_{SFT}during start-up. Once the current exceeds the thresholds, the HFET is turned off completely within tSC. Thereafter, the devices tries to turn the HFET back on after a short de-glitch interval (30µs) in a current limited manner instead of a dVdt limited manner. This ensures that the HFET has a faster recovery after a transient overcurrent event and minimizes the output voltage droop. However, if the fault is persistent, the device stays in current limit causing the junction temperature to rise and eventually enter thermal shutdown. See Overtemperature Protection (OTP) section for details on the device response to overtemperature.

7.3.3.3 Current Limit in Start-up

The LM7311x responds to overcurrent condition in start-up by limiting the current to a fixed limit of I_{LIM} if the output current set by the DVDT capacitor exceeds I_{LIM} but stays below the I_{SFT}(2 x I_{LIM}). The current limit circuit employs a foldback mechanism. The current limit threshold in the foldback region (0V < VOUT < V_{FB}) is lower than the startup-up current limit threshold (I_{LIM}). During this period if the resulting device power dissipation results in the internal device temperature (T_J to exceed the thermal shutdown threshold(TSD), the device shuts off due to TSD fault. The FLTb pin is asserted during the TSD fault. In the latched off version it will stay latched off or restart after the fixed delay (tTSD,RST) once the device cools down sufficiently below the TSD Hysterisis(TSDHYS) level.

7.3.4 Analog Load Current Monitor

The device allows the system to accurately monitor the output load current by providing an analog current sense output on the IMON pin which is proportional to the current through the FET. The user can sense the voltage (VIMON) across the RIMON to get a measure of the output load current.

$$\text{ILOAD (A)} = \frac{\text{VIMON (µV)}}{\text{RILM (Ω)} \times \text{GIMON (µA/A)}} \quad (4)$$

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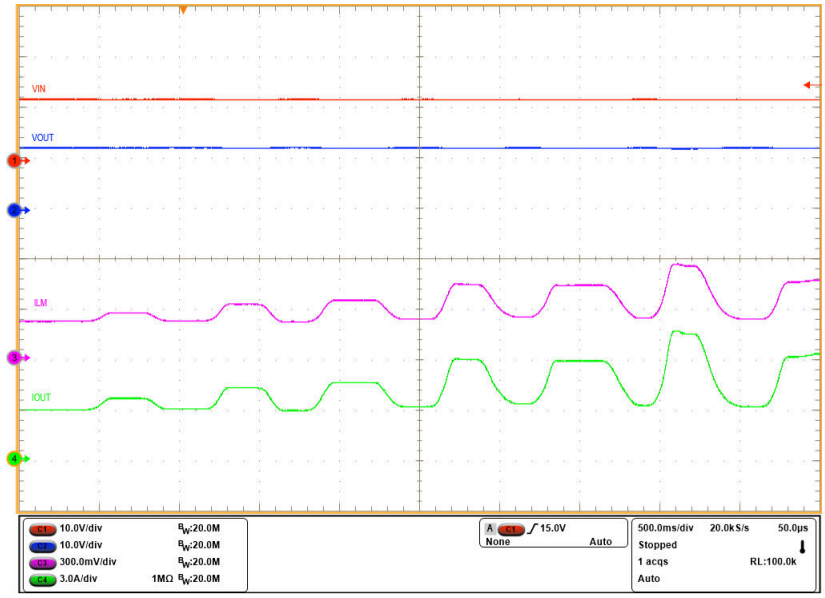

Figure 7-3. Analog Load Current Monitor Response

7.3.5 Reverse Current Protection

The LM73100 functions like an ideal diode and blocks reverse current flow from OUT to IN under all conditions. The device has integrated back-to-back MOSFETs connected in a common drain configuration. The voltage drop between the IN and OUT pins is constantly monitored and the gate drive of the blocking FET (BFET) is adjusted as needed to regulate the forward voltage drop at VFWD. This closed loop regulation scheme enables graceful turn off of the MOSFET during a reverse current event and ensures there's no DC reverse current flow.

The device also uses a conventional comparator (VREVTH) based reverse blocking mechanism to provide fast response to transient reverse currents.Once the device enters reverse current blocking condition, it waits for the (VIN - VOUT) forward drop to exceed the VFWDTH before it performs a fast recovery to reach full forward conduction state. This provides sufficient hysterisis to prevent supply noise or ripple from affecting the reverse current blocking response. The recovery from reverse current blocking is very fast (tSWRCB). This ensures minimum supply droop which is helpful in applications such as power MUX/ORing

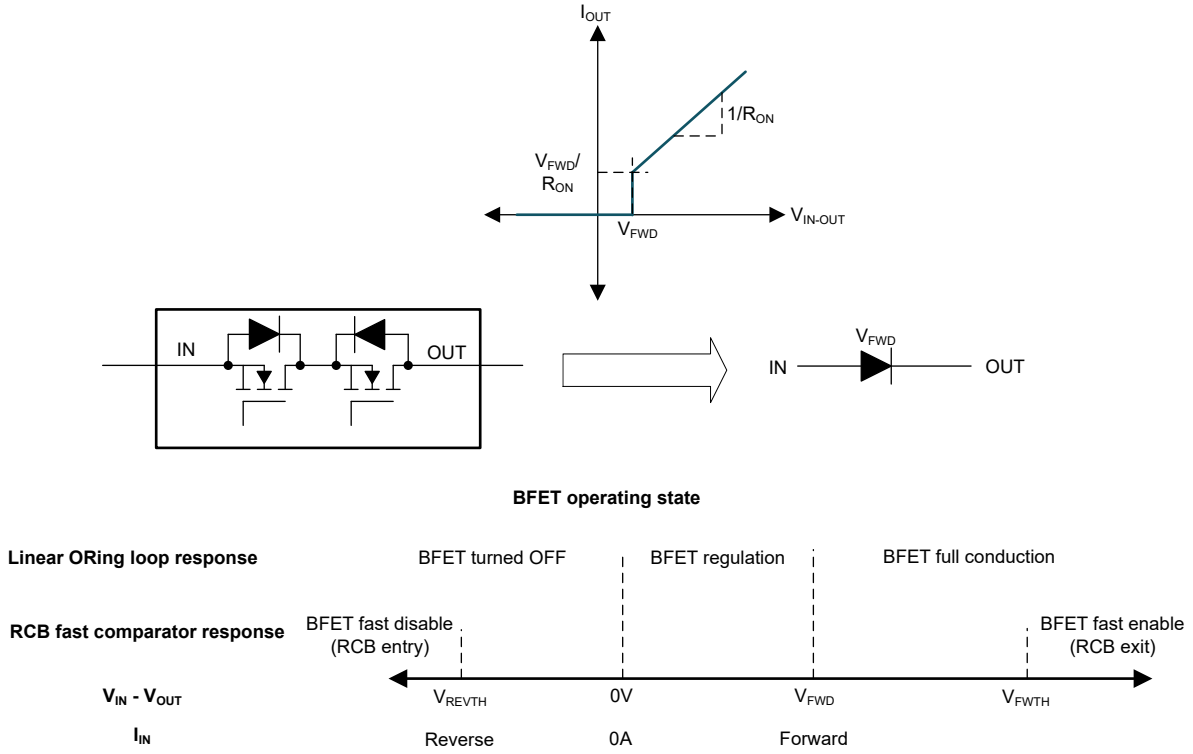

Figure 7-4. Reverse Current Blocking Response

When the input supply droops or gets disconnected while the output storage element (bulk capacitor or super capacitor) is charged to the full voltage, the linear ORing scheme minimizes the self-discharge from OUT to IN. This ensures maximum holdup time for the output storage element in critical power back-up applications.

It also prevents incorrect supply presence indication in applications which sense the input voltage to detect if the supply is connected.

7.3.6 Overtemperature Protection (OTP)

The LM73100 monitors the internal die temperature (TJ) at all times and shuts down the part as soon as the temperature exceeds a safe operating level (TSD) thereby protecting the device from damage. The LM7311A (Auto retry) does not turn back on until the junction cools down sufficiently, that is the die temperature falls below (TSD - TSDHYS).

When the LM7311L (latch-off variant) detects thermal overload, the device shuts down and remain latched-off until the device is power cycled or re-enabled. When the LM7311A (auto-retry variant) detects thermal overload, the device remain off until the device has cooled down by TSD_{HYS}. Thereafter, the device remains off for an additional delay of t_{RST} after which the device automatically retries to turn on if the device is still enabled.

Table 7-1. Thermal Shutdown

Device	Enter TSD	Exit TSD
LM7311L (Latch-Off)	$T_J \geq$ TSD	$T_J <$ TSD – TSD_{HYS} V_{IN} cycled to 0 V and then above $V_{UVP(R)}$ OR EN/UVLO toggled below $V_{SD(F)}$
LM7311A (Auto-Retry)	$T_J \geq$ TSD	$T_J <$ TSD – TSD_{HYS} V_{IN} cycled to 0 V and then above $V_{UVP(R)}$ OR EN/UVLO toggled below $V_{SD(F)}$ OR t_{RST} timer expired

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7.3.7 Fault Response and Indication ($\overline{FLT}$)

The following table summarizes the device response to various fault conditions.

Table 7-2. Fault Summary

Event	Protection Response	Fault Latched Internally	$\overline{FLT}$ Pin Status	Device Behaviour after Fault is removed
Overtemperature	Shutdown after TSD threshold	Y	L	Auto Retry(LM7311A)
				Latch off (LM7311L)
Undervoltage (UVP or UVLO) on VIN or EN	Shutdown	N	H	Restart
Input Overvoltage	Shutdown after T_{OVP}	Y	L	Latch off
Output Short-Circuit to GND	Circuit Breaker followed by Current Limit	N	H	Auto Retry.
		Y after TSD	L after TSD	If TSD is hit during Current limit device behaviour is Auto retry (LM7311A) or Latch off (LM7311L) depending on the variant
Reverse Current ((V_{OUT} - V_{IN}) > V_{REVTH})	Reverse Current Blocking	N	H	Restart

Faults which are not latched internally are automatically cleared once the trigger condition goes away and thereafter the device recovers without any external intervention. Faults which are latched internally can be cleared either by power cycling the part (pulling VIN to 0 V and then above VUVP(R)) or by pulling the EN/UVLO pin voltage below VSD(F)

7.4 Device Functional Modes

The device has one mode of operation that applies when operated within the Recommended Operating Conditions

ADVANCE INFORMATION

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LM7311 is an 3.5 V to 23 V, 5-A eFuse with reverse current blocking ,that is typically used for power rail protection applications. The LM7311 operates from 3.5 V to 23 V with adjustable undervoltage protection and fixed overvoltage protection of 24V. The LM7311 provides ability to control inrush current and protection against reverse current conditions. The LM7311 can be used in a variety of systems such as adapter or charger input protection, USB PD protection in smartphone, tablet, PC, notebook, monitor, dock, server and PC motherboard, add-on cards, enterprise storage – RAID/HBA/SAN/eSSD, power MUXing/ORing. The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirement.

8.2 Single Device, Self-Controlled

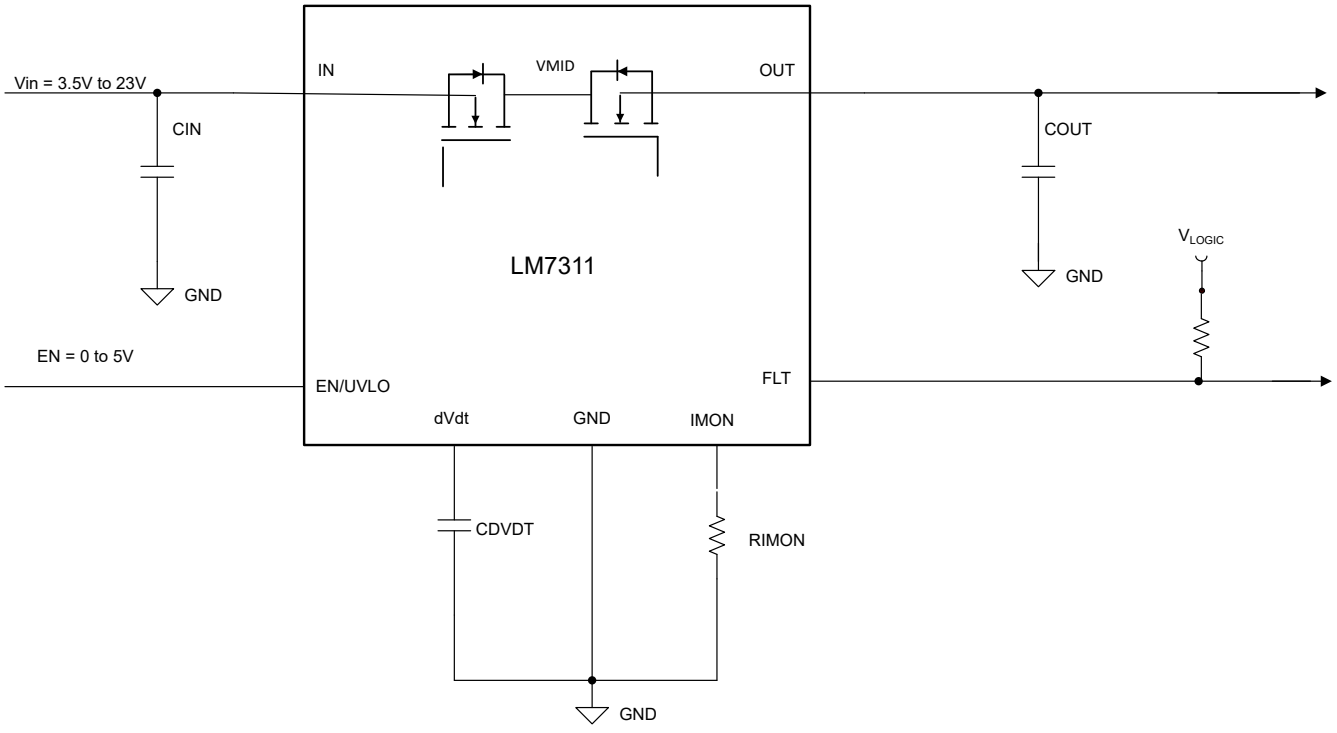


Figure 8-1. Single Device, Self-Controlled

Other variations:

In a Host MCU controlled system, EN/UVLO can also be driven from the host GPIO to control the device.

IMON pin can be connected to the MCU ADC input for current monitoring purpose.

Note

It is recommended to keep parasitic capacitance on IMON pin below 50 pF to ensure stable operation.

ADVANCE INFORMATION

8.3 Typical Application

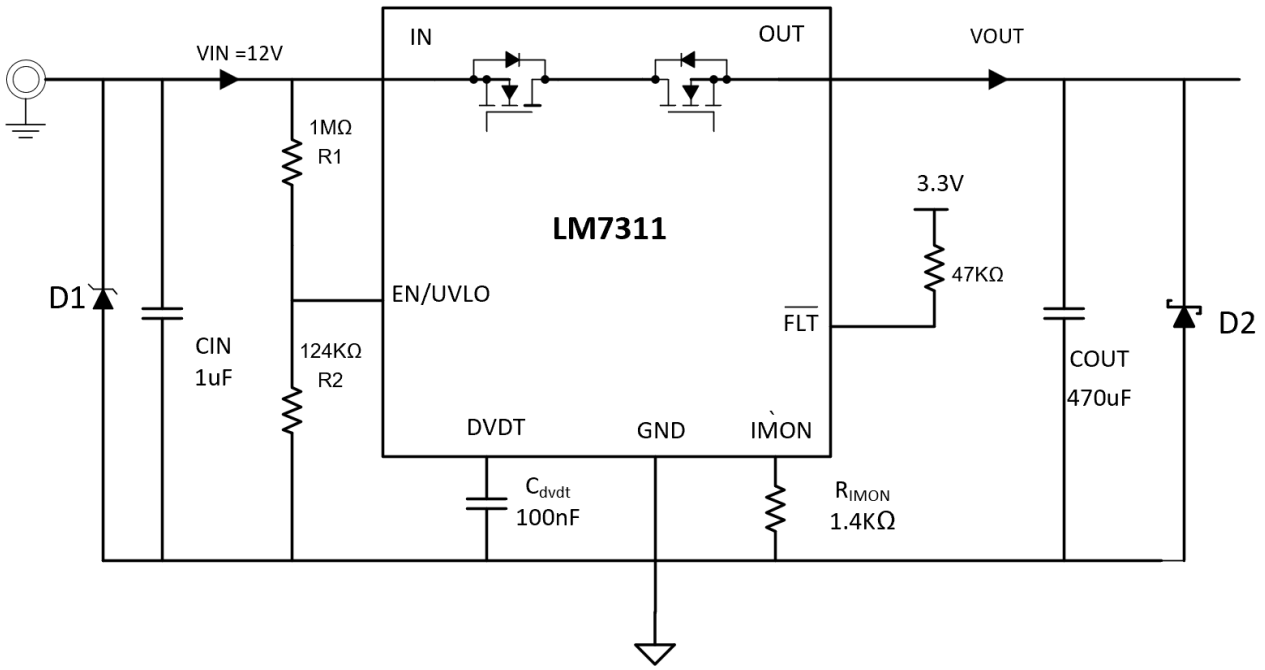


Figure 8-2. AC-DC Adapter Powered System - Barrel Jack Input Protection

* Optional circuit components needed for transient protection depending on input and output inductance. Please refer to *Transient Protection* section for detai

8.3.1 Design Requirements

Table 8-1. Design Parameters

PARAMETER	VALUE
Bus voltage during charging (V_{IN})	12V
Fixed overvoltage protection threshold during charging ($VIN_{(OV)}$)	24 V
Undervoltage protection threshold during charging ($VIN_{(UV)}$)	10.8V
Max continuous charging current	5 A
Output capacitance (C_{OUT})	470µF
Output rise time (t_R)	24ms
Analog load current monitor voltage range (VIMONmax)	1V

8.3.2 Detailed Design Procedure

8.3.2.1 Setting Undervoltage Threshold

The supply undervoltage threshold is set using the resistors, R1 and R2, whose values can be calculated as:

$$V_{IN(UV)} = \frac{V_{UVLO(R)} \times (R_1 + R_2)}{R_2} \quad (5)$$

Where $V_{UVLO(R)}$ is the UVLO rising threshold. Because R1, R2 leak the current from input supply V_{IN}, these resistors must be selected based on the acceptable leakage current from input power supply V_{IN}. The current drawn by R1, R2 from the power supply is IR12 = V_{IN} / (R1 + R2). However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, IR12, must be chosen to be 20 times greater than the leakage current expected on the UVLO pin.

From the device electrical specifications, UVLO leakage current is 0.1 µA (maximum), $V_{UV(R)}$ = 1.2 V. From design requirements, $V_{IN(UV)}$ = 10.8V. To solve the equation, first choose the value of R1 = 1MΩ and use the above equation to solve for R2 = 125kΩ.

Using the closest standard 1% resistor values, we get R1 = 1MΩ, R2 = 124kΩ.

8.3.2.2 Setting Output Voltage Rise Time (t_R)

For a successful design, the junction temperature of device must be kept below the absolute maximum rating during both dynamic (start-up) and steady-state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and inrush current limit required with system capacitance to avoid thermal shutdown during start-up.

The slew rate (SR) needed to achieve the desired output rise time can be calculated as:

$$\text{SR (V/ms)} = \frac{\text{VIN (V)}}{\text{tR (ms)}} = \frac{12\ \text{V}}{24\ \ \text{ms}} = 0.5\ \ \text{V/ms} \tag{6}$$

The C_{dVdt} needed to achieve this slew rate can be calculated as:

$$\text{CdVdt (nF)} = \frac{55}{\text{SR (V/ms)}} = \frac{55}{0.5} = 110\ \text{nF} \tag{7}$$

Choose the nearest standard capacitor value as 110nF.

For this slew rate, the inrush current can be calculated as:

$$\text{IINRUSH (mA)} = \text{SR (V/ms)} \times \text{COUT (µF)} = 0.5 \times 470 = 235\ \text{mA} \tag{8}$$

The average power dissipation inside the part during inrush can be calculated as:

$$\text{PDINRUSH (W)} = \frac{\text{IINRUSH (A)} \times \text{VIN (V)}}{2} = \frac{0.235 \times 12}{2} = 1.41\text{W} \tag{9}$$

For the given power dissipation, the thermal shutdown time of the device must be greater than the ramp-up time t_R to avoid start-up failure.

8.3.2.3 Setting Analog Current Monitor Voltage (IMON) Range

The analog current monitor voltage range can be set using the RIMON resistor whose value can be calculated as:

$$R_{IMON} = \frac{V_{IMONmax}(V) \times 10^{(6)}}{I_{OUTmax}(A) \times G_{IMON}(\mu A/A)} = \frac{1 \times 10^{(6)}}{5 \times 142.8} = 1400.5\Omega \tag{10}$$

Choose nearest 1% standard resistor value as 1430Ω.

ADVANCE INFORMATION

8.3.2.4

8.3.3 Application Curves

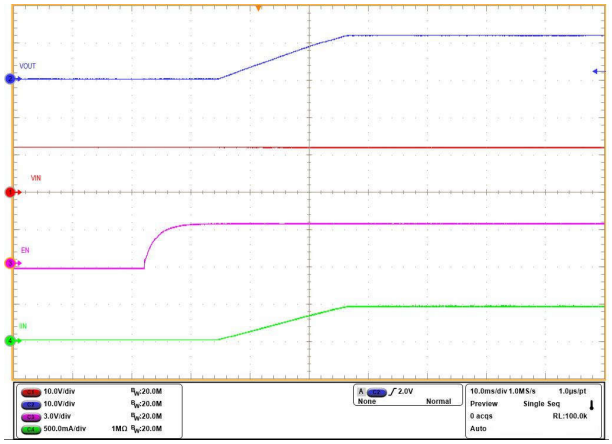


Figure 8-3. Power Up

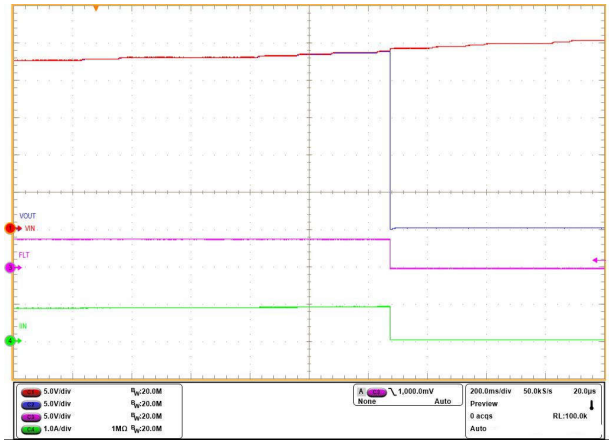


Figure 8-4. Overvoltage Protection

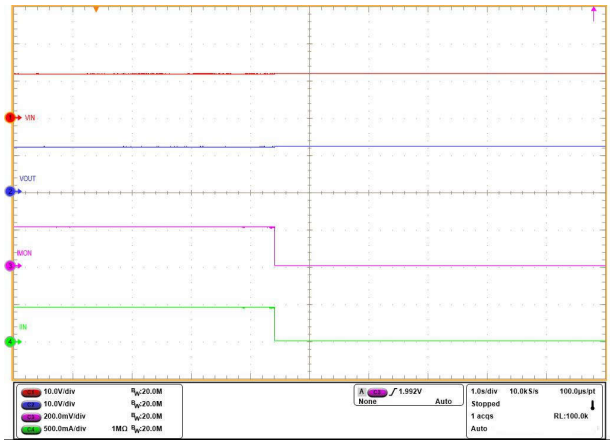


Figure 8-5. Analog load current monitor output

8.4 Active ORing

A typical redundant power supply configuration is shown in Figure 8-6below. Schottky ORing diodes have been popular for connecting parallel power supplies, such as parallel operation of wall adapter with a battery or a hold-up storage capacitor. The disadvantage of using ORing diodes is high voltage drop and associated power loss. The LM7311 with integrated, low-ohmic, back-to-back FETs provide a simple and efficient Figure 8-6 shows the Active ORing implementation using LM7311 devices.

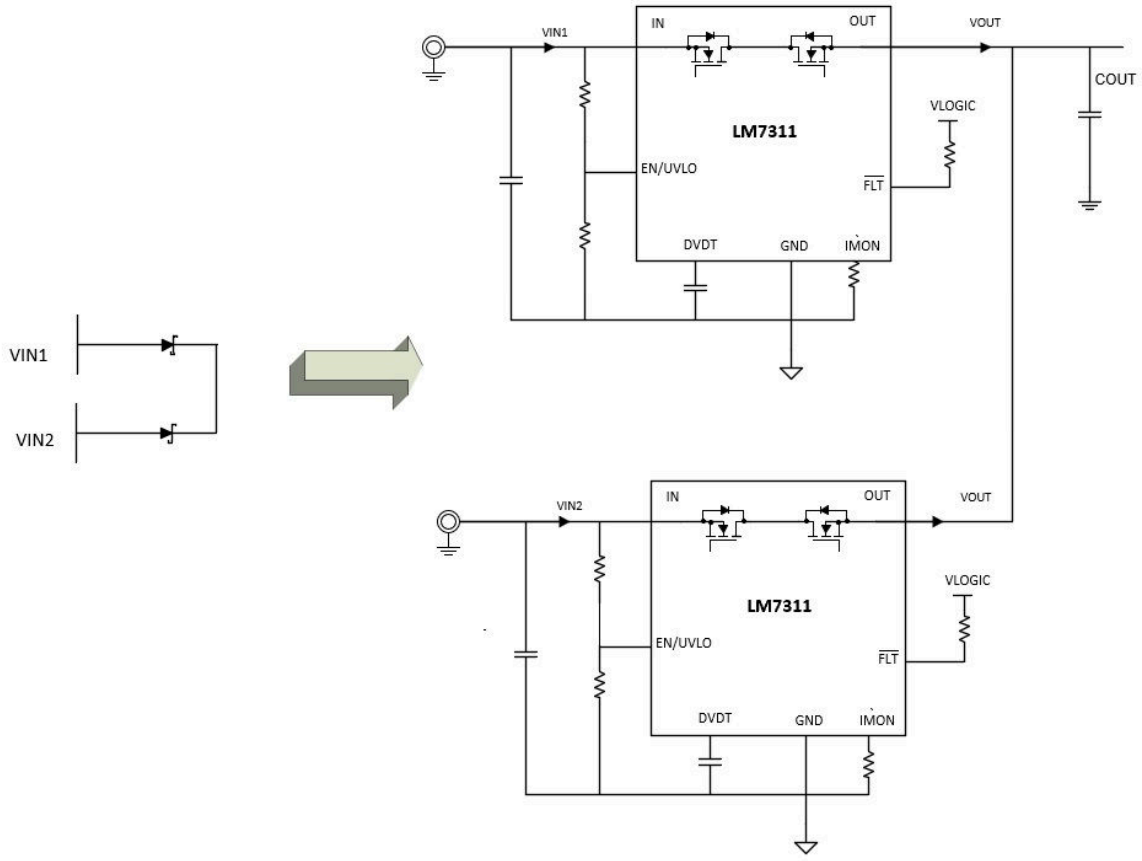


Figure 8-6. Two Devices, Active ORing Configuration

The linear ORing mechanism in LM7311 maintain that there's no reverse current flowing from one power source to the other during fast or slow ramp of either supply.

The following waveform illustrates the active ORing behavior when the supply rails are being ramped up sequentially.

Figure 8-7. Active ORing Response

When the bus voltages (IN1 and IN2) are matched, device in each path sees a forward voltage drop and is ON delivering the load current. During this period, current is shared between the rails in the ratio of differential voltage drop across each device.

In addition to supply ORing, the devices protect the system from overvoltage, excessive inrush current, overload and short-circuit faults at all times.

Note

ORing can be done either between two similar rails or between dissimilar rails. For ORing cases with skewed voltage combinations, the dVdt pin capacitor rating must be chosen based on the highest of the 2 supplies. Refer to Recommended Operating Conditions table for more details.

ADVANCE INFORMATION

8.5 Power Supply Recommendations

The LM7311 devices are designed for a supply voltage range of 3.5 V ≤ V_{IN} or V_{OUT} ≤ 23 V. An input ceramic bypass capacitor higher than 0.1 µF is recommended if the input supply is located more than a few inches from the device. The power supply must be rated higher than the set current limit to avoid voltage droops during overcurrent and short-circuit conditions.

8.5.1 Transient Protection

In the case of a short-circuit and overload current limit when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Connect a Schottky diode from the OUT pin ground to absorb negative spikes.
- Connect a low ESR capacitor larger than 1 µF at the OUT pin very close to the device.
- Use a low-value ceramic capacitor C_{IN} = 1 µF to absorb the energy and dampen the transients. The capacitor voltage rating should be atleast twice the input supply voltage to be able to withstand the positive voltage excursion during inductive ringing.

  The approximate value of input capacitance can be estimated with the equation:

$$\mathrm{VSPIKE(ABSOLUTE)} = \mathrm{VIN} + \mathrm{ILOAD} \times \sqrt{\frac{\mathrm{LIN}}{\mathrm{CIN}}} \tag{11}$$

  where

  – V_{IN} is the nominal supply voltage.
  – • I_{LOAD} is the load current.
  – L_{IN} equals the effective inductance seen looking into the source.
  – C_{IN} is the capacitance present at the input.
- Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. In some cases, even if the maximum amplitude of the transients is below the absolute maximum rating of the device, a TVS can help to absorb the excessive energy dump and prevent it from creating very fast transient voltages on the input supply pin of the IC, which can couple to the internal control circuits and cause unexpected behavior.
- For applications such as USB-C ports where a powered cable can be plugged to the output of the device, there could be excess voltage stress from OUT to IN which exceeds the absolute maximum rating of the device. It's recommended to add a TVS diode from OUT to IN to clamp the voltage to a safe level.

The circuit implementation with optional protection components is shown in Figure 8-8.

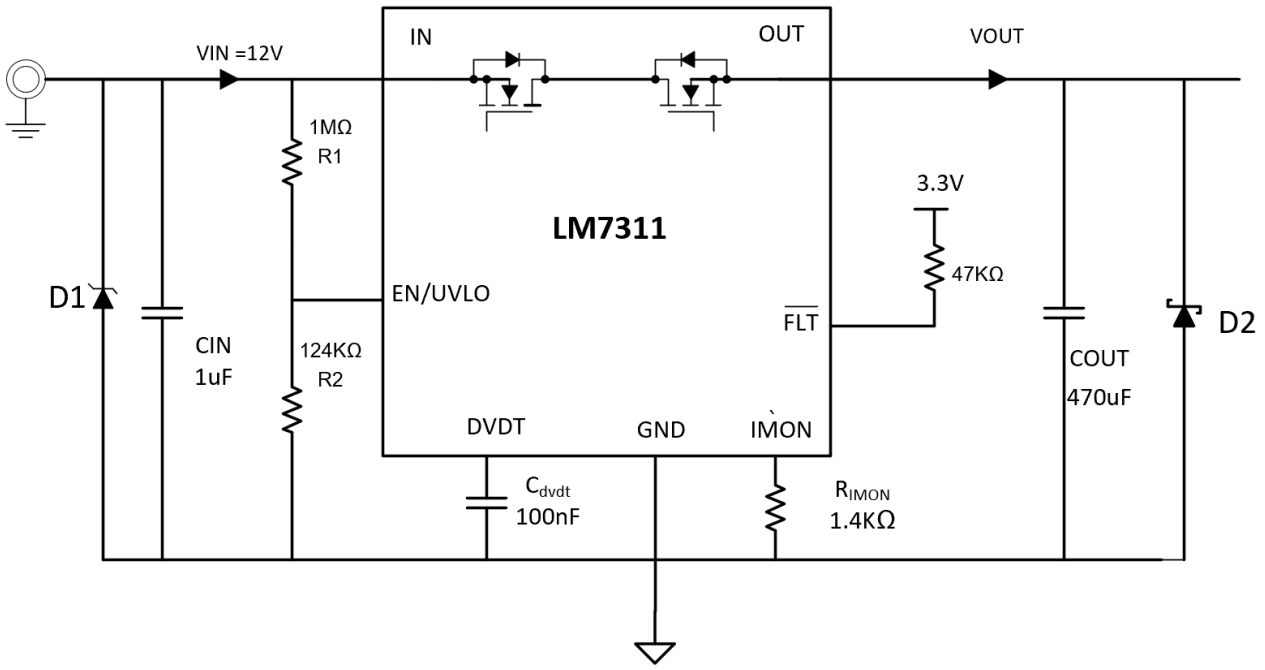


Figure 8-8. Circuit Implementation with Optional Protection Components

8.5.2 Output Short-Circuit Measurements

Obtaining repeatable and similar short-circuit testing results is difficult. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because the short microscopically bounces and arcs. Maintain that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

8.6 Layout

8.6.1 Layout Guidelines

- For all applications, a ceramic decoupling capacitor of 0.1 µF or greater is recommended between the IN terminal and GND terminal.
- The desired placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.

ADVANCE INFORMATION

- The GND terminal must be tied to the PCB ground plane at the terminal of the IC with the shortest possible trace. The PCB ground must be a copper plane or island on the board. TI recommends to have a separate ground plane island for the eFuse. This plane does not carry any high currents and serves as a quiet ground reference for all the critical analog signals of the eFuse. The device ground plane must be connected to the system power ground plane using a star connection.
- The IN and OUT pads are used for heat dissipation. Connect to as much copper area on top and bottom PCB layers using as possible with thermal vias. The vias under the device also help to minimize the voltage gradient across the IN and OUT pads and distribute current uniformly through the device, which is essential to achieve the best on-resistance and current sense accuracy.
- Locate the following support components close to the connection pins:
  - C_{dVdT}
  - Resistors for the EN/UVLO pin
- Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for C_{dVdt} component to the device must be as short as possible to reduce parasitic effects on the soft start timing. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device the diodes+ are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads. TI also recommends to add a ceramic decoupling capacitor of 1 µF or greater between OUT and GND. These components must be physically close to the OUT pins. Care must be taken to minimize the loop area formed by the Schottky diode/bypass-capacitor connection, the OUT pin and the GND terminal of the IC.

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- LM7311 EVM User guide

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2026	*	Initial Release

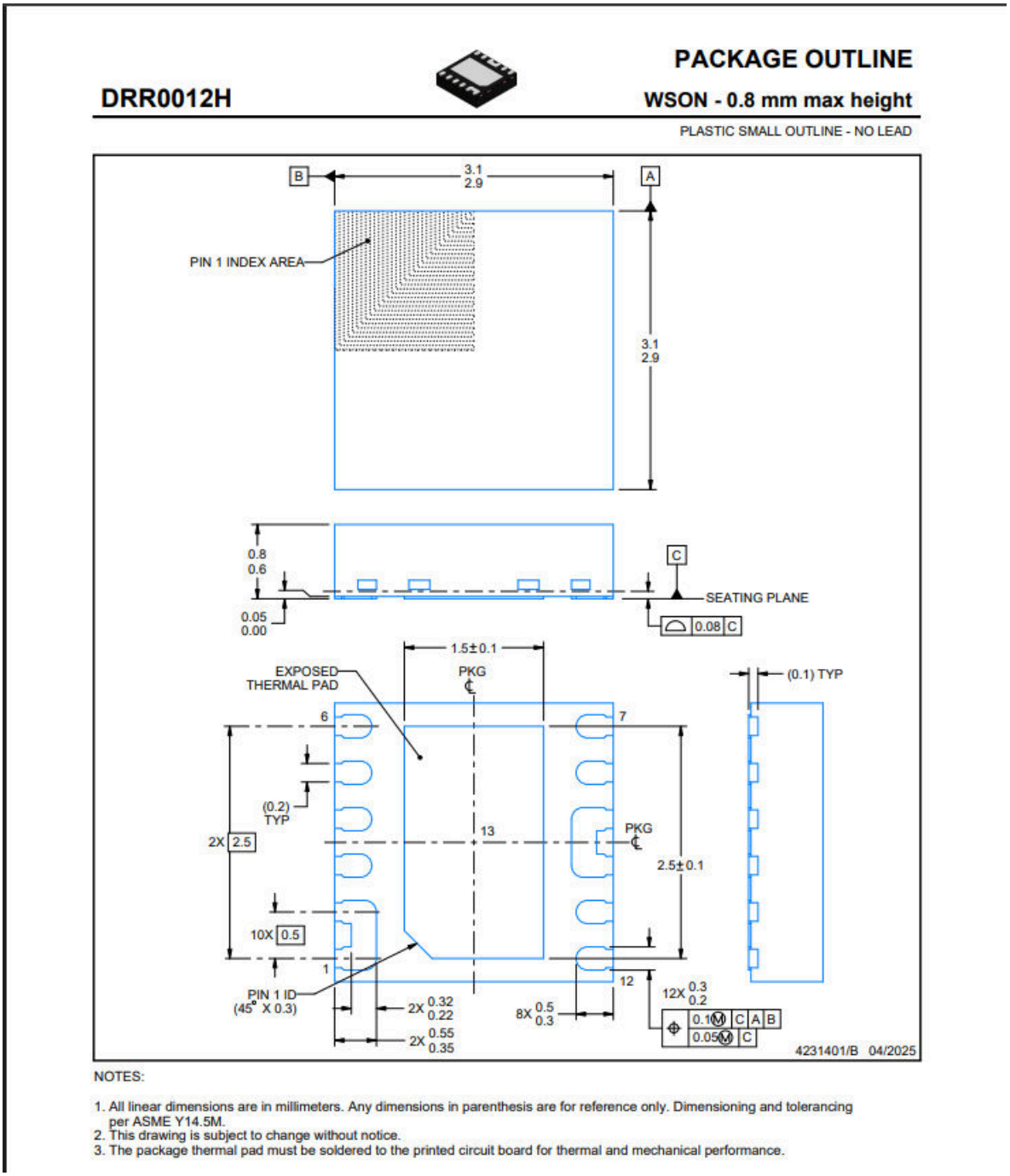
ADVANCE INFORMATION

ADVANCE INFORMATION

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Reference

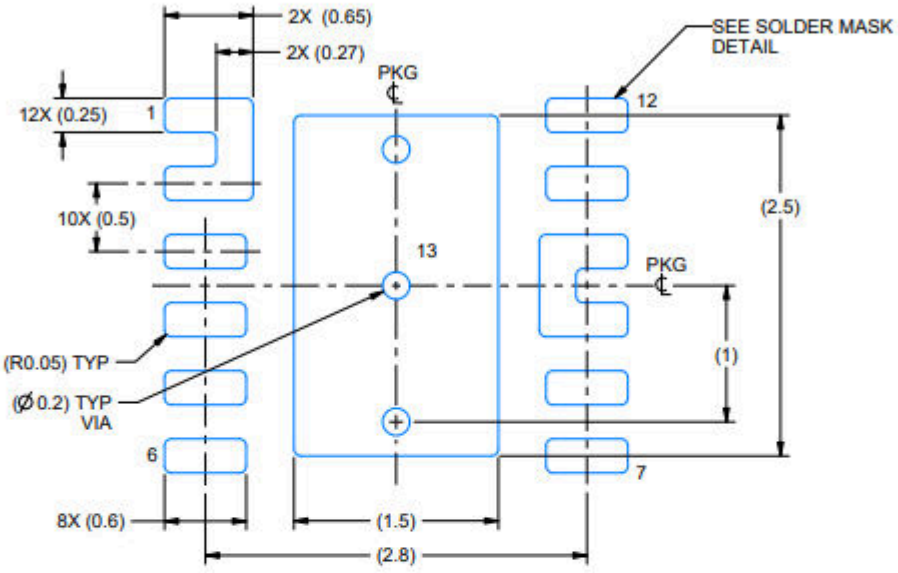


EXAMPLE BOARD LAYOUT

DRR0012H

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

SOLDER MASK DETAILS

4231401/B 04/2025

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

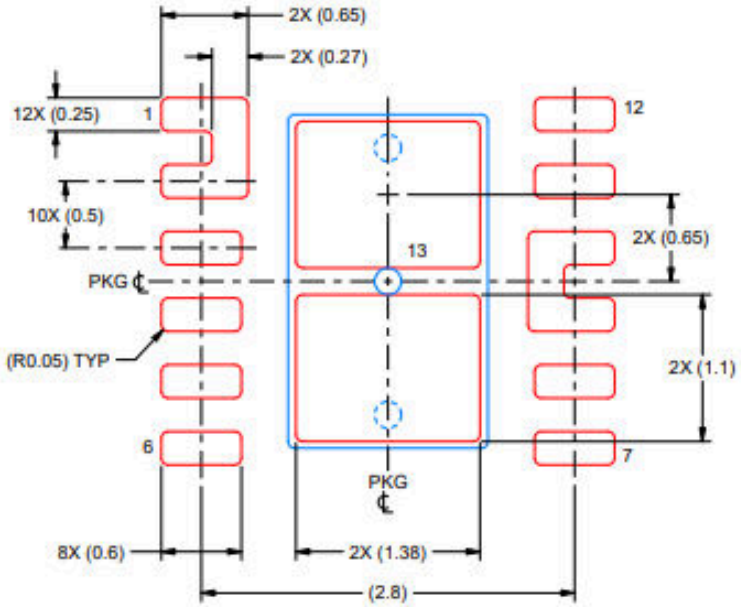
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DRR0012H — **WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 13
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4231401/B 04/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

11.2 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)	
PLM7311A00DRRR	PREVIEW	WSON	DRR	12	-	RoHS & Green	Call TI	Call TI	–40 to 125	PLM7311	
LM7311A00DRRR	PREVIEW	WSON	DRR	12	-	RoHS & Green	Call TI	Call TI	-40 to 125	LM7311	
PLM7311L00DRRR	PREVIEW	WSON	DRR	12	-	RoHS & Green	Call TI	Call TI	–40 to 125	PLM7311	
LM7311L00DRRR	PREVIEW	WSON	DRR	12	-	RoHS & Green	Call TI	Call TI	-40 to 125	LM7311	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

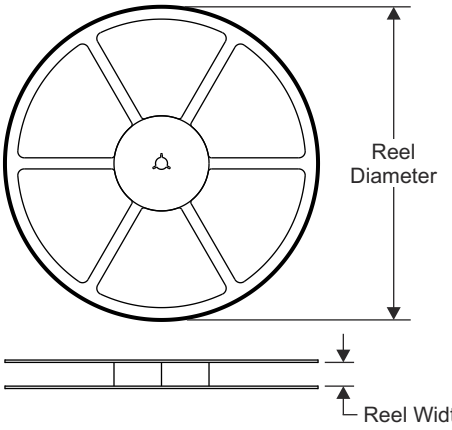
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

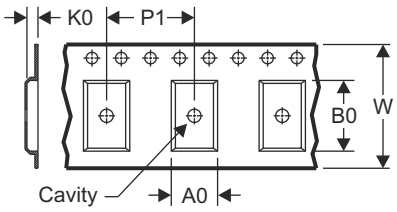
ADVANCE INFORMATION

11.3 Tape and Reel Information

REEL DIMENSIONS

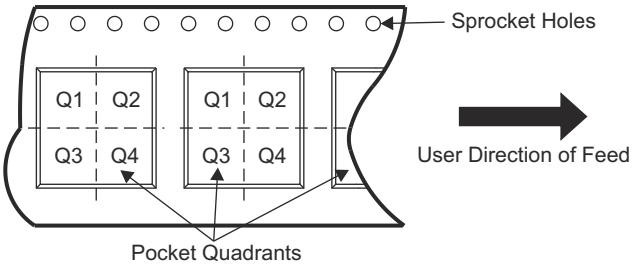


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

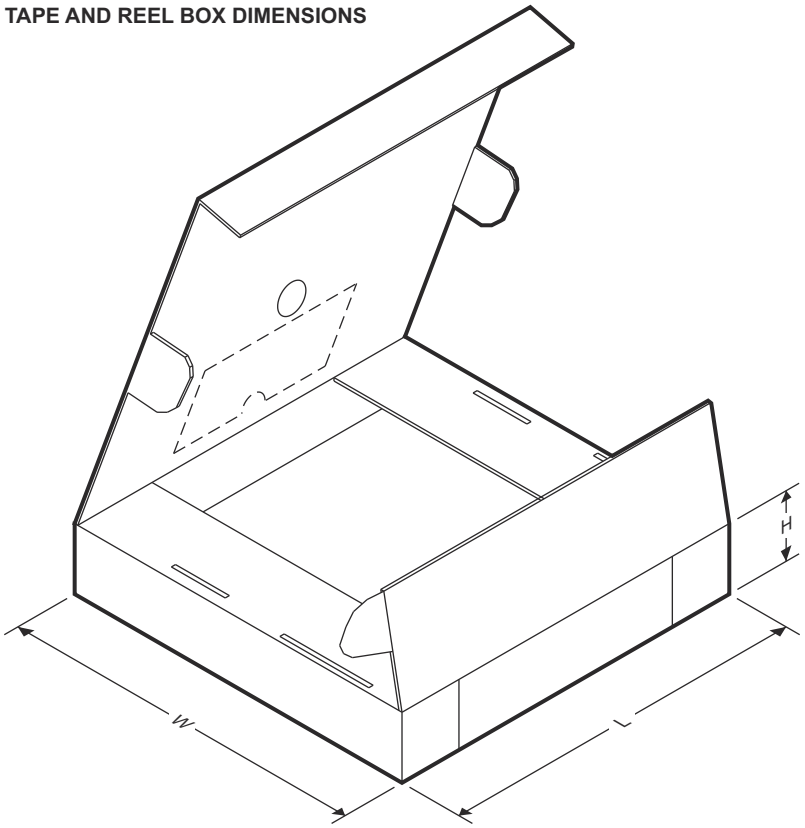
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PLM7311A00DRR	WSON	DRR	12	3000	330	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM7311A00DRR	WSON	DRR	12	3000	330	12.4	3.3	3.3	1.1	8.0	12.0	Q2
PLM7311L00DRR	WSON	DRR	12	3000	330	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM7311L00DRR	WSON	DRR	12	3000	330	12.4	3.3	3.3	1.1	8.0	12.0	Q2

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PLM7311DRRR	Active	Preproduction	WSON (DRR) | 12	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

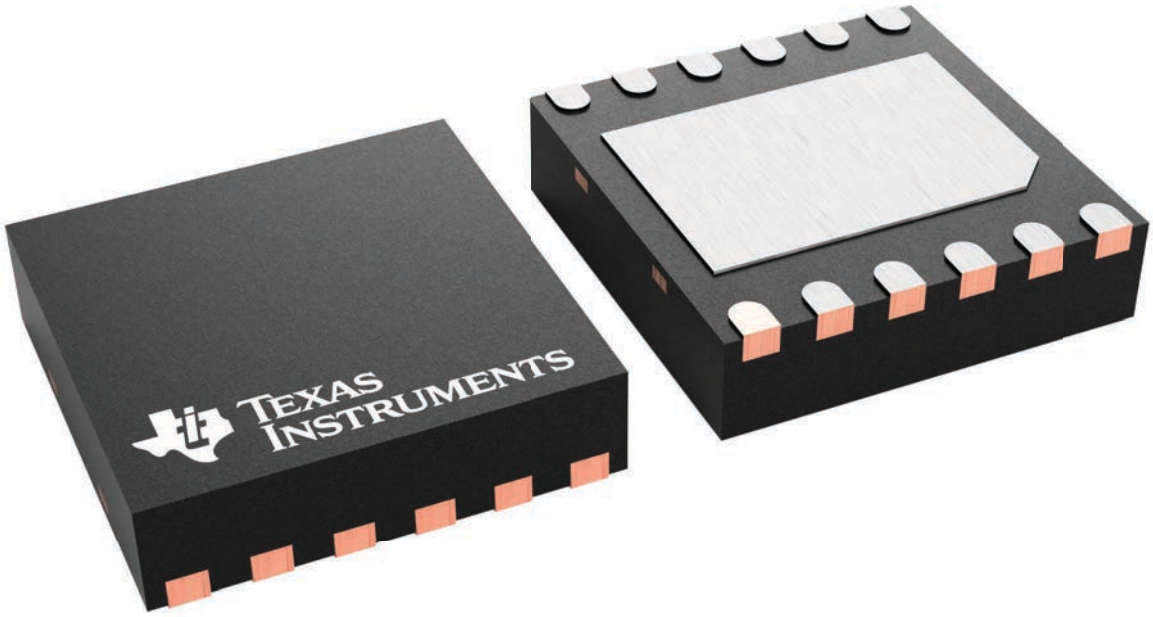
DRR 12

WSON - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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