LM7332 Dual Rail-to-Rail Input and Output 30V, Wide Voltage Range, High Output, Operational Amplifier

1 Features

- V_S = ±15V, T_A = 25°C, Typical Values Unless Specified
- Wide Supply Voltage Range: 2.7V to 32V
- Wide Input Common Mode Voltage: 0.3V Beyond Rails
- Output Short Circuit Current: >100mA
- GBWP: 24MHz
- Slew Rate: 35V/µs
- Capacitive Load Tolerance Unlimited
- Total Supply Current: 2.7mA
- Temperature Range: −40°C to +125°C

2 Applications

- MOSFET and Power Transistor Driver
- Replaces Discrete Transistors in High Current Output Circuits
- Instrumentation 4mA to 20mA Current Loops
- Analog Data Transmission
- Multiple Voltage Power Supplies and Battery Chargers
- High-Side and Low-Side Current Sensing
- Bridge and Sensor Driving
- Digital-to-Analog Converter Output

3 Description

The LM7332 device is a dual rail-to-rail input and output amplifier with a wide operating temperature range (−40°C to +125°C) that meets the needs of automotive, industrial, and power supply applications. The LM7332 has an output current of 125mA, which is higher than that of most monolithic operational amplifiers. Circuit designs with high output current requirements often require discrete transistors because many operational amplifiers have low current output. The LM7332 has enough current output to drive many loads directly, saving the cost and space of the discrete transistors.

The exceptionally wide operating supply voltage range of 2.7V to 32V alleviates any concerns over functionality under extreme conditions and offers flexibility of use in a multitude of applications. Most parameters of this device are insensitive to power supply variations; this design enhancement is another step in simplifying usage. Greater than rail-to-rail input common mode voltage range allows operation in many applications, including high-side and low-side sensing, without exceeding the input range.

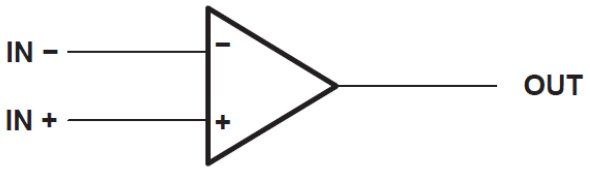
The LM7332 can drive unlimited capacitive loads without oscillations.

The LM7332 is offered in the 8-pin VSSOP and SOIC packages.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LM7332	DGK (VSSOP, 8)	3.00mm × 3.00mm
	D (SOIC, 8)	3.91mm × 4.90mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Symbol (each amplifier)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

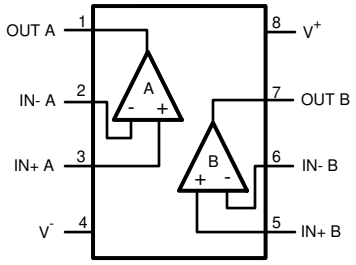


Figure 4-1. DGK Package 8-Pin VSSOP Top View

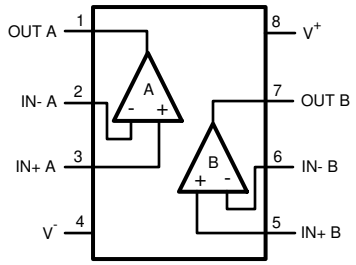


Figure 4-2. D Package 8-Pin SOIC Top View

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IN+ A	3	I	Non-inverting Input for Amplifier A
IN– A	2	I	Inverting Input for Amplifier A
IN+ B	5	I	Non-inverting Input for Amplifier B
IN– B	6	I	Inverting Input for Amplifier AB
OUT A	1	O	Output for Amplifier A
OUT B	7	O	Output for Amplifier B
V^+	8	P	Positive Supply
V^-	4	P	Negative Supply

(1) I = input, O = output, P = power

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5 Specifications

5.1 Absolute Maximum Ratings

Over operating ambient temperature range(1)

		MIN	MAX	UNIT
V_{IN} differential (5)			±10	V
Output short-circuit duration (2) (3)		Continuous		
Supply voltage ($V_S = V^+ – V^–$)			33	V
Voltage at input/output pins (6)		($V^–$) − 0.5V	(V^+) + 0.5V	V
Junction temperature(4)			150	°C
Soldering information	Infrared or convection (20 sec.)		235	°C
	Wave soldering (10 sec.)		260	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(3) Short-circuit test is a momentary test. Output short circuit duration is infinite for $V_S \leq 6V$ at room temperature and below. For $V_S > 6V$, allowable short circuit duration is 1.5ms.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.
(5) Input pins are connected by back-to-back diodes for input protection. If the differential input voltage may exceed 0.5V, limit the input current to 10mA or less.
(6) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) (2)	±2000	V
		Machine model (MM)	±200	
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(3)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22A115A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22C101C (ESD FICDM std. of JEDEC).
(3) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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5.3 Thermal Information

THERMAL METRIC[1]		LM7332		UNIT
		DGK (VSSOP)	D (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance [2]	169.6	124.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.6	67.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.2	68.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.0	19.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	89.7	67.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

5.4 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply voltage ($V_S = V^+ – V^–$)	2.7	32	V
Temperature range[2]	−40	125	°C

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5.5 Electrical Characteristics

For V_S = (V+) – (V–) = 2.7V to 32V (±1.35V to ±16V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
V_{OS}	Input offset voltage	V_{CM} = V−		−4	±0.35	4	mV
V_{OS}	Input offset voltage temperature drift(4)	V_{CM} = V−			±2.5		µV/°C
I_B	Input bias current(5)	V_{CM} = V−	T_A = –40°C to +125°C	−2	±0.4	2	µA
I_{OS}	Input offset current	V_{CM} = V−	T_A = –40°C to +125°C		7	250	nA
CMRR	Common-mode rejection ratio	V_S = 32V, V– < V_{CM} < (V+) – 2V (Main Input Pair)	T_A = –40°C to 125°C	109	125		dB
		V_S = 5V, V– < V_{CM} < (V+) – 2V (Main Input Pair)(1)	T_A = –40°C to 125°C	93	111		
		V_S = 2.7V, V– < V_{CM} < (V+) – 2V (Main Input Pair)	T_A = –40°C to 125°C		114		
		V_S = 2.7 – 32V, (V+) – 1V < V_{CM} < V+ (Aux Input Pair)	T_A = –40°C to 125°C		77		
		(V+) – 2V < V_{CM} < (V+) – 1V	T_A = –40°C to 125°C	See Figure 5-22			
PSRR	Power supply rejection ration	V_{CM} = V–, V_S = 5V to 32V	T_A = –40°C to 125°C	78	100		dB
CMVR	Input common-mode voltage range			(V−) − 0.1		(V+) + 0.1	V
A_{OL}	Open-loop voltage gain	V_S = 32V, V_{CM} = V_S / 2, (V–) + 1V < V_O < (V+) – 1V		72	87		dB
			T_A = –40°C to 125°C	70	87		
		V_S = 5V, V_{CM} = V_S / 2, (V–) + 1V < V_O < (V+) – 1V(1)		72	80		
			T_A = –40°C to 125°C	70	80		
		V_S = 2.7V, V_{CM} = V_S / 2, (V–) + 1V < V_O < (V+) – 1V(1)		70	80		
			T_A = –40°C to 125°C	65	80		
V_O	Output swing high	R_L = 10kΩ to 0V V_{ID} = 100mV			50	250	mV from either rail
			T_A = –40°C to 125°C			300	
		R_L = 2kΩ to 0V V_{ID} = 100mV			50	350	
			T_A = –40°C to 125°C			400	
	Output swing low	R_L = 10kΩ to 0V V_{ID} = −100mV			50	250	
			T_A = –40°C to 125°C			300	
		R_L = 2kΩ to 0V V_{ID} = −100mV			50	350	
			T_A = –40°C to 125°C			400	
I_{SC}	Short-circuit current	V_S = 32V		±62	±125		
		V_S = 5V		±50	±85		
		V_S = 2.7V		±30	±60		
I_S	Total supply current	No Load, V_{CM} = V−			2.7	3.86	mA
			T_A = –40°C to 125°C			4.46	
SR	Slew rate	A_V = +1, V_I = 10V step, C_L = 20pF			35		V/µs
R_{OUT}	Close-loop output resistance	A_V = +1, f = 100kHz			1		Ω

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For V_S = (V+) – (V–) = 2.7V to 32V (±1.35V to ±16V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS	MIN (2)	TYP (3)	MAX (2)	UNIT
f_u	Unity-gain frequency	R_L = 10MΩ, C_L = 20pF		11		MHz
GBWP	Gain bandwidth product			24		MHz
e_n	Input-referred voltage noise	f = 2kHz		14.7		nV/√HZ
i_n	Input-referred current noise	f = 2kHz		1.3		pA/√HZ
THD+N	Total harmonic distortion + noise	V_O = $3V_{RMS}$, G = 1, f = 1kHz, R_L = 10kΩ		−113		dB
CT Rej.	Crosstalk rejection	f = 3MHz, driver R_L = 10kΩ		120		dB

(1) *Electrical Characteristics* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No promised specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) All limits are verified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values can vary over time and also depend on the application and configuration. The typical values are not tested and are not promised on shipped production material.
(4) Offset voltage temperature drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing in the device.

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5.6 Typical Characteristics

Unless otherwise specified, T_A = 25°C.

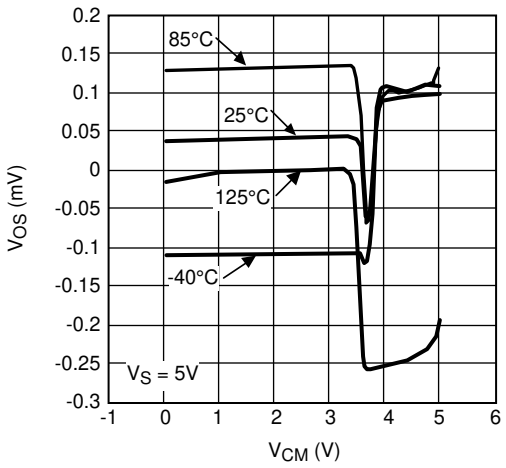


Figure 5-1. V_{OS} vs V_{CM} (Unit 1), Old Die

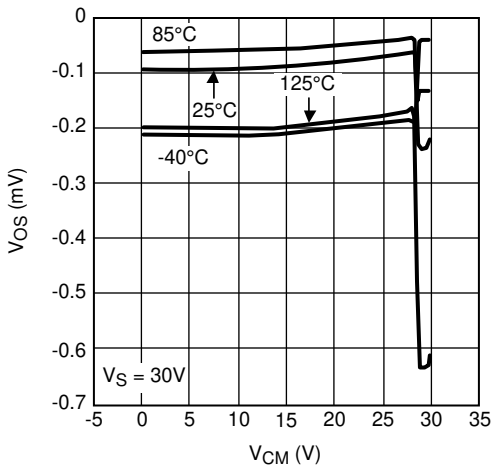


Figure 5-2. V_{OS} vs V_{CM} (Unit 1), Old Die

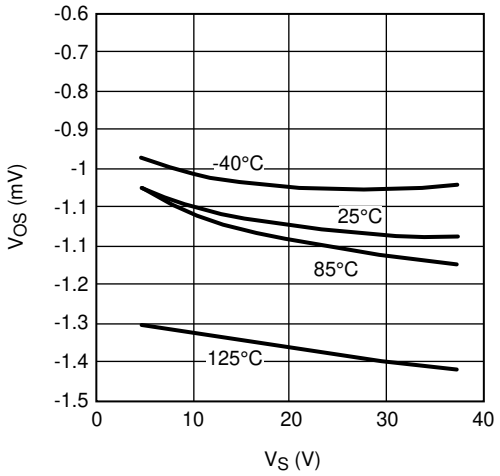


Figure 5-3. V_{OS} vs V_S (Unit 1), Old Die

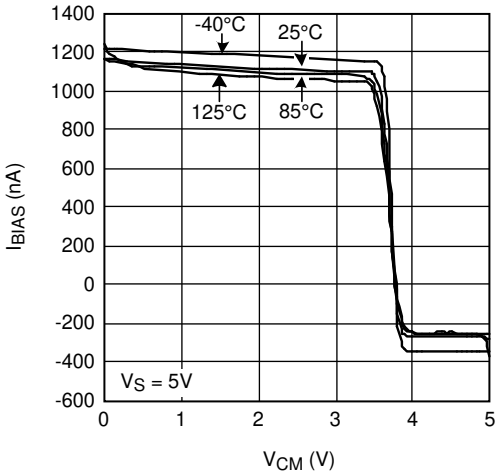


Figure 5-4. I_{BIAS} vs V_{CM}, Old Die

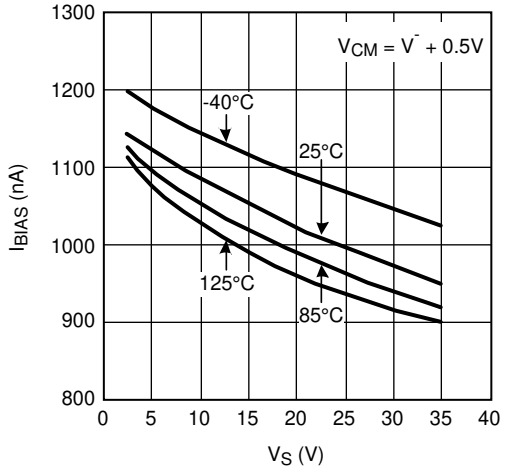


Figure 5-5. I_{BIAS} vs Supply Voltage, Old Die

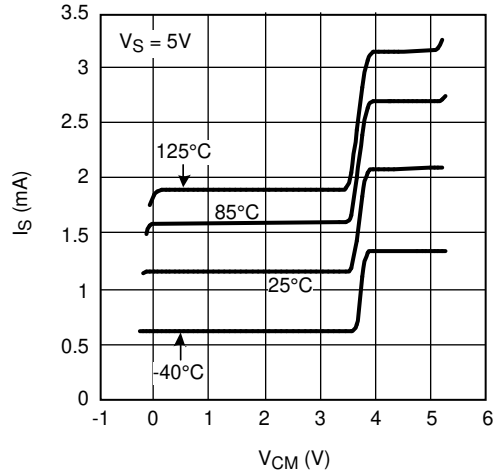


Figure 5-6. I_S vs V_{CM}, Old Die

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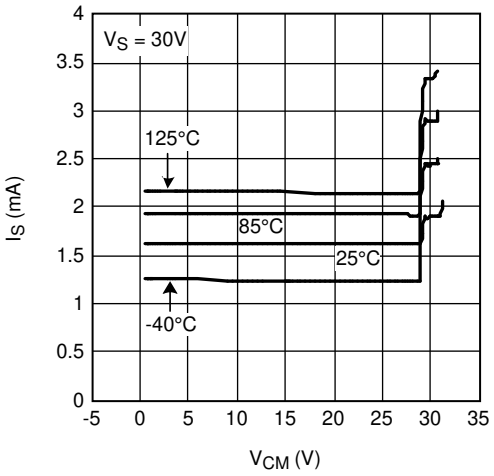


Figure 5-7. I_S vs V_{CM}, Old Die

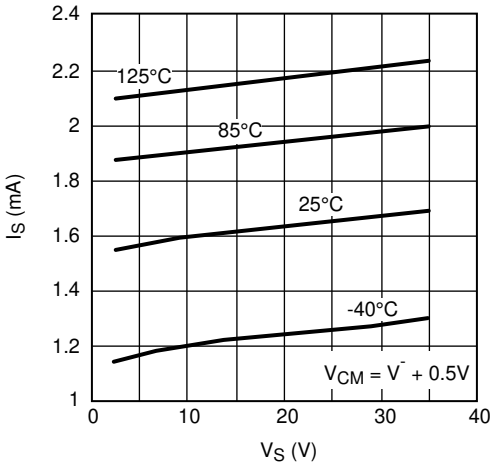


Figure 5-8. I_S vs Supply Voltage, Old Die

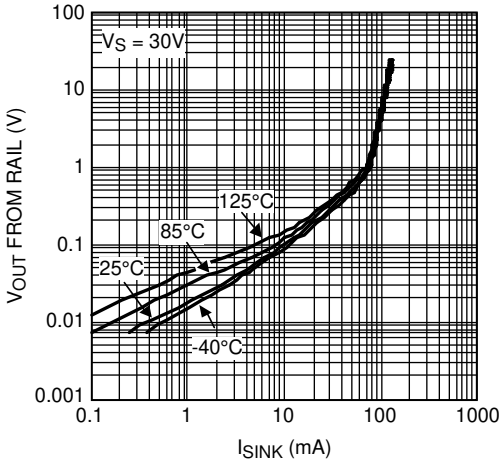


Figure 5-9. Output Swing vs Sinking Current, Old Die

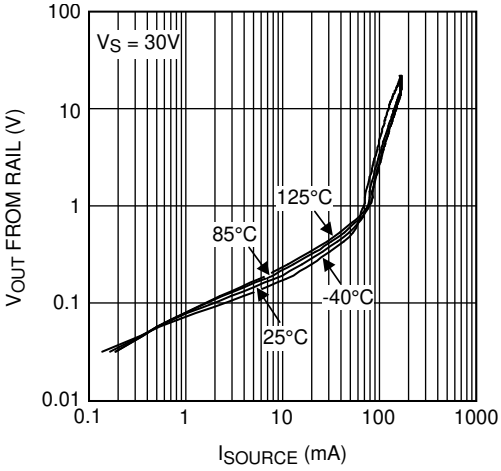


Figure 5-10. Output Swing vs Sourcing Current, Old Die

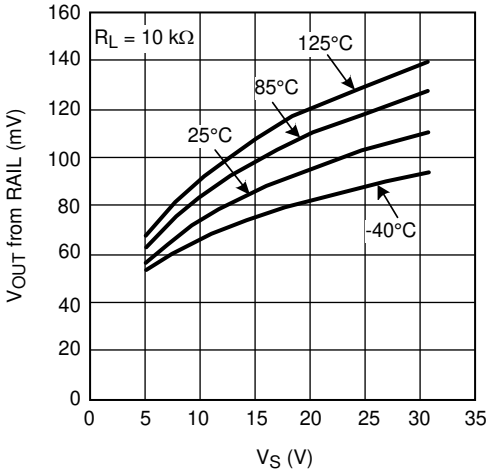


Figure 5-11. Positive Output Swing vs Supply Voltage, Old Die

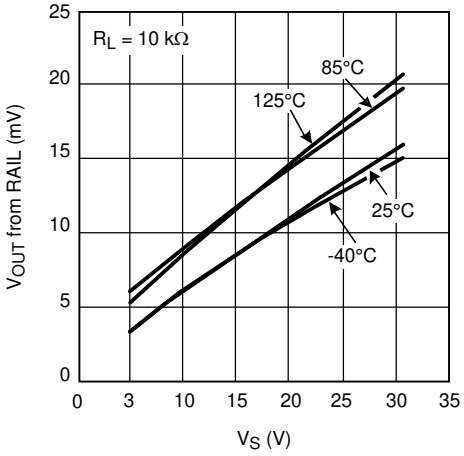


Figure 5-12. Negative Output Swing vs Supply Voltage, Old Die

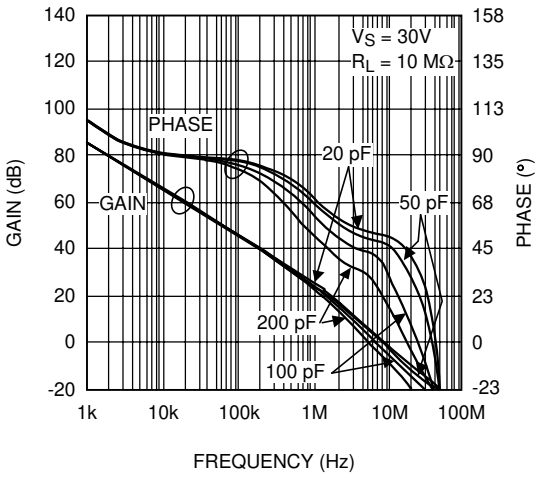


Figure 5-13. Open-Loop Frequency Response With Various Capacitive Loads, Old Die

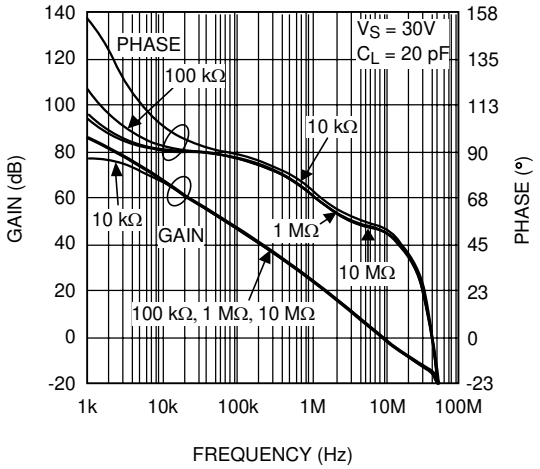


Figure 5-14. Open-Loop Frequency Response vs With Various Resistive Loads, Old Die

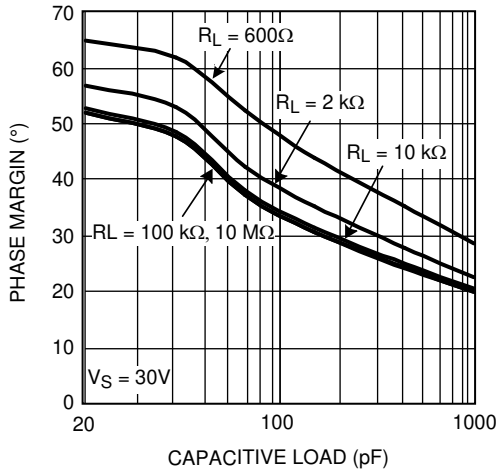


Figure 5-15. Phase Margin vs Capacitive Load, Old Die

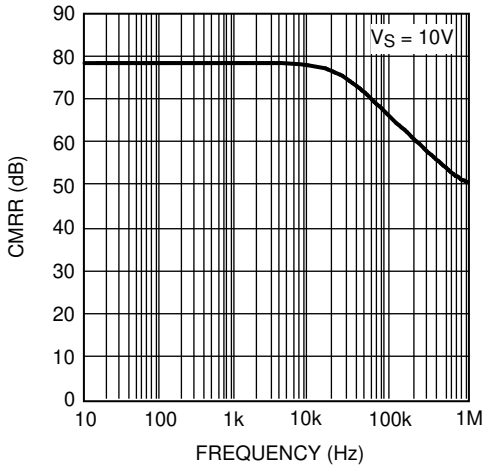


Figure 5-16. CMRR vs Frequency, Old Die

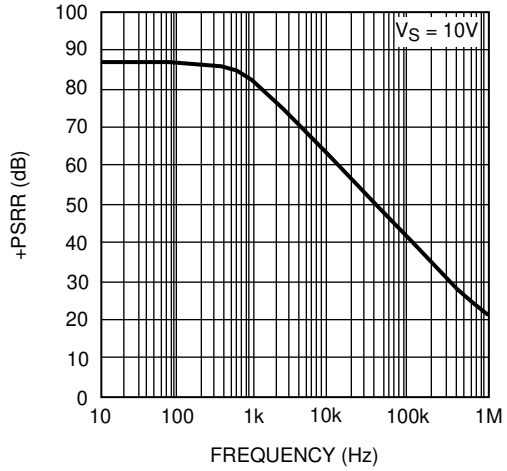


Figure 5-17. +PSRR vs Frequency, Old Die

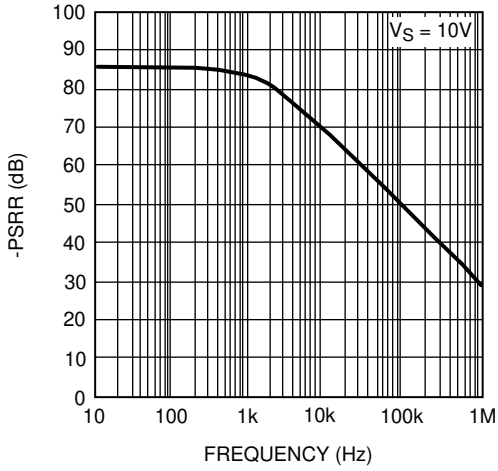


Figure 5-18. −PSRR vs Frequency, Old Die

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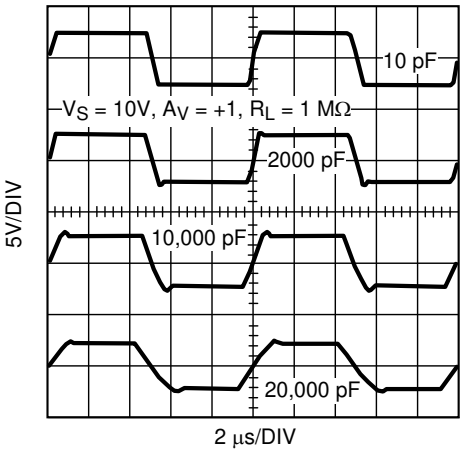


Figure 5-19. Large Signal Step Response for Various Capacitive Loads, Old Die

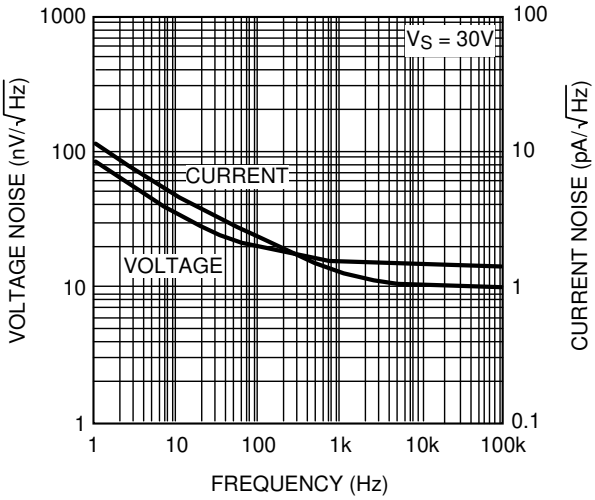


Figure 5-20. Input-Referred Noise Density vs Frequency, Old Die

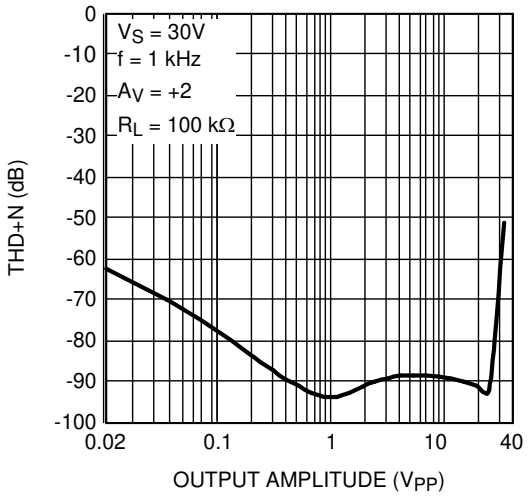


Figure 5-21. THD+N vs Output Amplitude (V_{PP}), Old Die

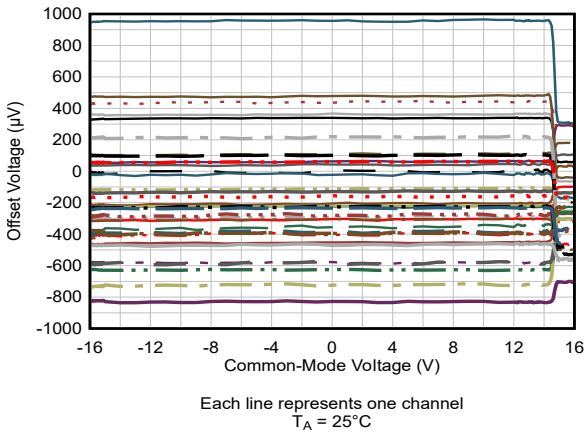


Figure 5-22. Offset Voltage vs Common-Mode Voltage

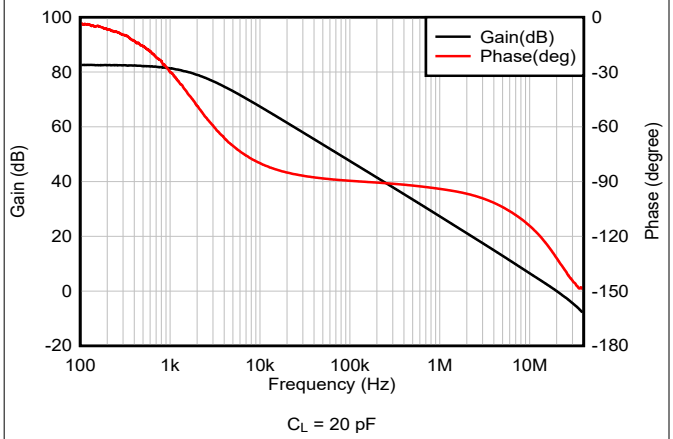


Figure 5-23. Open-Loop Gain and Phase vs Frequency, New Die

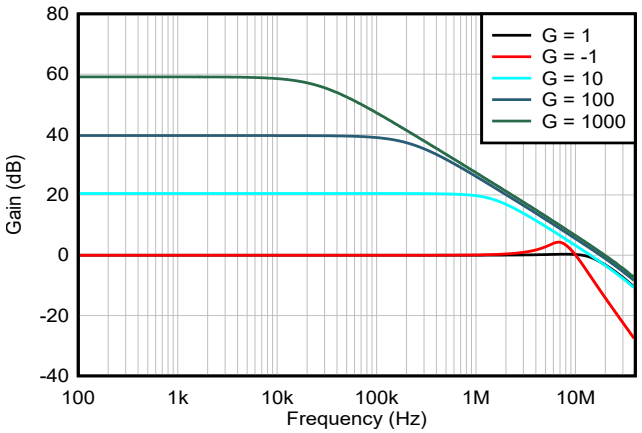


Figure 5-24. Closed-Loop Gain vs Frequency, New Die

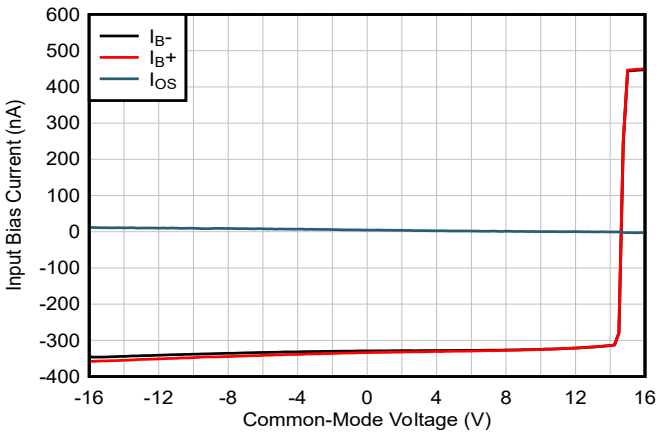
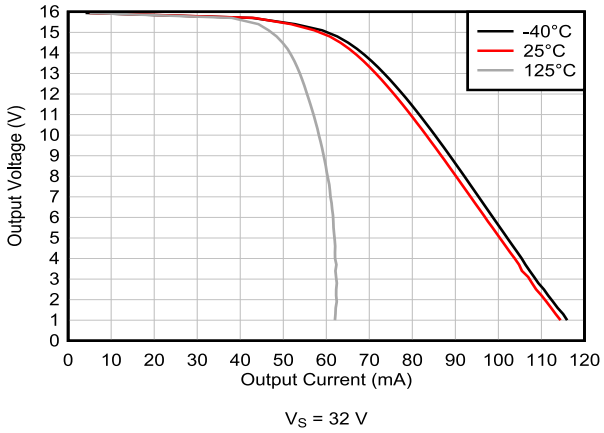
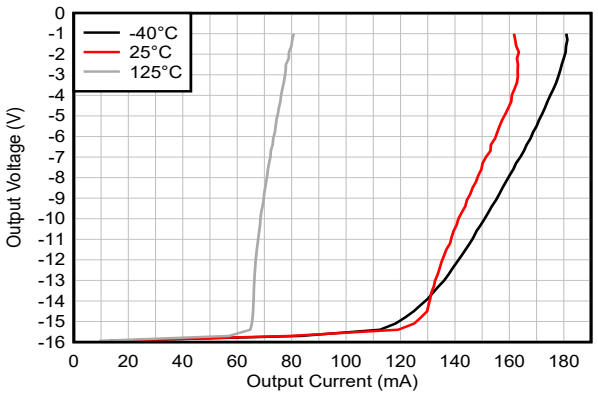


Figure 5-25. Input Bias Current and Offset Current vs Common-Mode Voltage, New Die



V_S = 32 V

Figure 5-26. Output Voltage Swing vs Output Current (Sourcing), New Die



V_S = 32 V

Figure 5-27. Output Voltage Swing vs Output Current (Sinking), New Die

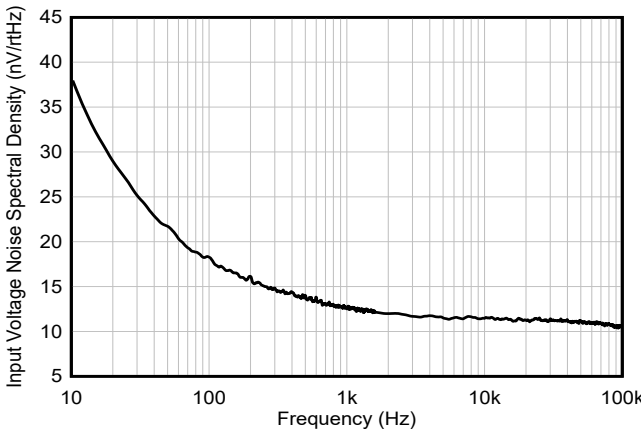
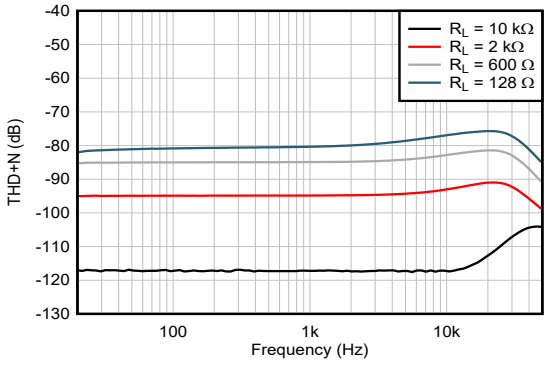
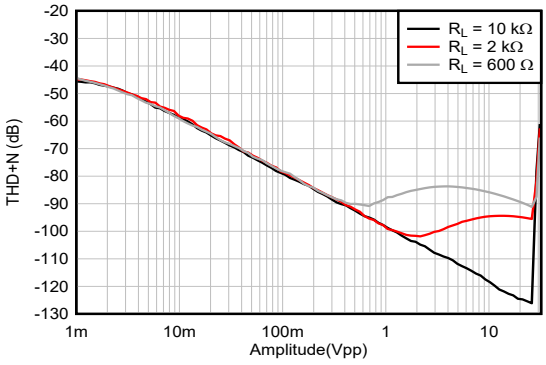


Figure 5-28. Input Voltage Noise Spectral Density vs Frequency, New Die



G = +1
V_{OUT} = 3 V_{RMS}
BW = 80 kHz

Figure 5-29. THD+N Ratio vs Frequency, New Die



f = 1 kHz
BW = 80 kHz
G = +1

Figure 5-30. THD+N vs Output Amplitude, New Die

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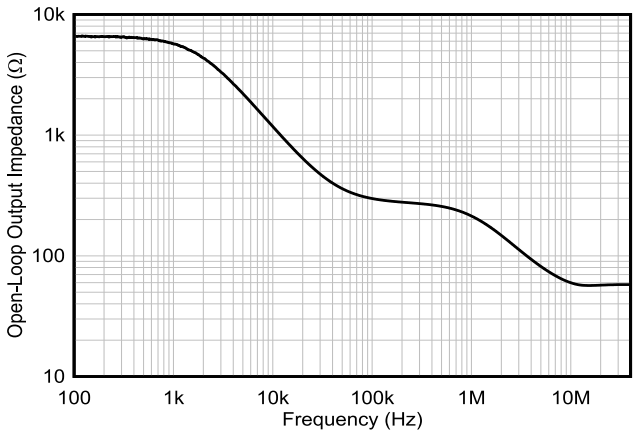


Figure 5-31. Open-Loop Output Impedance vs Frequency, New Die

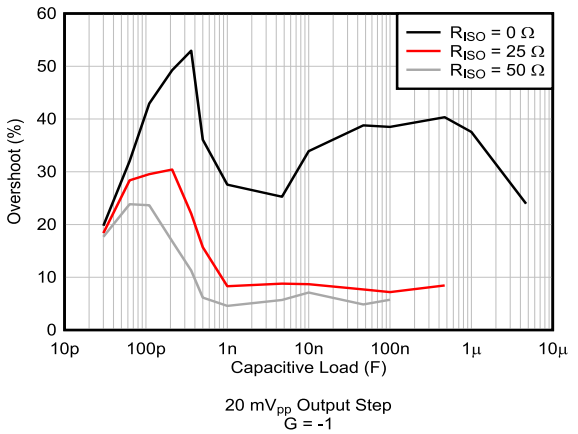


Figure 5-32. Small-Signal Overshoot vs Capacitive Load, New Die

5.7 Old vs. New Die Comparison

As of the publication of revision C of this data sheet, Texas Instruments has moved manufacturing of the die for LM7332 to a modern fabrication site. The two different die are referred to in this document as “old” (previous fabrication site) and “new” die. The die origin can be separated from the “Chip Source Origin” (CSO) parameter in the shipping information. The old die CSO is “GF6”, for the new die the CSO is “RFB”. The old die information is in the shipping information. The old die CSO is “GF6”, for the new die the CSO is “RFB”. The old die information is maintained in this data sheet for comparison purposes, but all new manufacturing has moved to the new die.

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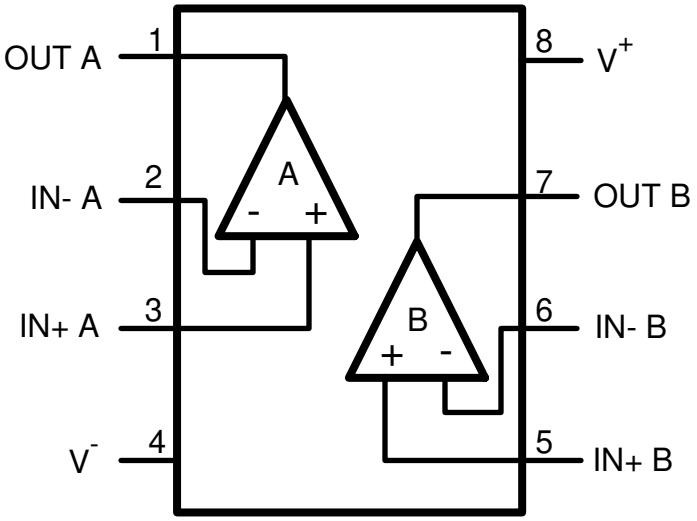
6 Detailed Description

6.1 Overview

The LM7332 device is a rail-to-rail input and output amplifier with wide operating voltages and high-output currents. The LM7322 is efficient, achieving 35V/µs slew rate and 24MHz unity gain bandwidth while requiring only 2.7mA of total supply current. The LM7332 device performance is fully specified for operation at 2.7V to 32V.

The LM7332 device is designed to drive unlimited capacitive loads without oscillations. Most device parameters are insensitive to power supply voltage, and this makes the parts easier to use where supply voltage can vary, such as automotive electrical systems and battery-powered equipment. The LM7332 has a true rail-to-rail output and can supply a respectable amount of current (±60mA) with minimal head room from either rail (1V).

6.2 Functional Block Diagram



6.3 Device Functional Modes

6.3.1 Driving Capacitive Loads

The LM7332 is specifically designed to drive unlimited capacitive loads without oscillations.

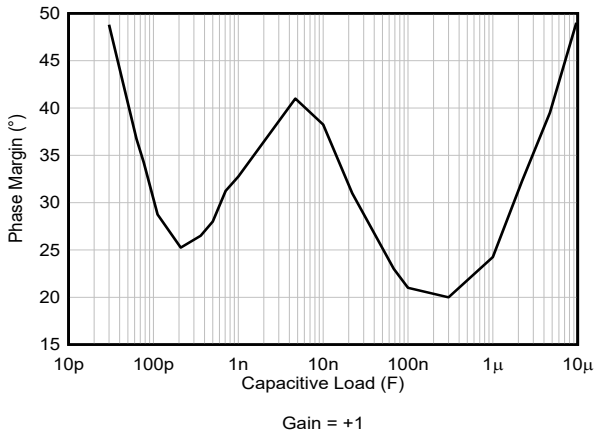


Figure 6-1. Phase Margin vs Capacitive Load

In addition, the output current handling capability of the device allows for good slewing characteristics even with large capacitive loads. The combination of these features is an excellent choice for applications such as TFT flat panel buffers, A/D converter input amplifiers, and power transistor driver.

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However, as in most operational amplifiers, addition of a series isolation resistor between the operational amplifier and the capacitive load improves the settling and overshoot performance.

To keep an acceptable phase margin, unlimited capacitive load drive devices lower the gain bandwidth product under larger capacitive loads. The LM7332 is specified to have a gain bandwidth product of 24MHz without significant capacitive load, but this value begins to decrease at the point where a traditional amplifier begins to become unstable. This tradeoff is what extends the output drive capability. LM7332 is designed with a wide gain bandwidth product to make sure there is headroom for many general-purpose applications with higher capacitive loads.

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6.4 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a solid understanding of basic ESD circuitry and the relevance of that circuitry to an electrical overstress event is highly beneficial. Figure 6-2 shows an illustration of the ESD circuits contained in the LM7332 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

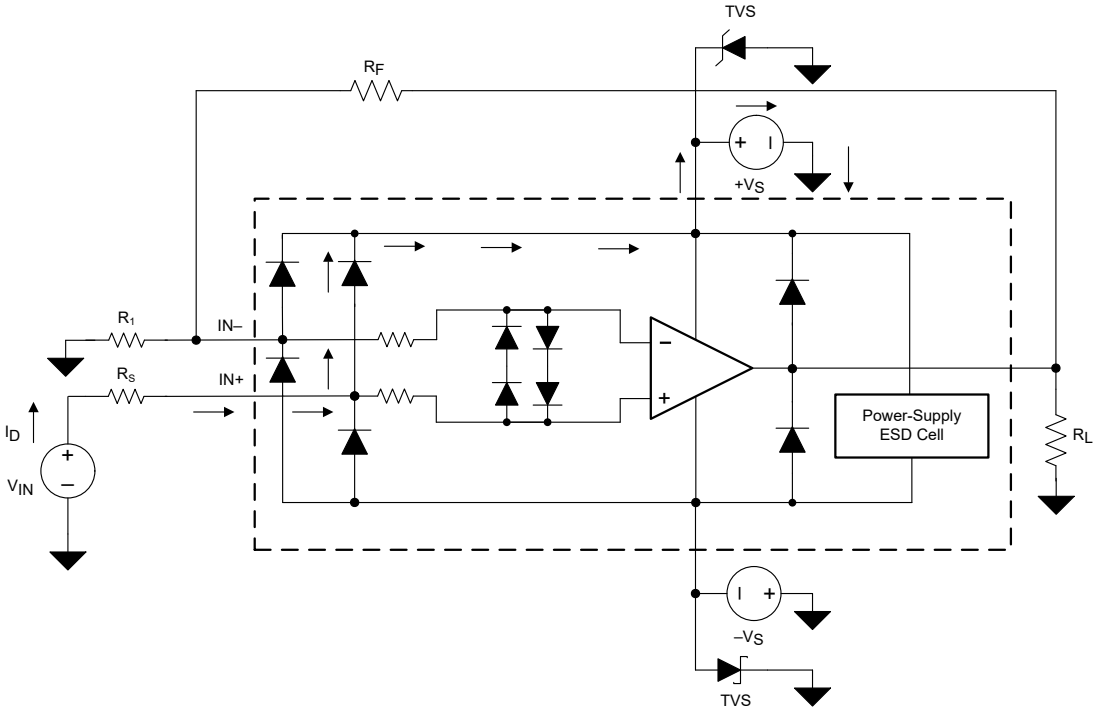


Figure 6-2. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

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An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device terminals, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the LM7332 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (as shown in Figure 6-2), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given terminal. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 6-2 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0V. Again, this question depends on the supply characteristic while at 0V, or at a level below the input-signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier cannot operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply terminals. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply terminal begins to rise above the safe-operating, supply-voltage level.

The LM7332 input terminals are protected from excessive differential voltage with back-to-back diodes; see Figure 6-2. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast - ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. These diodes can also be forward-biased in some comparator applications. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the LM7332. Figure 6-2 shows an example configuration that implements a current-limiting feedback resistor.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The LM7332 is a rail-to-rail input and output part with a GBW of 24MHz. The device has a current capability of ±125mA, and can drive unlimited capacitive loads. The LM7332 is available in both VSSOP and SOIC packages.

7.2 Typical Application

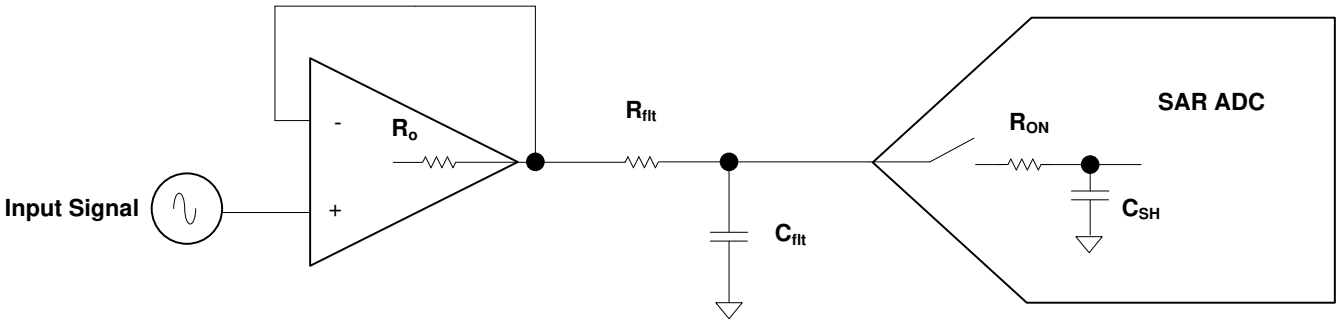


Figure 7-1. Drive Amplifier for SAR ADC Schematic

7.2.1 Design Requirements

Assume a portable application requires the use of a 12-bit SAR ADC with acquisition time (t_{AQ}) of 1µs and sample and hold capacitance (C_{SH}) of 80pF.

The ADC runs on a single supply voltage of 5V and has a full scale input of $2.5V_{PP}$. A total harmonic distortion plus noise (THD+N) of less than –80dB is required to maintain signal fidelity. Determine if the LM7332 is a practical drive amplifier and find the values of R_{flt} and C_{flt}.

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7.2.2 Detailed Design Procedure

The LM7332 can be used as a drive amplifier for SAR ADCs as shown in Figure 7-1.

The values of R_{flt} and C_{flt} depend on the ADC specifications, as well as amplifier gain bandwidth product (GBWP) and output resistance (R_O). A single ground-referenced supply voltage is also common, allowing sampling of signals up to half that voltage with low distortion.

To determine whether or not the LM7332 is a practical driver for this application, one must compare the settling time of the amplifier to the acquisition time of the ADC with Equation 1:

$$GBWP_{min} \geq 4 \times (N + 1) \times \ln(2) / (2\pi \times t_{AQ}) \quad (1)$$

where

- $GBWP_{min}$: The minimum required gain bandwidth product of the drive amplifier
- N: Number of bits in ADC
- t_{AQ}: The acquisition time of the ADC

Using a value of 12 bits for N and 1µs for t_{AQ}, the $GBWP_{min}$ must be greater than 5.7MHz. The LM7332 has a GBWP of 24MHz so LM7332 is indeed a practical driver for this application.

Next, determine the value of C_{flt} with Equation 2:

$$20 \times C_{SH} \leq C_{flt} \leq 60 \times C_{SH} \quad (2)$$

where

- C_{SH}: The ADC sample and hold capacitance
- C_{flt}: The external filter capacitance

Using a value of 80pF for C_{SH}, the value of C_{flt} must be between 1600pF and 4800pF. The LM7332 can drive a capacitive load of 2000pF with $5V_{PP}$ and settle within 1µs, therefore select 1800pF as the nearest common capacitor value within the range.

Next determine the value of R_{flt} with Equation 3:

$$R_{flt} = 40 / (2\pi \times C_{flt} \times GBWP_{min}) - R_O \quad (3)$$

where

- R_{flt}: The external filter resistance
- C_{flt}: The external filter capacitance determined above
- $GBWP_{min}$: The minimum required gain bandwidth product of the drive amplifier determined above
- R_O: The closed loop output impedance of the drive amplifier typically specified in the electrical characteristics table

Using a value of 1800pF for C_{flt}, 5.7MHz for $GBWP_{min}$, and a value of 1Ω for R_O the value of R_{flt} is determined to be 630Ω. Use closest value of 626Ω for a filter frequency (f_{flt}) of 141kHz given Equation 4:

$$f_{flt} = 1 / [2\pi \times (R_O + R_{flt}) \times C_{flt}] \quad (4)$$

The last requirement is to drive input signals of $2.5V_{PP}$ on a single 5V supply with THD+N less than –80dB.

Figure 7-2 shows the THD+N response of the LM7332 with a dual supply voltage of 16V. The LM7332 can maintain THD+N levels as low as –110dB for output levels up to $4V_{PP}$. Therefore, the final requirement has been met, and the LM7332 is a practical drive amplifier for the 12-bit SAR ADC in this design example.

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7.2.3 Application Curves

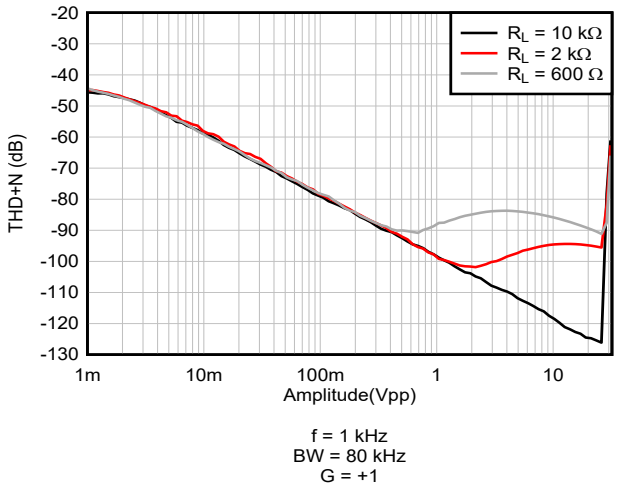


Figure 7-2. THD+N vs Output Amplitude

7.3 Power Supply Recommendations

The use of supply decoupling is mandatory in most applications. As with most relatively high-speed or high output current operational amplifiers, best results are achieved when each supply line is decoupled with two capacitors: a small value ceramic capacitor (approximately 0.01µF) placed very close to the supply lead in addition to a large value tantalum or aluminum capacitor (>4.7µF). The large capacitor can be shared by more than one device if necessary. The small ceramic capacitor maintains low supply impedance at high frequencies while the large capacitor acts as the charge *bucket* for fast load current spikes at the operational amplifier output. The combination of these capacitors provides supply decoupling and helps keep the operational amplifier oscillation free under any load.

7.4 Layout

7.4.1 Layout Guidelines

Take care to minimize the loop area formed by the bypass capacitor connection between supply pins and ground. A ground plane underneath the device is recommended; any bypass components to ground must have a nearby via to the ground plane. The optimum bypass capacitor placement is closest to the corresponding supply pin. Use of thicker traces from the bypass capacitors to the corresponding supply pins lowers the power supply inductance and provide a more stable power supply.

The feedback components must be placed as close to the device as possible to minimize stray parasitics.

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7.4.2 Layout Example

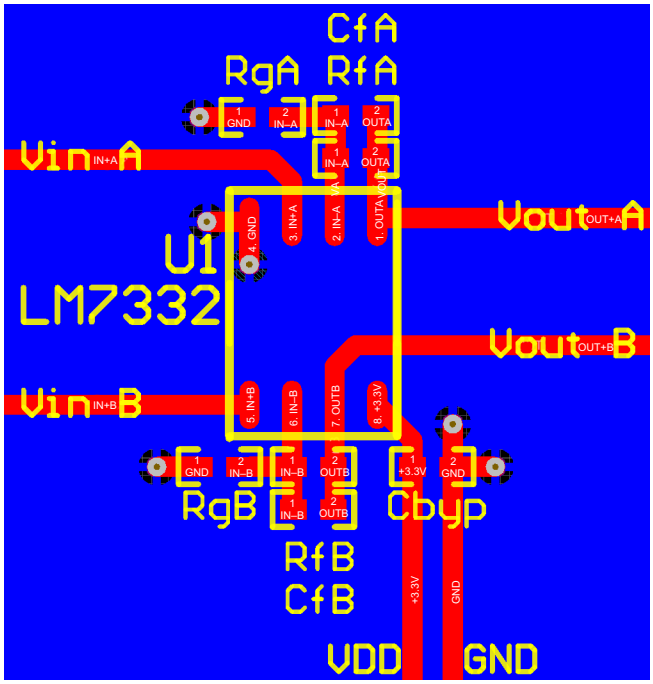


Figure 7-3. LM7332 Layout Example

7.4.3 Output Short Circuit Current and Dissipation Issues

The LM7332 output stage is designed for maximum output current capability. Even though momentary output shorts to ground and either supply can be tolerated at all operating voltages, longer-lasting short conditions can cause the junction temperature to rise beyond the absolute maximum rating of the device, especially at higher supply voltage conditions.

With the operational amplifier tied to a load, the device power dissipation consists of the quiescent power due to the supply current flow into the device, in addition to power dissipation due to the load current. The load portion of the power can include an average value (due to a DC load current) and an AC component. DC load current flows if there is an output voltage offset, or the output AC average current is non-zero, or if the operational amplifier operates in a single-supply application where the output is maintained somewhere in the range of linear operation.

Therefore,

$$P_{TOTAL} = P_Q + P_{DC} + P_{AC} \quad (5)$$

The operational amplifier quiescent power dissipation is calculated by Equation 6:

$$P_Q = I_S \times V_S \tag{6}$$

where

- I_S: Supply Current
- V_S: Total Supply Voltage ($V^+ - V^-$)

The DC load power is calculated by Equation 7:

$$P_{DC} = I_O \times (V_r - V_O) \tag{7}$$

where

- V_O: Average Output Voltage
- V_r: V^+ for sourcing and V^- for sinking current

The AC load power is calculated as P_{AC} = the value shown in Table 7-1.

Table 7-1 shows the maximum AC component of the load power dissipated by the operational amplifier for standard sinusoidal, triangular, and square waveforms:

Table 7-1. Normalized AC Power Dissipated in the Output Stage for Standard Waveforms

P_{AC} (W.Ω/V²)		
SINUSOIDAL	TRIANGULAR	SQUARE
50.7×10^{-3}	46.9×10^{-3}	62.5×10^{-3}

The table entries are normalized to $V_S{}^2/R_L$. To figure out the AC load current component of power dissipation, simply multiply the table entry corresponding to the output waveform by the factor $V_S{}^2/R_L$. For example, with ±12V supplies, a 600Ω load, and triangular waveform power dissipation in the output stage is calculated as:

$$P_{AC} = \left(46.9 \times 10^{-3}\right) \times \left(24^2 / \ 600\right) = \ 45.0\text{mW} \tag{8}$$

The maximum power dissipation allowed at a certain temperature is a function of maximum die junction temperature ($T_{J(MAX)}$) allowed, ambient temperature T_A, and package thermal resistance from junction to ambient, $R_{\theta JA}$.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \tag{9}$$

For the LM7332, the maximum junction temperature allowed is 150°C at which no power dissipation is allowed. The power capability at 25°C is given by:

For VSSOP package:

$$P_{D(MAX)} = \frac{150℃ - \ 25℃}{169.6℃} = 0.737\text{W} \tag{10}$$

For SOIC package:

$$P_{D(MAX)} = \frac{150℃ - \ 25℃}{124℃} = 1.008\text{W} \tag{11}$$

Similarly, the power capability at 125°C is given by:

For VSSOP package:

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$$P_{D(MAX)} = \frac{150℃ - 25℃}{169.6℃} = 0.147W \quad (12)$$

For SOIC package:

$$P_{D(MAX)} = \frac{150℃ - 25℃}{124℃} = 0.202W \quad (13)$$

When the device works in the operating area where P_{TOTAL} is less than $P_{D(MAX)}$, the device junction temperature remains below 150°C. When high power is required and ambient temperature cannot be reduced, providing air flow is an effective approach to reduce thermal resistance therefore to improve power capability.

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8 Device and Documentation Support

8.1 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.2 Trademarks

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8.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.4 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2015) to Revision C (August 2026)	Page
• Updated Wide Supply Voltage Range minimum from 2.5V to 2.7V	1
• Removed High Output Current feature	1
• Updated GBWP from 21MHz to 24MHz	1
• Updated Slew Rate from 15.2V/µs to 35V/µs	1
• Updated Total Supply Current from 2mA to 2.7mA	1
• Updated Supply voltage ($V_S = V^+ – V^–$) from 35V to 33V	4
• Updated Voltage at input/output pins minimum from $V^+ + 0.3V$ to $V^– – 0.5V$ and maximum from $V^– – 0.3V$ to $V^+ + 0.5V$	4
• Added Charged-device model Ratings	4
• Updated Junction-to-ambient thermal resistance for DGK (VSSOP) package from 161.1°C/W to 169.6°C/W	5
• Updated Junction-to-ambient thermal resistance for D (SOIC) package from 109.1°C/W to 124.0°C/W	5
• Updated Junction-to-case (top) thermal resistance for DGK (VSSOP) package from 55°C/W to 61.6°C/W	5
• Updated Junction-to-case (top) thermal resistance for D (SOIC) package from 55.8°C/W to 67.3°C/W	5
• Updated Junction-to-board thermal resistance for DGK (VSSOP) package from 80.5°C/W to 91.2°C/W	5
• Updated Junction-to-board thermal resistance for D (SOIC) package from49.2°C/W to 68.4°C/W	5
• Updated Junction-to-top characterization parameter for DGK (VSSOP) package from 5.5°C/W to 9.0°C/W	5
• Updated Junction-to-top characterization parameter for D (SOIC) package from 10.7°C/W to 19.9°C/W	5
• Updated Junction-to-board characterization parameter for DGK (VSSOP) package from 79.2°C/W to 89.7°C/W	5
• Updated Junction-to-board characterization parameter for D (SOIC) package from 48.7°C/W to 67.6°C/W	5
• Updated Wide Supply Voltage Range minimum from 2.5V to 2.7V	5
• Updated Input offset voltage typical value from ±1.6mV to ±0.35	6
• Updated Input offset voltage temperature drift typical value from ±2µV/°C to ±2.5µV/°C	6
• Updated Input bias current typical value from ±1µA to 0.4µA	6
• Updated Input offset current typical value from 20nA to 7nA	6
• Updated Input common-mode voltage range minimum value from 5.1V to (V−) − 0.1	6

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- Updated Input common-mode voltage range minimum value from −5.1V to (V+) + 0.1 ... 6
- Removed Input common-mode voltage range typical value ... 6
- Updated all Output swing high and Output swing low typical values to 50mV (from either rail) ... 6
- Updated CMRR specification as per New Die Characteristics ... 6
- Updated Total supply current typical value from 1.5mA to 2.7mA and maximum values for T_A= 25°C from 2.4mA to 3.86mA and for T_A = –40°C to +125°C from 2.6mA to 4.46mA ... 6
- Updated Slew rate typical value from 13.2V/µs to 35V/µs ... 6
- Updated Close-loop output resistance from 3Ω to 1Ω ... 6
- Updated Unity-gain frequency 7.9MHz to 11MHz ... 6
- Updated Gain bandwidth product from 19.9MHz to 24MHz ... 6
- Updated Total harmonic distortion + noise from -87dB to -113dB ... 6
- Updated Crosstalk rejection from 68dB to 120dB ... 6
- Updated plots as per New Die Characteristics ... 8
- Added *Old vs. New Die Comparison* section ... 13
- Removed *Output Voltage Swing Close to V⁻* section ... 14
- Added *Electrical Overstress* section ... 16

Changes from Revision A (March 2013) to Revision B (December 2015) **Page**

- Added *Device Information, ESD Ratings* and *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision * (March 2013) to Revision A (March 2013) **Page**

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM7332MA/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	LM733 2MA
LM7332MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LM733 2MA
LM7332MAX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM733 2MA
LM7332MM/NOPB	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	-40 to 125	AA5A
LM7332MMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AA5A
LM7332MMX/NOPB.B	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AA5A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

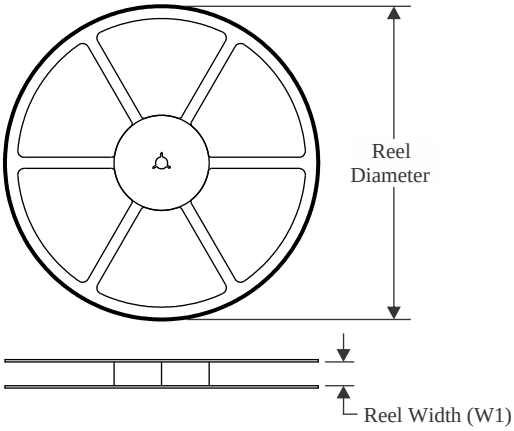
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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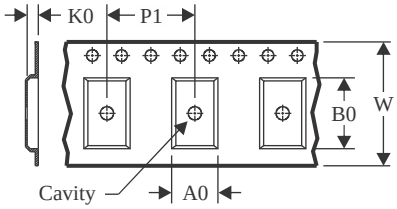
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

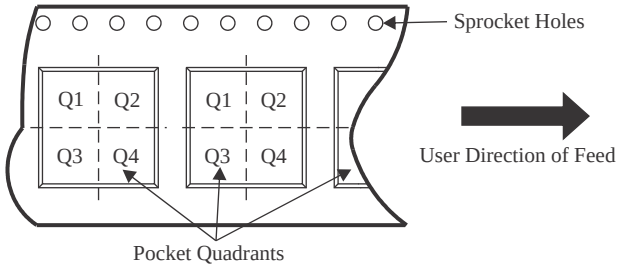


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

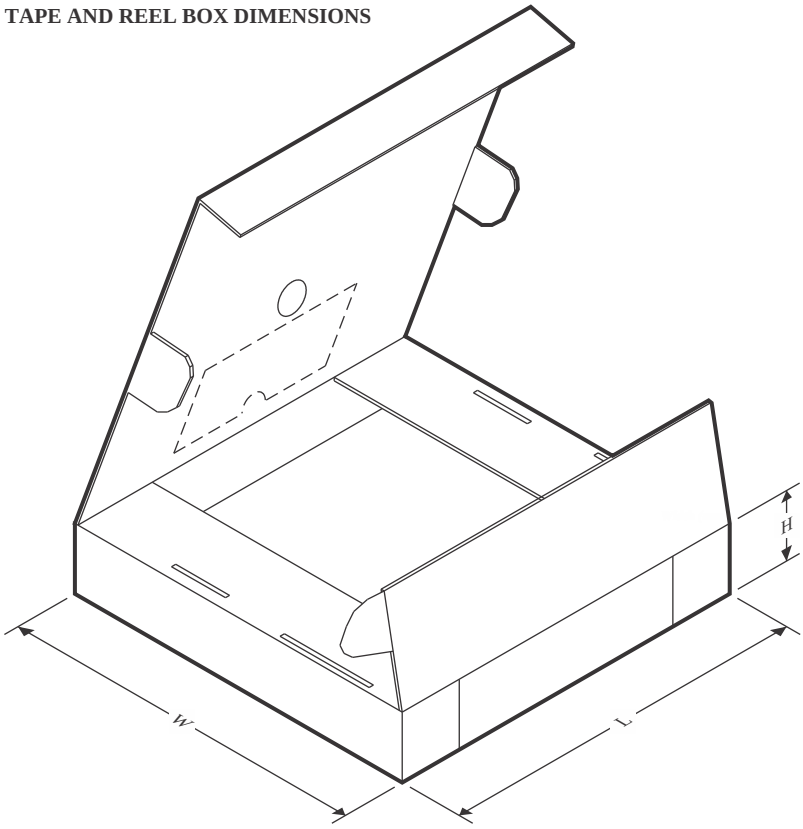
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM7332MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM7332MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
LM7332MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

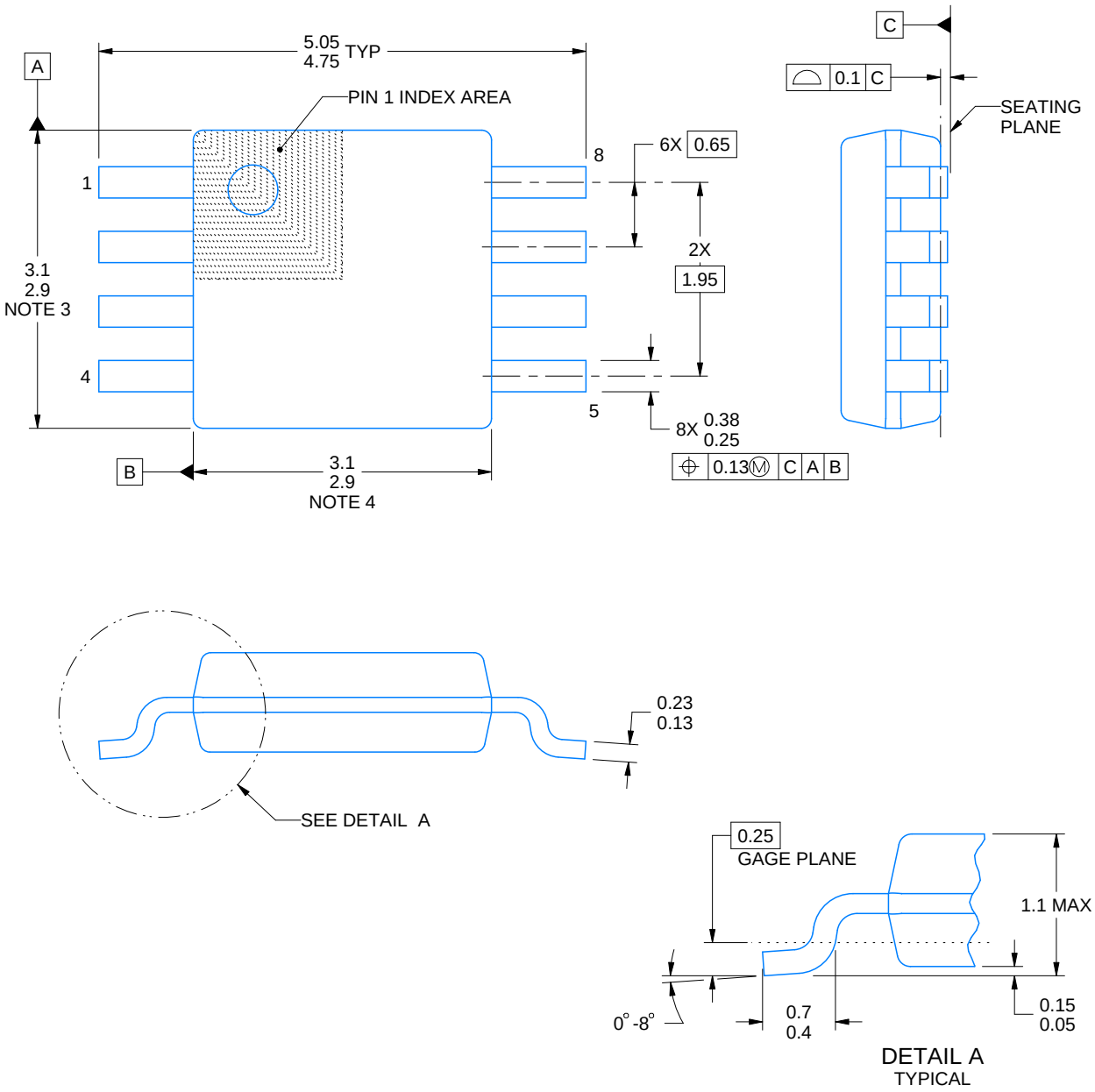
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM7332MAX/NOPB	SOIC	D	8	2500	353.0	353.0	32.0
LM7332MMX/NOPB	VSSOP	DGK	8	3500	366.0	364.0	50.0
LM7332MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

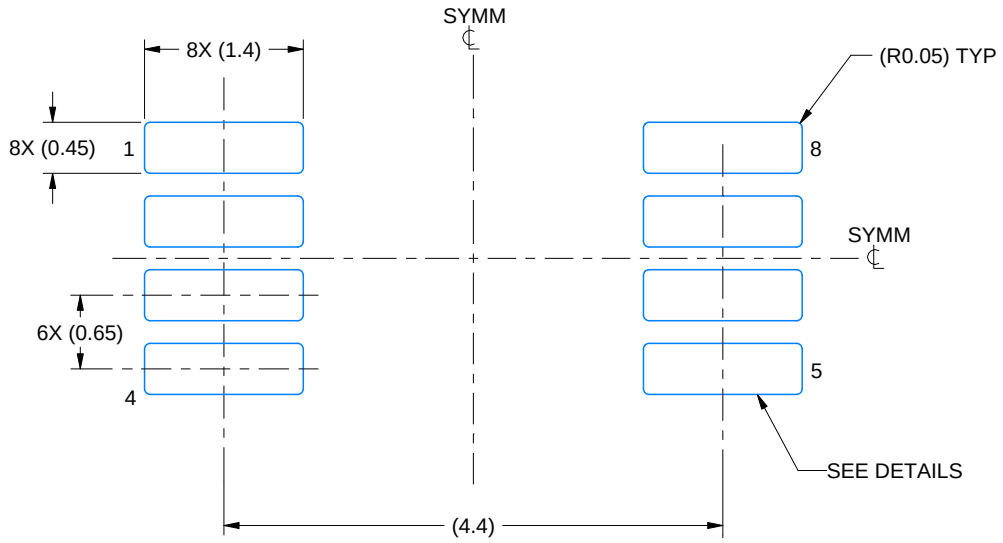
SMALL OUTLINE PACKAGE



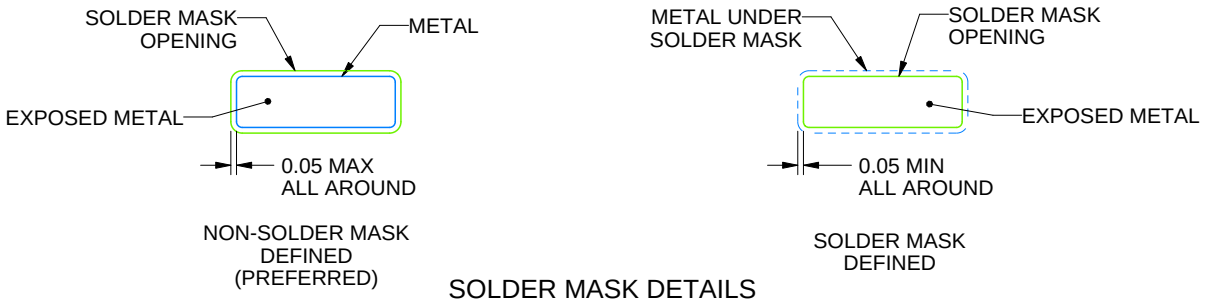
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

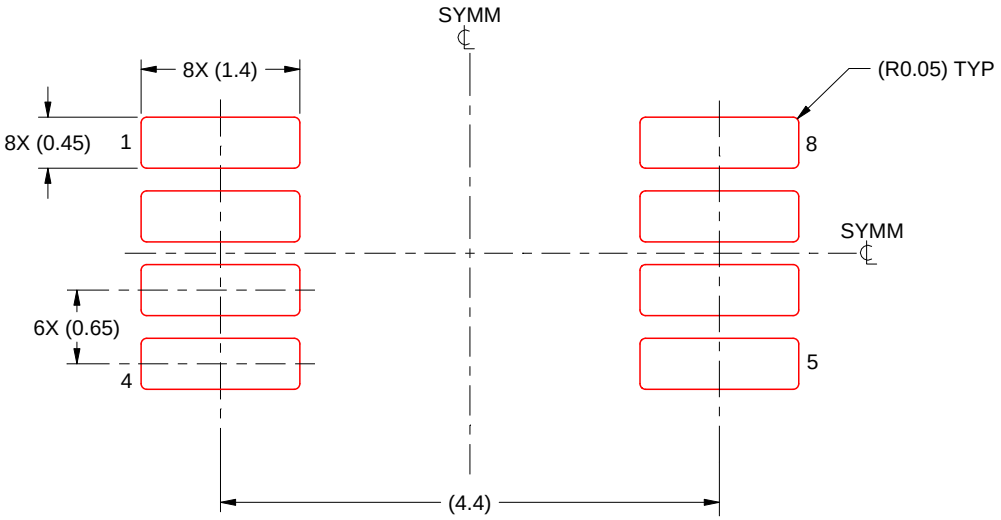


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

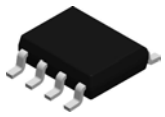


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

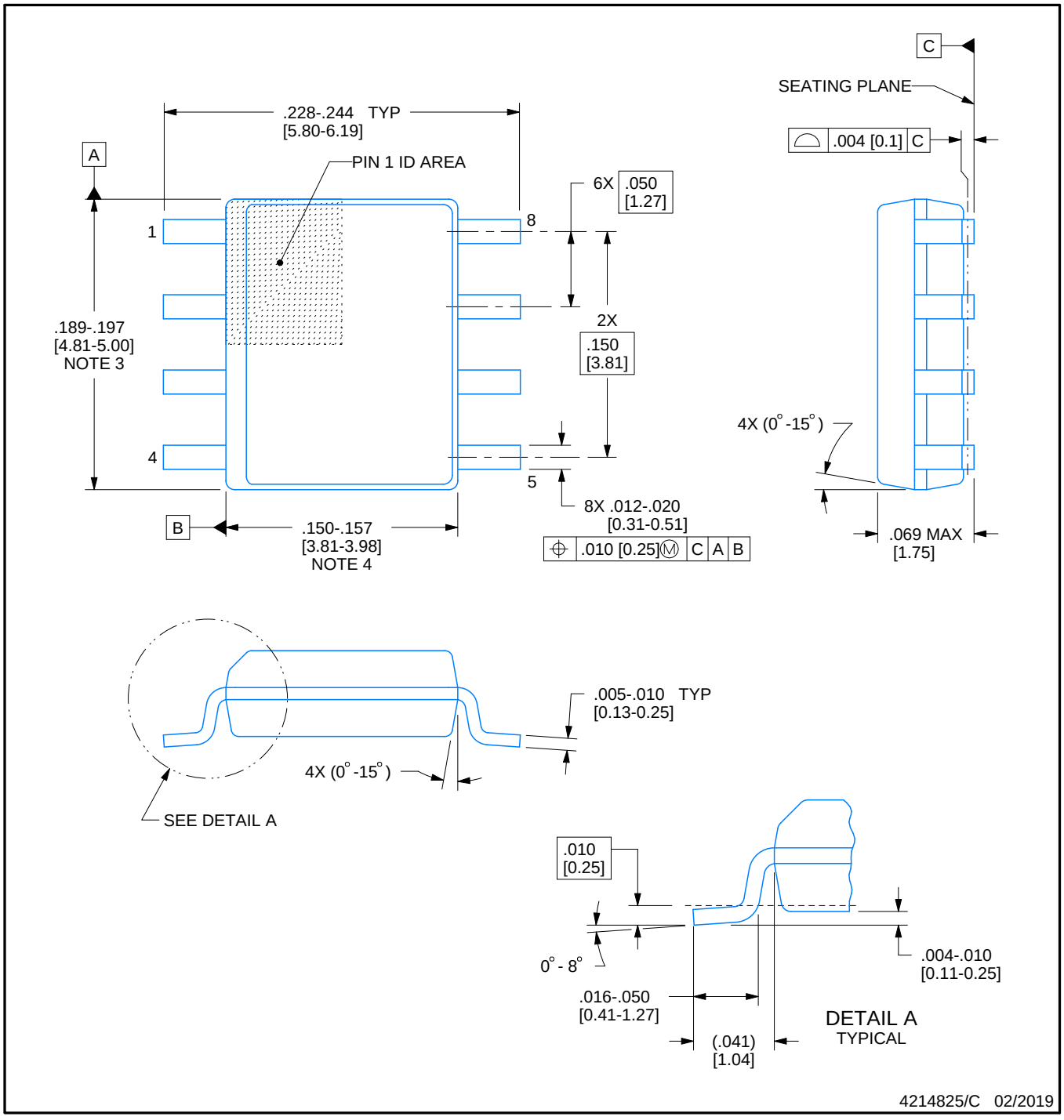


PACKAGE OUTLINE

D0008A

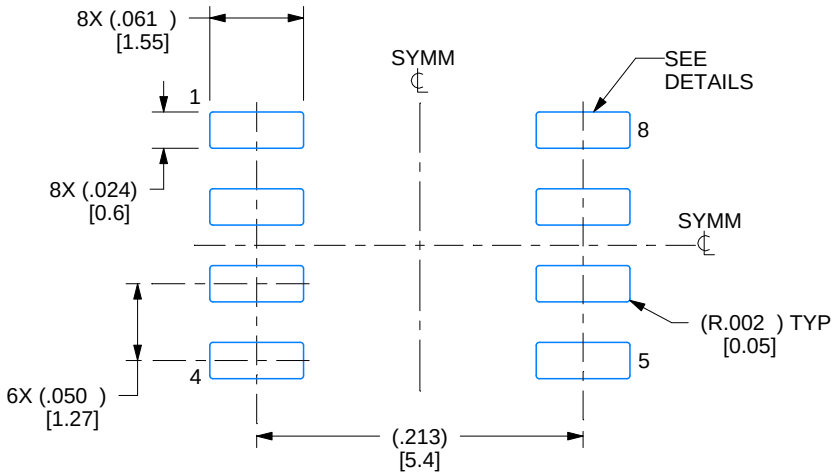
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

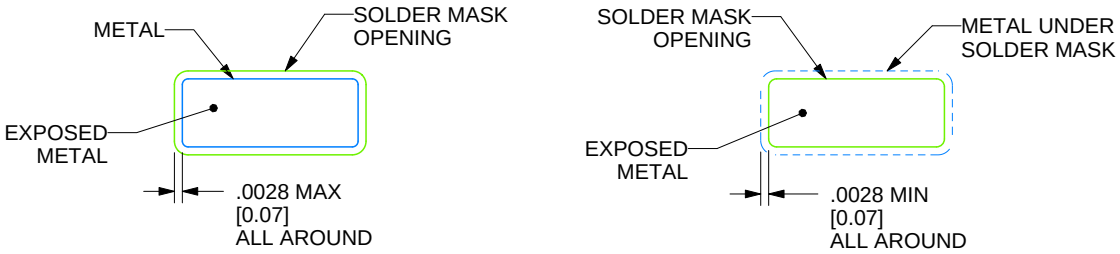


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

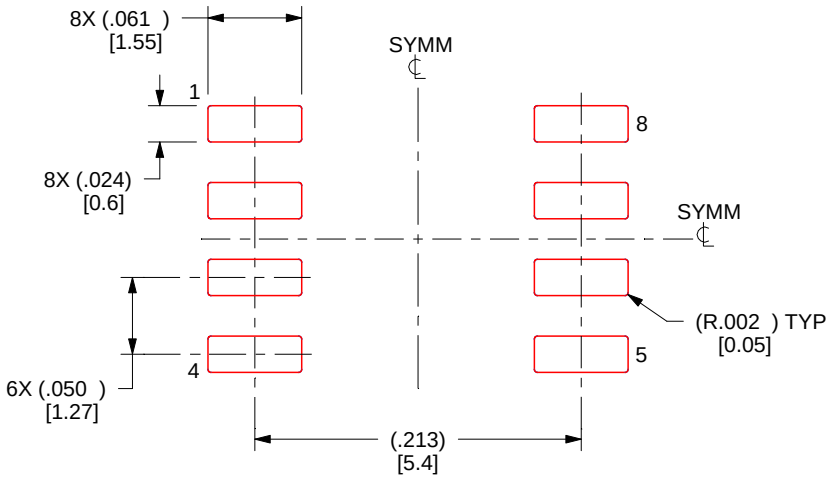
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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