LM747QML Dual Operational Amplifier

Check for Samples: LM747QML

FEATURES

- **No Frequency Compensation Required**
- **Short-Circuit Protection**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Power Consumption**
- **No Latch-Up**

DESCRIPTION

The LM747 is a general purpose dual operational amplifier. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent.

Additional features of the LM747 are: no latch-up when input common mode range is exceeded, freedom from oscillations, and package flexibility.

Connection Diagrams

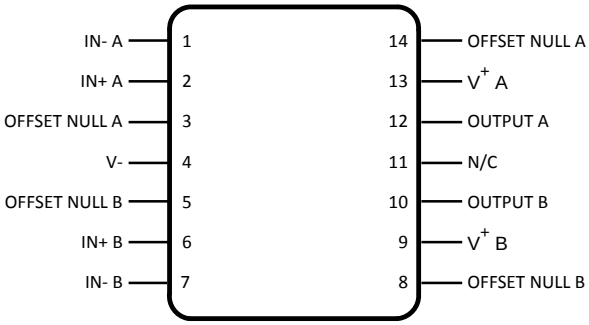


Figure 1. CDIP Top View
See Package Number J (R-GDIP-T14)

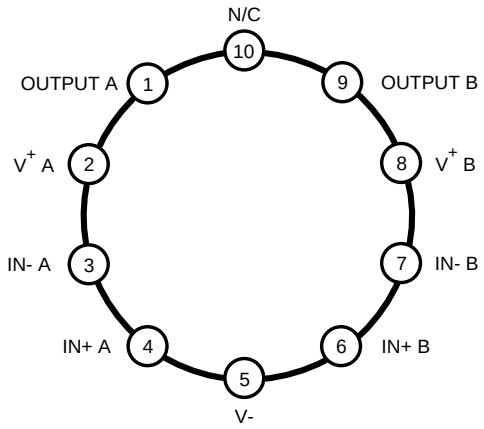


Figure 2. TO-100
See Package Number LME (O-MBCY-W10)

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Supply voltage	±22V
Power Dissipation(2)	800mW
Differential Input Voltage	±30V
Input Voltage(3)	±15V
Output Short-Circuit Duration	Indefinite
Maximum Junction Temperature (T_{Jmax})	150°C
Operating Temperature Range	−55°C ≤ T_A ≤ +125°C
Storage Temperature Range	−65°C ≤ T_A ≤ +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

(3) For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

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LM747 Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub- groups
V_{IO}	Input Offset Voltage	R_S = 50Ω, V_{CM} = -12V		-5.0	5.0	mV	1
				-6.0	6.0	mV	2, 3
		R_S = 50Ω, V_{CM} = 12V		-5.0	5.0	mV	1
				-6.0	6.0	mV	2, 3
		R_S = 50Ω		-5.0	5.0	mV	1
				-6.0	6.0	mV	2, 3
		R_S = 50Ω, V_{CC} = ±5V		-5.0	5.0	mV	1
				-6.0	6.0	mV	2, 3
I_{IO}	Input Offset Current	V_{CM} = -12V		-200	200	nA	1
				-500	500	nA	2, 3
		V_{CM} = 12V		-200	200	nA	1
				-500	500	nA	2, 3
				-200	200	nA	1
				-500	500	nA	2, 3
		V_{CC} = ±5V		-200	200	nA	1
				-500	500	nA	2, 3
I_{IB}^+	Input Bias Current	V_{CM} = -12V		0.0	500	nA	1
				0.0	1500	nA	2, 3
		V_{CM} = 12V		0.0	500	nA	1
				0.0	1500	nA	2, 3
				0.0	500	nA	1
				0.0	1500	nA	2, 3
		V_{CC} = ±5V		0.0	500	nA	1
				0.0	1500	nA	2, 3
I_{IB}^-	Input Bias Current	V_{CM} = -12V		0.0	500	nA	1
				0.0	1500	nA	2, 3
		V_{CM} = 12V		0.0	500	nA	1
				0.0	1500	nA	2, 3
				0.0	500	nA	1
				0.0	1500	nA	2, 3
		V_{CC} = ±5V		0.0	500	nA	1
				0.0	1500	nA	2, 3
$V_{IO\ Adj}^+$	Input Offset Voltage Adjustment Range		See(1)	6.0		mV	1, 2, 3
$V_{IO\ Adj}^-$	Input Offset Voltage Adjustment Range				-6.0	mV	1, 2, 3
$PSRR^+$	Power Supply Rejection Ratio	R_S = 50Ω, V_{CC} = ±15V to ±5V		77		dB	1, 2, 3
$PSRR^-$	Power Supply Rejection Ratio	R_S = 50Ω, V_{CC} = ±15V to ±5V		77		dB	1, 2, 3
CMRR	Common Mode Rejection Ratio	R_S = 50Ω, V_{CM} = ±12V		70		dB	1, 2, 3
I_{OS}^+	Output Short Circuit Current			-45	-9.0	mA	1, 2
				-50	-9.0	mA	3
I_{OS}^-	Output Short Circuit Current			9.0	45	mA	1, 2
				9.0	50	mA	3
I_{CC}	Supply Current				5.6	mA	1
					5.0	mA	2
					6.6	mA	3

(1) Tested for CDIP only.

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LM747 Electrical Characteristics DC Parameters (continued)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub- groups
V_{OP}^+	Output Voltage Swing	R_L = 10KΩ		12		V	1, 2, 3
		R_L = 2KΩ		10		V	1, 2, 3
		V_{CC} = ±20V, R_L = 10KΩ		16		V	1, 2, 3
		V_{CC} = ±20V, R_L = 2KΩ		15		V	1, 2, 3
V_{OP}^-	Output Voltage Swing	R_L = 10KΩ			-12	V	1, 2, 3
		R_L = 2KΩ			-10	V	1, 2, 3
		V_{CC} = ±20V, R_L = 10KΩ			-16	V	1, 2, 3
		V_{CC} = ±20V, R_L = 2KΩ			-15	V	1, 2, 3
A_{VS}^+	Open Loop Voltage Gain	V_O = 0 to +10V, R_L = 2K	See(2)	50		V/mV	1
				25		V/mV	2, 3
A_{VS}^-	Open Loop Voltage Gain	V_O = 0 to -10V, R_L = 2K	See(2)	50		V/mV	1
				25		V/mV	2, 3
V_I	Input Voltage Range		See(3)	12	−12	V	1, 2, 3
V_{OP}	Output Voltage Swing	V_{CC} = ±5V	See(4)	2	−2	V	1, 2, 3

(2) Datalog reading in K = V/mV
(3) Parameter tested go-no-go only, specified by CMRR test.
(4) Specified parameter, not tested.

LM747 Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified.
AC: V_{CC} = ±15V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub- groups
SR^+	Slew Rate	A_V = 1, V_I = -5V to +5V		0.2		V/µS	9
SR^-	Slew Rate	A_V = 1, V_I = +5V to -5V		0.2		V/µS	9
GBW	Gain Bandwidth	V_I = 50mV, f = 20KHz, R_L = 2KΩ		0.25		Mhz	9

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Table 1. Revision History

Released	Revision	Section	Changes
12/16/2010	A	New Release, Corporate format	1 MDS data sheet converted into one Corp. data sheet format. The drift table was eliminated from the 883 section since it did not apply; MNLM747-X Rev 0BL will be archived.
03/25/2013	A	All Sections	Changed layout of National Data Sheet to TI format

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM747 MD8	Active	Production	DIESALE (Y) | 0	456 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
LM747H/883	Active	Production	TO-100 (LME) | 10	20 | TRAY NON-STD	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LM747H/883 Q ACO LM747H/883 Q >T
LM747J/883	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM747J/883 Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

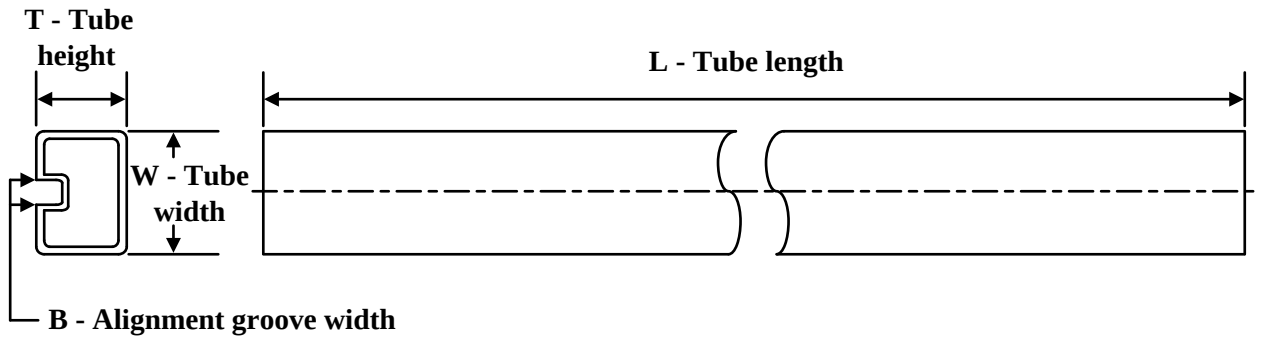
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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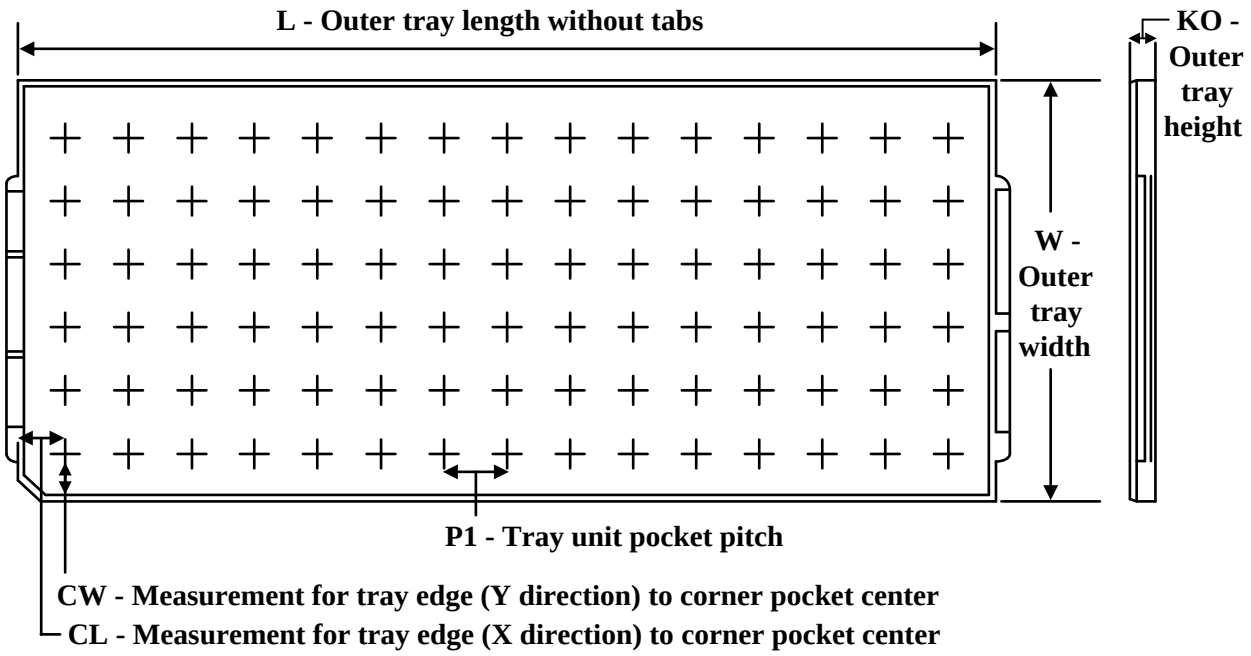
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM747J/883	J	CDIP	14	25	506.98	15.24	13440	NA

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

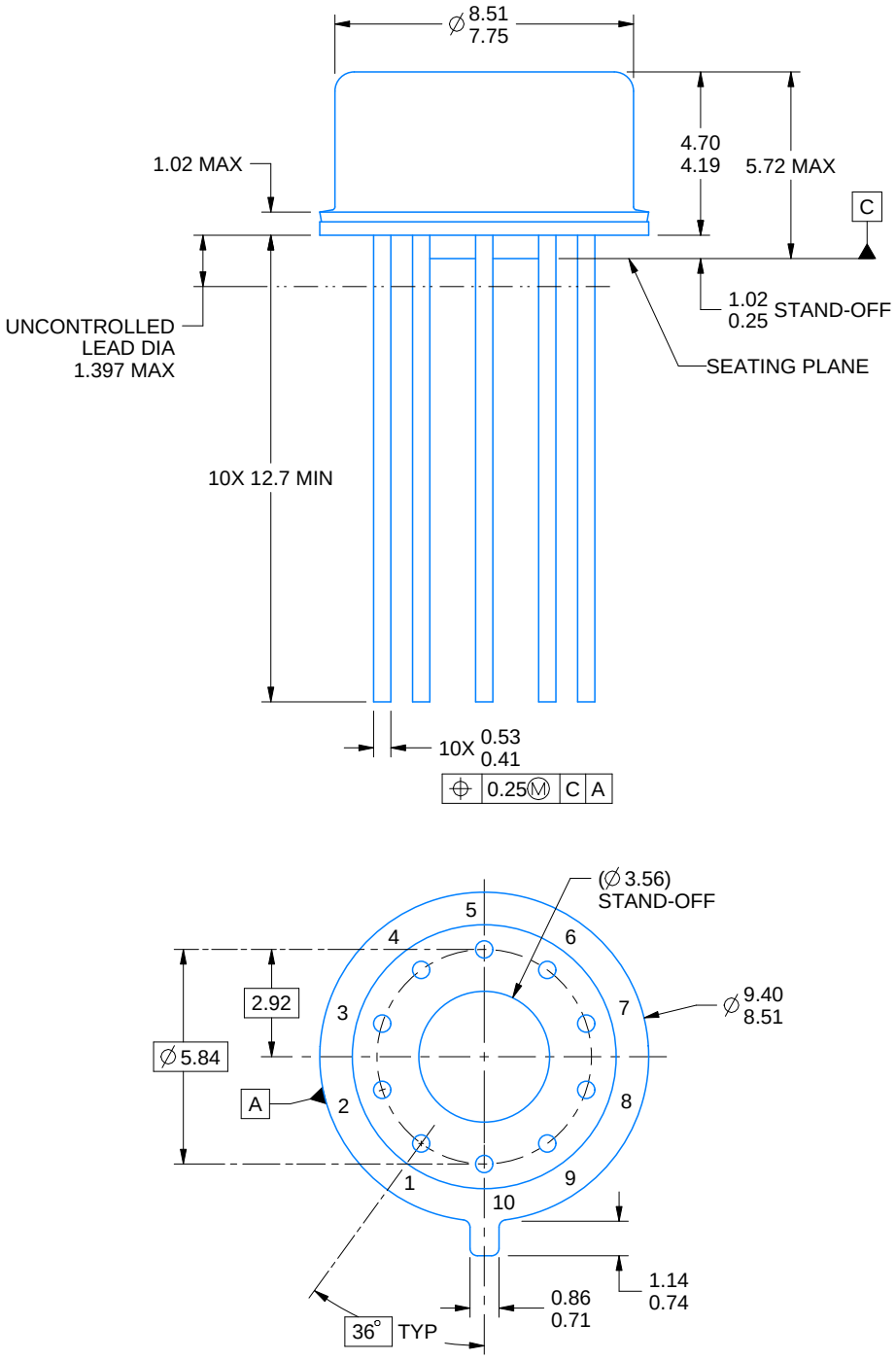
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
LM747H/883	LME	TO-CAN	10	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54

PACKAGE OUTLINE

LME0010A

TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



4220604/B 09/2024

NOTES:

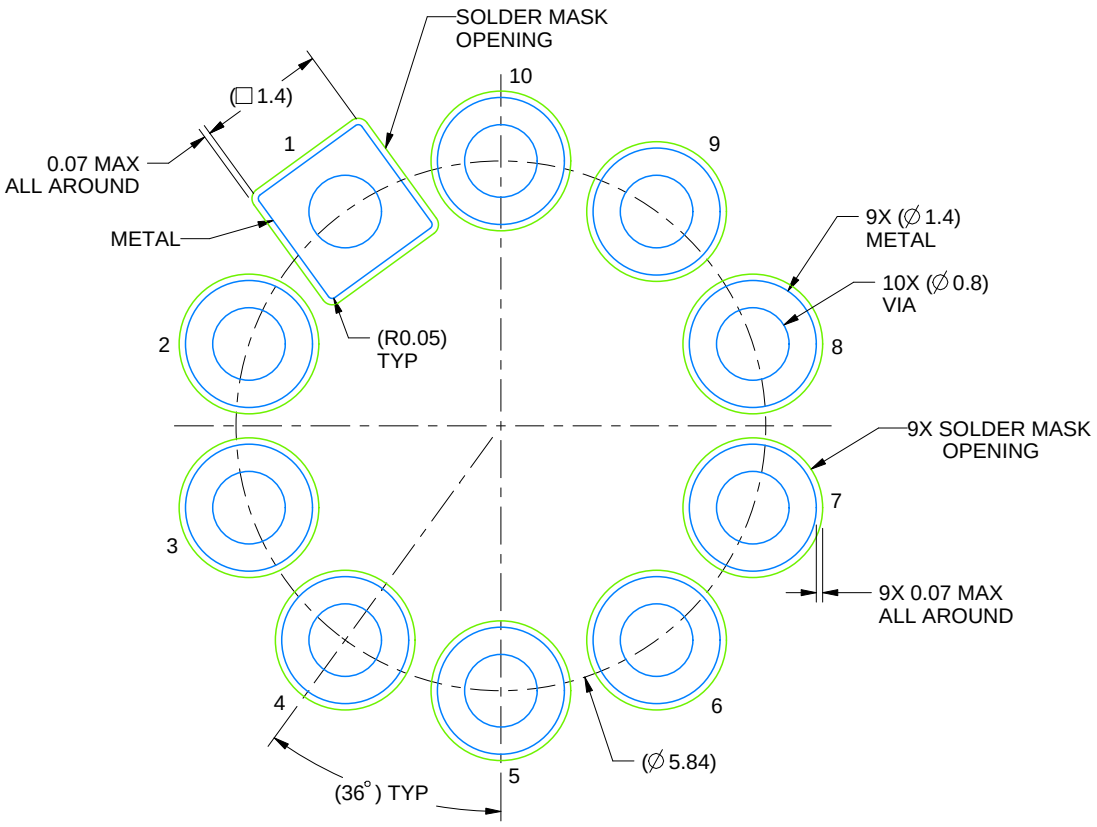
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-006/TO-100.

EXAMPLE BOARD LAYOUT

LME0010A

TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



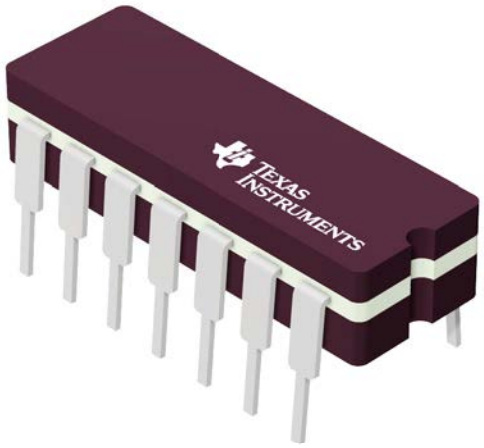
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

4220604/B 09/2024

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

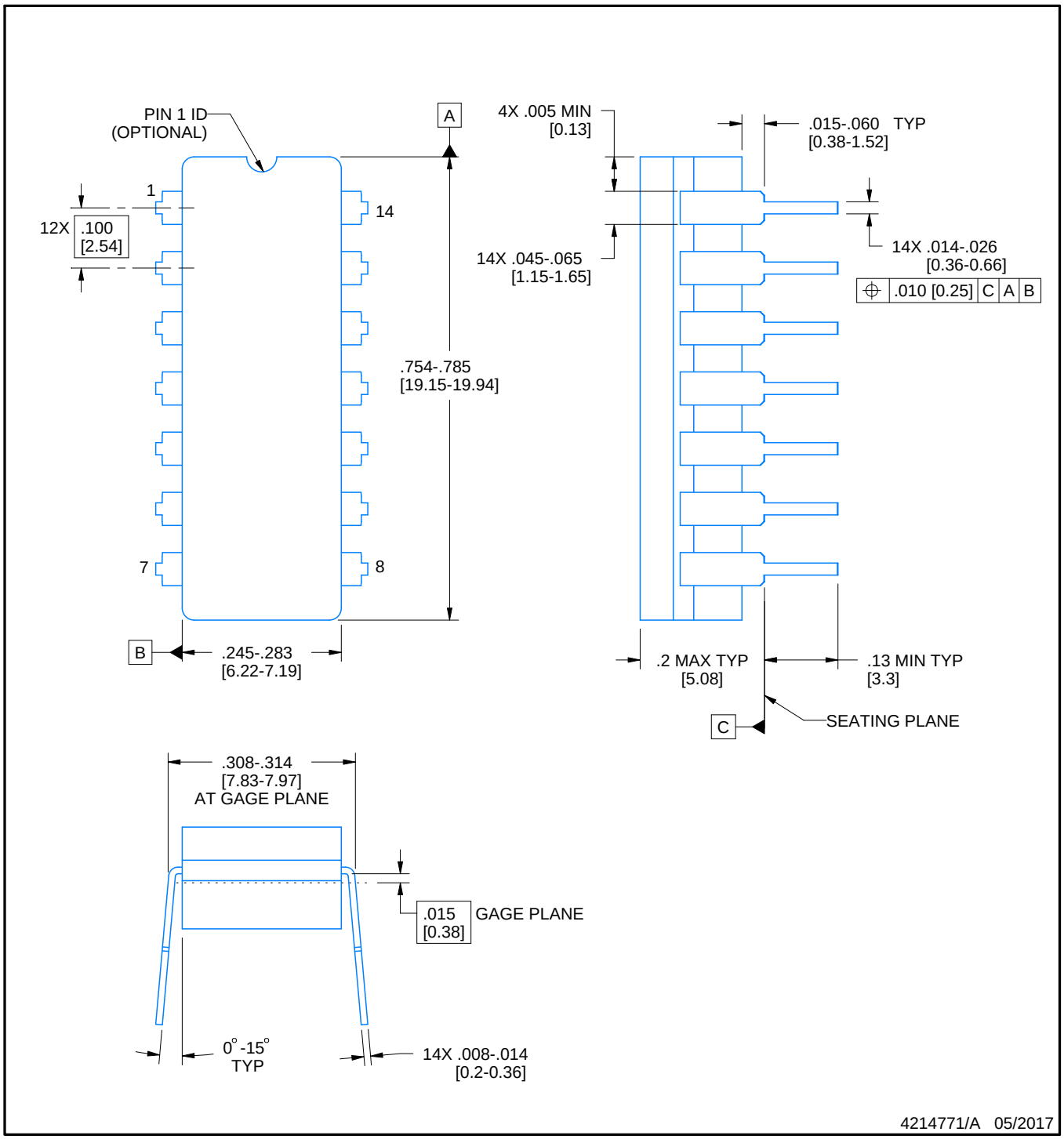


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

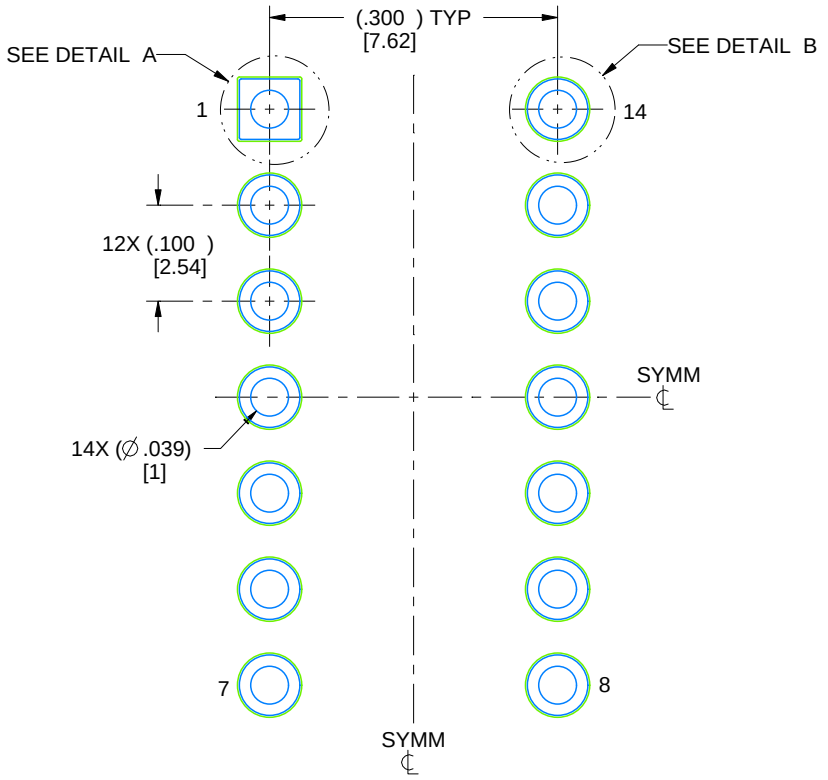
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

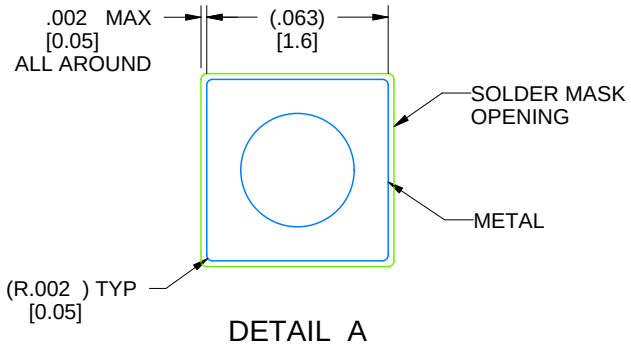
J0014A

CDIP - 5.08 mm max height

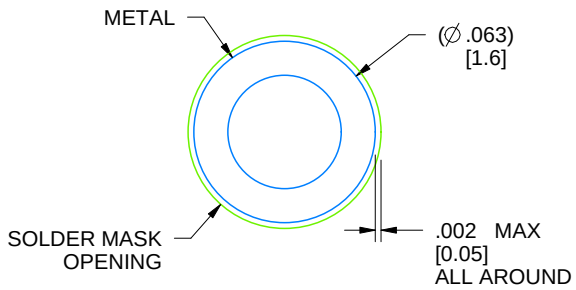
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

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