LMC555 CMOS Timer

1 Features

- Fast astable frequency of 3MHz
- Available in industry's smallest 8-bump DSBGA package (1.43mm × 1.41mm)
- Less than 1mW typical power dissipation at 5V supply
- 1.5V specified supply operating voltage
- output fully compatible with TTL and CMOS logic at 5V supply
- Tested to −10mA, 50mA output current levels
- Reduced supply current spikes during output transitions
- Extremely low reset, trigger, and threshold currents
- Excellent temperature stability
- Pin-for-pin compatible with 555 series of timers

2 Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generators

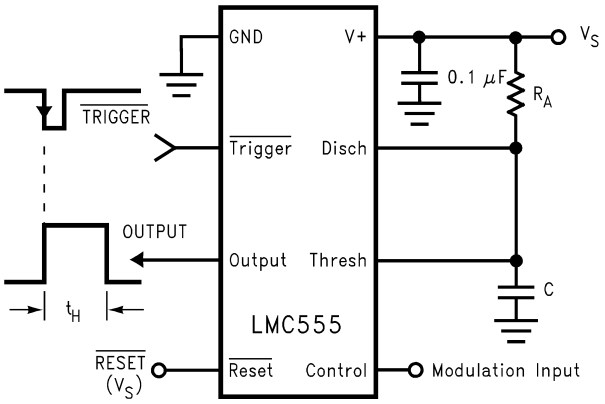
3 Description

The LMC555 device is a CMOS version of the industry standard 555 series general-purpose timers. In addition to the standard SOIC, VSSSOP, and PDIP packages, the LMC555 is also available in a chip-sized, 8-bump DSBGA package using TI's DSBGA package technology. The LMC555 offers the same capability of generating accurate time delays and frequencies as the LM555, but with much lower power dissipation and supply current spikes. When operated as a one-shot, the time delay is precisely controlled by a single external resistor and capacitor. In astable mode, the oscillation frequency and duty cycle are accurately set by two external resistors and one capacitor. TI's LMCMOS process extends both the frequency range and the low supply capability.

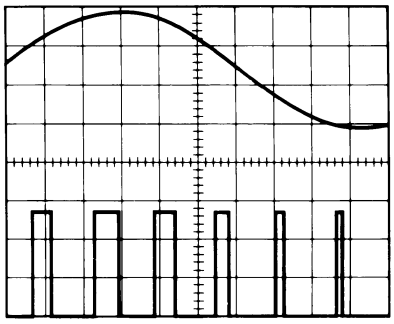
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMC555	D (SOIC, 8)	4.9mm × 6mm
	DGK (VSSOP, 8)	3mm × 4.9mm
	P (PDIP, 8)	9.81mm × 9.43mm
	YBF (DSBGA, 8)	1.75mm × 1.75mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Pulse Width Modulator



Pulse Width Modulator Waveform:
Top Waveform—Modulation
Bottom Waveform—Output Voltage

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4 Pin Configuration and Functions

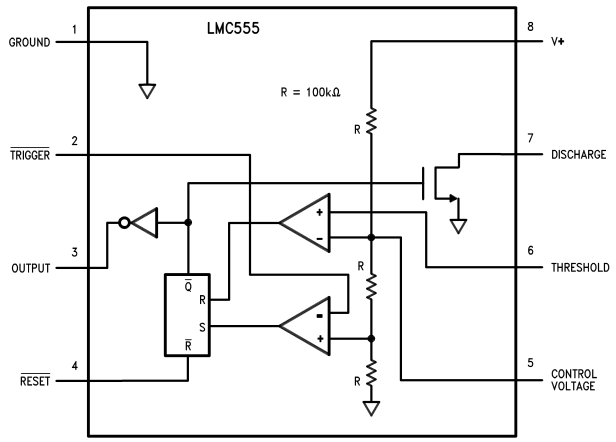


Figure 4-1. D Package, 8-Pin SOIC, DGK Package, 8-Pin VSSOP, and P Package, 8-Pin PDIP (Top View)

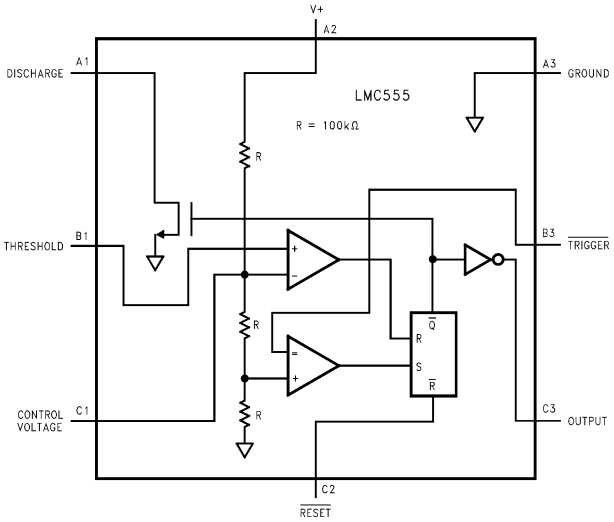


Figure 4-2. YPB Package, 8-Pin DSBGA (Top View)

Table 4-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	NO.			
	D (SOIC), DGK (VSSOP), P (PDIP)	YPB (DSBGA)		
CONTROL VOLTAGE	5	C1	Input	Control voltage controls the threshold and trigger levels. This pin determines the pulse duration of the output waveform. An external voltage applied to this pin can also be used to modulate the output waveform.
DISCHARGE	7	A1	Output	Open collector output that discharges a capacitor between intervals (in phase with output). This pin toggles the output from high to low when voltage reaches 2/3 of the supply voltage (V+).
GROUND	1	A3	Power	Ground reference voltage
OUTPUT	3	C3	Output	Output driven waveform
$\overline{\text{RESET}}$	4	C2	Input	Negative pulse applied to this pin to disable or reset the timer. When not used for reset purposes, connect this pin to V+ to avoid false triggering.
THRESHOLD	6	B1	Input	Compares the voltage applied to the pin with a reference voltage of 2/3 V+. The amplitude of voltage applied to this pin is responsible for the set state of the flip-flop.
$\overline{\text{TRIGGER}}$	2	B3	Input	Responsible for transition of the flip-flop from set to reset. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin.
V+	8	A2	Power	Supply voltage with respect to ground

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted.(1)(2)(3)

		MIN	MAX	UNIT
Voltage	Supply		15	V
	Input	–0.3	(V+) + 0.3	
	Output		15	
Current	Output		100	mA
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 5.3*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See AN-1112 (SNVA009) for DSBGA considerations.
(3) If military- or aerospace-specified devices are required, contact the TI Sales Office or Distributors for availability and specifications.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Temperature	LMC555IM	−40		125	°C
	LMC555CM, MM, N, TP	−40		85	
Maximum allowable power dissipation at 25°C	PDIP-8			1126	mW
	SOIC-8			740	
	VSSOP-8			555	
	8-bump DSBGA			568	

5.4 Thermal Information

THERMAL METRIC(1)		LMC555				UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	YPB (DSBGA)	
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.9	188.3	93.1	102.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.8	78.8	82.5	0.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.9	110.2	69.6	31.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.2	18.5	52.0	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	86.9	108.6	69.2	31.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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5.5 Electrical Characteristics

Test Circuit, T = 25°C, all switches open, $\overline{\text{RESET}}$ to V_S unless otherwise noted(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Supply current	V_S = 1.5V		130	200	µA
		V_S = 5V		180	250	
		V_S = 12V		220	400	
V_{CTRL}	Control voltage	V_S = 1.5V	0.8	1.0	1.2	V
		V_S = 5V	2.9	3.3	3.8	
		V_S = 12V	7.4	8.0	8.6	
V_{DIS}	Discharge saturation voltage	V_S = 1.5V, I_{DIS} = 1mA		75	150	mV
		V_S = 5V, I_{DIS} = 10mA		150	300	
V_{OL}	Output voltage (low)	V_S = 1.5V, I_O = 1mA		0.2	0.4	V
		V_S = 5V, I_O = 8mA		0.3	0.6	
		V_S = 12V, I_O = 50mA		1.0	2.0	
V_{OH}	Output voltage (high)	V_S = 1.5V, I_O = −0.25mA	1.0	1.25		V
		V_S = 5V, I_O = −2mA	4.4	4.7		
		V_S = 12V, I_O = −10mA	10.5	11.3		
V_{TRIG}	Trigger voltage	V_S = 1.5V	0.4	0.5	0.6	V
		V_S = 12V	3.7	4.0	4.3	
I_{TRIG}	Trigger current	V_S = 5V		10		pA
V_{RES}	Reset voltage	V_S = 1.5V (2)	0.4	0.7	1.0	V
		V_S = 12V	0.4	0.75	1.1	
I_{RES}	Reset current	V_S = 5V		10		pA
I_{THRESH}	Threshold current	V_S = 5V		10		pA
I_{DIS}	Discharge leakage	V_S = 12V		1.0	100	nA

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) If the $\overline{\text{RESET}}$ pin is to be used at temperatures of −20°C and less, then ensure that V_S is 2.0V or greater.

5.6 Switching Characteristics

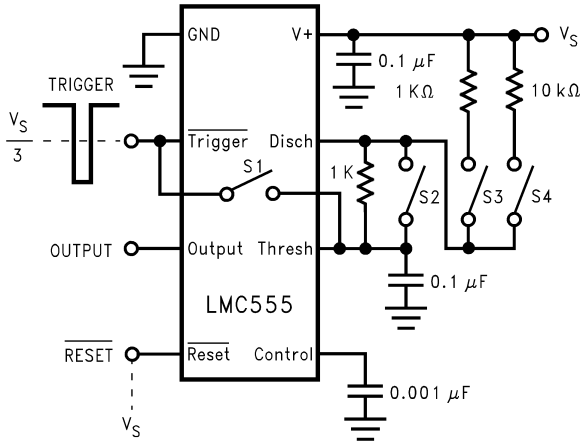
Test Circuit, T = 25°C, all switches open, $\overline{\text{RESET}}$ to V_S unless otherwise noted.(1) Characteristic values are specified by design, characterization, or both.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t	Timing accuracy	SW 2, 4 closed	V_S = 1.5V	0.9	1.1	1.25	ms
			V_S = 5V	1.0	1.1	1.20	
			V_S = 12V	1.0	1.1	1.25	
$\Delta t/\Delta V_S$	Timing shift with supply	V_S = 5V ± 1V			0.3		%/V
$\Delta t/\Delta T$	Timing shift with temperature	V_S = 5V			75		ppm/°C
f_A	Astable frequency	SW 1, 3 closed, V_S = 12V		4.0	4.8	5.6	kHz
f_{MAX}	Maximum frequency	Maximum frequency test circuit, V_S = 5V			2.4		MHz
t_R, t_F	Output rise and fall times	Maximum frequency test circuit V_S = 5V, C_L = 10pF			15		ns
t_{PD}	Trigger propagation delay	V_S = 5V, measure delay from trigger to output			150		ns

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.

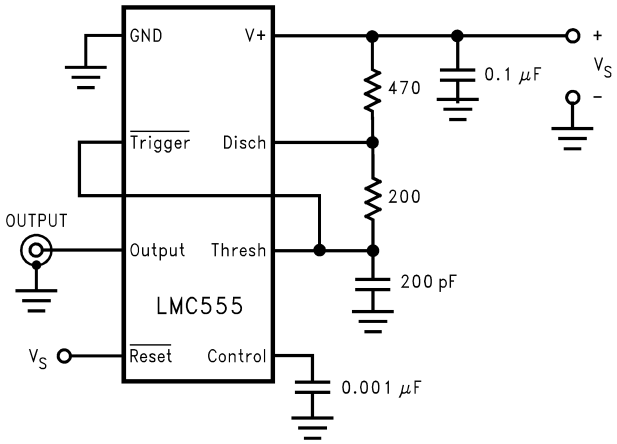
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6 Parameter Measurement Information



For device pinout, see *Section 4*.

Figure 6-1. Test Circuit



For device pinout, see *Section 4*.

Figure 6-2. Maximum Frequency Test Circuit

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7 Detailed Description

7.1 Overview

The LMC555 is a CMOS version of the industry standard 555 series general-purpose timers. In addition to the standard SOIC, VSSSOP, and PDIP packages, the LMC555 is also available in a chip-sized package (8-bump DSBGA) using TI's DSBGA package technology. The LMC555 offers the same capability of generating accurate time delays and frequencies as the LM555 but with much lower power dissipation and supply current spikes. When operated as a one-shot, the time delay is precisely controlled by a single external resistor and capacitor. In the astable mode, the oscillation frequency and duty cycle are accurately set by two external resistors and one capacitor. The use of TI's LMCMOS process extends both the frequency range and the low supply capability.

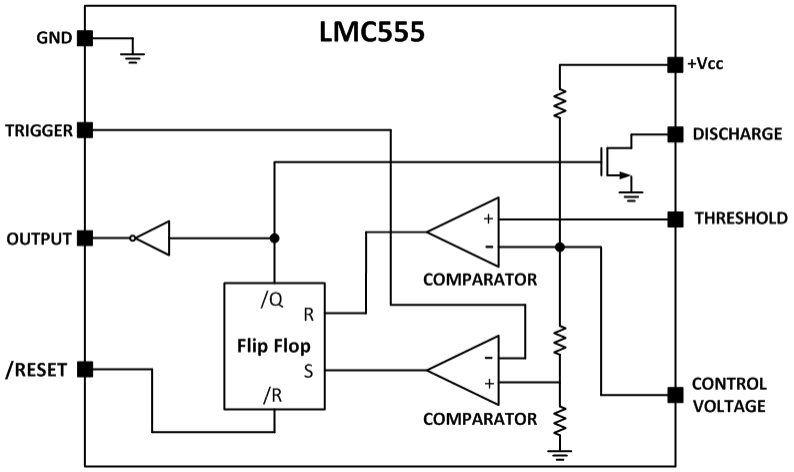
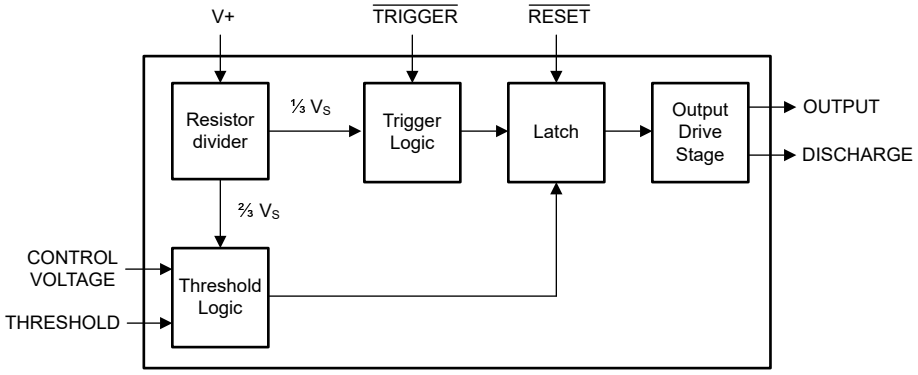


Figure 7-1. Simplified Schematic

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Low-Power Dissipation

The LMC555 offers the same capability of generating accurate time delays and frequencies as the LM555 but with much lower power dissipation. A power dissipation of less than 0.2mW can be achieved with a 1.5V operating supply voltage and less than 1mW with a 5V operating supply voltage. The use of TI's LMCMOS process allows this low supply current and voltage capability. Reduced supply current spikes during output transitions and extremely low reset, trigger and threshold currents also provide low power dissipation advantages with the LMC555.

7.3.2 Various Packages and Compatibility

There are various packages available for use of the LMC555. In addition to the standard package (8-pin SOIC, VSSOP, and PDIP, the LMC555 is also available in a chip-sized package (8-bump DSBGA). The PDIP, SOIC, and VSSOP packages for the LMC555 are pin-for-pin compatible with the 555 series of timers (NE555/SE555/LM555) allowing flexibility in design and unnecessary modifications to PCB schematics and layouts.

7.3.3 Operates in Both Astable and Monostable Mode

The LMC555 can operate in both astable and monostable mode depending on the application requirements.

- Monostable mode: The LMC555 timer acts as a "one-shot" pulse generator. The pulse begins when the LMC555 timer receives a signal at the trigger input that falls below a 1/3 of the voltage supply. The width of the output pulse is determined by the time constant of an RC network. The output pulse ends when the voltage on the capacitor equals 2/3 of the supply voltage. The output pulse width can be extended or shortened depending on the application by adjusting the R and C values.
- Astable (free-running) mode: The LMC555 timer can operate as an oscillator and puts out a continuous stream of rectangular pulses having a specified frequency. The frequency of the pulse stream depends on the values of RA, RB, and C.

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7.4 Device Functional Modes

7.4.1 Monostable Operation

In this mode of operation, the timer functions as a one-shot (Figure 7-2). The external capacitor is initially held discharged by internal circuitry. Upon application of a negative trigger pulse of less than 1/3 V_S to the $\overline{\text{TRIGGER}}$ pin, the flip-flop is set, which both releases the short circuit across the capacitor and drives the output high.

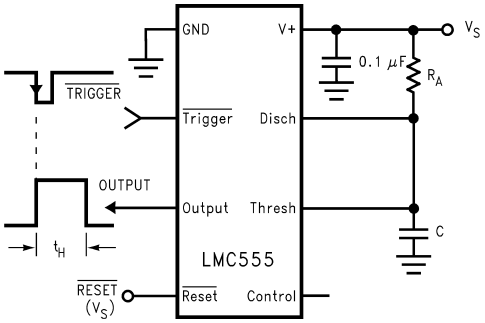
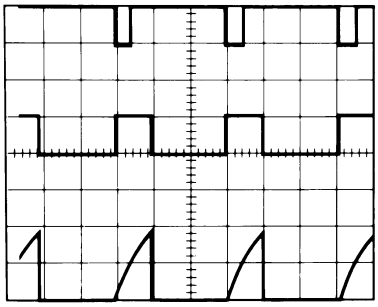


Figure 7-2. Monostable (One-Shot)

The voltage across the capacitor then increases exponentially for a period of t_H = 1.1 R_AC. This period is also the time that the output stays high, at the end of which time the voltage equals 2/3 V_S. The comparator then resets the flip-flop, which in turn discharges the capacitor and drives the output to the low state. Figure 7-3 shows the waveforms generated in this mode of operation. Because the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.



V_S = 5V
TIME = 0.1ms/div
Top trace: Input 5V/div
Middle trace: Output 5V/div
Bottom trace: Capacitor voltage 2V/div
R_A = 9.1kΩ
C = 0.01µF

Figure 7-3. Monostable Waveforms

$\overline{\text{RESET}}$ overrides $\overline{\text{TRIGGER}}$, which can override THRESHOLD. Therefore, ensure that the trigger pulse is shorter than the desired t_H. The minimum pulse duration for $\overline{\text{TRIGGER}}$ is 20ns, and is 400ns for $\overline{\text{RESET}}$. During the timing cycle when the output is high, the further application of a trigger pulse does not effect the circuit as long as the trigger input is returned high at least 10µs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the $\overline{\text{RESET}}$ pin. The output remains in the low state until a trigger pulse is applied again.

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When the reset function is not used, connect the $\overline{\text{RESET}}$ pin to V+ to avoid any possibility of false triggering. Figure 7-4 is a nomograph for easy determination of RC values for various time delays.

Note

In monostable operation, drive the trigger high before the end of timing cycle.

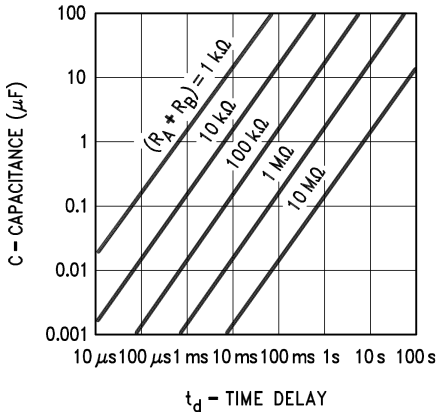


Figure 7-4. Time Delay

7.4.2 Astable Operation

If the circuit is connected as shown in Figure 7-5 ($\overline{\text{TRIGGER}}$ and THRESHOLD pins connected together), the circuit triggers and free runs as a multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus, the duty cycle can be precisely set by the ratio of these two resistors.

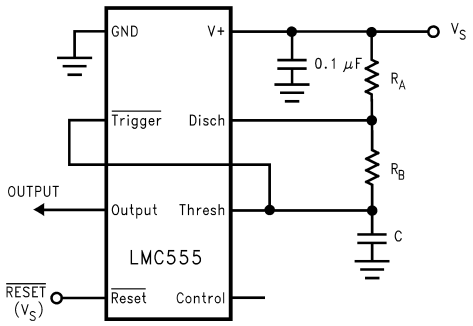
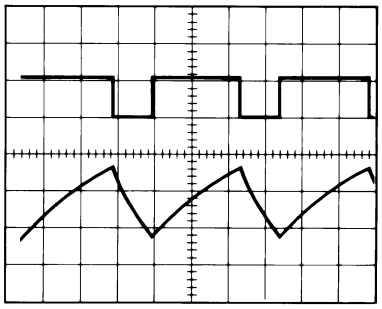


Figure 7-5. Astable (Variable Duty Cycle Oscillator)

In this mode of operation, the capacitor charges and discharges between 1/3 V_S and 2/3 V_S. As in the triggered mode, the charge and discharge times, and therefore, the frequency are independent of the supply voltage.

Figure 7-6 shows the waveform generated in this mode of operation.

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V_S = 5V
TIME = 20µs/div
Top trace: Output 5V/div
Bottom trace: Capacitor voltage 1V/div
R_A = 1.78kΩ
R_B = 4.12kΩ
C = 0.01µF

Figure 7-6. Astable Waveforms

The charge time (output high) is given by

$$t_1 = 0.693\ (R_A + R_B)C \quad (1)$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)C \quad (2)$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)C \quad (3)$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C} \quad (4)$$

Figure 7-7 can be used for quick determination of these RC Values. The duty cycle, as a fraction of total period that the output is low, is:

$$D = \frac{R_B}{R_A + 2R_B} \quad (5)$$

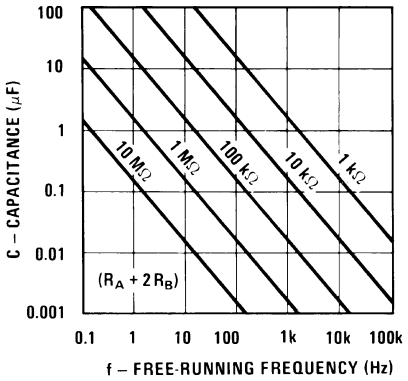


Figure 7-7. Free-Running Frequency

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMC555 timer can be used a various configurations, but the most commonly used configuration is in monostable mode. A typical application for the LMC555 timer in monostable mode is to turn on an LED for a specific time duration. A pushbutton is used as the trigger to output a high pulse when trigger pin is pulsed low. This simple application can be modified to fit any application requirement.

8.2 Typical Applications

8.2.1 Flash LED in Monostable Mode

Figure 8-1 shows the schematic of an LMC555 that flashes an LED in monostable mode.

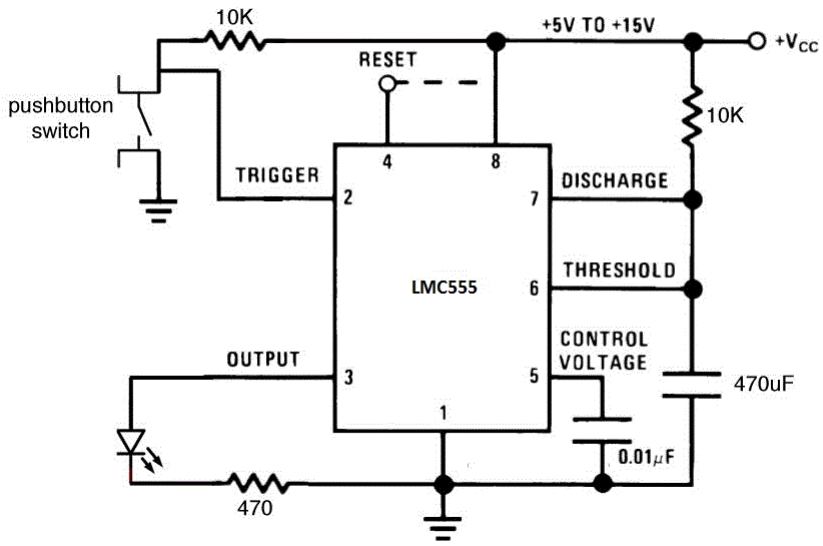


Figure 8-1. Schematic of Monostable Mode to Flash an LED

8.2.1.1 Design Requirements

The main design requirement for this application requires calculating the duration of time that the output stays high. The duration of time depends on the R and C values (shown in Figure 7-4) and is calculated by the following equation:

$$t = 1.1 \times R \times C \text{ seconds} \quad (6)$$

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8.2.1.2 Detailed Design Procedure

To allow the LED to flash on for a noticeable amount of time, a 5-second time delay was chosen for this application. Using Equation 6, R × C equals 4.545.

If R is chosen as 100kΩ, C = 45.4µF. The values of R = 100kΩ and C = 47µF were chosen based on standard values of resistors and capacitors.

A momentary push button switch connected to ground is connected to the trigger input with a 10kΩ current limiting resistor pull up to the supply voltage. When the push button is pressed, the $\overline{\text{TRIGGER}}$ pin goes to GND. An LED is connected to the OUTPUT pin with a current limiting resistor in series from the output of the LMC555 to GND. The $\overline{\text{RESET}}$ pin is not used and was connected to the supply voltage.

8.2.1.3 Application Curve

The data shown in Figure 8-2 were collected with the circuit used in the typical applications section. The LMC555 was configured in the monostable mode with a time delay of 5.17s. The waveforms correspond to:

- Top Waveform (Blue) – Capacitor voltage
- Middle Waveform (Purple) – $\overline{\text{TRIGGER}}$
- Bottom Waveform (Green) – OUTPUT

As the $\overline{\text{TRIGGER}}$ pin pulses low, the capacitor voltage starts charging and the output goes high. The output goes low as soon as the capacitor voltage reaches 2/3 of the supply voltage, which is the time delay set by the R and C value. For this example, the time delay is 5.17 seconds.

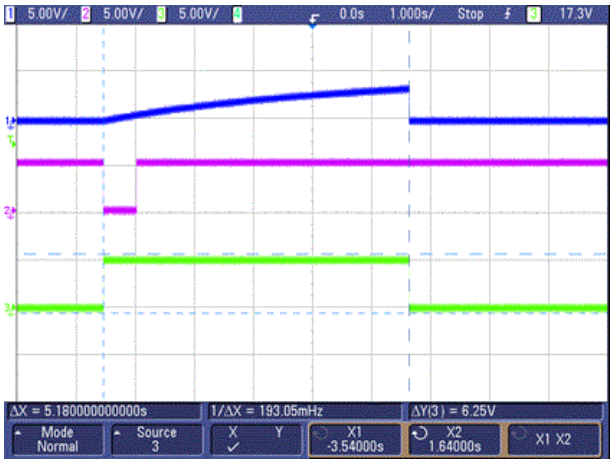


Figure 8-2. $\overline{\text{TRIGGER}}$, Capacitor Voltage, and OUTPUT Waveforms in Monostable Mode

8.2.2 Frequency Divider

The monostable circuit of Figure 8-3 can be used as a frequency divider by adjusting the length of the timing cycle. Figure 8-4 shows the waveforms generated in a divide by three circuit.

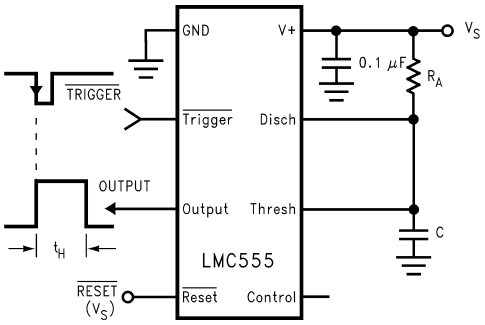


Figure 8-3. Monostable (One-Shot)

8.2.2.1 Design Requirements

Design a frequency divider by adjusting the length of the timing cycle.

8.2.2.2 Application Curve

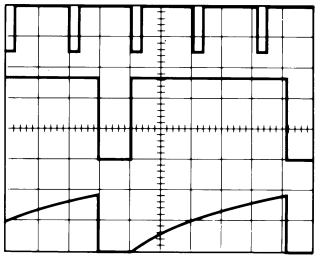


Figure 8-4. Frequency Divider Waveforms

8.2.3 Pulse Width Modulator

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to the control voltage terminal. Figure 8-5 shows the circuit, and in Figure 8-6 are some waveform examples.

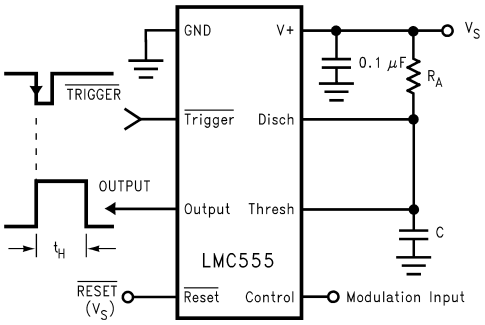


Figure 8-5. Pulse Width Modulator

8.2.3.1 Design Requirements

Modulator the output pulse width by the signal applied to the control voltage terminal.

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8.2.3.2 Application Curve

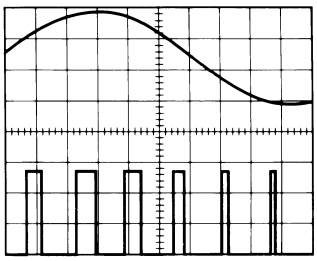


Figure 8-6. Pulse Width Modulator Waveforms

8.2.4 Pulse Position Modulator

This application uses the timer connected for astable operation, as in Figure 8-7, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 8-8 shows the waveforms generated for a triangle wave modulation signal.

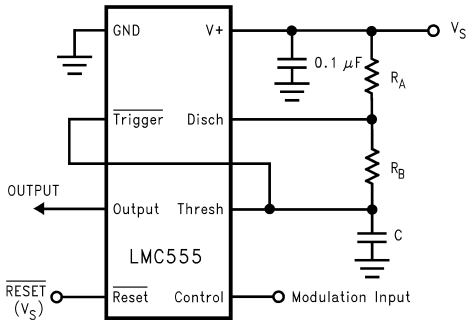


Figure 8-7. Pulse Position Modulator

8.2.4.1 Design Requirements

Using astable operation vary the pulse position with a modulating signal applied to the control voltage terminal.

8.2.4.2 Application Curve

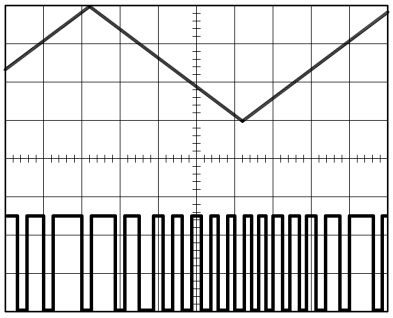


Figure 8-8. Pulse Position Modulator Waveforms

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8.2.5 50% Duty Cycle Oscillator

The frequency of oscillation is:

$$f = 1/(1.4\ R_C C) \quad (7)$$

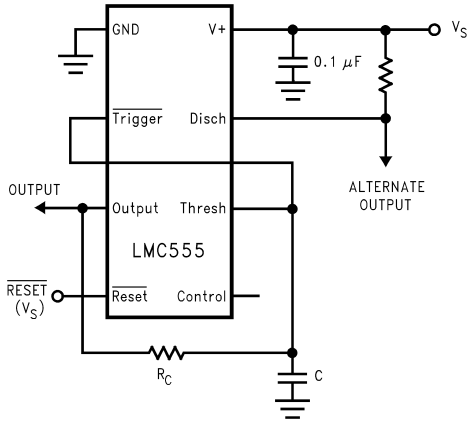


Figure 8-9. 50% Duty Cycle Oscillator

8.2.5.1 Design Requirements

An oscillator with a 50% duty cycle output.

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8.3 Power Supply Recommendations

The LMC555 requires a voltage supply within 1.5V to 15V. Adequate power supply bypassing is necessary to protect associated circuitry; the minimum recommended is 0.1µF in parallel with 1µF electrolytic. Place the bypass capacitors as close as possible to the LMC555 and minimize the trace length.

8.4 Layout

8.4.1 Layout Guidelines

Standard PCB rules apply to routing the LMC555. Keep the 0.1µF capacitor in parallel with a 1µF electrolytic capacitor as close as possible to the LMC555. Place the capacitor used for the time delay as close as possible to the DISCHARGE pin. Use a ground plane on the bottom layer to provide better noise immunity and signal integrity.

8.4.2 Layout Example

The figure below is the basic layout for various applications.

- C1 – based on time delay calculations
- C2 – 0.01µF bypass capacitor for control voltage pin
- C3 – 0.1µF bypass ceramic capacitor
- C4 – 1µF electrolytic bypass capacitor
- R1 – based on time delay calculations
- U1 – LMC555

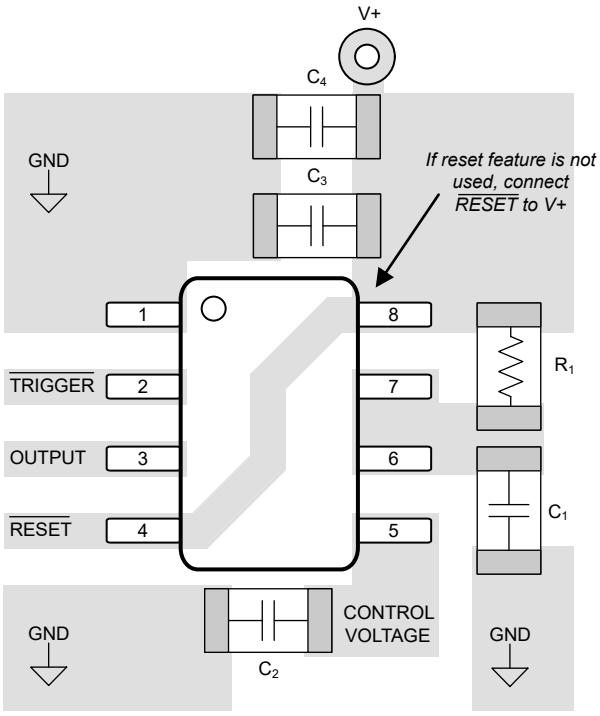


Figure 8-10. PCB Layout

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9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision N (March 2024) to Revision O (November 2026)	Page
• Changed DISCHARGE type to Output in *Pin Configuration and Functions*	3
• Changed Reset current (I_{RES}) test condition to be V_{RES} independent in *Electrical Characteristics*	5
• Changed Maximum frequency (f_{MAX}) typical value from 3MHz to 2.4MHz in *Switching Characteristics*	5
• Changed Trigger propagation delay (t_{PD}) typical value from 100ns to150ns in *Switching Characteristics*	5

Changes from Revision M (July 2016) to Revision N (March 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated wording of *Features* bullets for clarity	1
• Updated GROUND and V+ pin types in *Pin Configuration and Functions*	3
• Changed V_{CC} to V+ in *Pin Configuration and Functions*	3
• Added (V+) to DISCHARGE description in *Pin Configuration and Functions*	3
• Updated $R_{\theta JA}$ and added detailed thermal characteristics for all packages in *Thermal Information*	4
• Moved timing accuracy, timing shift with supply, timing shift with temperature, astable frequency, maximum frequency, output rise and fall times, and trigger propagation delay parameters from *Electrical Characteristics* to *Switching Characteristics*	5
• Changed supply current (I_S) typical values from 50µA to 130µA at V_S = 1.5V; from 100µA to 180µA at V_S = 1.5V; and from 150µA to 220µA at V_S = 12V, in *Electrical Characteristics*	5
• Changed supply current (I_S) max value from 150µA to 200µA at V_S = 1.5V in *Electrical Characteristics*	5
• Changed reset current (I_{RES}) test condition to V_{RES} = V_S in *Electrical Characteristics*	5
• Added new reset current (I_{RES}) typical value for test condition V_{RES} = 0V to *Electrical Characteristics*	5

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- Updated *Switching Characteristics* to clarify that values are specified by design, characterization, or both.....5
- Changed units of timing shift with temperature from %V to %/V (typo) in *Switching Characteristics*.....5
- Changed functional block diagram to simplified schematic and moved to *Overview*.....7
- Updated *Functional Block Diagram*.....7
- Changed values of R_A from 3.9kΩ to 1.78kΩ, and R_B and 9kΩ to 4.12kΩ in Figure 7-6.....10
- Changed "LM555" to "LMC555" (typo) in *Typical Applications*.....12
- Updated figure in *Layout Example*.....17

Changes from Revision L (February 2016) to Revision M (July 2016) **Page**

- Changed order of *Features*.....1
- Changed stable to astable (typo).....1
- Changed stable to astable - typo. 7
- Changed beings to begins typo.....8
- Changed typo LM555 to LMC555. 12
- Changed typo LM555 to LMC555. 12
- Added additional applications. 14

Changes from Revision K (January 2015) to Revision L (February 2016) **Page**

- Changed typo - temp range from 185 to 85 4

Changes from Revision J (March 2013) to Revision K (October 2014) **Page**

- Added *Pin Configuration and Functions*, *ESD Ratings*, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections 1

Changes from Revision I (March 2013) to Revision J (March 2013) **Page**

- Changed layout of National Semiconductor Data Sheet to TI format 17

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMC555CM/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	LMC 555CM
LMC555CMM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	ZC5
LMC555CMM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	ZC5
LMC555CMMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	ZC5
LMC555CMMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	ZC5
LMC555CMMX/NOPB.B	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	ZC5
LMC555CMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(LM555C, LMC) 555CM
LMC555CMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(LM555C, LMC) 555CM
LMC555CMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(LM555C, LMC) 555CM
LMC555CN/NOPB	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	(LMC, LMC555CN) 555CN
LMC555CN/NOPB.A	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	(LMC, LMC555CN) 555CN
LMC555CN/NOPBG4	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	LMC555CN
LMC555CN/NOPBG4.A	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	LMC555CN
LMC555CTP/NOPB	Active	Production	DSBGA (YPB) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	F 02
LMC555CTP/NOPB.A	Active	Production	DSBGA (YPB) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	F 02
LMC555CTP/NOPB.B	Active	Production	DSBGA (YPB) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	F 02
LMC555CTPX/NOPB	Active	Production	DSBGA (YPB) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	F 02
LMC555CTPX/NOPB.A	Active	Production	DSBGA (YPB) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	F 02
LMC555CTPX/NOPB.B	Active	Production	DSBGA (YPB) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	F 02

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMC555IM/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	LMC 555IM
LMC555IMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LM555I, LMC) 555IM
LMC555IMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LM555I, LMC) 555IM
LMC555IMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LM555I, LMC) 555IM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

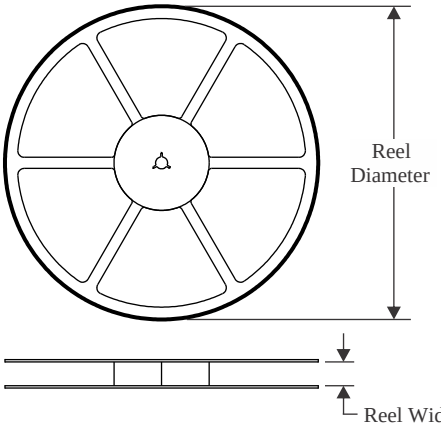
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

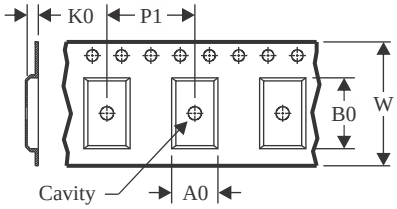
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

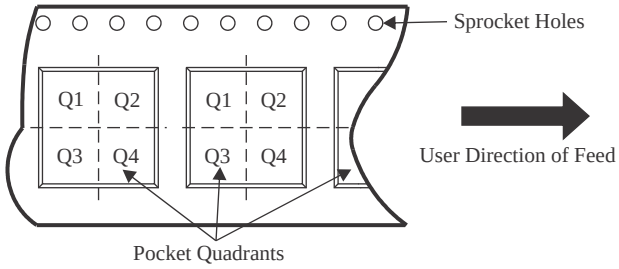


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

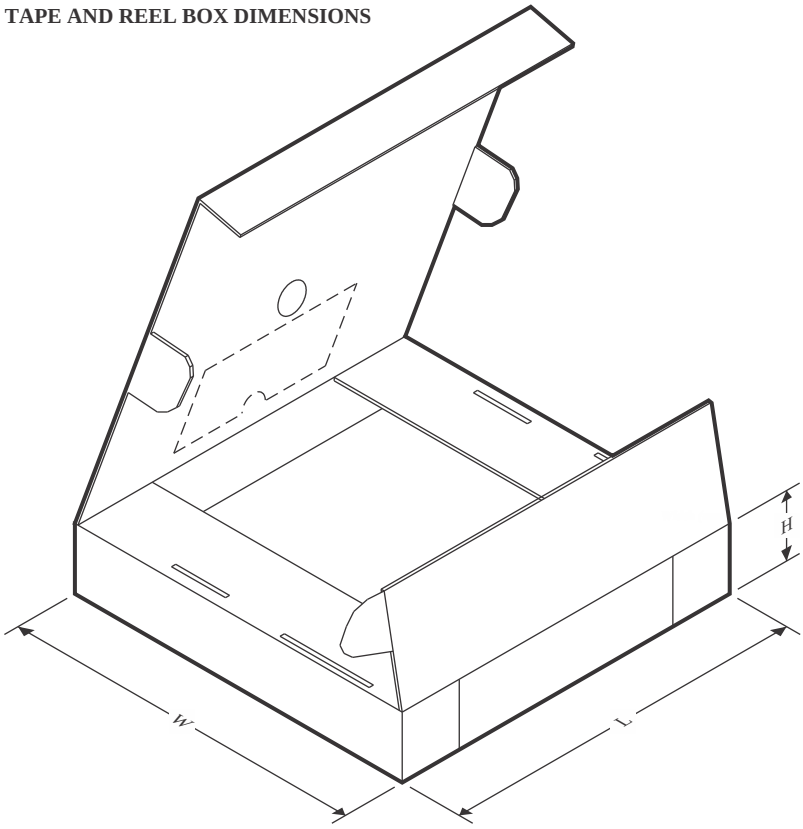
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC555CMM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC555CMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC555CMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
LMC555CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMC555CTP/NOPB	DSBGA	YPB	8	250	178.0	8.4	1.5	1.5	0.66	4.0	8.0	Q1
LMC555CTPX/NOPB	DSBGA	YPB	8	3000	178.0	8.4	1.5	1.5	0.66	4.0	8.0	Q1
LMC555IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

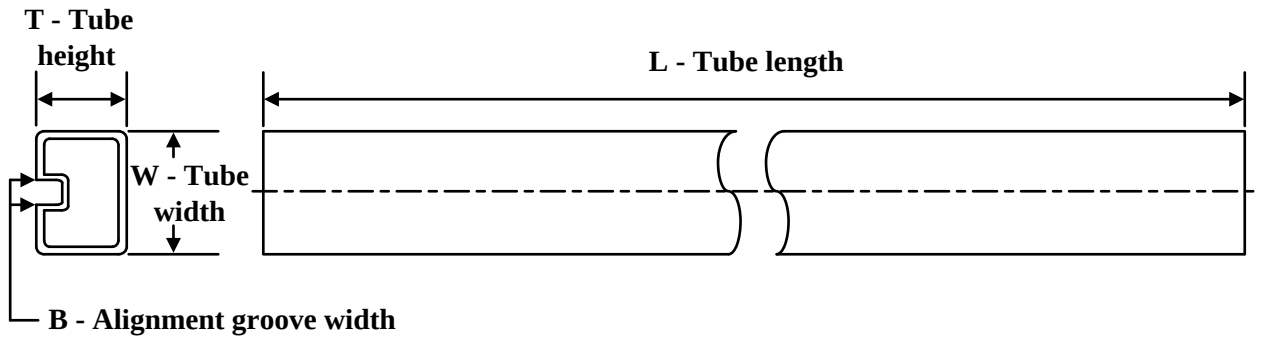
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

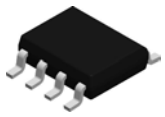
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC555CMM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMC555CMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMC555CMMX/NOPB	VSSOP	DGK	8	3500	366.0	364.0	50.0
LMC555CMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC555CTP/NOPB	DSBGA	YPB	8	250	208.0	191.0	35.0
LMC555CTPX/NOPB	DSBGA	YPB	8	3000	208.0	191.0	35.0
LMC555IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMC555CN/NOPB	P	PDIP	8	40	506	13.97	11230	4.32
LMC555CN/NOPB	P	PDIP	8	40	506	13.97	11230	4.32
LMC555CN/NOPB	P	PDIP	8	40	502	14	11938	4.32
LMC555CN/NOPB	P	PDIP	8	40	506	13.97	11230	4.32
LMC555CN/NOPB.A	P	PDIP	8	40	506	13.97	11230	4.32
LMC555CN/NOPB.A	P	PDIP	8	40	506	13.97	11230	4.32
LMC555CN/NOPB.A	P	PDIP	8	40	502	14	11938	4.32
LMC555CN/NOPB.A	P	PDIP	8	40	506	13.97	11230	4.32
LMC555CN/NOPBG4	P	PDIP	8	40	506	13.97	11230	4.32
LMC555CN/NOPBG4.A	P	PDIP	8	40	506	13.97	11230	4.32

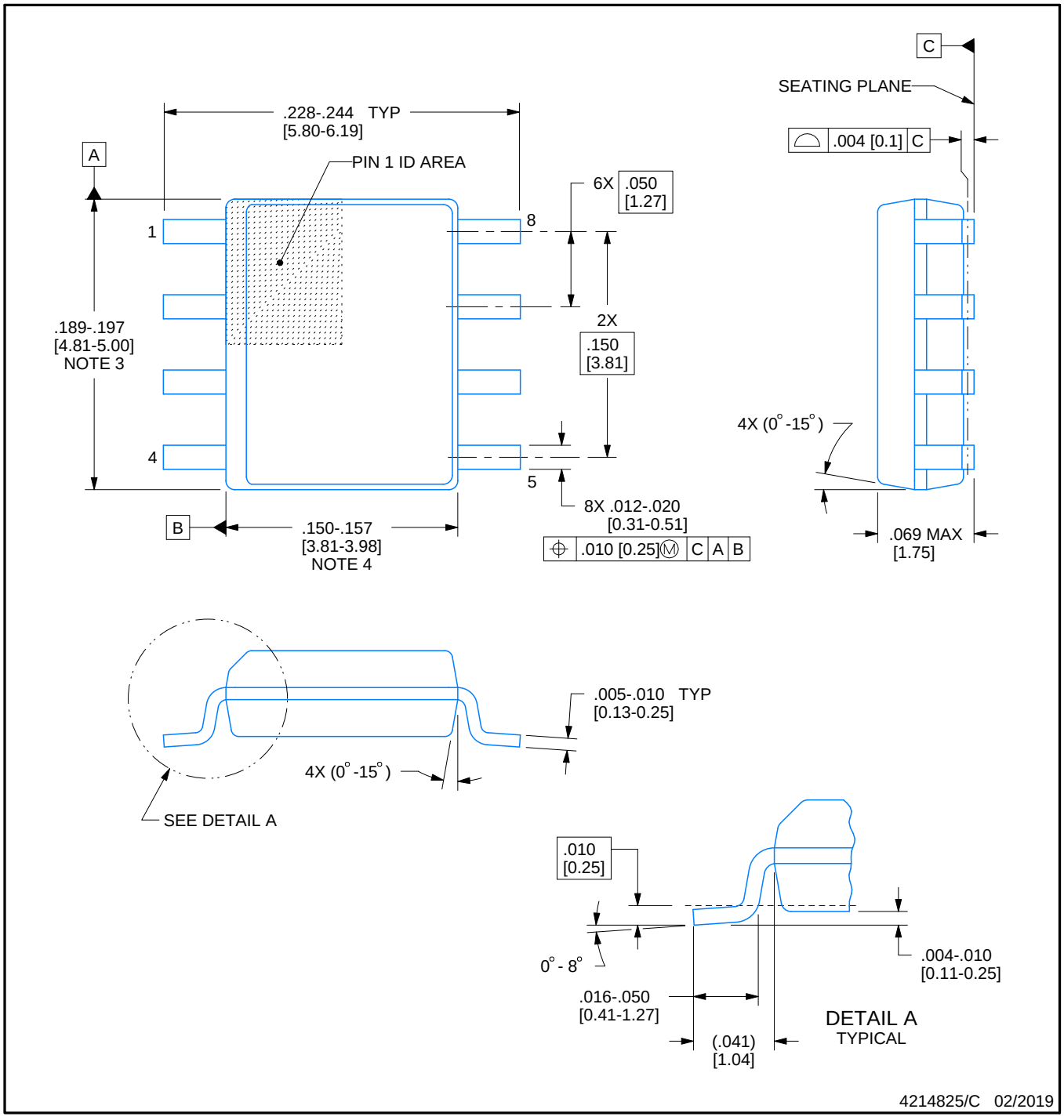


PACKAGE OUTLINE

D0008A

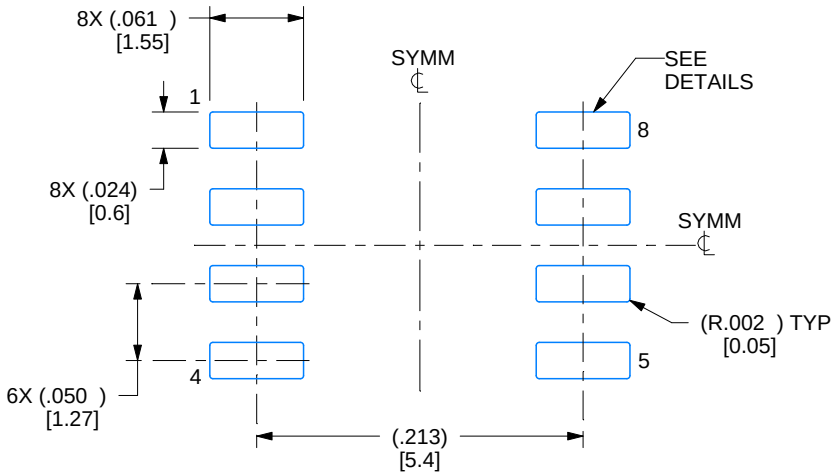
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

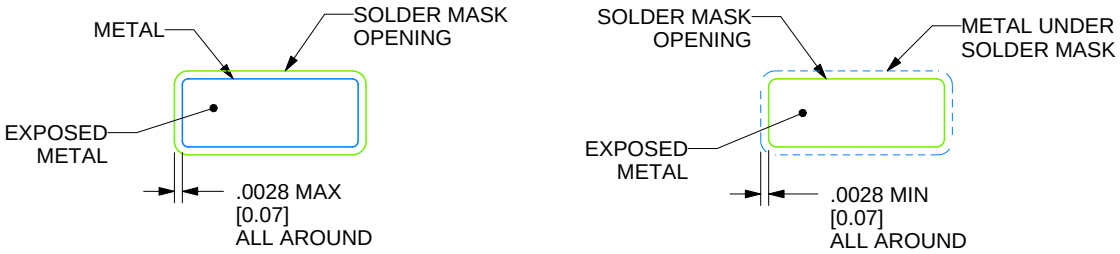


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

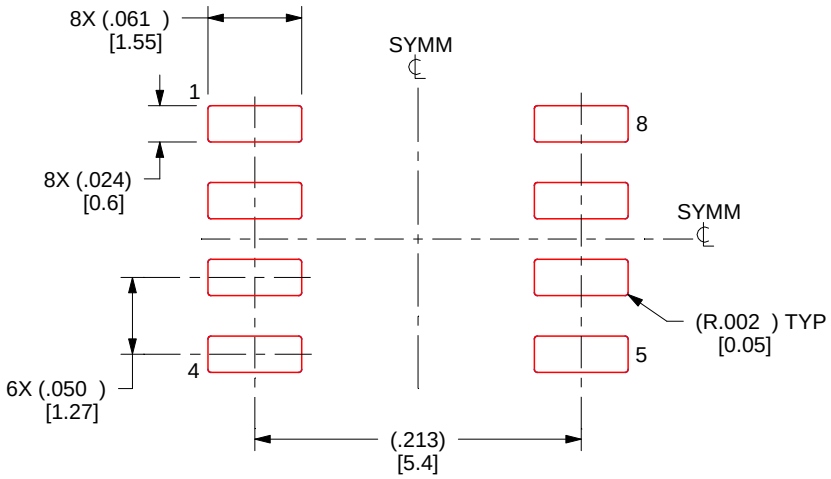
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



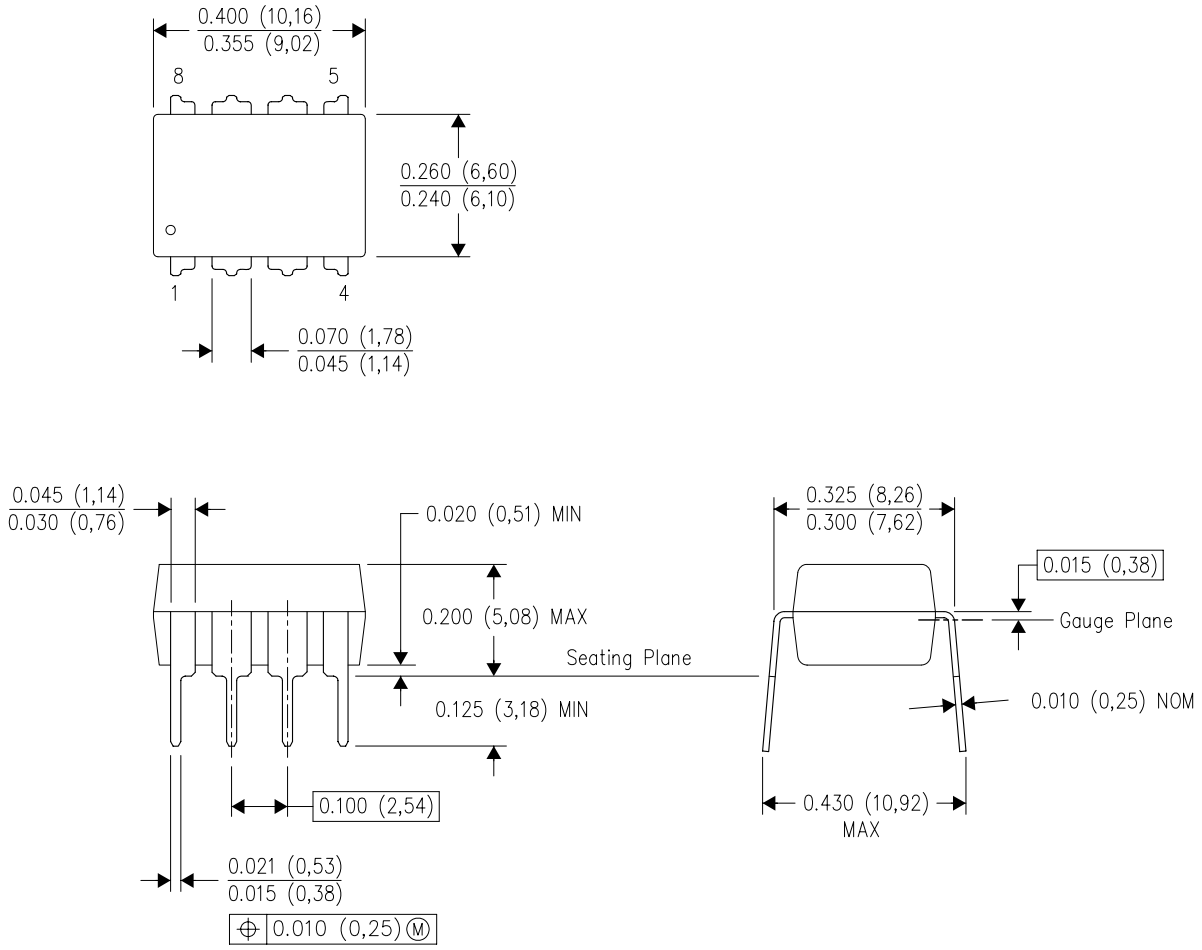
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



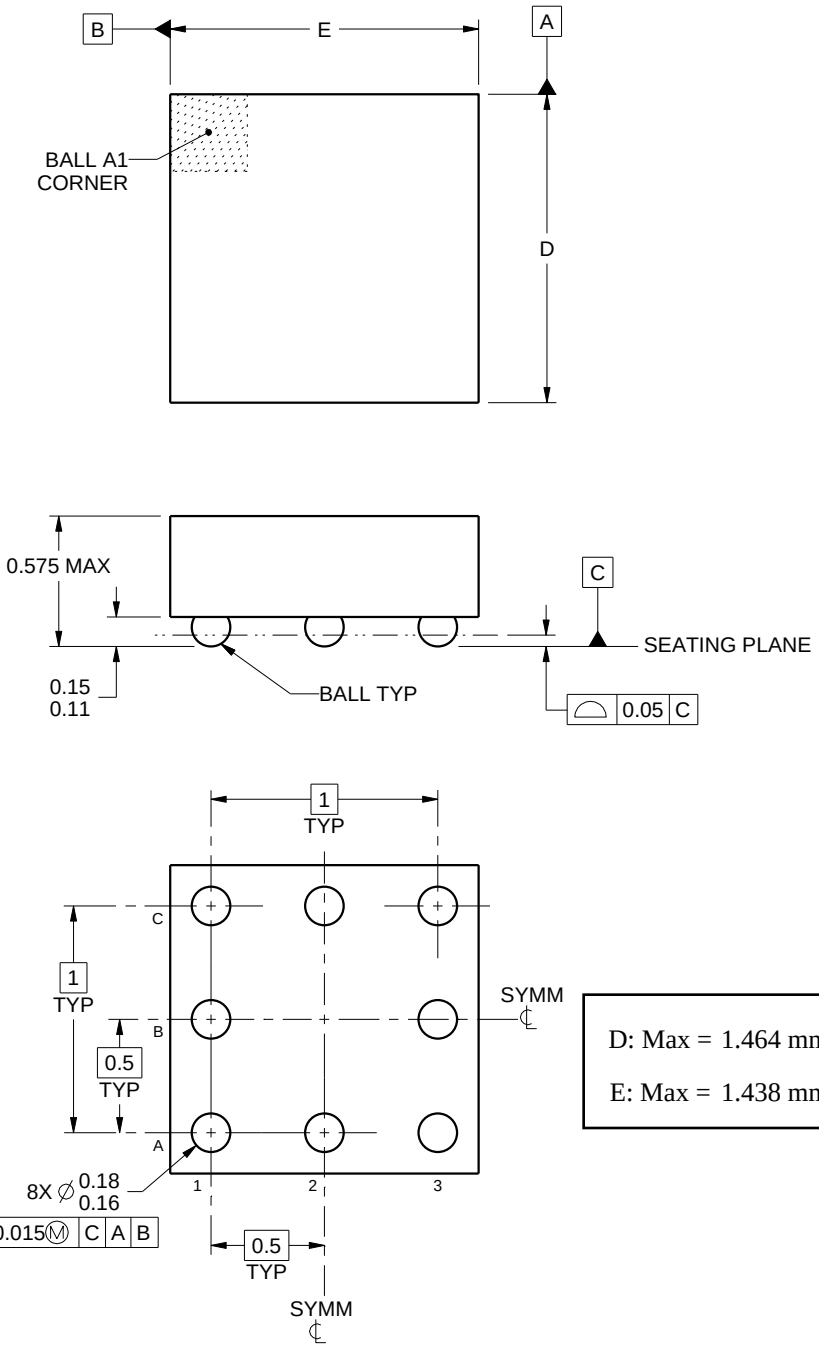
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

YPB0008

DSBGA - 0.575 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

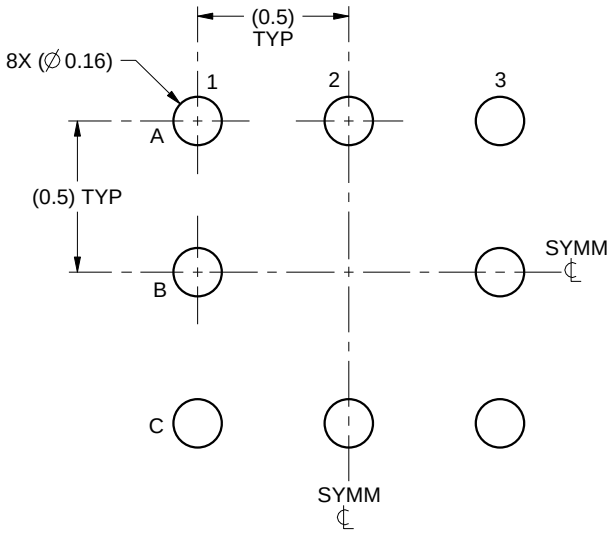
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

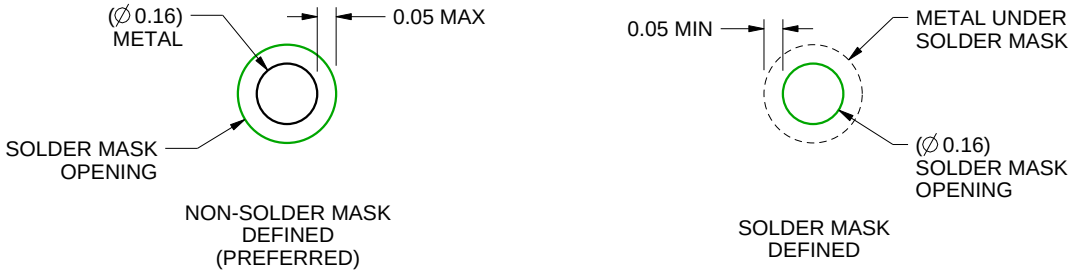
YPB0008

DSBGA - 0.575 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X

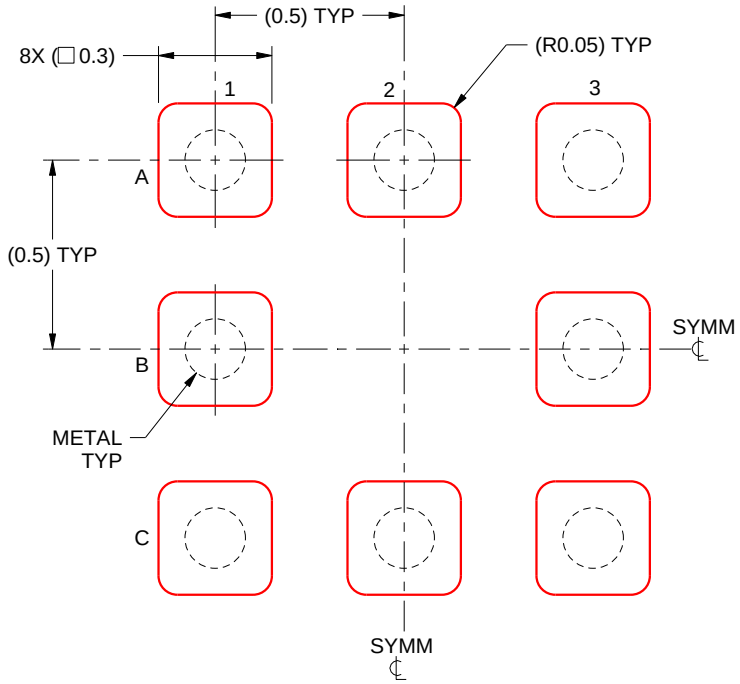


SOLDER MASK DETAILS
NOT TO SCALE

4215100/B 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL
SCALE:50X

4215100/B 07/2016

NOTES: (continued)

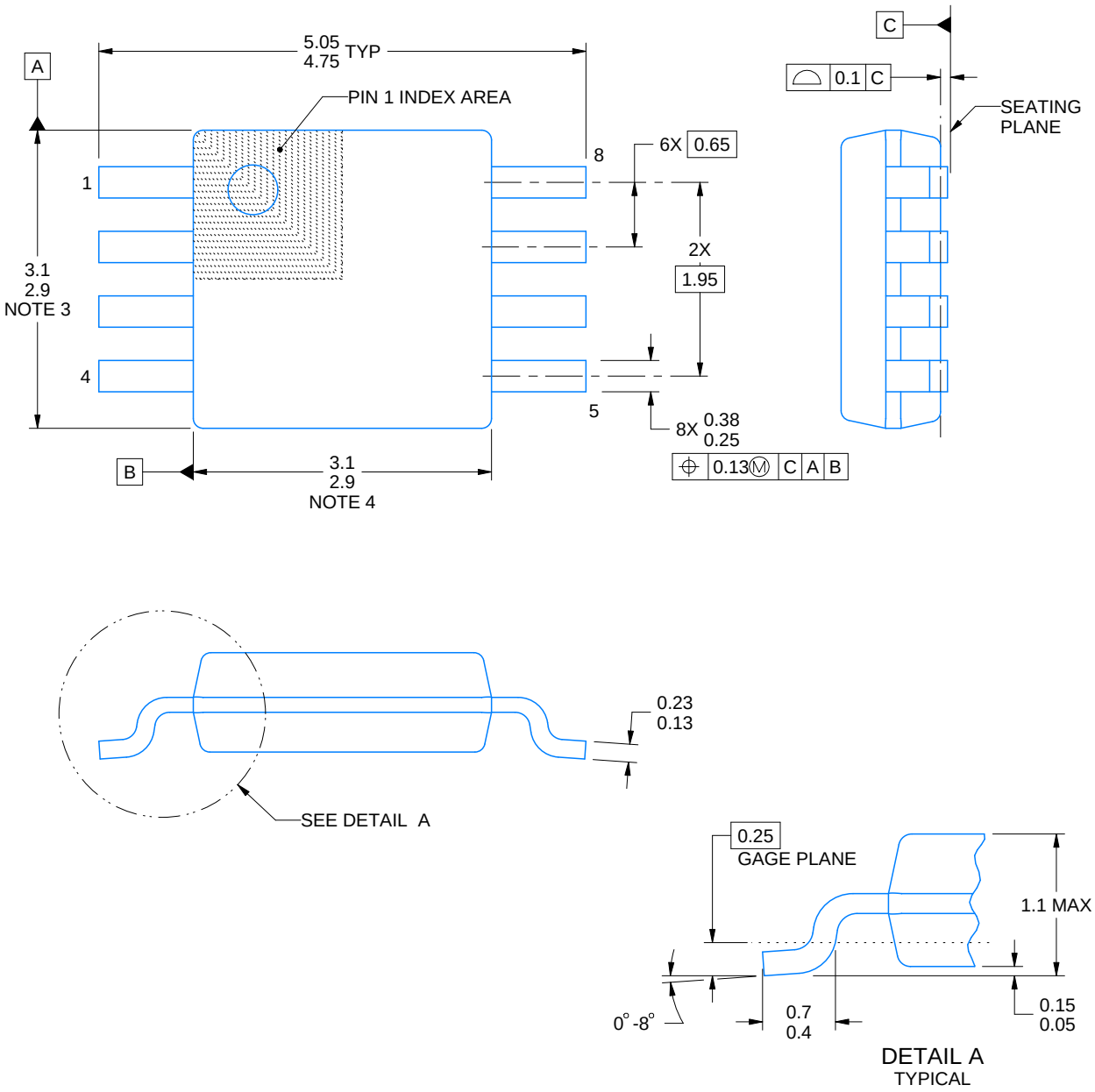
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

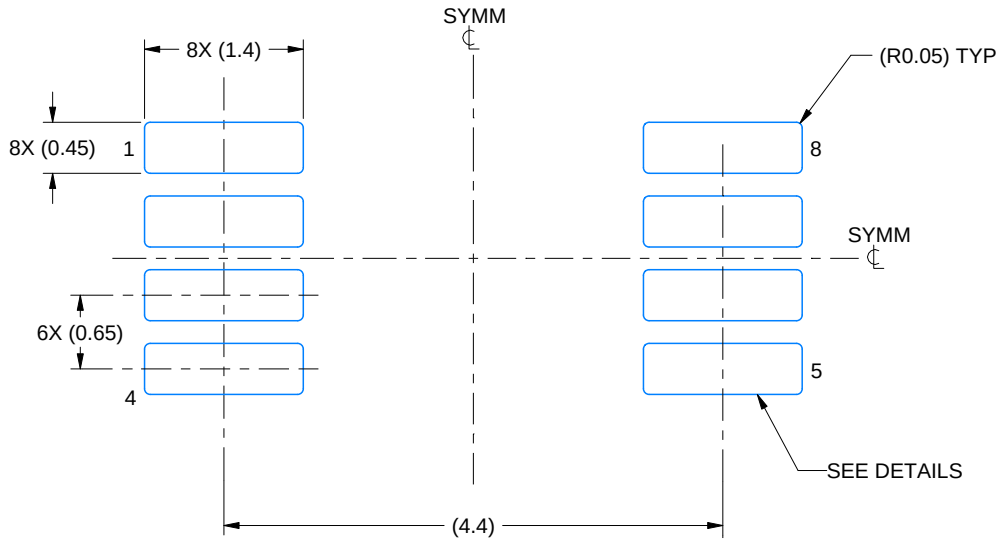
SMALL OUTLINE PACKAGE



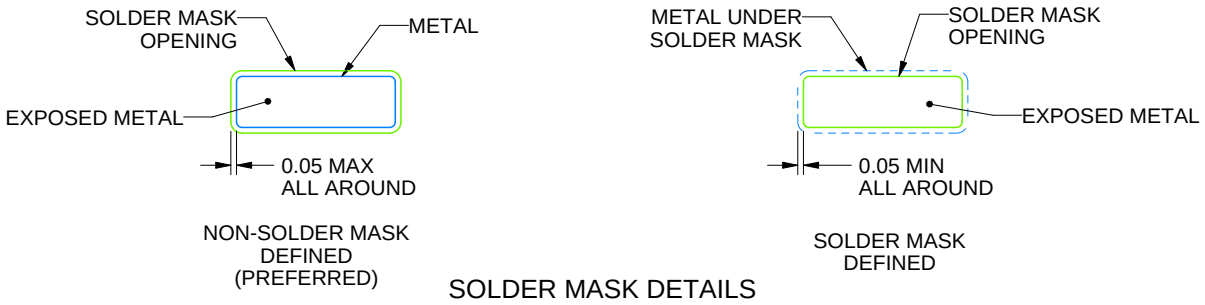
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

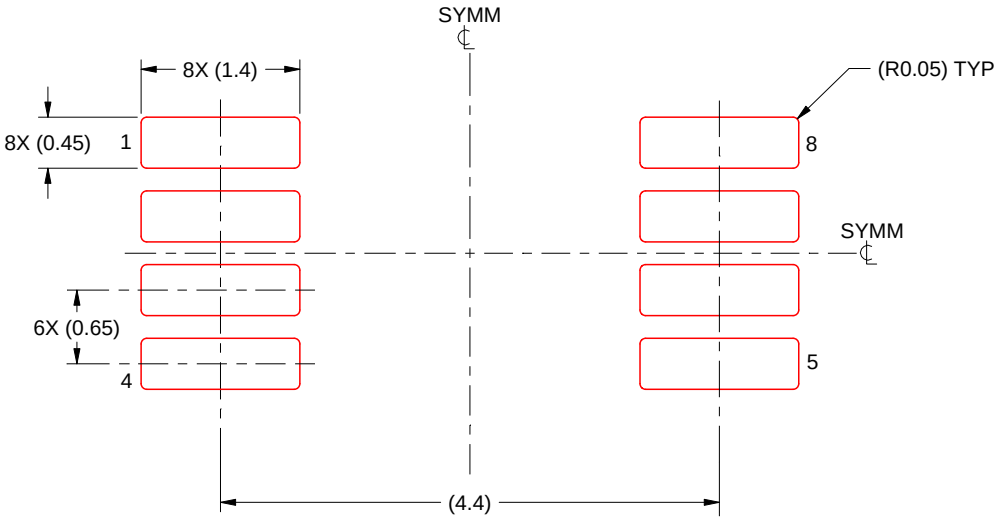


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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