

LMI800PS High Voltage Isolated Hotswap Controller with PMBus™ Interface

1 Features

- Isolated floating hotswap controller
 - Support 2-wire, 3-wire system architectures with high and low-side configurations
- Integrated Isolated Power Supply for hotswap controller bias
- GND referenced signals with Reinforced insulation to 800V
 - PGOOD, Fault assertion on $\overline{\text{SMBA}}$ and PMBus Telemetry
- Robust isolation barrier:
 - High lifetime at up to 1000VDC working voltage
 - Up to 5000VRMS isolation rating
 - Up to 10.4kV surge capability
- SYNC pin for coordination between high and low side hotswap controllers
- DISC pin for output capacitor discharge control
- Strong gate pull down (1.2A) for fast turn OFF
- Robust short circuit protection (360ns)
- Failed FET detection
- Programable UV, OV, t_{FAULT} thresholds
- External FET temperature sensing
- PMBus® interface for telemetry, control, configuration and debug
 - On chip EEPROM nonvolatile memory for configuration
 - Precision V_{IN} , V_{OUT} , I_{IN} , P_{IN} , V_{AUX} monitoring V ($<\pm 1.5\%$); I ($<\pm 1\%$); P ($<\pm 2\%$)
 - Power cycle with a single command
 - Blackbox fault recording of multiple events with relative time stamp stored in internal EEPROM
- 12-bit ADC with 250kHz sampling rate
- $-40^{\circ}\text{C} < T_{\text{J}} < 125^{\circ}\text{C}$ operation

2 Applications

- 800V servers and datacenter
- Base station power distribution
- Networking routers and switchers
- PLC power management
- 400V to 800V industrial systems

3 Description

The LMI800PS is high voltage isolated floating hotswap controller designed to support 2-wire and 3-wire system architecture with high and low side configuration for server and datacentres. This device requires only single power supply input referred to user ground and utilizes inbuilt isolated power supply for the hotswap controller bias. All user interface are reinforced isolated to 800V and ensured alignment with UL safety standards.

The LMI800PS comes with SYNC pin for coordination between high and low side hotswap controllers which provides user a liberty to optimize the FET rating. The DISC pin provides control feature to discharge the output load capacitor during system plug out.

It has Programmable power limit threshold along with adjustable fault time (t_{FAULT}) which further limits maximum power dissipation and ensure FET SOA protection under all critical events.

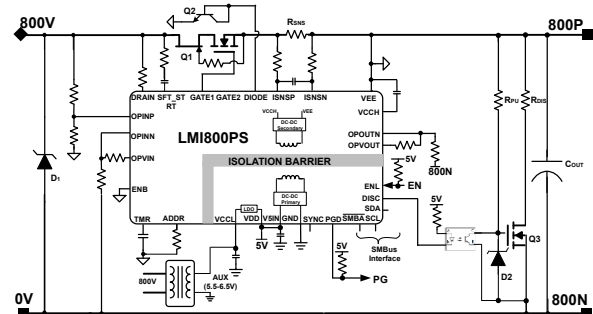
An integrated PMBus™ interface enables remote monitoring, control, and configuration of the system in real time. Key parameters can be accessed remotely for telemetry, and various thresholds can be configured through PMBus or stored in internal non volatile memory.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
PLMI800PSDVVR	DVV (SSOP 40)	10.65mm × 7.5mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.

LMI800 Simplified Schematic



4 Device and Documentation Support

4.1 Third-Party Products Disclaimer

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4.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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4.4 Trademarks

PMBus™ is a trademark of SMIF, Inc.

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4.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2026	*	Initial Release

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

6.1 Package Option Addendum

Packaging Information

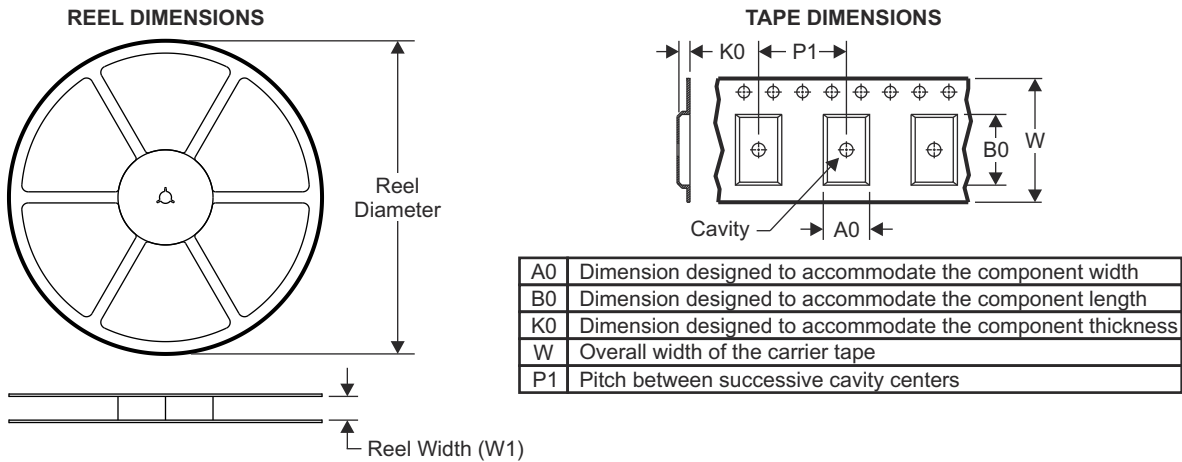
Orderable part number	Status ⁽¹⁾	Material type ⁽²⁾	Package Pins	Package qty Carrier	RoHS ⁽³⁾	Lead finish/Ball material ⁽⁴⁾	MSL rating/Peak reflow ⁽⁵⁾	Op temp (°C)	Part marking ⁽⁶⁾
PLMI800PSDVVR	Preview	Preproduction	DVV (SSOP) 40	3000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	–40 to 125	P800PS

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part. Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

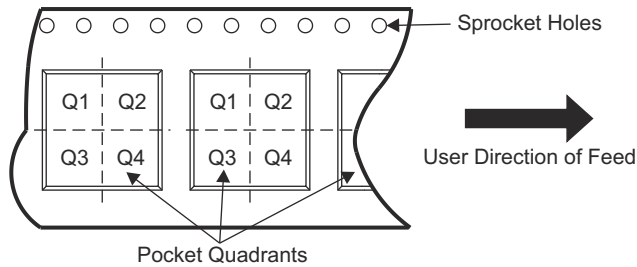
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6.2 Tape and Reel Information

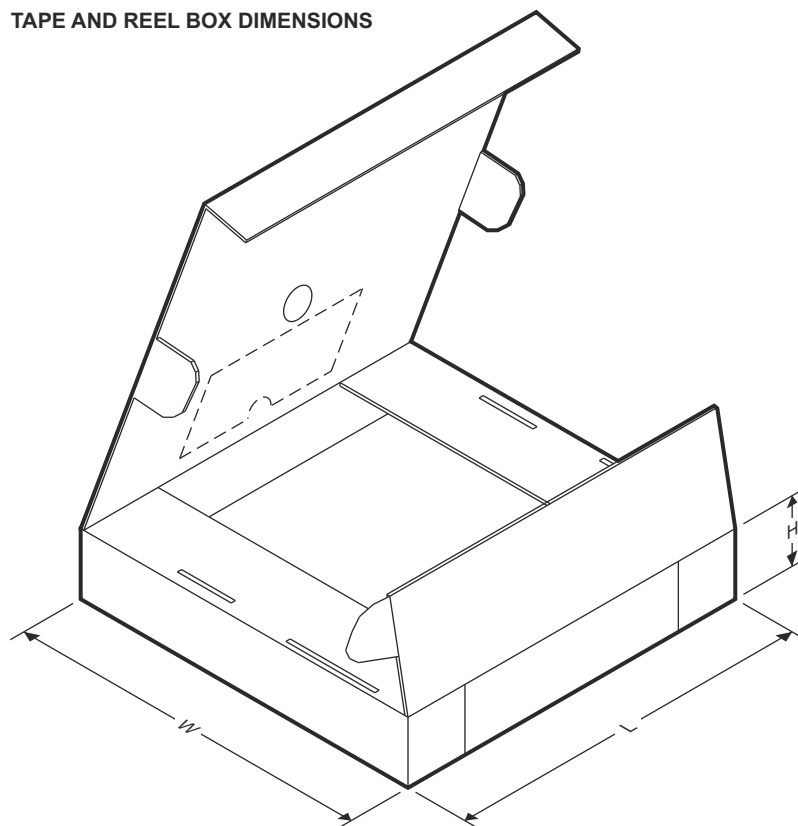


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PLMI800PSDVVR	SSOP	DVV	40	2000	330	24.4	10.90	11.10	2.70	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PLMi800PSDVVR	SSOP	DVV	40	2000	356.0	356.0	45

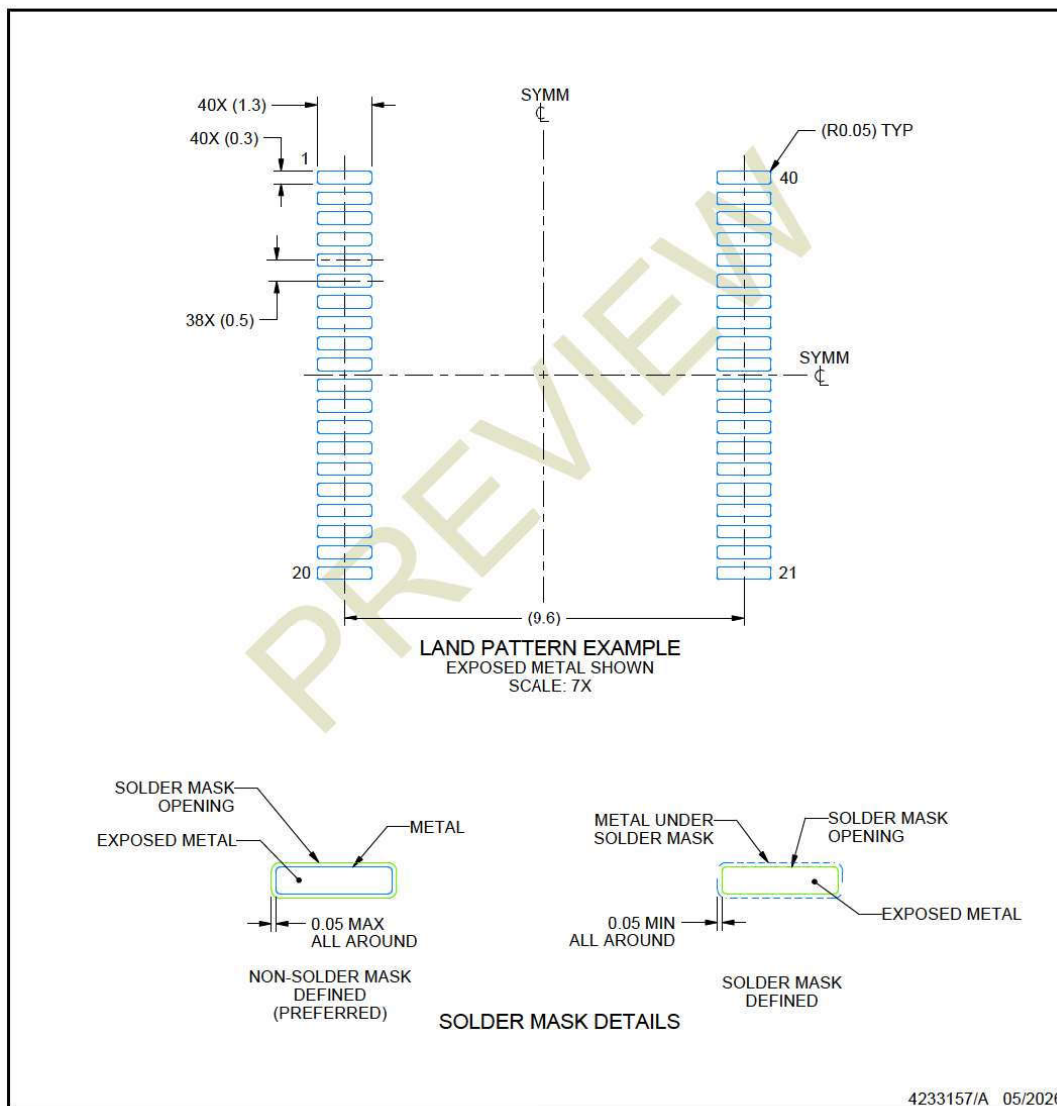
6.3 Mechanical Data

EXAMPLE BOARD LAYOUT

DVV0040A

SSOP - 2.65 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

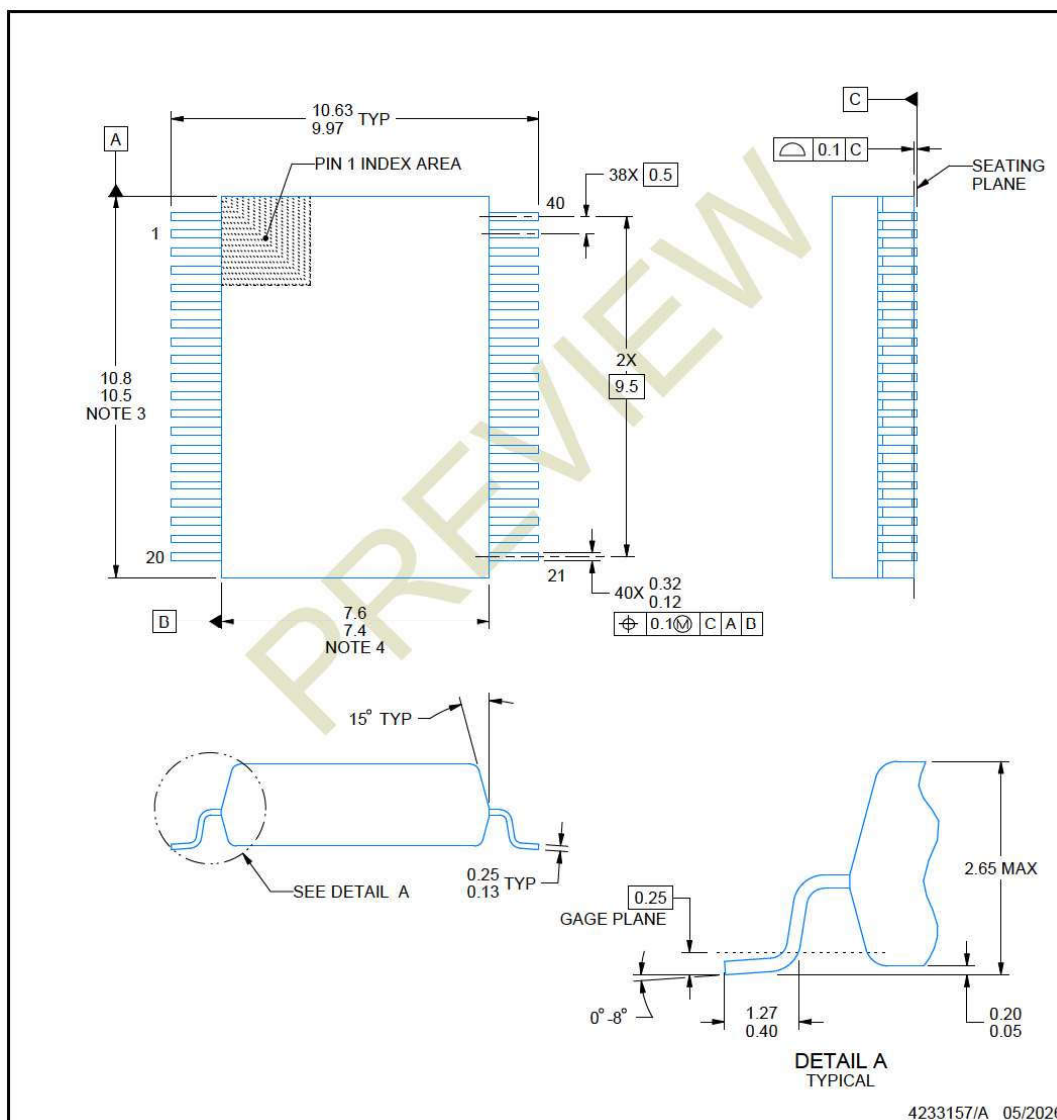
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



DVV0040A

PACKAGE OUTLINE
SSOP - 2.65 mm max height

SMALL OUTLINE PACKAGE



NOTES:

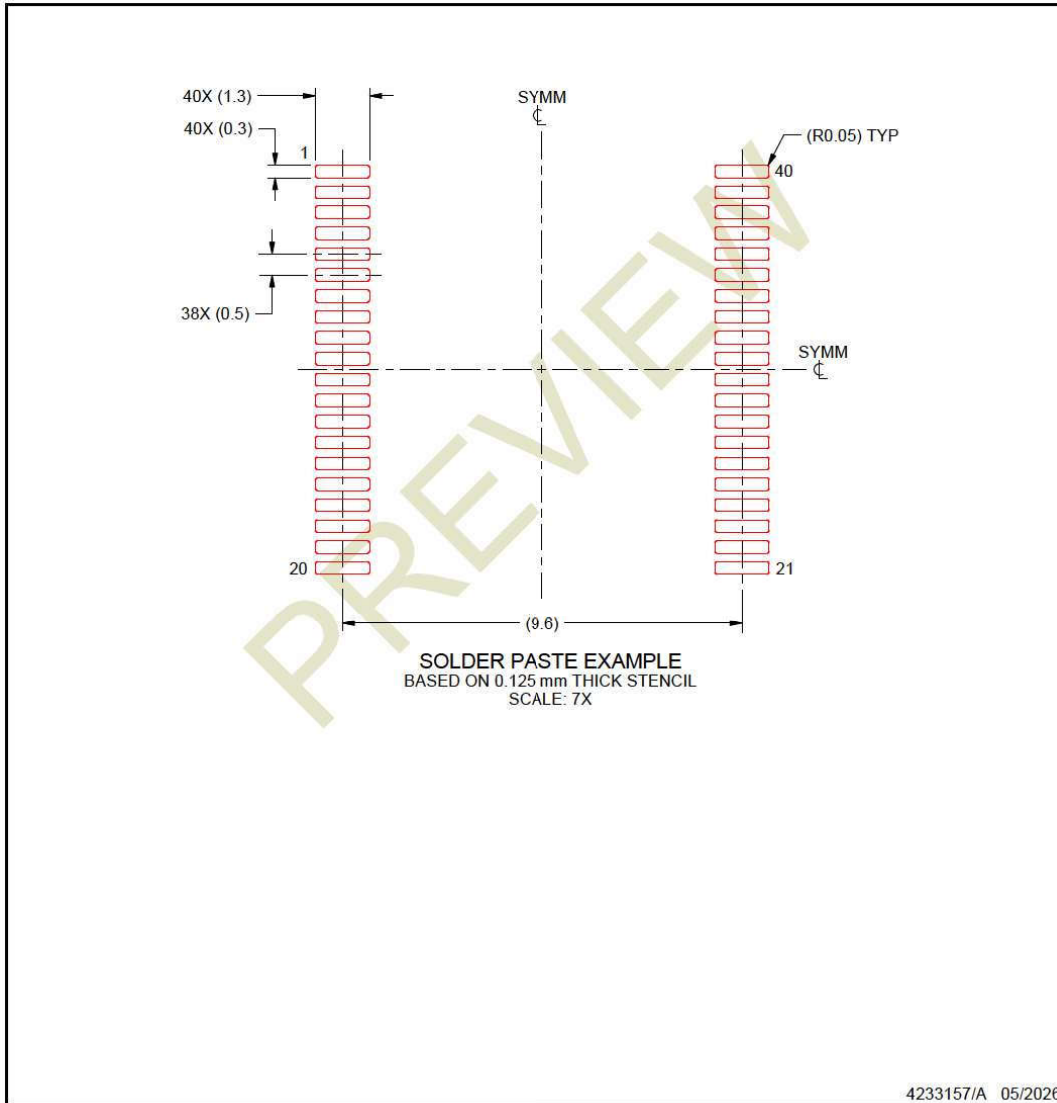
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

EXAMPLE STENCIL DESIGN

DVV0040A

SSOP - 2.65 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025