# LMK62XX High-Performance Low Jitter Oscillator

## 1 Features

- Low noise, high performance
  - Jitter: 150 fs RMS typical Fout > 100 MHz
  - PSRR: –60 dBc, robust supply noise immunity
- Supported output format:
  - LVPECL, LVDS and HCSL up to 400 MHz
- Total frequency tolerance: ±50 ppm (LMK62X2) and ±25 ppm (LMK62X0)
- 3.3-V operating voltage
- Industrial temperature range: –40°C to +85°C
- 5-mm × 3.2-mm 6-pin package that is pin-compatible with industry standard 5032 XO package

## 2 Applications

- High-performance replacement for crystal-, SAW-, or silicon-based oscillators
- Switches, routers, network line cards, Base Band Units (BBU), servers, storage/SAN
- Test and measurement
- Medical imaging
- FPGA, processor attach

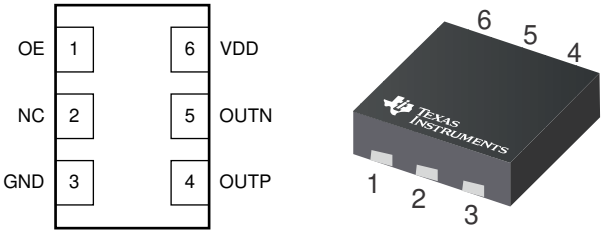
## 3 Description

The LMK62XX device is a low jitter oscillator that generates a commonly used reference clock. The device is pre-programmed in factory to support any reference clock frequency; supported output formats are LVPECL, LVDS and HCSL up to 400 MHz. Internal power conditioning provide excellent power supply ripple rejection (PSRR), reducing the cost and complexity of the power delivery network. The device operates from a single 3.3-V ±5% supply.

**Device Information**

| PART NUMBER | OUTPUT FREQUENCY (MHz) AND FORMAT | TOTAL FREQUENCY STABILITY (ppm) | PACKAGE SIZE(1) (2) |
|---|---|---|---|
| LMK62E2-100M | 100 LVPECL | ±50 | SIA (QFM, 6) 5.00 mm × 3.20 mm |
| LMK62E2-156M | 156.25 LVPECL | ±50 | |
| LMK62E0-156M | 156.25 LVPECL | ±25 | |
| LMK62A2-100M | 100 LVDS | ±50 | |
| LMK62A2-150M | 150 LVDS | ±50 | |
| LMK62A2-156M | 156.25 LVDS | ±50 | |
| LMK62A2-200M | 200 LVDS | ±50 | |
| LMK62A2-266M | 266.66 LVDS | ±50 | |
| LMK62I0-100M | 100 HCSL | ±25 | |
| LMK62I0-156M | 156.25 HCSL | ±25 | |

(1) For all available packages, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Pinout**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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# 4 Pin Configuration and Functions

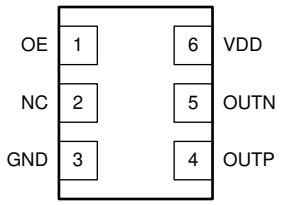



**Figure 4-1. SIA Package 6-pin QFM Top View**

**Table 4-1. Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| **POWER** | | | |
| GND | 3 | Ground | Device ground |
| VDD | 6 | Analog | 3.3-V power supply |
| **OUTPUT BLOCK** | | | |
| OUTP | 4 | Universal | Differential output pair (LVPECL, LVDS or HCSL). |
| OUTN | 5 | | |
| **DIGITAL CONTROL / INTERFACES** | | | |
| NC | 2 | N/A | No connect |
| OE | 1 | LVCMOS | Output enable (internal pulldown). When set to low, output pair is disabled and set at high impedance.<br>The recommended external pullup resistor value is 10 kΩ. |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| VDD | Device supply voltage | –0.3 | 3.6 | V |
| $V_{IN}$ | Output voltage for logic inputs | –0.3 | VDD + 0.3 | V |
| $V_{OUT}$ | Output voltage for clock outputs | –0.3 | VDD + 0.3 | V |
| $T_J$ | Junction temperature | | 150 | °C |
| $T_{stg}$ | Storage temperature | –40 | 125 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VDD | Device supply voltage | 3.135 | 3.3 | 3.465 | V |
| $T_A$ | Ambient temperature | –40 | 25 | 85 | °C |
| $T_J$ | Junction temperature | | | 105 | °C |
| $t_{RAMP}$ | VDD power-up ramp time | 0.1 | | 100 | ms |

## 5.4 Thermal Information

| THERMAL METRIC(1) | | LMK62XX (2) (3) (4) SIA (QFM ) 6 PINS Airflow (LFM) 0 | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 94.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 65.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 59 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 23.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 64.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal resistance is calculated on a 4-layer JEDEC board.
(3) Connected to GND with 2 thermal vias (0.3-mm diameter).
(4) $\psi_{JB}$ (junction to board) is used when the main heat flow is from the junction to the GND pad. Please refer to Thermal Considerations section for more information on ensuring good system reliability and quality.

## 5.5 Electrical Characteristics - Power Supply

VDD = 3.3 V ± 5%, $T_A$ = –40°C to 85°C(1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| IDD | Device current consumption | LVPECL(2) | | 95 | 110 | mA |
| | | LVDS | | 85 | 100 | |
| | | HCSL(3) | | 90 | 105 | |
| IDD-PD | Device current consumption when output is disabled | OE = GND | | 70 | | mA |

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) On-chip power dissipation should exclude 40 mW, dissipated in the 150-Ω termination resistors, from total power dissipation.
(3) Excludes load current.

## 5.6 LVPECL Output Characteristics

VDD = 3.3 V ± 5%, $T_A$ = –40°C to 85°C(1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output frequency(2) | | | | 400 | MHz |
| $V_{OD}$ | Output voltage swing ($V_{OH}$ – $V_{OL}$)(2) | | 700 | 950 | 1200 | mV |
| $V_{OUT, DIFF, PP}$ | Differential output peak-to-peak swing | | | 2 × \|$V_{OD}$\| | | V |
| $V_{OS}$ | Output common-mode voltage | | | VDD – 1.45 | | V |
| $t_R$ / $t_F$ | Output rise/fall time (20% to 80%)(3) | | | 260 | 350 | ps |
| ODC | Output duty cycle(3) | | 45% | | 55% | |

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) An output frequency over $f_{OUT}$ max spec is possible, but output swing may be less than $V_{OD}$ min spec.


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(3) Ensured by characterization.

## 5.7 LVDS Output Characteristics

VDD = 3.3 V ± 5%, $T_A$ = –40°C to 85°C(1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output frequency(1) | | | | 400 | MHz |
| $V_{OD}$ | Output voltage swing ($V_{OH}$ - $V_{OL}$)(1) | | 300 | 390 | 480 | mV |
| $V_{OUT, DIFF, PP}$ | Differential output peak-to-peak swing | | | 2 x $\|V_{OD}\|$ | | V |
| $V_{OS}$ | Output common-mode voltage | | 1.125 | 1.2 | 1.375 | V |
| $t_R$ / $t_F$ | Output rise/fall time (20% to 80%)(2) | | | 260 | 350 | ps |
| ODC | Output duty cycle(2) | | 45% | | 55% | |
| $R_{OUT}$ | Differential output impedance | | | 107 | | Ω |

(1) An output frequency over $f_{OUT}$ max spec is possible, but output swing may be less than $V_{OD}$ min spec.
(2) Ensured by characterization.

## 5.8 HCSL Output Characteristics

VDD = 3.3 V ± 5%, $T_A$ = –40°C to 85°C(1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output frequency | | | | 400 | MHz |
| $V_{OH}$ | Output high voltage | | 660 | | 900 | mV |
| $V_{OL}$ | Output low voltage | | –100 | | 100 | mV |
| $V_{CROSS}$ | Absolute crossing voltage(2) (3) | | 250 | | 475 | mV |
| $V_{CROSS-DELTA}$ | Variation of $V_{CROSS}$ (2) (3) | | 0 | | 140 | mV |
| dV/dt | Slew rate(4) | | 1 | | 3 | V/ns |
| ODC | Output duty cycle(4) | | 45% | | 55% | |

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) Measured from -150 mV to +150 mV on the differential waveform with the 300 mVpp measurement window centered on the differential zero crossing.
(3) Ensured by design.
(4) Ensured by characterization.

## 5.9 OE Input Characteristics

VDD = 3.3 V ± 5%, $T_A$ = –40°C to 85°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | | 1.4 | | | V |
| $V_{IL}$ | Input low voltage | | | | 0.6 | V |
| $I_{IH}$ | Input high current | $V_{IH}$ = VDD | –40 | | 40 | µA |
| $I_{IL}$ | Input low current | $V_{IL}$ = GND | –40 | | 40 | µA |
| $C_{IN}$ | Input capacitance | | | 2 | | pF |

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## 5.10 Frequency Tolerance Characteristics

VDD = 3.3 V ± 5%, $T_A$ = –40°C to 85°C(1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_T$ | Total frequency tolerance | LMK62X2: All output formats, frequency bands and device junction temperature up to 105°C; includes initial freq tolerance, temperature & supply voltage variation, solder reflow and 5-year aging at 40°C | –50 | | 50 | ppm |
| | | LMK62X0: All output formats, frequency bands and device junction temperature up to 105°C; includes initial freq tolerance, temperature & supply voltage variation, solder reflow and 5-year aging at 40°C | –25 | | 25 | ppm |

(1) Ensured by characterization.

## 5.11 Power-On/Reset Characteristics (VDD)

VDD = 3.3 V ± 5%, $T_A$ = –40°C to 85°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{THRESH}$ | Threshold voltage(1) | | 2.85 | | 3 | V |
| $V_{DROOP}$ | Allowable voltage droop(2) | | | | 0.1 | V |
| $t_{STARTUP}$ | Start-up time (1) | Time elapsed from VDD at 3.135 V to output enabled | | | 10 | ms |
| $t_{OE-EN}$ | Output enable time(2) | Time elapsed from OE at $V_{IH}$ to output enabled | | | 50 | µs |
| $t_{OE-DIS}$ | Output disable time(2) | Time elapsed from OE at $V_{IL}$ to output disabled | | | 50 | µs |

(1) Ensured by characterization.
(2) Ensured by design.

## 5.12 PSRR Characteristics

VDD = 3.3 V, $T_A$ = 25°C(1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| PSRR | Spurs induced by 50-mV power supply ripple(2) (3) at 156.25-MHz output, all output types | Sine wave at 50 kHz | | –60 | | dBc |
| | | Sine wave at 100 kHz | | –60 | | |
| | | Sine wave at 500 kHz | | –60 | | |
| | | Sine wave at 1 MHz | | –60 | | |

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) Measured max spur level with 50 mVpp sinusoidal signal between 50 kHz and 1 MHz applied on VDD pin
(3) $DJ_{SPUR}$ (ps, pk-pk) = [2*10(SPUR/20) / (π*$f_{OUT}$)]*1e6, where PSRR or SPUR in dBc and $f_{OUT}$ in MHz.

## 5.13 PLL Clock Output Jitter Characteristics

VDD = 3.3 V ± 5%, $T_A$ = –40°C to 85°C(1) (3)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| RJ | RMS phase jitter(2) (12 kHz – 20 MHz) | $f_{OUT}$ ≥ 100 MHz, all output types | | 150 | 250 | fs RMS |

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) Ensured by characterization.
(3) Phase jitter measured with Agilent E5052 signal source analyzer using a differential-to-single ended converter (balun or buffer).


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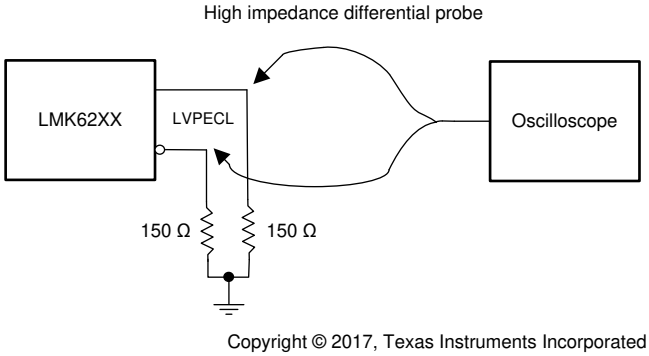
## 5.14 Additional Reliability and Qualification

| PARAMETER | CONDITION / TEST METHOD |
|---|---|
| Mechanical Shock | MIL-STD-202, Method 213 |
| Mechanical Vibration | MIL-STD-202, Method 204 |
| Moisture Sensitivity Level | J-STD-020, MSL3 |

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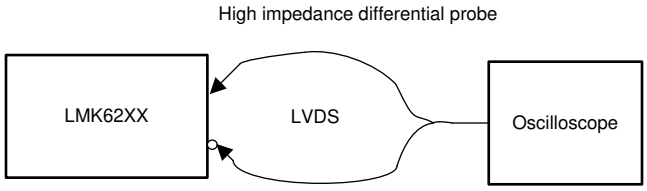
# 6 Parameter Measurement Information

## 6.1 Device Output Configurations



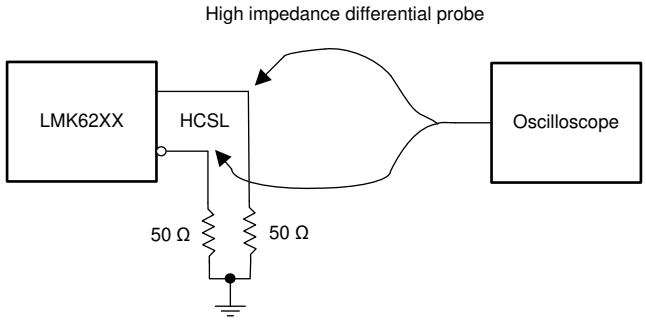

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**Figure 6-1. LVPECL Output DC Configuration During Device Test**



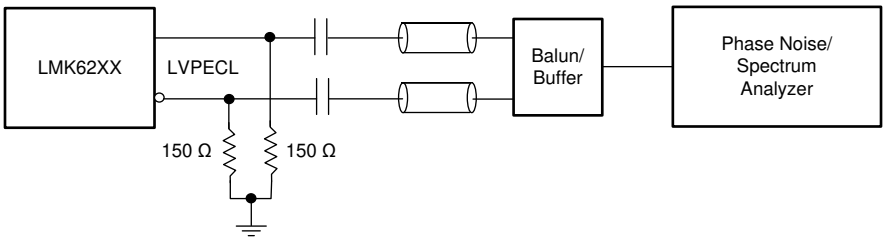

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**Figure 6-2. LVDS Output DC Configuration During Device Test**




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**Figure 6-3. HCSL Output DC Configuration During Device Test [1]**

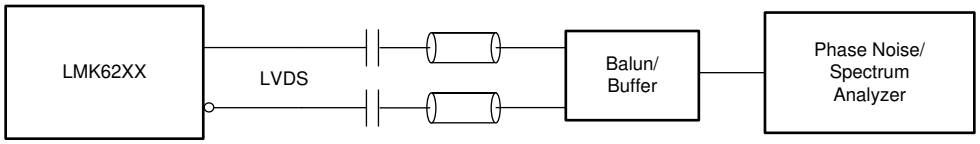



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**Figure 6-4. LVPECL Output AC Configuration During Device Test**

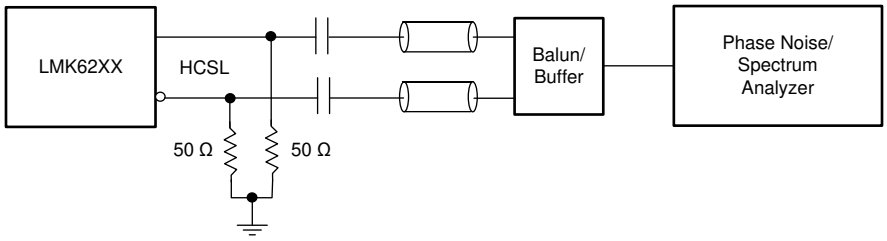
[1] Also compatible with 85 Ω termination


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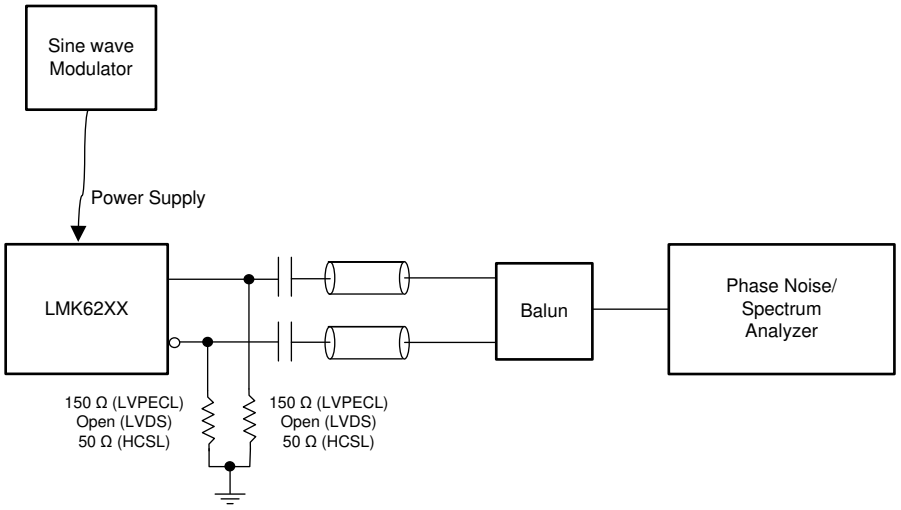

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**Figure 6-5. LVDS Output AC Configuration During Device Test**




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**Figure 6-6. HCSL Output AC Configuration During Device Test**




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**Figure 6-7. PSRR Test Setup**

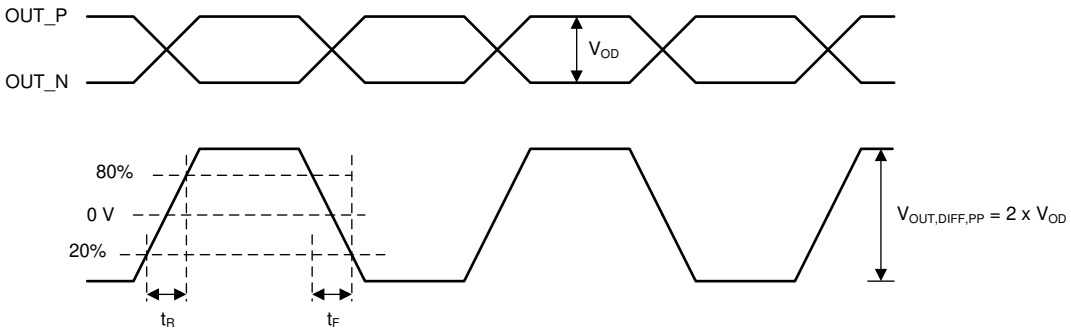



**Figure 6-8. Differential Output Voltage and Rise/Fall Time**

# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Power Supply Recommendations

For best electrical performance of LMK62XX, TI recommends using a combination of 10 µF, 1 µF, and 0.1 µF on the power-supply bypass network of the device. TI also recommends using component side mounting of the power-supply bypass capacitors and it is best to use 0201 or 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane. Figure 7-1 shows the layout recommendation for power supply decoupling of LMK62XX.

## 7.2 Layout

### 7.2.1 Layout Guidelines

The following sections provides recommendations for board layout, solder reflow profile and power supply bypassing when using LMK62XX to ensure good thermal / electrical performance and overall signal integrity of entire system.

#### *7.2.1.1 Ensuring Thermal Reliability*

The LMK62XX is a high-performance device. Therefore, pay careful attention to the device configuration and printed-circuit board (PCB) layout with respect to power consumption. The ground pin must be connected to the ground plane of the PCB through three vias or more, as shown in Figure 7-1, to maximize thermal dissipation out of the package.

Equation 1 shows the relationship between the PCB temperature around the LMK62XX and the junction temperature.

$$T_B = T_J - \Psi_{JB} \times P \quad (1)$$

where

- $T_B$: PCB temperature around the LMK62XX
- $T_J$: Junction temperature of LMK62XX
- $\Psi_{JB}$: Junction-to-board thermal resistance parameter of LMK62XX (64.1°C/W without airflow)
- P: On-chip power dissipation of LMK62XX

To ensure that the maximum junction temperature of LMK62XX is below 105°C, it can be calculated that the maximum PCB temperature without airflow should be at 81°C or below when the device is optimized for best performance, resulting in maximum on-chip power dissipation of 0.36 W.

#### *7.2.1.2 Best Practices for Signal Integrity*

For best electrical performance and signal integrity of entire system with LMK62XX, TI recommends routing vias into decoupling capacitors and then into the LMK62XX. TI also recommends increasing the via count and width of the traces wherever possible. These steps ensure lowest impedance and shortest path for high frequency current flow. Figure 7-1 shows the layout recommendation for LMK62XX.


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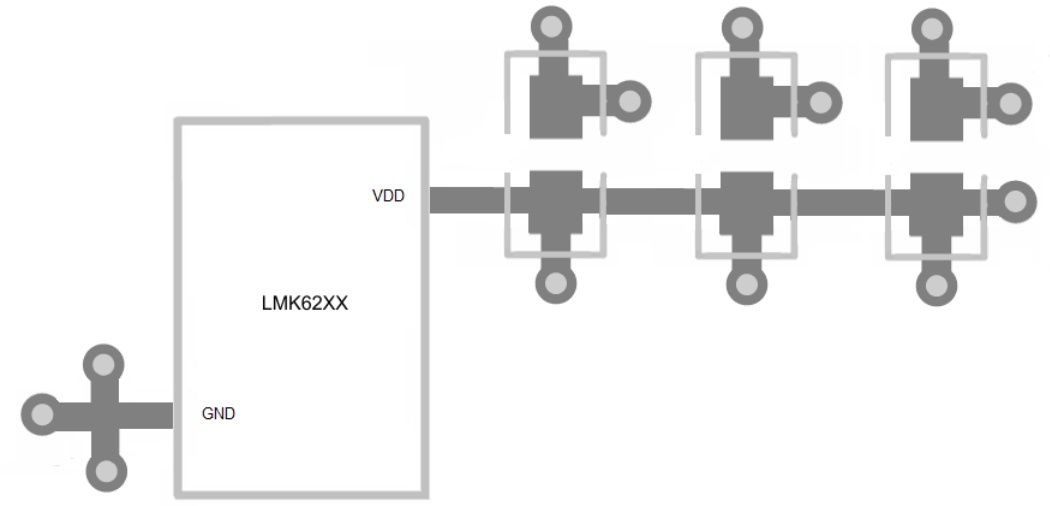



**Figure 7-1. LMK62XX Layout Recommendation for Power Supply and Ground**

#### *7.2.1.3 Recommended Solder Reflow Profile*

TI recommends following the recommendations set by the solder paste supplier to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20. Processing LMK62XX with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label is preferred. The exact temperature profile would depend on several factors including maximum peak temperature for the component as rated on the MSL label, board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, as well as the recommended soldering profile from the manufacturer, and capability of the reflow equipment to as confirmed by the SMT assembly operation.

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# 8 Device and Documentation Support

## 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 8.3 Trademarks

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## 8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision D (July 2018) to Revision E (December 2023) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • Changed the *Device Information* table | 1 |
| • Changed the OE pin description in the *Pin Functions* table | 3 |

| Changes from Revision C (December 2017) to Revision D (July 2018) | Page |
|---|---|
| • Added $V_{OS}$ minimum and maximum values to the *LVDS Output Characteristics* table | 5 |

| Changes from Revision B (June 2017) to Revision C (December 2017) | Page |
|---|---|
| • Added the LMK62E2-100M, LMK62I0-100M, and LMK62I0-156M to device list | 1 |

| Changes from Revision A (April 2017) to Revision B (June 2017) | Page |
|---|---|
| • Added the LMK62E0-156M, LMK62A2-100M, LMK62A2-150M, LMK62A2-156M, LMK62A2-200M, and LMK62A2-266M to device list | 1 |

| Changes from Revision * (December 2016) to Revision A (April 2017) | Page |
|---|---|
| • Updated advanced information data sheet to production data | 1 |

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

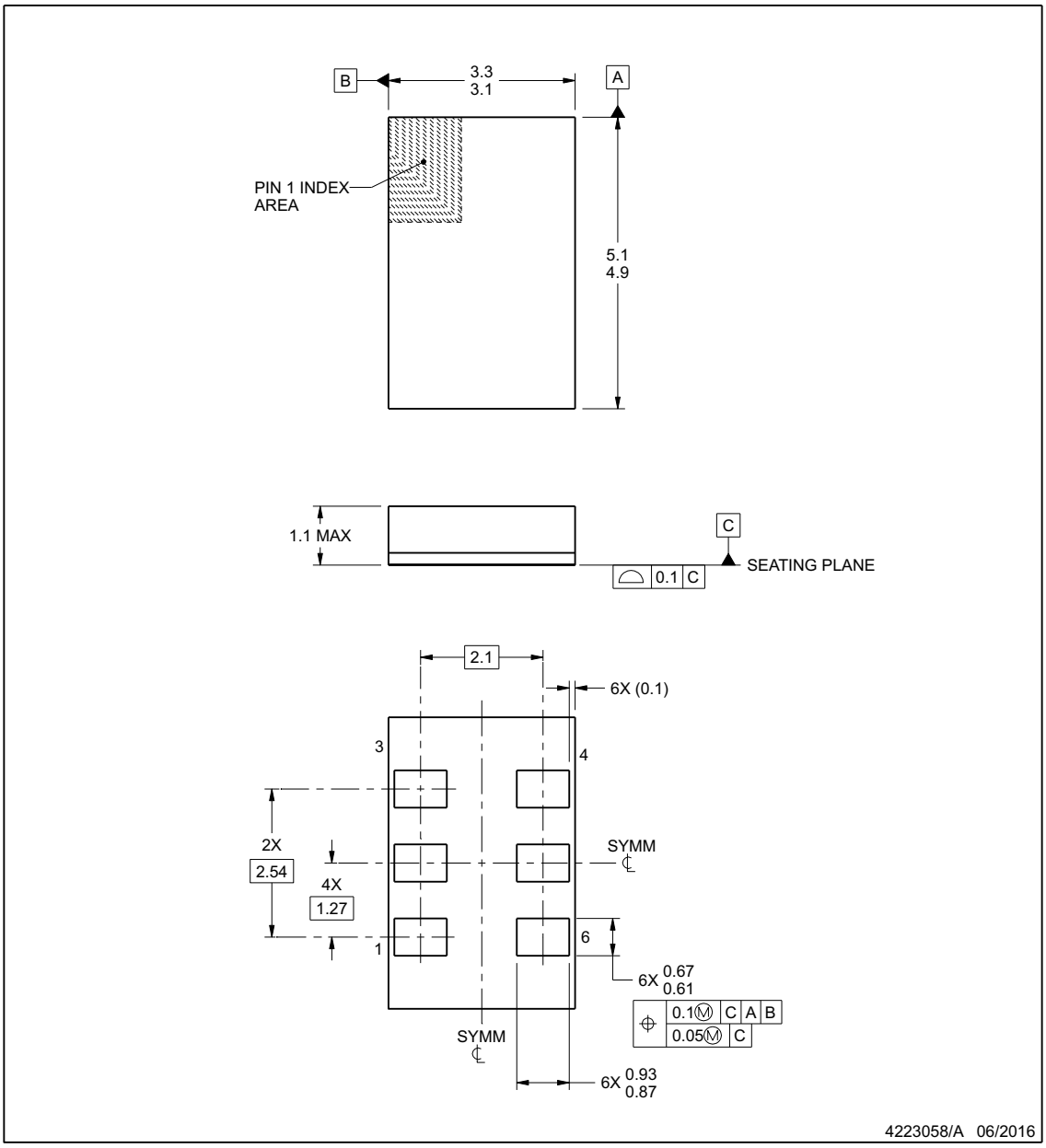

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# PACKAGE OUTLINE

## SIA0006B

## QFM - 1.1 mm max height

QUAD FLAT MODULE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



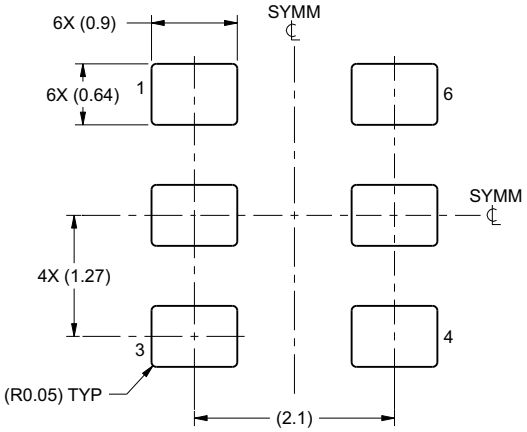
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## EXAMPLE BOARD LAYOUT

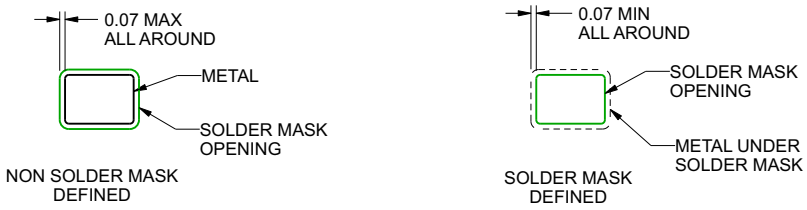
### SIA0006B

### QFM - 1.1 mm max height

QUAD FLAT MODULE




LAND PATTERN EXAMPLE
1:1 RATIO WITH PACKAGE SOLDER PADS
SCALE:15X




SOLDER MASK DETAILS
NOT TO SCALE

4223058/A 06/2016

NOTES: (continued)

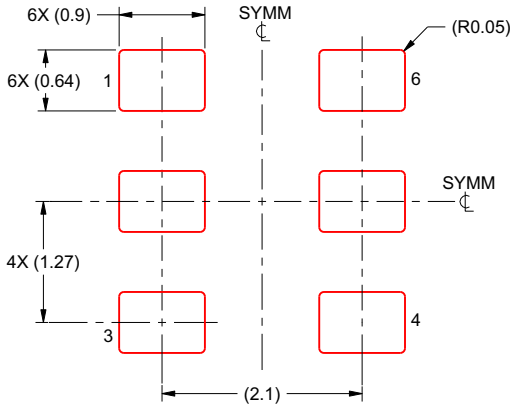
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).


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## EXAMPLE STENCIL DESIGN

**SIA0006B** **QFM - 1.1 mm max height**

QUAD FLAT MODULE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA
ALL PADS: 100%
SCALE:15X

4223058/A 06/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LMK62A2-100M00SIAR | NRND | Production | QFM (SIA) \| 6 | 2500 \| LARGE T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 10000 |
| LMK62A2-100M00SIAR.A | NRND | Production | QFM (SIA) \| 6 | 2500 \| LARGE T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 10000 |
| LMK62A2-100M00SIAT | NRND | Production | QFM (SIA) \| 6 | 250 \| SMALL T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 10000 |
| LMK62A2-100M00SIAT.A | NRND | Production | QFM (SIA) \| 6 | 250 \| SMALL T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 10000 |
| LMK62A2-150M00SIAR | NRND | Production | QFM (SIA) \| 6 | 2500 \| LARGE T&R | Yes | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 15000 |
| LMK62A2-150M00SIAR.A | NRND | Production | QFM (SIA) \| 6 | 2500 \| LARGE T&R | Yes | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 15000 |
| LMK62A2-150M00SIAT | NRND | Production | QFM (SIA) \| 6 | 250 \| SMALL T&R | Yes | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 15000 |
| LMK62A2-150M00SIAT.A | NRND | Production | QFM (SIA) \| 6 | 250 \| SMALL T&R | Yes | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 15000 |
| LMK62A2-156M25SIAR | NRND | Production | QFM (SIA) \| 6 | 2500 \| LARGE T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 15625 |
| LMK62A2-156M25SIAR.A | NRND | Production | QFM (SIA) \| 6 | 2500 \| LARGE T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 15625 |
| LMK62A2-156M25SIAT | NRND | Production | QFM (SIA) \| 6 | 250 \| SMALL T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 15625 |
| LMK62A2-156M25SIAT.A | NRND | Production | QFM (SIA) \| 6 | 250 \| SMALL T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 15625 |
| LMK62A2-200M00SIAR | NRND | Production | QFM (SIA) \| 6 | 2500 \| LARGE T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 20000 |
| LMK62A2-200M00SIAR.A | NRND | Production | QFM (SIA) \| 6 | 2500 \| LARGE T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 20000 |
| LMK62A2-200M00SIAT | NRND | Production | QFM (SIA) \| 6 | 250 \| SMALL T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 20000 |
| LMK62A2-200M00SIAT.A | NRND | Production | QFM (SIA) \| 6 | 250 \| SMALL T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 20000 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LMK62A2-266M66SIAR | Active | Production | QFM (SIA) \| 6 | 2500 \| LARGE T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 26666 |
| LMK62A2-266M66SIAR.A | Active | Production | QFM (SIA) \| 6 | 2500 \| LARGE T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 26666 |
| LMK62A2-266M66SIAT | NRND | Production | QFM (SIA) \| 6 | 250 \| SMALL T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 26666 |
| LMK62A2-266M66SIAT.A | NRND | Production | QFM (SIA) \| 6 | 250 \| SMALL T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 26666 |
| LMK62E0-156M25SIAR | NRND | Production | QFM (SIA) \| 6 | 2500 \| LARGE T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62E0 15625 |
| LMK62E0-156M25SIAR.A | NRND | Production | QFM (SIA) \| 6 | 2500 \| LARGE T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62E0 15625 |
| LMK62E0-156M25SIAT | NRND | Production | QFM (SIA) \| 6 | 250 \| SMALL T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62E0 15625 |
| LMK62E0-156M25SIAT.A | NRND | Production | QFM (SIA) \| 6 | 250 \| SMALL T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62E0 15625 |
| LMK62E2-100M00SIAR | NRND | Production | QFM (SIA) \| 6 | 2500 \| LARGE T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62E2 10000 |
| LMK62E2-100M00SIAR.A | NRND | Production | QFM (SIA) \| 6 | 2500 \| LARGE T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62E2 10000 |
| LMK62E2-100M00SIAT | NRND | Production | QFM (SIA) \| 6 | 250 \| SMALL T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62E2 10000 |
| LMK62E2-100M00SIAT.A | NRND | Production | QFM (SIA) \| 6 | 250 \| SMALL T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62E2 10000 |
| LMK62E2-156M25SIAR | NRND | Production | QFM (SIA) \| 6 | 2500 \| LARGE T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62E2 15625 |
| LMK62E2-156M25SIAR.A | NRND | Production | QFM (SIA) \| 6 | 2500 \| LARGE T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62E2 15625 |
| LMK62E2-156M25SIAT | NRND | Production | QFM (SIA) \| 6 | 250 \| SMALL T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62E2 15625 |
| LMK62E2-156M25SIAT.A | NRND | Production | QFM (SIA) \| 6 | 250 \| SMALL T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62E2 15625 |
| LMK62I0-100M00SIAR | NRND | Production | QFM (SIA) \| 6 | 2500 \| LARGE T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62I0 10000 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LMK62I0-100M00SIAR.A | NRND | Production | QFM (SIA) \| 6 | 2500 \| LARGE T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62I0 10000 |
| LMK62I0-100M00SIAT | NRND | Production | QFM (SIA) \| 6 | 250 \| SMALL T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62I0 10000 |
| LMK62I0-100M00SIAT.A | NRND | Production | QFM (SIA) \| 6 | 250 \| SMALL T&R | In-Work | NIAU | Level-3-260C-168 HR | -40 to 85 | 62I0 10000 |
| LMK62I0-156M25SIAR | NRND | Production | QFM (SIA) \| 6 | 2500 \| LARGE T&R | Yes | NIAU | Level-3-260C-168 HR | -40 to 85 | 62I0 15625 |
| LMK62I0-156M25SIAR.A | NRND | Production | QFM (SIA) \| 6 | 2500 \| LARGE T&R | Yes | NIAU | Level-3-260C-168 HR | -40 to 85 | 62I0 15625 |
| LMK62I0-156M25SIAT | NRND | Production | QFM (SIA) \| 6 | 250 \| SMALL T&R | Yes | NIAU | Level-3-260C-168 HR | -40 to 85 | 62I0 15625 |
| LMK62I0-156M25SIAT.A | NRND | Production | QFM (SIA) \| 6 | 250 \| SMALL T&R | Yes | NIAU | Level-3-260C-168 HR | -40 to 85 | 62I0 15625 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

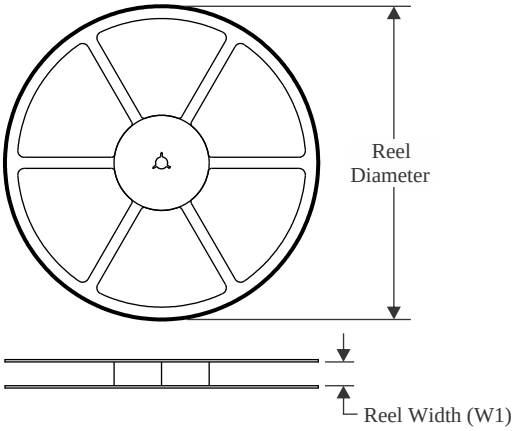
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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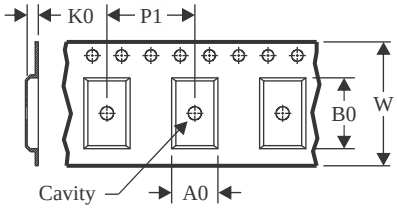
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

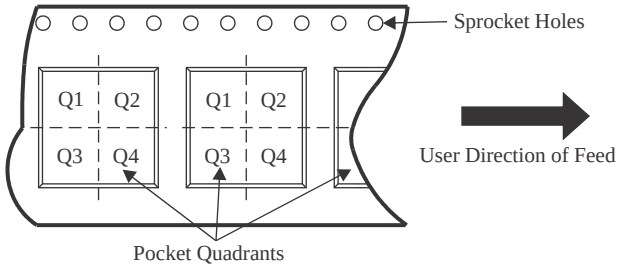



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

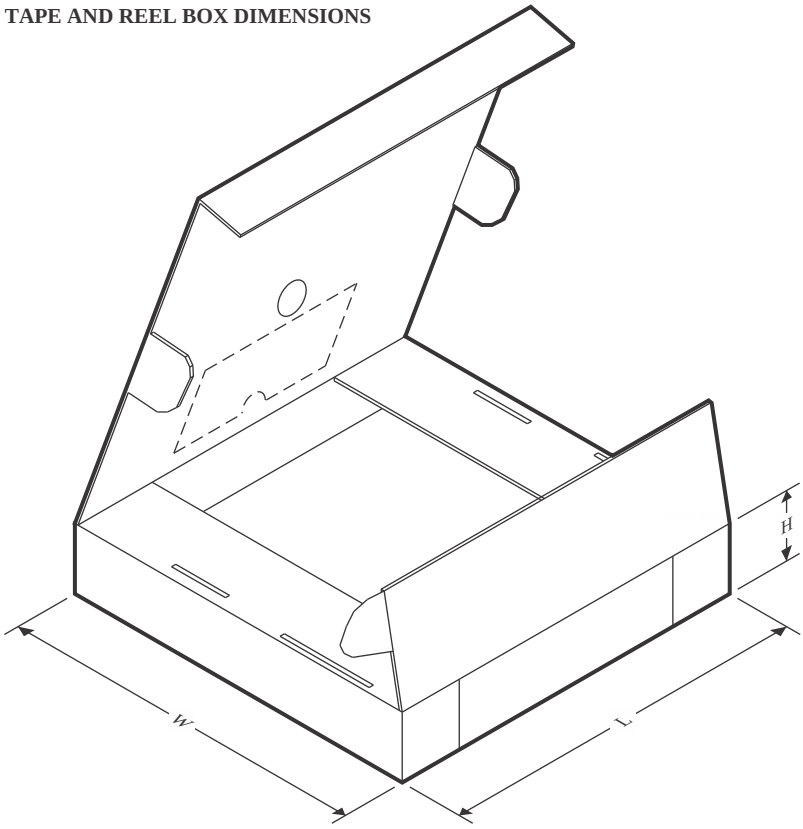



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMK62A2-100M00SIAR | QFM | SIA | 6 | 2500 | 330.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62A2-100M00SIAT | QFM | SIA | 6 | 250 | 180.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62A2-150M00SIAR | QFM | SIA | 6 | 2500 | 330.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62A2-150M00SIAT | QFM | SIA | 6 | 250 | 180.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62A2-156M25SIAR | QFM | SIA | 6 | 2500 | 330.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62A2-156M25SIAT | QFM | SIA | 6 | 250 | 180.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62A2-200M00SIAR | QFM | SIA | 6 | 2500 | 330.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62A2-200M00SIAT | QFM | SIA | 6 | 250 | 180.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62A2-266M66SIAR | QFM | SIA | 6 | 2500 | 330.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62A2-266M66SIAT | QFM | SIA | 6 | 250 | 180.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62E0-156M25SIAR | QFM | SIA | 6 | 2500 | 330.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62E0-156M25SIAT | QFM | SIA | 6 | 250 | 180.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62E2-100M00SIAR | QFM | SIA | 6 | 2500 | 330.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62E2-100M00SIAT | QFM | SIA | 6 | 250 | 180.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62E2-156M25SIAR | QFM | SIA | 6 | 2500 | 330.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62E2-156M25SIAT | QFM | SIA | 6 | 250 | 180.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMK62I0-100M00SIAR | QFM | SIA | 6 | 2500 | 330.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62I0-100M00SIAT | QFM | SIA | 6 | 250 | 180.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62I0-156M25SIAR | QFM | SIA | 6 | 2500 | 330.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62I0-156M25SIAT | QFM | SIA | 6 | 250 | 180.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMK62A2-100M00SIAR | QFM | SIA | 6 | 2500 | 367.0 | 367.0 | 35.0 |
| LMK62A2-100M00SIAT | QFM | SIA | 6 | 250 | 210.0 | 185.0 | 35.0 |
| LMK62A2-150M00SIAR | QFM | SIA | 6 | 2500 | 346.0 | 346.0 | 33.0 |
| LMK62A2-150M00SIAT | QFM | SIA | 6 | 250 | 210.0 | 185.0 | 35.0 |
| LMK62A2-156M25SIAR | QFM | SIA | 6 | 2500 | 346.0 | 346.0 | 33.0 |
| LMK62A2-156M25SIAT | QFM | SIA | 6 | 250 | 210.0 | 185.0 | 35.0 |
| LMK62A2-200M00SIAR | QFM | SIA | 6 | 2500 | 346.0 | 346.0 | 33.0 |
| LMK62A2-200M00SIAT | QFM | SIA | 6 | 250 | 210.0 | 185.0 | 35.0 |
| LMK62A2-266M66SIAR | QFM | SIA | 6 | 2500 | 367.0 | 367.0 | 35.0 |
| LMK62A2-266M66SIAT | QFM | SIA | 6 | 250 | 210.0 | 185.0 | 35.0 |
| LMK62E0-156M25SIAR | QFM | SIA | 6 | 2500 | 367.0 | 367.0 | 35.0 |
| LMK62E0-156M25SIAT | QFM | SIA | 6 | 250 | 210.0 | 185.0 | 35.0 |
| LMK62E2-100M00SIAR | QFM | SIA | 6 | 2500 | 346.0 | 346.0 | 33.0 |
| LMK62E2-100M00SIAT | QFM | SIA | 6 | 250 | 210.0 | 185.0 | 35.0 |
| LMK62E2-156M25SIAR | QFM | SIA | 6 | 2500 | 346.0 | 346.0 | 33.0 |
| LMK62E2-156M25SIAT | QFM | SIA | 6 | 250 | 210.0 | 185.0 | 35.0 |
| LMK62I0-100M00SIAR | QFM | SIA | 6 | 2500 | 346.0 | 346.0 | 33.0 |
| LMK62I0-100M00SIAT | QFM | SIA | 6 | 250 | 210.0 | 185.0 | 35.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMK62I0-156M25SIAR | QFM | SIA | 6 | 2500 | 346.0 | 346.0 | 33.0 |
| LMK62I0-156M25SIAT | QFM | SIA | 6 | 250 | 210.0 | 185.0 | 35.0 |

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