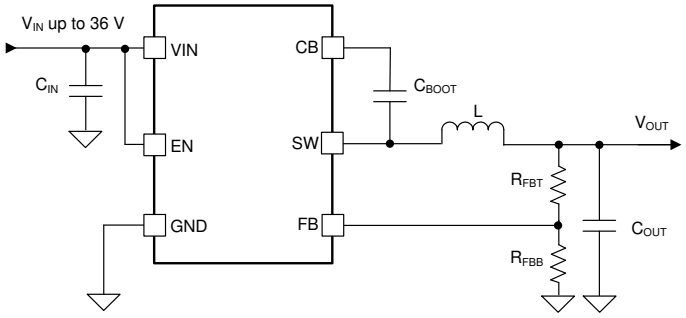
LMR51420 SIMPLE SWITCHER® Power Converter 4.5-V to 36-V, 2-A, Synchronous Buck Converter in a SOT-23 Package

1 Features

- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Configured for rugged industrial applications
  - 4.5-V to 36-V input voltage range
  - 2-A continuous output current
  - 70-ns minimum switching on time
  - 500-kHz and 1.1-MHz fixed switching frequency options
  - –40°C to 150°C junction temperature range
  - 98% maximum duty cycle
  - Start-up with prebiased output
  - Internal short circuit protection with hiccup mode
  - ±1.5% tolerance voltage reference
  - Precision enable
- Small solution size and ease of use
  - Integrated synchronous rectification
  - Internal compensation for ease of use
  - SOT-23 package
- Pin-to-pin compatible with the TPS54202 and TPS54302
- PFM and forced PWM (FPWM) options available
- Create a custom design using the LMR51420 with the WEBENCH® Power Designer

2 Applications

- Appliances
- Building automation
- Motor drives
- General purpose wide V_{IN} power supplies



Simplified Schematic

3 Description

The LMR51420 is a wide-V_{IN}, easy-to-use SIMPLE SWITCHER® power converter synchronous buck converter capable of driving up to 2-A load current. With a wide input range of 4.5 V to 36 V, the device is suitable for a wide range of industrial applications for power conditioning from an unregulated source.

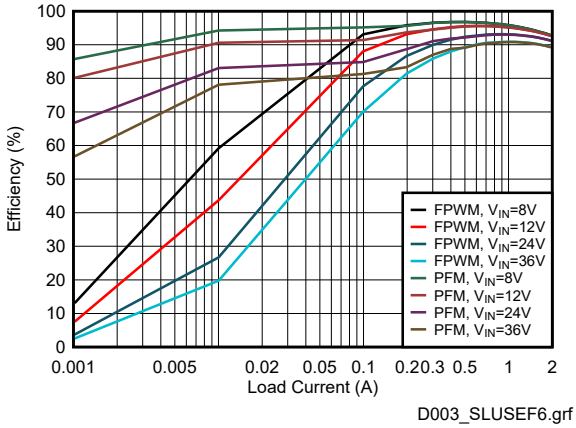
The LMR51420 operates at 500-kHz and 1.1-MHz switching frequency to support use of relatively small inductors for an optimized solution size. The device has a PFM version to realize high efficiency at light load and FPWM version to achieve constant frequency, and small output voltage ripple over the full load range. Soft-start and compensation circuits are implemented internally, which allows the device to be used with minimum external components.

The device has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, and thermal shutdown in case of excessive power dissipation. The LMR51420 is available in a 6-pin SOT-23 package.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
LMR51420	DBV (SOT-23, 6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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Efficiency vs Output Current, V_{OUT} = 5 V, 500 kHz

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2022) to Revision C (November 2022)	Page
• Added "power converter" after the SIMPLE SWITCHER® trademark	1
• Changed the t_hiccup in *Overcurrent and Short-Circuit Protection* to 135 ms	14
• Changed the quoted equation number in the design example as "Equation 12," "Equation 13," and "Equation 14"	18

Changes from Revision A (March 2022) to Revision B (August 2022)	Page
• Changed device status from Advance Information to Production Data	1

5 Device Comparison Table

ORDERABLE PART NUMBER	FREQUENCY	PFM OR FPWM	OUTPUT
LMR51420XDDCR	500 kHz	PFM	Adjustable
LMR51420XFDDCR	500 kHz	FPWM	Adjustable
LMR51420YDDCR	1.1 MHz	PFM	Adjustable
LMR51420YFDDCR	1.1 MHz	FPWM	Adjustable

6 Pin Configuration and Functions

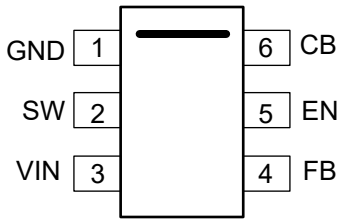


Figure 6-1. 6-Pin SOT-23 DBV Package (Top View)

Table 6-1. Pin Functions

Pin		Type(1)	Description
Name	NO.		
GND	1	G	Power ground terminals. This pin connects to the source of the low-side FET internally. Connect to system ground, and the ground side of CIN and COUT. The path to CIN must be as short as possible.
SW	2	P	Switching output of the converter. This pin connects to the source of the high-side FET and drain of the low-side FET. Connect this pin to the power inductor.
VIN	3	P	Supply input terminal to internal bias LDO and high-side FET. Connect this pin to the input supply and input bypass capacitors, C_{IN}. Input bypass capacitors must be directly connected to this pin and GND.
FB	4	A	Feedback input to the converter. Connect a resistor divider to set the output voltage. Never short this pin to ground during operation.
EN	5	A	Precision enable input to the converter. Do not float. High = on, low = off. This pin can be tied to VIN. Precision enable input allows adjustable UVLO by an external resistor divider. If the EN pin is left floating, the device is disabled.
CB	6	P	Bootstrap capacitor connection for the high-side FET driver. Connect a high quality 100-nF capacitor from this pin to the SW pin.

(1) A = Analog, P = Power, G = Ground

7 Specifications

7.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	38	V
	EN	–0.3	V_{IN} + 0.3	
	FB	–0.3	5.5	
Output voltage	SW, DC	–0.3	38	V
	SW, transient < 20 ns	–3.0	38	
	CB	–0.3	43.5	
	CB to SW	–0.3	5.5	
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input voltage	VIN to GND	4.5		36	V
	EN(2)	0		V_{IN}	
	FB	0		4.5	
Output voltage	V_{OUT} (3)	0.6		95% of V_{IN}	V
Output current	Iout(4)		2		A
T_J	Operating junction temperature(5)	–40		+150	°C

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For compliant specifications, see the *Electrical Characteristics* table.
(2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.
(3) Under no conditions must the output voltage be allowed to fall below 0 V.
(4) Maximum continuous DC current can be derated when operating with high switching frequency, high ambient temperature, or both. See *Application and Implementation* section for details.
(5) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 150°C.

7.4 Thermal Information

The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For example, with a 2-layer PCB, a $R_{\theta JA}$ = 80°C/W can be achieved. For design information, see Maximum Output Current Versus Ambient Temperature.

THERMAL METRIC(1)		DDC (SOT-23-6) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Limits apply over operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits(1) are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4.5 V to 36 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN quiescent current (non-switching)(2)	V_{EN} = 3 V, PFM variant only		40	65	µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{EN} = 0 V		3	15	µA
UVLO						
$VIN_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising		3.89	4.5	V
$VIN_{UVLO(F)}$	VIN UVLO falling threshold	V_{IN} falling	3.35	3.58		V
$VIN_{UVLO(H)}$	VIN UVLO hysteresis			0.3		V
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	1.1	1.227	1.36	V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching	0.95	1.08	1.22	V
$I_{EN(P2)}$	EN pin sourcing current post EN rising threshold	V_{EN} = 3 V		10	200	nA
REFERENCE VOLTAGE						
Vfb	Reference voltage		0.591	0.6	0.609	V
$I_{FB(LKG)}$	FB input leakage current	V_{FB} = 1.2 V		0.8	50	nA
SWITCHING FREQUENCY						
$f_{SW1(CCM)}$	Switching frequency, CCM operation	500-kHz trim option	450	500	560	kHz
$f_{SW2(CCM)}$	Switching frequency, CCM operation	1.1-MHz trim option	0.95	1.1	1.25	MHz
STARTUP						
t_{SS}	Internal fixed soft-start time		3.2	4.0	5.4	ms
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	T_J = 25°C		0.12		Ω
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	T_J = 25°C		0.07		Ω
$t_{ON(min)}$	Minimum ON pulse width	V_{IN} = 12 V, I_{OUT} = 2 A		70		ns
$t_{ON(max)}$	Maximum ON pulse width	V_{IN} = 12 V, I_{OUT} = 2 A		6.76		µs
$t_{OFF(min)}$	Minimum OFF pulse width	V_{IN} = 4.5 V		150		ns
OVERCURRENT PROTECTION						
$I_{HS\_PK(OC)}$	High-side peak current limit(3)	LM51420	2.7	3.5	5.1	A

7.5 Electrical Characteristics (continued)

Limits apply over operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits(1) are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4.5 V to 36 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LS\_V(OC)}$	Low-side valley current limit(3)	LM51420	1.7	2.5	3.4	A
$I_{LS(NOC)}$	Low-side negative current limit	LM51420 FPWM Only		–1		A
I_{ZC}	Zero-cross detection current threshold			0.02		A
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold(4)	Temperature rising		163		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis(4)			22		°C

(1) MIN and MAX limits are 100% production tested at 25°C. Limits over the operating temperature range verified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.
(3) The current limit values in this table are tested, open loop, in production. They may differ from those found in a closed loop application
(4) Specified by design

7.6 System Characteristics

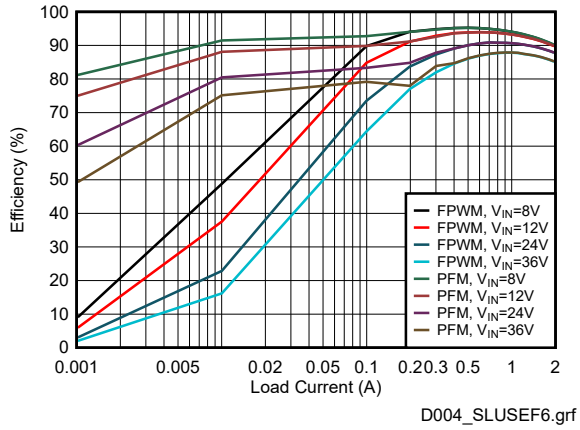
The following specifications apply to a typical application circuit with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 150°C. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Operating input voltage range		4.5		36	V
V_{OUT}	Adjustable output voltage regulation(1)	PFM operation	–1.5%		2.5%	
V_{OUT}	Adjustable output voltage regulation(1)	FPWM operation	–1.5		1.5	%
I_{SUPPLY}	VIN quiescent current (non-switching)	V_{IN} =12 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A, R_{FBT} = 1 MΩ, PFM variant		40		µA
D_{MAX}	Maximum switch duty cycle(2)			98%		
V_{HC}	FB pin voltage required to trip short-circuit hiccup mode			0.24		V
t_D	Switch voltage dead-time			6.5		ns
T_{SD}	Thermal shutdown temperature	Shutdown temperature		163		°C
T_{SD}	Thermal shutdown temperature	Recovery temperature		141		°C

(1) Deviation in V_{OUT} from nominal output voltage value at V_{IN} = 24 V, I_{OUT} = 0 A to full load
(2) In dropout, the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately: f_{MIN} = 1 / (t_{ON-MAX} + $t_{OFF-MIN}$). D_{MAX} = t_{ON-MAX} / (t_{ON-MAX} + $t_{OFF-MIN}$).

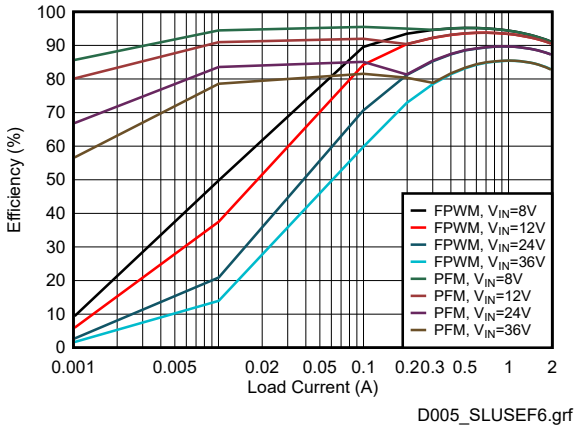
7.7 Typical Characteristics

V_{IN} = 12 V, f_{SW} = 500 kHz ,T_A = 25°C, unless otherwise specified.



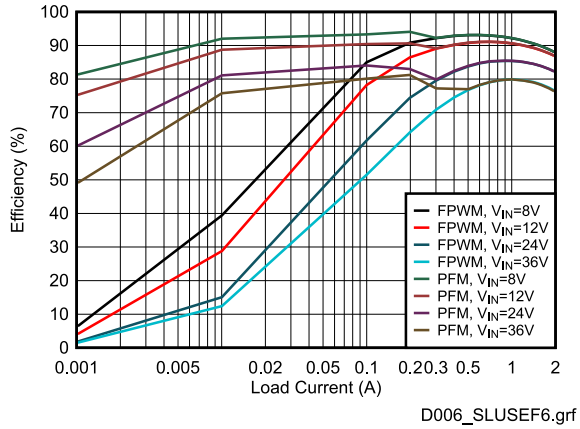
f_{SW} = 500 kHz V_{OUT} = 3.3 V

Figure 7-1. 3.3-V Efficiency vs Load Current



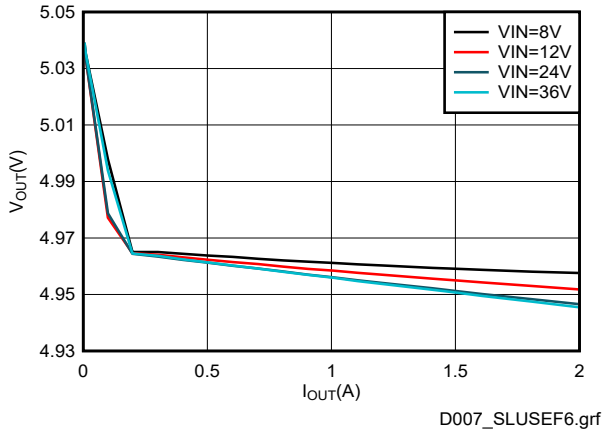
f_{SW} = 1.1 MHz V_{OUT} = 5 V

Figure 7-2. 5-V Efficiency vs Load Current



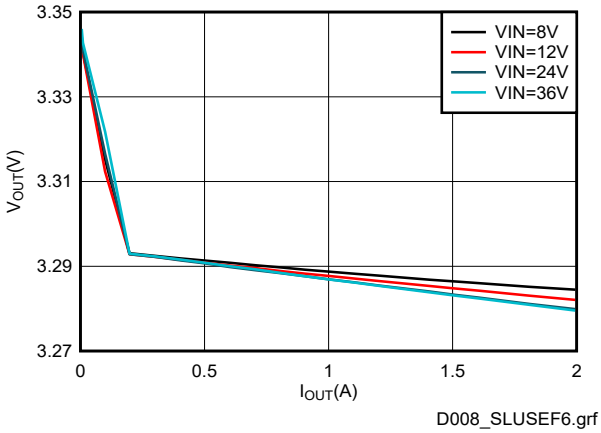
f_{SW} = 1.1 MHz V_{OUT} = 3.3 V

Figure 7-3. 3.3-V Efficiency vs Load Current



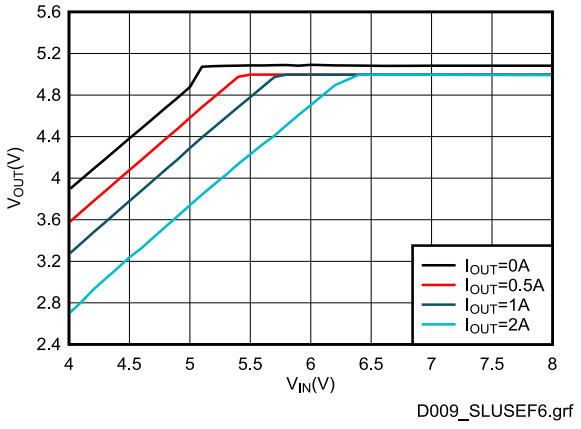
f_{SW} = 500 kHz V_{OUT} = 5 V PFM version

Figure 7-4. 5-V Load Regulation



f_{SW} = 500 kHz V_{OUT} = 3.3 V PFM version

Figure 7-5. 3.3-V Load Regulation



f_{SW} = 500 kHz V_{OUT} = 5 V FPM version

Figure 7-6. 5-V Dropout

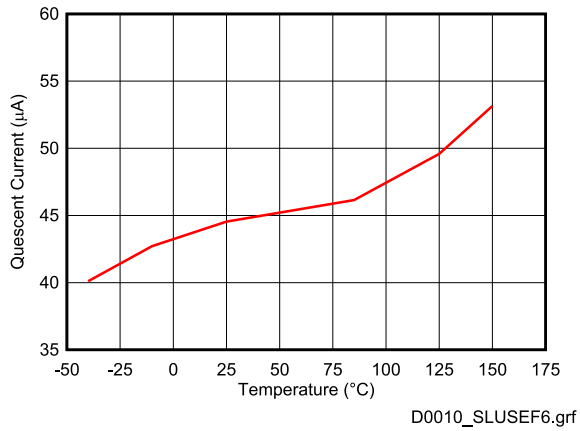


Figure 7-7. I_Q vs Temperature

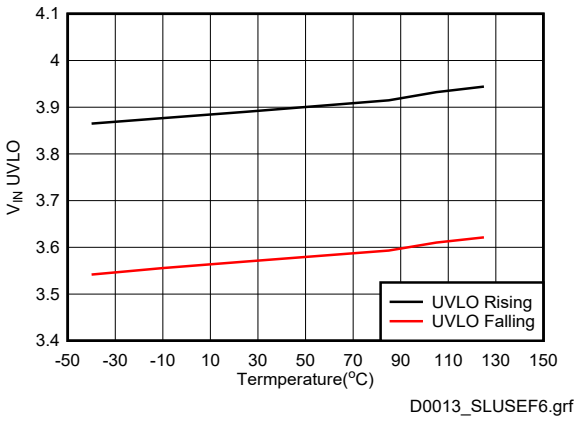


Figure 7-8. V_{IN} UVLO vs Temperature

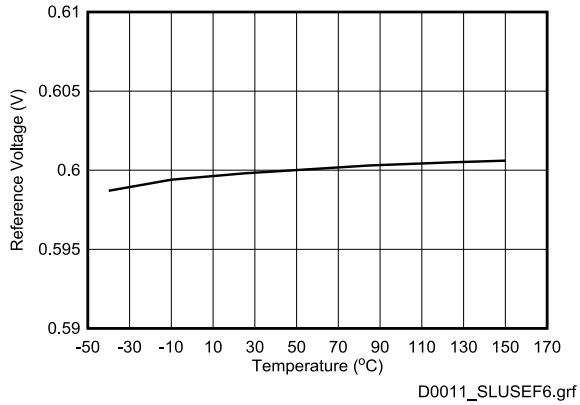


Figure 7-9. Reference Voltage vs Temperature

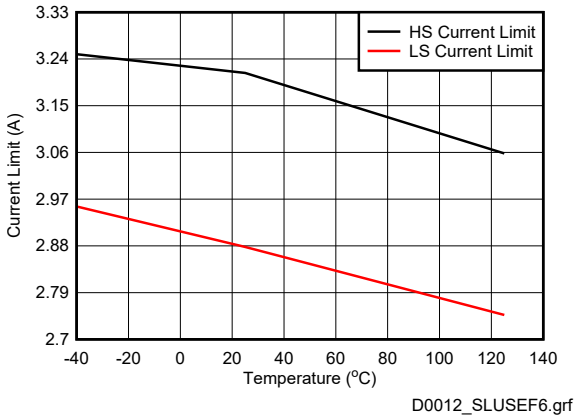


Figure 7-10. HS and LS Current Limit vs Temperature

8 Detailed Description

8.1 Overview

The LMR51420 is an easy-to-use synchronous step-down DC-DC converter operating from a 4.5-V to 36-V supply voltage. The device is capable of delivering up to 2-A DC load current in a very small solution size. The family has multiple versions applicable to various applications. See Section 5 for detailed information.

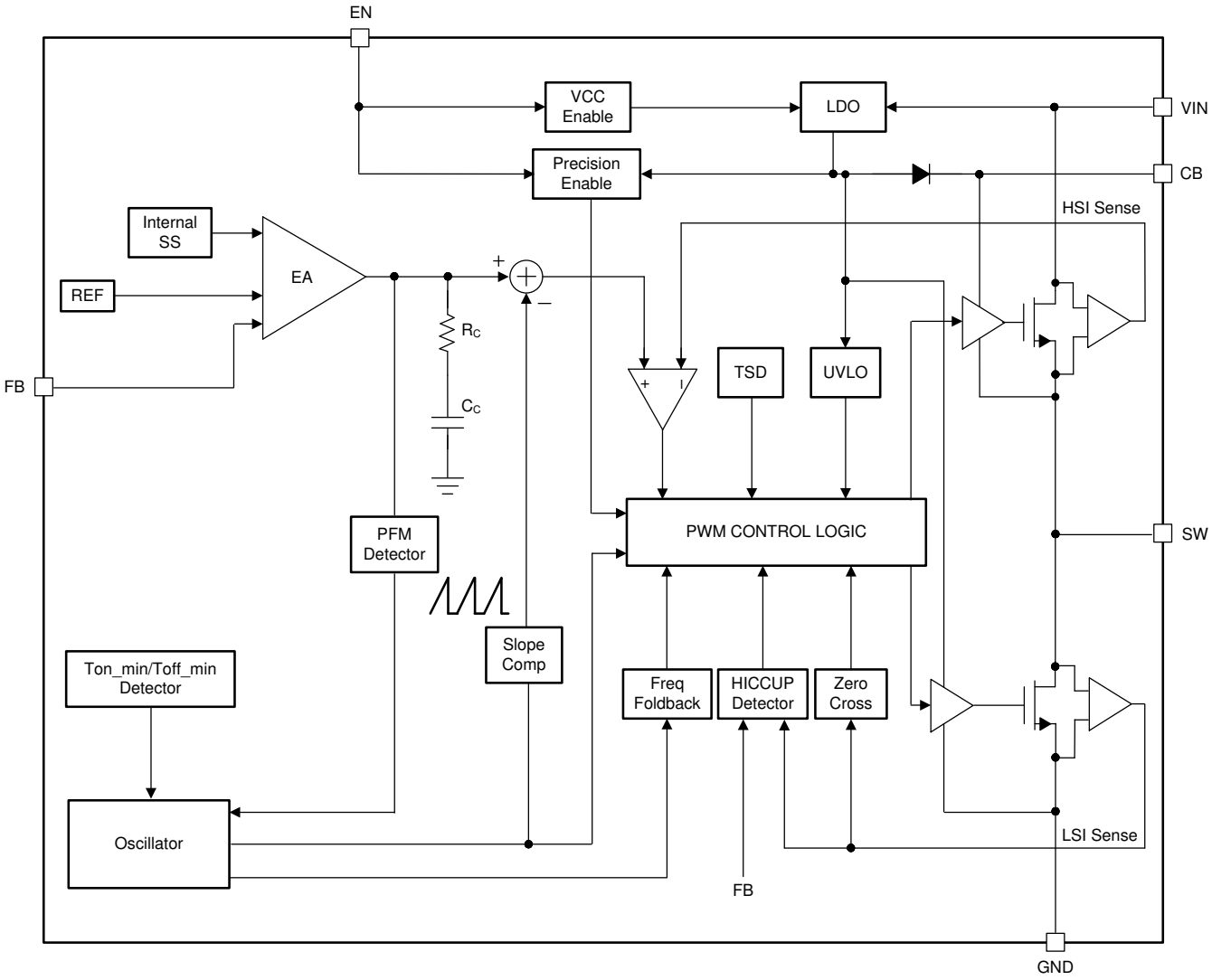
The LMR51420 employs fixed-frequency peak-current mode control. The PFM version enters PFM mode at light load to achieve high efficiency. A FPWM version is provided to achieve low output voltage ripple, tight output voltage regulation, and constant switching frequency at light load. The device is internally compensated, which reduces design time and requires few external components.

Additional features such as precision enable and internal soft start provide a flexible and easy-to-use solution for a wide range of applications. Protection features include the following:

- Thermal shutdown
- V_{IN} undervoltage lockout
- Cycle-by-cycle current limit
- Hiccup mode short-circuit protection

This family of devices requires very few external components and has a pinout designed for simple, optimal PCB layout.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fixed Frequency Peak Current Mode Control

The following operating description of the LMR51420 refers to Section 8.2 and to the waveforms in Figure 8-1. The LMR51420 is a step-down synchronous buck converter with integrated high-side (HS) and low-side (LS) switches (synchronous rectifier). The LMR51420 supplies a regulated output voltage by turning on the high-side and low-side NMOS switches with controlled duty cycle. During the high-side switch on time, the SW pin voltage swings up to approximately V_{IN}, and the inductor current, i_L, increases with a linear slope of (V_{IN} – V_{OUT}) / L. When the high-side switch is turned off by the control logic, the low-side switch is turned on after an anti-shoot–through dead time. Inductor current discharges through the low-side switch with a slope of –V_{OUT} / L. The control parameter of a buck converter is defined as:

$$\text{Duty Cycle } D = t_{ON} / t_{SW} \quad (1)$$

where

- t_{ON} is the high-side switch on time.
- t_{SW} is the switching period.

The converter control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal buck converter where losses are ignored, and D is proportional to the output voltage and inversely proportional to the input voltage:

$$D = V_{OUT} / V_{IN} \quad (2)$$

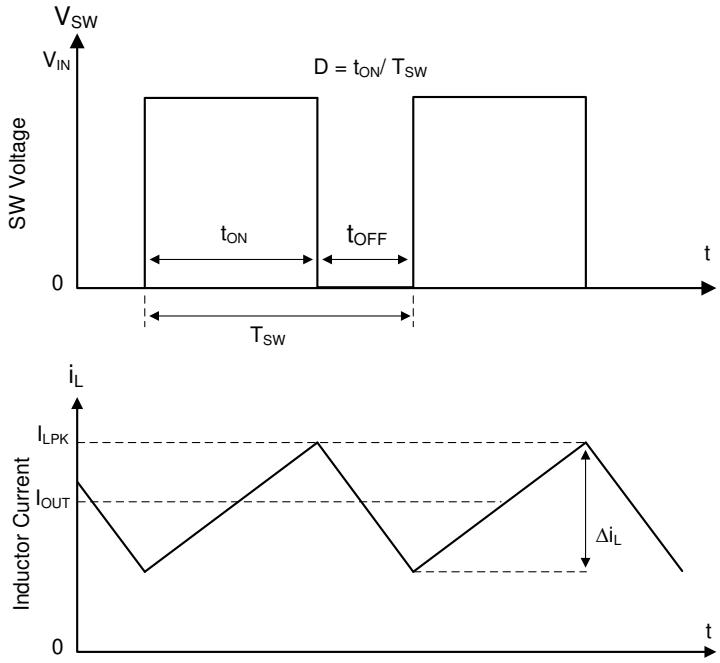


Figure 8-1. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The LMR51420 employs fixed-frequency peak-current mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak-current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current threshold to control the on time of the high-side switch. The voltage feedback loop is internally compensated, which allows for fewer external components, making designing easy and providing stable operation when using a variety of output capacitors. The converter operates with fixed switching frequency at normal load conditions. During light-load condition, the LMR51420 operates in PFM mode to maintain high efficiency (PFM version) or in FPWM mode for low output voltage ripple, tight output voltage regulation, and constant switching frequency (FPWM version).

8.3.2 Adjustable Output Voltage

A precision 0.6-V reference voltage (V_{REF}) is used to maintain a tightly regulated output voltage over the entire operating temperature range. The output voltage is set by a resistor divider from V_{OUT} to the FB pin. TI recommends using 1% tolerance resistors with a low temperature coefficient for the FB divider. Select the bottom-side resistor, R_{FBB}, for the desired divider current and use Equation 3 to calculate the top-side resistor, R_{FBT}. The recommend range for R_{FBT} is 10 kΩ to 100 kΩ. A lower R_{FBT} value can be used if pre-loading is desired to reduce V_{OUT} offset in PFM operation. Lower R_{FBT} reduces efficiency at very light load. Less static current goes through a larger R_{FBT} and can be more desirable when light-load efficiency is critical. However, TI does not recommend R_{FBT} larger than 1 MΩ because it makes the feedback path more susceptible to noise. Larger R_{FBT} values require a more carefully designed feedback path trace from the feedback resistors to the feedback pin of the device. The tolerance and temperature variation of the resistor divider network affect the output voltage regulation.

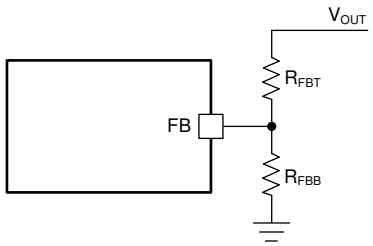


Figure 8-2. Output Voltage Setting

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (3)$$

8.3.3 Enable

The voltage on the EN pin controls the ON and OFF operation of the LMR51420. A voltage of less than 0.95 V shuts down the device, while a voltage of greater than 1.36 V is required to start the converter. The EN pin is an input and cannot be left open or floating. The simplest way to enable the operation of the LMR51420 is to connect EN to VIN. This allows self-start–up of the LMR51420 when V_{IN} is within the operating range.

Many applications benefit from the employment of an enable divider R_{ENT} and R_{ENB} (Figure 8-3) to establish a precision system UVLO level for the converter. System UVLO can be used for supplies operating from utility power as well as battery power. System UVLO can also be used for sequencing, ensuring reliable operation, or supplying protection, such as a battery discharge level. An external logic signal can also be used to drive EN input for system sequencing and protection.

Note

The EN pin voltage must not to be greater than V_{IN} + 0.3 V. Do not apply EN voltage when V_{IN} is 0 V.

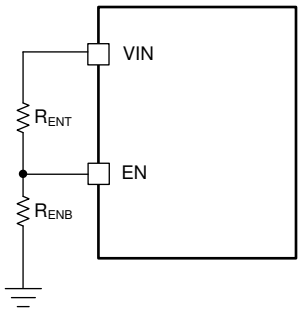


Figure 8-3. System UVLO by an Enable Divider

8.3.4 Minimum On Time, Minimum Off Time, and Frequency Foldback

Minimum on time (t_{ON_MIN}) is the shortest duration of time that the high-side switch can be turned on. t_{ON_MIN} is typically 70 ns for the LMR51420. Minimum off time (t_{OFF_MIN}) is the shortest duration of time that the high-side switch can be off. t_{OFF_MIN} is typically 150 ns. In CCM operation, t_{ON_MIN} and t_{OFF_MIN} limit the voltage conversion range without switching frequency foldback.

The minimum duty cycle without frequency foldback allowed is:

$$D_{MIN} = t_{ON\_MIN} \times f_{SW} \quad (4)$$

The maximum duty cycle without frequency foldback allowed is:

$$D_{MAX} = 1 - t_{OFF\_MIN} \times f_{SW} \quad (5)$$

Given a required output voltage, the maximum V_{IN} without frequency foldback can be found by:

$$V_{IN\_MAX} = \frac{V_{OUT}}{f_{SW} \times T_{ON\_MIN}} \quad (6)$$

The minimum V_{IN} without frequency foldback can be calculated by:

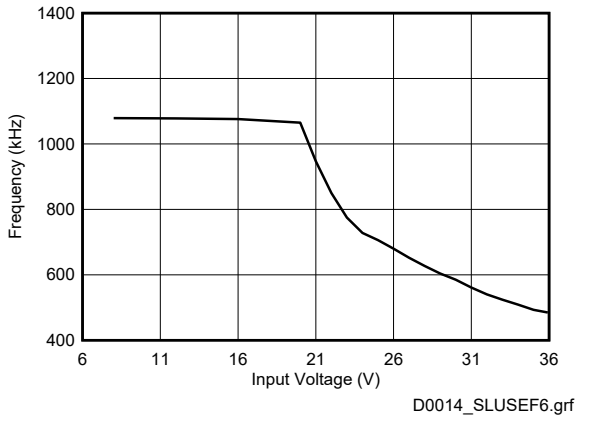
$$V_{IN\_MIN} = \frac{V_{OUT}}{1 - f_{SW} \times T_{OFF\_MIN}} \quad (7)$$

In the LMR51420, a frequency foldback scheme is employed after t_{ON_MIN} or t_{OFF_MIN} is triggered, which can extend the maximum duty cycle or lower the minimum duty cycle.

The on time decreases while V_{IN} voltage increases. After the on time decreases to t_{ON_MIN}, the switching frequency starts to decrease while V_{IN} continues to increase, which lowers the duty cycle further to keep V_{OUT} in regulation according to Equation 4.

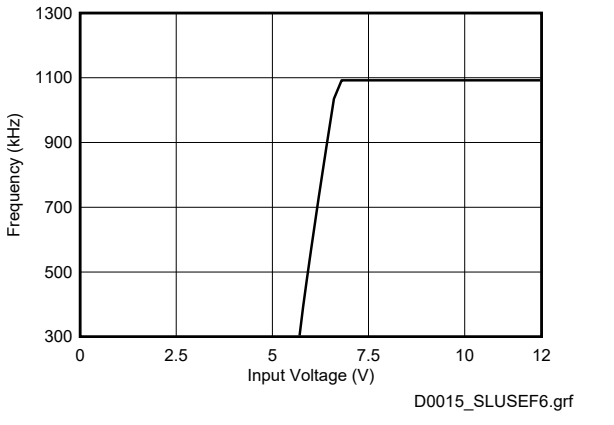
The frequency foldback scheme also works after larger duty cycle is needed under low V_{IN} condition. The frequency decreases after the device reaches t_{OFF_MIN}, which extends the maximum duty cycle according to Equation 5. In such condition, the frequency can be as low as approximately 133 kHz. A wide range of frequency foldback allows for the LMR51420 output voltage to stay in regulation with a much lower supply voltage V_{IN}, which leads to a lower effective dropout.

With frequency foldback while maintaining a regulated output voltage, V_{IN_MAX} is raised, and V_{IN_MIN} is lowered by decreased f_{SW}.



V_{OUT} = 1.8 V f_{SW} = 1.1 MHz I_{OUT} = 2.0 A

Figure 8-4. Frequency Foldback at t_{ON_MIN}



V_{OUT} = 5.0 V f_{SW} = 1.1 MHz I_{OUT} = 2.0 A

Figure 8-5. Frequency Foldback at t_{ON_MIN}

8.3.5 Bootstrap Voltage

The LMR51420 provides an integrated bootstrap voltage converter. A small capacitor between the CB and SW pins provides the gate drive voltage for the high-side MOSFET. The bootstrap capacitor is refreshed when the high-side MOSFET is off and the low-side switch is on. The recommended value of the bootstrap capacitor is 0.1 µF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 16 V or higher for stable performance over temperature and voltage.

8.3.6 Overcurrent and Short-Circuit Protection

The LMR51420 incorporates both peak and valley inductor current limit to provide protection to the device from overloads and short circuits and limit the maximum output current. Valley current limit prevents inductor current runaway during short circuits on the output, while both peak and valley limits work together to limit the maximum output current of the converter. Cycle-by-cycle current limit is used for overloads, while hiccup mode is used for sustained short circuits.

High-side MOSFET overcurrent protection is implemented by the nature of the peak current mode control. The high-side switch current is sensed when the high-side is turned on after a set blanking time. The high-side switch current is compared to the output of the Error Amplifier (EA) minus slope compensation every switching cycle. See *Functional Block Diagram* for more details. The peak current of high-side switch is limited by a clamped maximum peak current threshold, I_{sc} (see the *Electrical Characteristics*), which is constant.

The current going through the low-side MOSFET is also sensed and monitored. When the low-side switch turns on, the inductor current begins to ramp down. The low-side switch is not turned OFF at the end of a switching cycle if its current is above the low-side current limit, I_{LS_LIMIT} (see the *Electrical Characteristics*). The low-side switch is kept ON so that inductor current keeps ramping down until the inductor current ramps below I_{LS_LIMIT}. Then, the low-side switch is turned OFF and the high-side switch is turned on after a dead-time. After I_{LS_LIMIT} is achieved, peak and valley current limit controls the max current deliver and it can be calculated using Equation 8.

$$I_{OUT}\Big|_{max} = \frac{I_{LS\_LIMIT} + I_{SC}}{2} \tag{8}$$

If the feedback voltage is lower than 40% of V_{REF}, the current of the low-side switch triggers I_{LS_LIMIT} for 256 consecutive cycles and hiccup current protection mode is activated. In hiccup mode, the converter shuts down and keeps off for a period of hiccup, t_{HICCUP} (135-ms typical), before the LMR51420 tries to start again. If an overcurrent or short-circuit fault condition still exist, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, preventing overheating and potential damage to the device.

For FPWM version, the inductor current is allowed to go negative. When this current exceeds the low-side negative current limit, I_{LS_NEG}, the low-side switch is turned off and high-side switch is turned on immediately. This is used to protect the low-side switch from excessive negative current.

8.3.7 Soft Start

The integrated soft-start circuit prevents input inrush current impacting the LMR51420 and the input power supply. Soft start is achieved by slowly ramping up the internal reference voltage when the device is first enabled or powered up. The typical soft-start time is 4.0 ms.

The LMR51420 also employs overcurrent protection blanking time, t_{OCP_BLK} (33 ms typical), at the beginning of power up. Without this feature, in applications with a large amount of output capacitors and high V_{OUT}, the inrush current is large enough to trigger the current-limit protection, which can cause a false start as the device enters into hiccup mode. This action results in a continuous recycling of soft start without raising up to the programmed output voltage. The LMR51420 is able to charge the output capacitor to the programmed V_{OUT} by controlling the average inductor current during the start-up sequence in the blanking time, t_{OCP_BLK}.

8.3.8 Thermal Shutdown

The LMR51420 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 163°C. Both high-side and low-side FETs stop switching in thermal shutdown. After the die temperature falls below 141°C, the device reinitiates the power-up sequence controlled by the internal soft-start circuitry.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control for the LMR51420. When V_{EN} is below 0.95 V, the device is in shutdown mode. The LMR51420 also employs V_{IN} undervoltage lockout protection (UVLO). If V_{IN} voltage is below its UVLO threshold of 3.58 V, the converter is turned off.

8.4.2 Active Mode

The LMR51420 is in active mode when both V_{EN} and V_{IN} are above their respective operating threshold. The simplest way to enable the LMR51420 is to connect the EN pin to VIN pin. This allows self-start–up when the input voltage is in the operating range of 4.5 V to 36 V. See Section 8.3.3 for details on setting these operating levels.

In active mode, depending on the load current, the LMR51420 is in one of four modes:

- Continuous conduction mode (CCM) with fixed switching frequency when load current is greater than half of the peak-to-peak inductor current ripple (for both PFM and FPWM versions)
- Discontinuous conduction mode (DCM) with fixed switching frequency when load current is less than half of the peak-to-peak inductor current ripple(only for PFM version)
- Pulse frequency modulation mode (PFM) when switching frequency is decreased at very light load (only for PFM version)
- Forced pulse width modulation mode (FPWM) with fixed switching frequency even at light load (only for FPWM version)

8.4.3 CCM Mode

Continuous conduction mode (CCM) operation is employed in the LMR51420 when the load current is greater than half of the peak-to-peak inductor current. In CCM operation, the frequency of operation is fixed, output voltage ripple is at a minimum in this mode and the maximum output current of 2 A can be supplied by the LMR51420.

8.4.4 Light-Load Operation (PFM Version)

For PFM version, when the load current is lower than half of the peak-to-peak inductor current in CCM, the LMR51420 operates in discontinuous conduction mode (DCM), also known as diode emulation mode (DEM). In DCM operation, the low-side switch is turned off when the inductor current drops to I_{ZC} (20 mA typical) to improve efficiency. Both switching losses and conduction losses are reduced in DCM, compared to forced PWM operation at light load.

During light-load operation, pulse frequency modulation (PFM) mode is activated to maintain high efficiency operation. When either the minimum high-side switch on time, t_{ON_MIN}, or the minimum peak inductor current, I_{PEAK_MIN} (0.3 A typical), is reached, the switching frequency decreases to maintain regulation. In PFM mode, switching frequency is decreased by the control loop to maintain output voltage regulation when load current reduces. Switching loss is further reduced in PFM operation due to a significant drop in effective switching frequency.

8.4.5 Light-Load Operation (FPWM Version)

For FPWM version, the LMR51420 is locked in PWM mode at full load range. This operation is maintained, even in no-load condition, by allowing the inductor current to reverse its normal direction. This mode trades off reduced light load efficiency for low output voltage ripple, tight output voltage regulation, and constant switching frequency.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LMR51420 is a step-down DC-to-DC converter. The device is typically used to convert a higher input voltage to a lower output DC voltage with a maximum output current of 2 A. The following design procedure can be used to select components for the LMR51420. Alternately, the WEBENCH® software can be used to generate complete designs. When generating a design, the WEBENCH software uses iterative design procedure and accesses comprehensive databases of components. Go to ti.com for more details.

9.2 Typical Application

The LMR51420 only requires a few external components to convert from a wide voltage range supply to a fixed output voltage. Figure 9-1 shows a basic schematic.

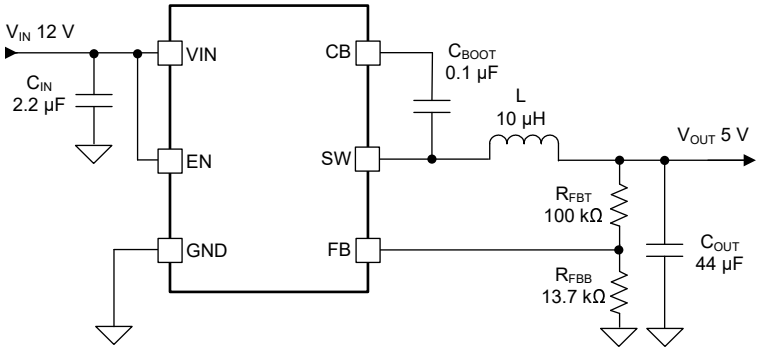


Figure 9-1. Application Circuit

The external components have to fulfill the needs of the application and the stability criteria of the control loop of the device. Table 9-1 can be used to simplify the output filter component selection.

Table 9-1. L and C_{OUT} Typical Values

f_{SW} (kHz)	V_{OUT} (V)	L (µH)	C_{OUT} (µF) (1)	R_{FBT} (kΩ)	R_{FBB} (kΩ)
500	3.3	8.2	2 × 22 µF / 16 V	100	22.1
	5	10	2 × 22 µF / 16 V	100	13.7
	12	22	2 × 22 µF / 25 V	100	5.23

Table 9-2. L and C_{OUT} Typical Values

f_{SW} (kHz)	V_{OUT} (V)	L (µH)	C_{OUT} (µF) (1)	R_{FBT} (kΩ)	R_{FBB} (kΩ)
1100	3.3	3.3	2 × 10 µF / 16 V	100	22.1
	5	4.7	2 × 10 µF / 16 V	100	13.7
	12	8.2	2 × 10 µF / 25 V	100	5.23

(1) A ceramic capacitor is used in this table.

9.2.1 Design Requirements

The detailed design procedure is described based on a design example. For this design example, use the parameters listed in Table 9-3 as the input parameters.

Table 9-3. Design Example Parameters

Parameter	Value
Input voltage, V_{IN}	12 V typical, range from 6 V to 36 V
Output voltage, V_{OUT}	5 V ±3%
Maximum output current, I_{OUT_MAX}	2 A
Output overshoot and undershoot 0.5 A to 1.5 A	5%
Output voltage ripple	0.5%
Operating frequency	500 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR51420 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Output Voltage Set-Point

The output voltage of the LMR51420 device is externally adjustable using a resistor divider network. The divider network is comprised of a top feedback resistor R_{FBT} and bottom feedback resistor R_{FBB}. Equation 9 is used to determine the output voltage of the converter:

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \tag{9}$$

Choose the value of R_{FBB} to be 13.7 kΩ. With the desired output voltage set to 5 V and the V_{REF} = 0.6 V, the R_{FBT} value can then be calculated using Equation 9. The formula yields a value 100.4 kΩ. A standard value of 100 kΩ is selected.

9.2.2.3 Switching Frequency

The higher switching frequency allows for lower-value inductors and smaller output capacitors, which result in a smaller solution size and lower component cost. However, higher switching frequency brings more switching loss, making the solution less efficient and produce more heat. The switching frequency is also limited by the minimum on time of the following as mentioned in Section 8.3.4:

- Integrated power switch
- Input voltage
- Output voltage
- Frequency shift limitation

For this example, a switching frequency of 500 kHz is selected.

9.2.2.4 Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current, and the RMS current. The inductance is based on the desired peak-to-peak ripple current, Δi_L. Because the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance, L_{MIN}. Use Equation 11 to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current of the device. A reasonable value of K_{IND} must be 20% to 60% of maximum I_{OUT} supported by the converter. During an instantaneous overcurrent operation event, the RMS and peak inductor current can be high. The inductor saturation current must be higher than peak current limit level.

$$\Delta i_L = \frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT} \right)}{V_{IN\_MAX} \times L \times f_{SW}} \tag{10}$$

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \tag{11}$$

In general, choose lower inductance in switching power supplies because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. Too low of an inductance can generate too large of an inductor current ripple such that overcurrent protection at the full load can be falsely triggered and generates more inductor core loss because the current ripple is larger. Larger inductor current ripple also implies larger output voltage ripple with the same output capacitors. With peak current mode control, ensure there is an adequate amount of inductor ripple current. A larger inductor ripple current improves the comparator signal-to-noise ratio.

For this design example, choose K_{IND} = 0.3. The minimum inductor value is calculated to be 9.7 µH. Choose the nearest standard 10-µH ferrite inductor with a capability of 3-A RMS current and 4-A saturation current.

9.2.2.5 Output Capacitor Selection

The device is designed to be used with a wide variety of LC filters. Minimize the output capacitance to keep cost and size down. The output capacitor or capacitors, C_{OUT}, must be chosen with care because it directly affects the steady state output voltage ripple, loop stability, and output voltage overshoot and undershoot during load current transient. The output voltage ripple is essentially composed of two parts. One part is caused by the inductor ripple current flowing through the Equivalent Series Resistance (ESR) of the output capacitors:

$$\Delta V_{OUT\_ESR} = \Delta i_L \times ESR = K_{IND} \times I_{OUT} \times ESR \tag{12}$$

The other part is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\_C} = \frac{\Delta i_L}{8 \times f_{SW} \times C_{OUT}} = \frac{K_{IND} \times I_{OUT}}{8 \times f_{SW} \times C_{OUT}} \tag{13}$$

The two components of the voltage ripple are not in-phase, therefore, the actual peak-to-peak ripple is less than the sum of the two peaks.

Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation with presence of large current steps and fast slew rates. When a large load step occurs, output capacitors provide the required charge before the inductor current can slew to an appropriate level. The control loop of the converter usually requires eight or more clock cycles to regulate the inductor current equal to the new load level during this time. The output capacitance must be large enough to supply the current difference for eight clock cycles to maintain the output voltage within the specified range. Equation 14 shows the minimum output capacitance needed for a specified V_{OUT} overshoot and undershoot.

$$C_{OUT} > \frac{1}{2} \times \frac{8 \times \left(I_{OH} - I_{OL} \right)}{f_{SW} \times \Delta V_{OUT\_SHOOT}} \tag{14}$$

where

- K_{IND} is the ripple ratio of the inductor current (Δi_L / I_{OUT}).
- I_{OL} is the low level output current during load transient.
- I_{OH} is the high level output current during load transient.
- V_{OUT_SHOOT} is the target output voltage overshoot or undershoot.

For this design example, the target output ripple is 30 mV. Assuming $\Delta V_{OUT\_ESR} = \Delta V_{OUT\_C}$ = 30 mV, choose K_{IND} = 0.3. Equation 12 yields ESR no larger than 75 mΩ and Equation 13 yields C_{OUT} no smaller than 12 µF. For the target overshoot and undershoot limitation of this design, ΔV_{OUT_SHOOT} = 5% × V_{OUT} = 250 mV. The C_{OUT} can be calculated to be no less than 32 µF by Equation 14. In summary, the most stringent criterion for the output capacitor is 44 µF. For this design, two 22-µF, 25-V, X7R ceramic capacitors with 5-mΩ ESR are used.

9.2.2.6 Input Capacitor Selection

The LMR51420 device requires a high frequency input decoupling capacitor or capacitor. The typical recommended value for the high frequency decoupling capacitor is 4.7 µF or higher. TI recommends a high-quality ceramic type X5R or X7R with a sufficient voltage rating. The voltage rating must be greater than the maximum input voltage. To compensate the derating of ceramic capacitors, TI recommends a voltage rating of twice the maximum input voltage. For this design, two 4.7-µF, X7R dielectric capacitor rated for 50 V are used for the input decoupling capacitor. The equivalent series resistance (ESR) is approximately 10 mΩ and the current rating is 1 A. Include a capacitor with a value of 0.1 µF for high-frequency filtering and place it as close as possible to the device pins.

9.2.2.7 Bootstrap Capacitor

Every LMR51420 design requires a bootstrap capacitor, C_{BOOT}. The recommended bootstrap capacitor is 0.1 µF and rated at 16 V or higher. The bootstrap capacitor is located between the SW pin and the CB pin. The bootstrap capacitor must be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

9.2.2.8 Undervoltage Lockout Set-Point

The system undervoltage lockout (UVLO) is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. Equation 15 can be used to determine the V_{IN} UVLO level.

$$V_{IN\_RISING} = V_{ENH} \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \tag{15}$$

The EN rising threshold (V_{ENH}) for the LMR51420 is set to be 1.23 V (typical). Choose a value of 200 kΩ for R_{ENB} to minimize input current from the supply. If the desired V_{IN} UVLO level is at 6.0 V, then the value of R_{ENT} can be calculated using Equation 16:

$$R_{ENT} = \left(\frac{V_{IN\_RISING}}{V_{ENH}} - 1 \right) \times R_{ENB} \tag{16}$$

The above equation yields a value of 775.6 kΩ, a standard value of 768 kΩ is selected. The resulting falling UVLO threshold, equals 5.3 V, can be calculated by Equation 17 where EN hysteresis voltage, V_{EN_HYS}, is 0.13 V (typical).

$$V_{IN\_FALLING} = \left(V_{ENH} - V_{EN\_HYS} \right) \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \tag{17}$$

9.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, V_{OUT} = 5 V, f_{SW} = 500 kHz, L = 10 µH, C_{OUT} = 44 µF, T = 25°C.

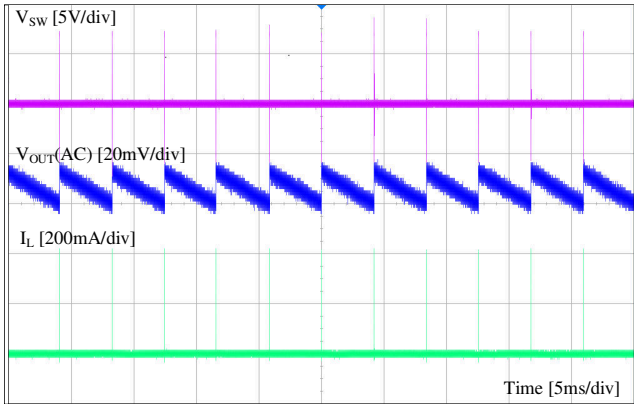


Figure 9-2. Ripple at No Load

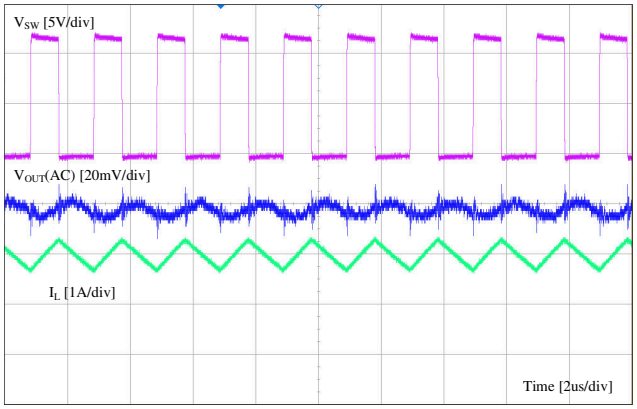


Figure 9-3. Ripple at Full Load

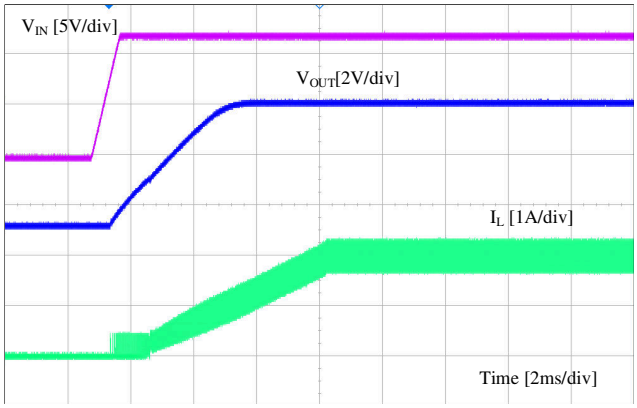


Figure 9-4. Start-Up by V_{IN}

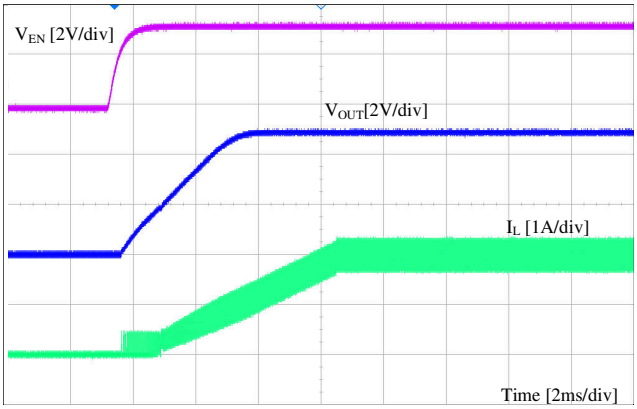


Figure 9-5. Start-Up by EN

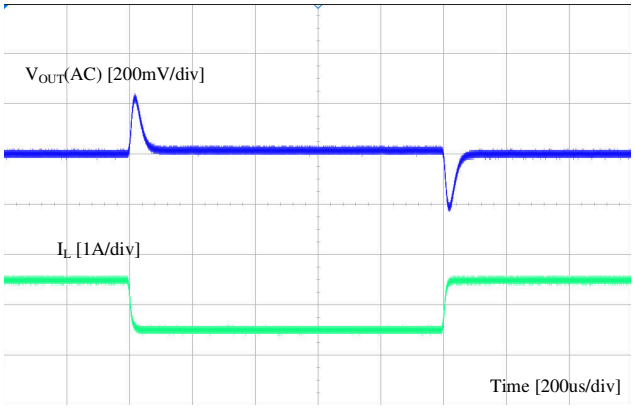


Figure 9-6. Load Transient

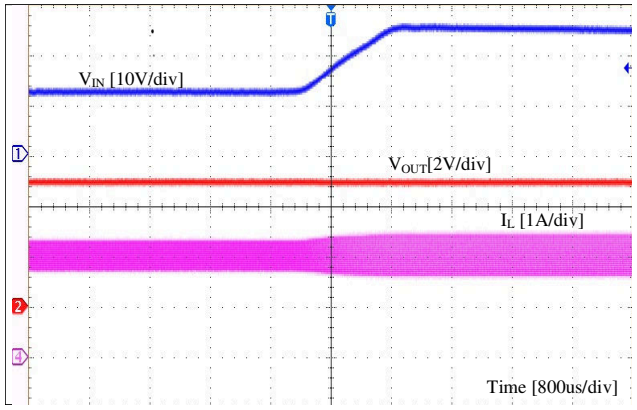


Figure 9-7. Line Transient

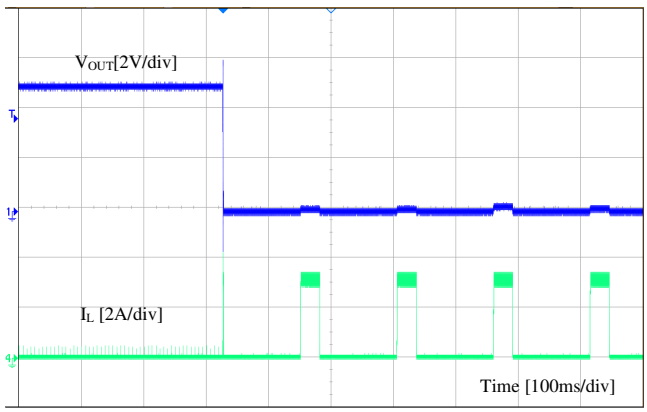


Figure 9-8. Short Protection

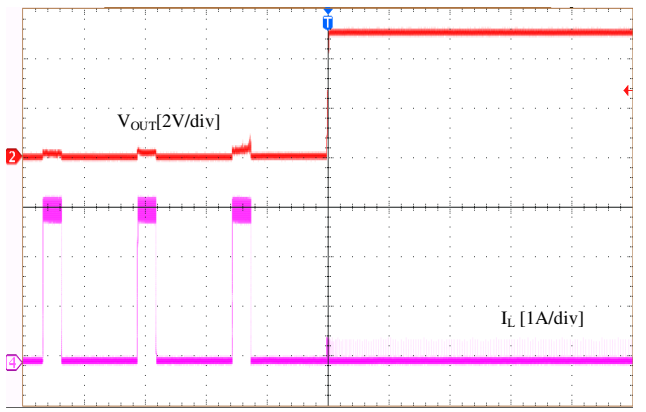


Figure 9-9. Short Recovery

9.3 Power Supply Recommendations

The LMR51420 is designed to operate from an input voltage supply range between 4.5 V and 36 V. This input supply must be well-regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LMR51420 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LMR51420 additional bulk capacitance can be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 10-µF or 22-µF electrolytic capacitor is a typical choice.

9.4 Layout

9.4.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

- The input bypass capacitor C_{IN} must be placed as close as possible to the VIN and GND pins. Grounding for both the input and output capacitors must consist of localized top-side planes that connect to the GND pin.
- Minimize trace length to the FB pin net. Both feedback resistors, R_{FBT} and R_{FBB}, must be located close to the FB pin. If V_{OUT} accuracy at the load is important, make sure V_{OUT} sense is made at the load. Route V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a shielded layer.
- Use the ground plane in one of the middle layers as noise shielding and heat dissipation path if possible.
- Make V_{IN}, V_{OUT}, and ground bus connections as wide as possible, which reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
- Provide adequate device heat-sinking. GND, VIN, and SW pins provide the main heat dissipation path. Make the GND, VIN, and SW plane area as large as possible. Use an array of heat-sinking vias to connect the top side ground plane to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

9.4.1.1 Compact Layout for EMI Reduction

Radiated EMI is generated by the high di/dt components in pulsing currents in switching converters. The larger area covered by the path of a pulsing current, the more EMI is generated. High frequency ceramic bypass capacitors at the input side provide a primary path for the high di/dt components of the pulsing current. Placing a ceramic bypass capacitor or capacitors as close as possible to the VIN and GND pins is the key to EMI reduction.

The SW pin connected to the inductor must be as short as possible, and just wide enough to carry the load current without excessive heating. Short, thick traces or copper pours (shapes) must be used for high current conduction path to minimize parasitic resistance. The output capacitors must be placed close to the V_{OUT} end of the inductor and closely grounded to the GND pin.

9.4.1.2 Feedback Resistors

To reduce noise sensitivity of the output voltage feedback path, make sure to place the resistor divider close to the FB pin, rather than close to the load. The FB pin is the input to the error amplifier, so it is a high impedance node and very sensitive to noise. Placing the resistor divider closer to the FB pin reduces the trace length of FB signal and reduces noise coupling. The output node is a low impedance node, so the trace from V_{OUT} to the resistor divider can be long if short path is not available.

If voltage accuracy at the load is important, make sure voltage sense is made at the load. Doing so corrects for voltage drops along the traces and provides the best output accuracy. The voltage sense trace from the load to the feedback resistor divider must be routed away from the SW node path and the inductor to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This effect is most important when high value resistors are used to set the output voltage. TI recommends to route the voltage sense trace and place the resistor divider on a different layer than the inductor and SW node path, such that there is a ground plane in between the feedback trace and inductor and SW node polygon, which provides further shielding for the voltage feedback path from EMI noises.

9.4.2 Layout Example

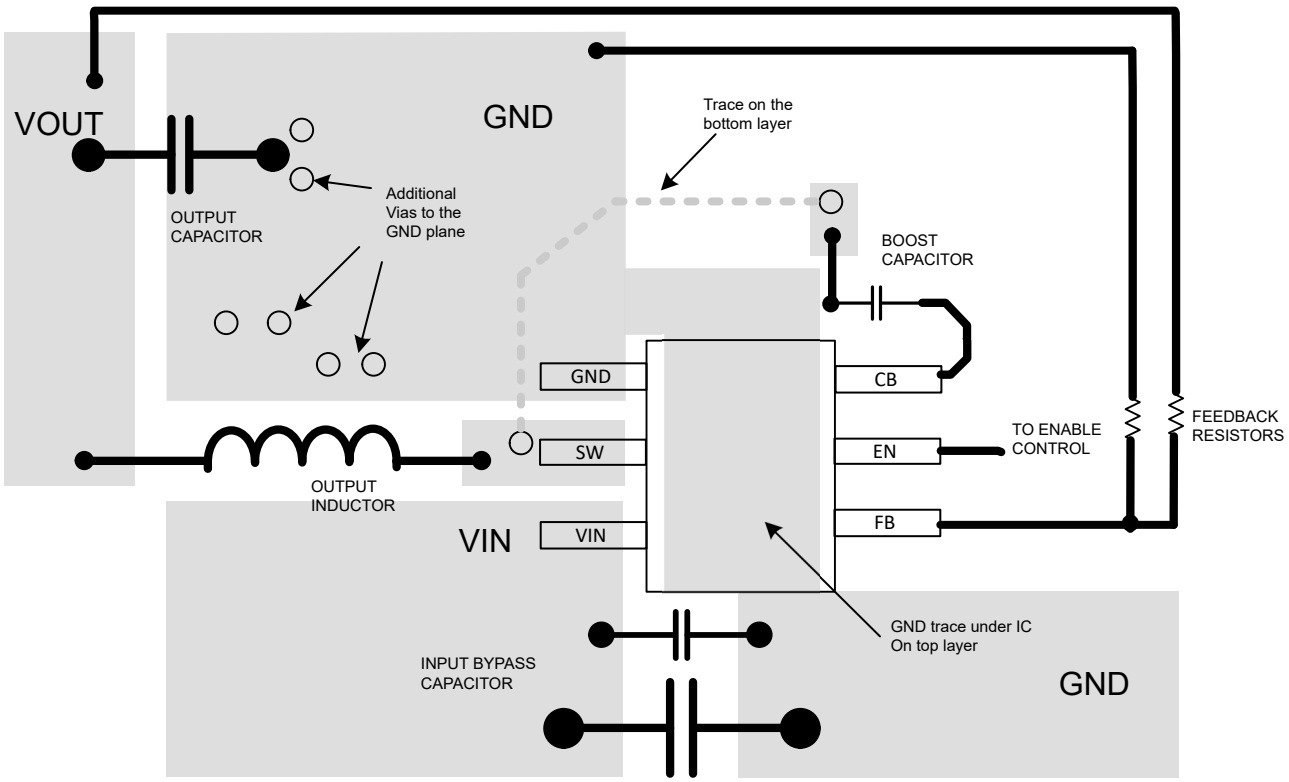


Figure 9-10. Layout

10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

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10.1.2 Development Support

10.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR51420 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies*

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

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WEBENCH® and SIMPLE SWITCHER® are registered trademarks of Texas Instruments.
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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMR51420XDDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 150	4AXP
LMR51420XDDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	4AXP
LMR51420XFDDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 150	4AXF
LMR51420XFDDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	4AXF
LMR51420YDDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 150	4AYP
LMR51420YDDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	4AYP
LMR51420YFDDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 150	4AYF
LMR51420YFDDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	4AYF

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

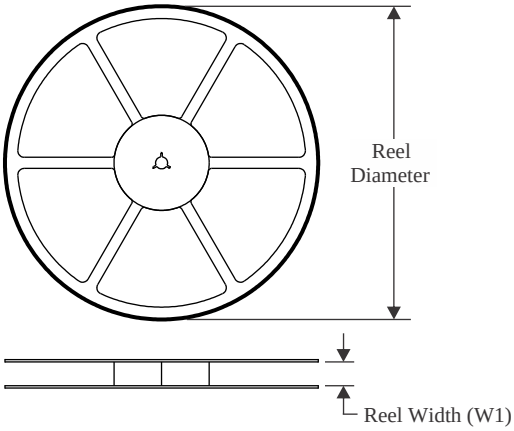
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

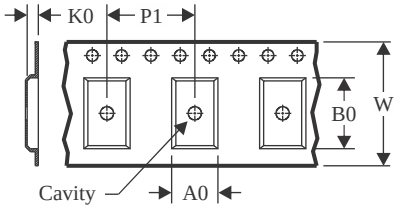
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

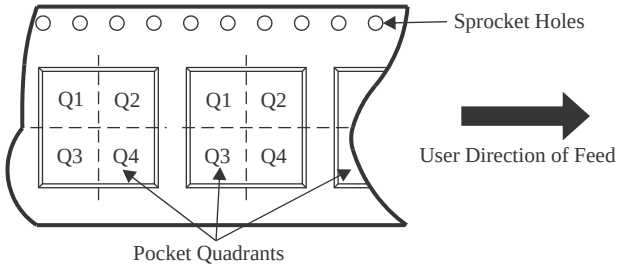


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

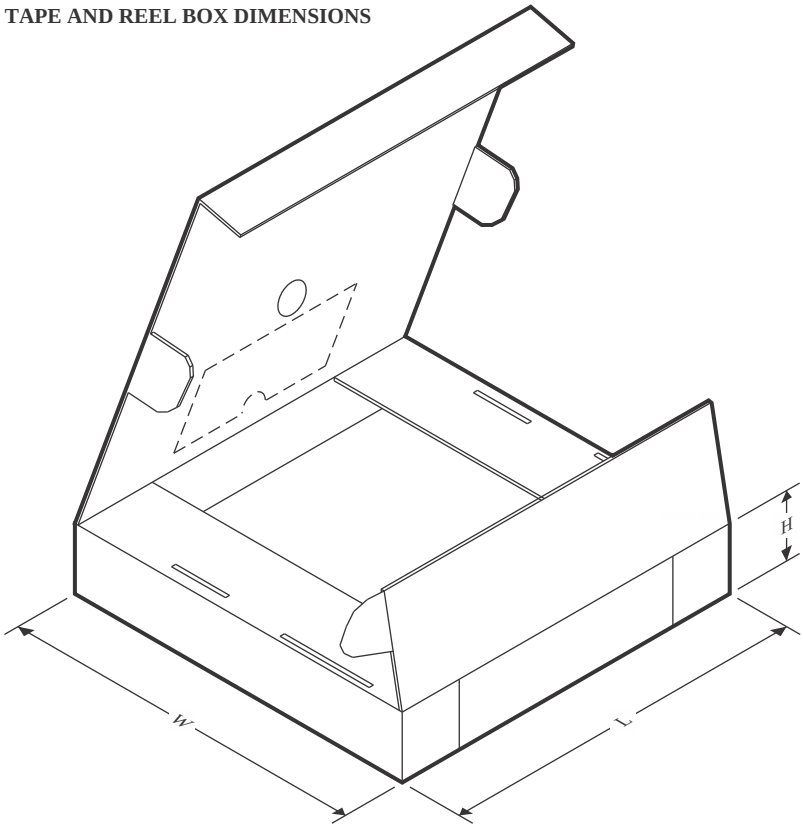
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR51420XDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR51420XFDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR51420YDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR51420YFDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

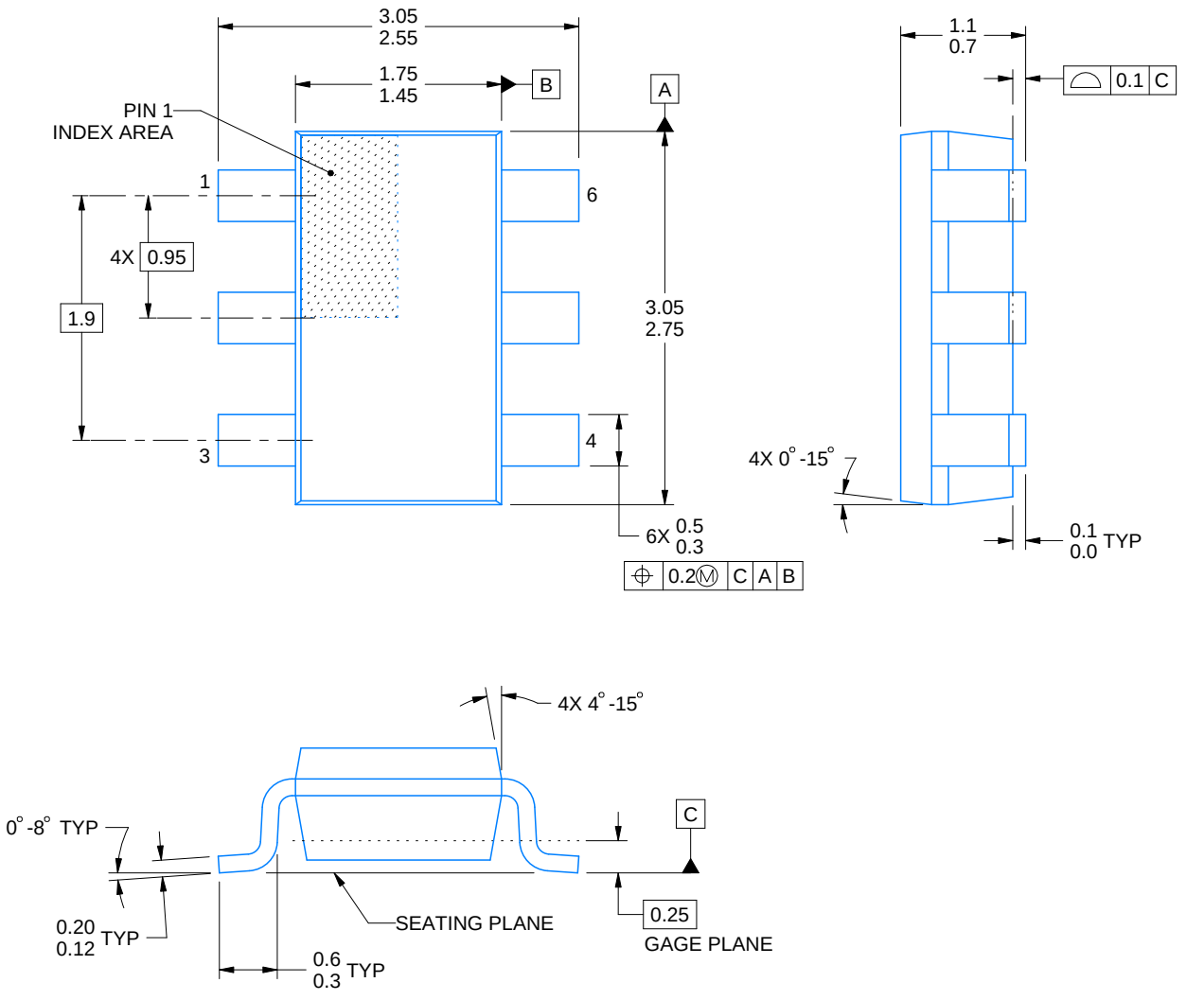
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR51420XDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMR51420XFDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMR51420YDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMR51420YFDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



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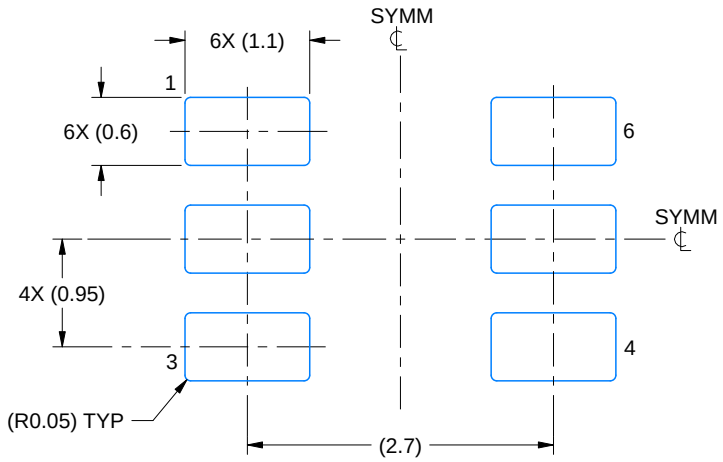
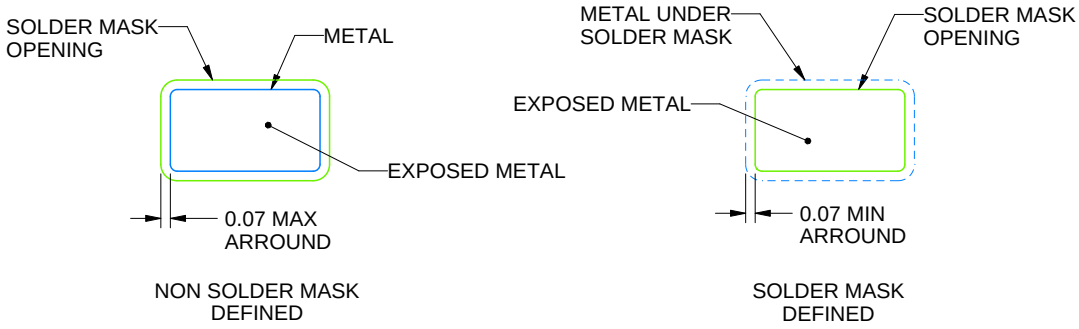
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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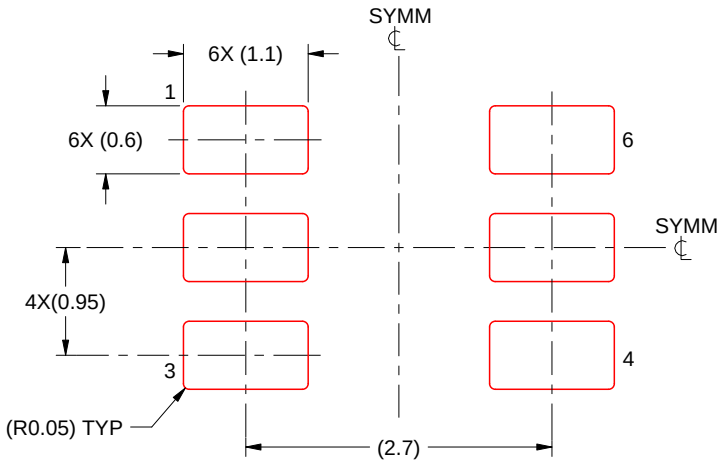
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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