LMR70410 4V to 40V, 1A Synchronous Buck Converter

1 Features

- Configured for rugged industrial applications
  - 4V to 40V input voltage range
  - 1A continuous output current
  - 60ns minimum on-time
  - 1.1MHz fixed switching frequency
  - –40ºC to 150ºC junction temperature range
  - Cycle-by-cycle short-circuit protection
  - Precision enable
  - ±1% voltage reference accuracy
  - 1.8ms internal soft start
- Small design size and ease of use
  - Integrated synchronous rectification
  - Internal compensation for ease of use
  - SOT23-6 package
- Forced pulse width modulation (FPWM) and pulse frequency modulation (PFM) modes available
- Pin-to-pin compatibility with existing SOT23-6 devices
  - TPS560430, LMR50410, LMR51410, LMR54410

2 Applications

- Appliances
- Building automation
- Energy infrastructure
- Power delivery

3 Description

LMR70410 is a 40V, 1A synchronous buck switching regulator in an easy to use SOT23-6 package. LMR70410 can deliver up to 1A DC load current in a small design size and can operate between 4V to 40V DC supply voltage. LMR70410 operates at a fixed 1.1MHz switching frequency to support the use of relatively small inductors to optimize overall design size.

LMR70410 features precision enable UVLO which allows the designer to program the input voltage at which the device is turned on or off through the use of a resistor divider between VIN and GND. LMR70410 implements cycle-by-cycle overcurrent protection which limits the maximum output current even as the output voltage falls to zero. Thermal shutdown is implemented to turn off the LMR70410 if the junction temperature exceeds the thermal shutdown threshold.

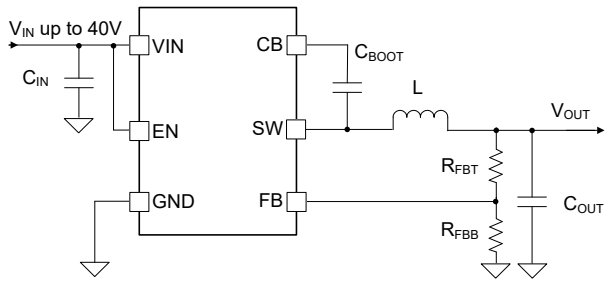
LMR70410 features both FPWM and PFM variants allowing designs to be optimized for either fixed frequency across load or higher light load efficiency. The internal soft-start time is set internally to be 1.8ms (typical).

LMR70410 is part of a family of pin-to-pin devices that support load currents ranging from 0.6A to 1A. This family is pin-to-pin compatible with other SOT23-6 devices, such as TPS560430 and LMR50410.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMR70410	DDC (SOT-23-THN, 6)	2.9mm × 2.8mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Device Comparison

ORDERABLE PART NUMBER	OUTPUT CURRENT (A)	FREQUENCY (kHz)	MODE
LMR70410YAPDDCR	1	1100	PFM
LMR70410YAFDDCR	1	1100	FPWM

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5 Pin Configuration and Functions

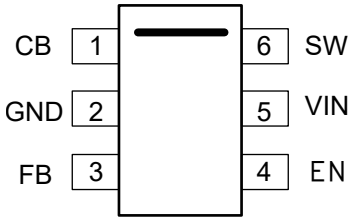

Figure 5-1. 6-Pin SOT-23-THN, DDC Package (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
CB	1	P	Bootstrap capacitor connection for high-side FET driver. Connect a high quality 100nF capacitor from this pin to the SW pin.
GND	2	G	Power ground terminals, connected to the source of low-side FET internally. Connect to system ground, ground side of CIN and COUT. Path to CIN must be as short as possible.
FB	3	I	Feedback input to the converter. Connect a resistor divider to set the output voltage. Never short this terminal to ground during operation.
EN	4	I	Precision enable input to the converter. Do not float. High = on, low = off. Can be tied to VIN. Precision enable input allows adjustable UVLO by external resistor divider
VIN	5	P	Supply input terminal to internal bias LDO and high-side FET. Connect to input supply and input bypass capacitors CIN. Input bypass capacitors must be directly connected to this pin and GND.
SW	6	P	Switching output of the converter. Internally connected to source of the high-side FET and drain of the low-side FET. Connect to power inductor.

(1) I = Input, G = Ground, P = Power.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	VIN to GND	–0.3	45	V
Pin voltage	EN to GND	–0.3	VIN + 0.3	V
Pin voltage	FB to GND	–0.3	5.5	V
Pin voltage	SW to GND	–0.3	45.3	V
Pin voltage	SW to GND less than 10ns transient	–3.5	45	V
Pin voltage	CB to SW	–0.3	5.5	V
Operating Junction Temperature T_J		–40	150	°C
Storage Temperature T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage range	4	40	V
V_{OUT}(2)	Adjustable output voltage range	1	28	V
I_{OUT}	Output current range (1A variant)	0	1	A
T_J	Operating junction temperature	–40	150	°C

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not speicfy specific performance limits. For specified specifications, see Electrical Characteristics.
(2) Under no conditions can the output voltage be allowed to fall below zero volts.

6.4 Thermal Information

THERMAL METRIC(1)		LMR704xx DDC (SOT23-6) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	122	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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(2) The value of $R_{\Theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. These values do not represent the performance obtained in an actual application. For example, the EVM can achieve $R_{\Theta JA}$ = 76°C/W.

6.5 Electrical Characteristics

Limits apply over operating junction temperature T_J range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: VIN = 12V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
$V_{IN_UVLO(R)}$	Undervoltage lockout threshold	Rising threshold	3.5	3.75	4	V
$V_{IN_UVLO(F)}$		Falling threshold			3.1	V
$I_{Q(VIN)}$	VIN quiescent current(1)	Non-switching, V_{EN} = 3.3V, V_{FB} = 1.1V		5	25	µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{EN} = 0V		0.7		µA
$I_{SUPPLY-FPWM}$	Input supply current when in FPWM(1)	Non-switching, V_{IN} = 24V, V_{EN} = 3.3V, V_{FB} = 1.1V		50		µA
ENABLE (EN PIN)						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	1.1	1.2	1.3	V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching	0.85	1.0	1.15	V
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	FB voltage		0.792	0.8	0.808	V
SWITCHING FREQUENCY						
$f_{SW(1.1MHz)}$	Switching frequency 1.1MHz variant		0.935	1.1	1.265	MHz
CURRENT LIMIT						
$I_{HS-PEAK}$	High-side peak current limit(2)	Duty-cycle approaches 0%	1.6	1.75	2.0	A
$I_{LS-VALLEY}$	Low-side valley current limit(2)	1A variant	1	1.2	1.4	A
I_{LS-NEG}	Low-side negative current limit(2)	Sinking current limit on LS FET		–600		mA
STARTUP						
t_{SS}	Internal fixed soft-start time	Time from first SW pulse to V_{FB} = 90% VREF		1.8		ms
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	T_J = 25°C, V_{IN} = 12V		420		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	T_J = 25°C, VIN = 12V		210		mΩ
$t_{ON(min)}$	Minimum ON pulse width	I_{OUT} = 250mA, V_{IN} = 18V, V_{OUT} = 1V		60		ns
$t_{OFF(min)}$	Minimum OFF pulse width	V_{IN} = 4V, V_{OUT} = 3.3V		100		ns
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold	Temperature rising		165		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis			10		°C

(1) The current limit values in this table are tested, open loop, in production. These values can differ from those found in a closed loop application

(2) This current value reported for this parameter is the current used by the device open loop. The current value reported for this parameter does not represent the total input current of the system when in regulation.

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6.6 Typical Characteristics

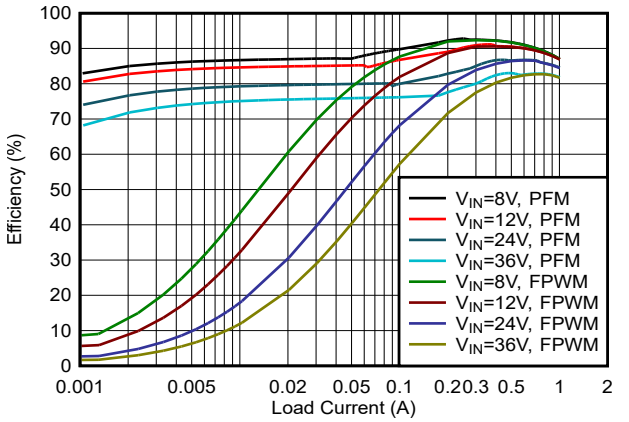

Figure 6-1. 1.1MHz 3.3V Efficiency vs Load Current

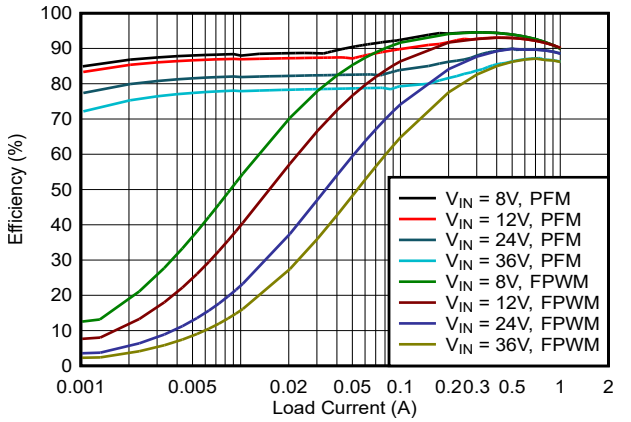

Figure 6-2. 1.1MHz 5V Efficiency vs Load Current

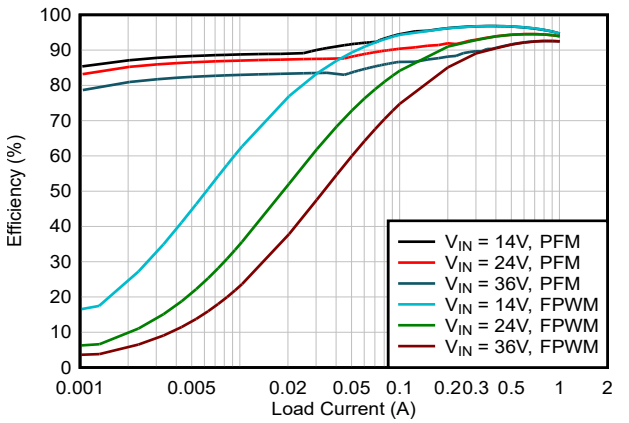

Figure 6-3. 1.1MHz 12V Efficiency vs Load Current

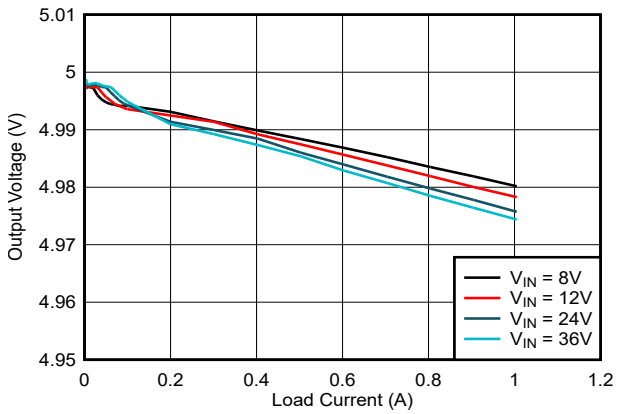

Figure 6-4. 5V Load Regulation

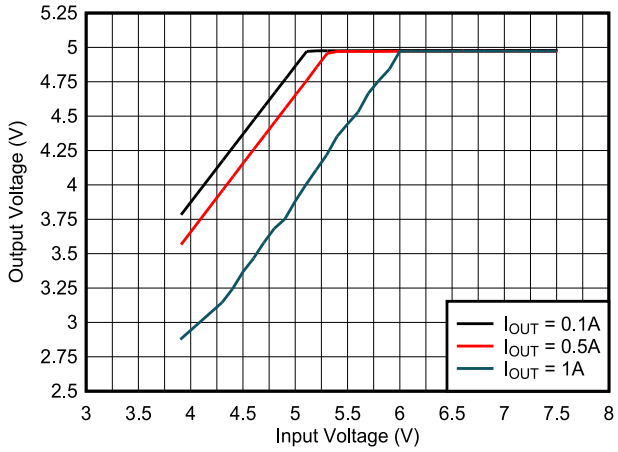

Figure 6-5. 5V Dropout 1.1MHz

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7 Detailed Description

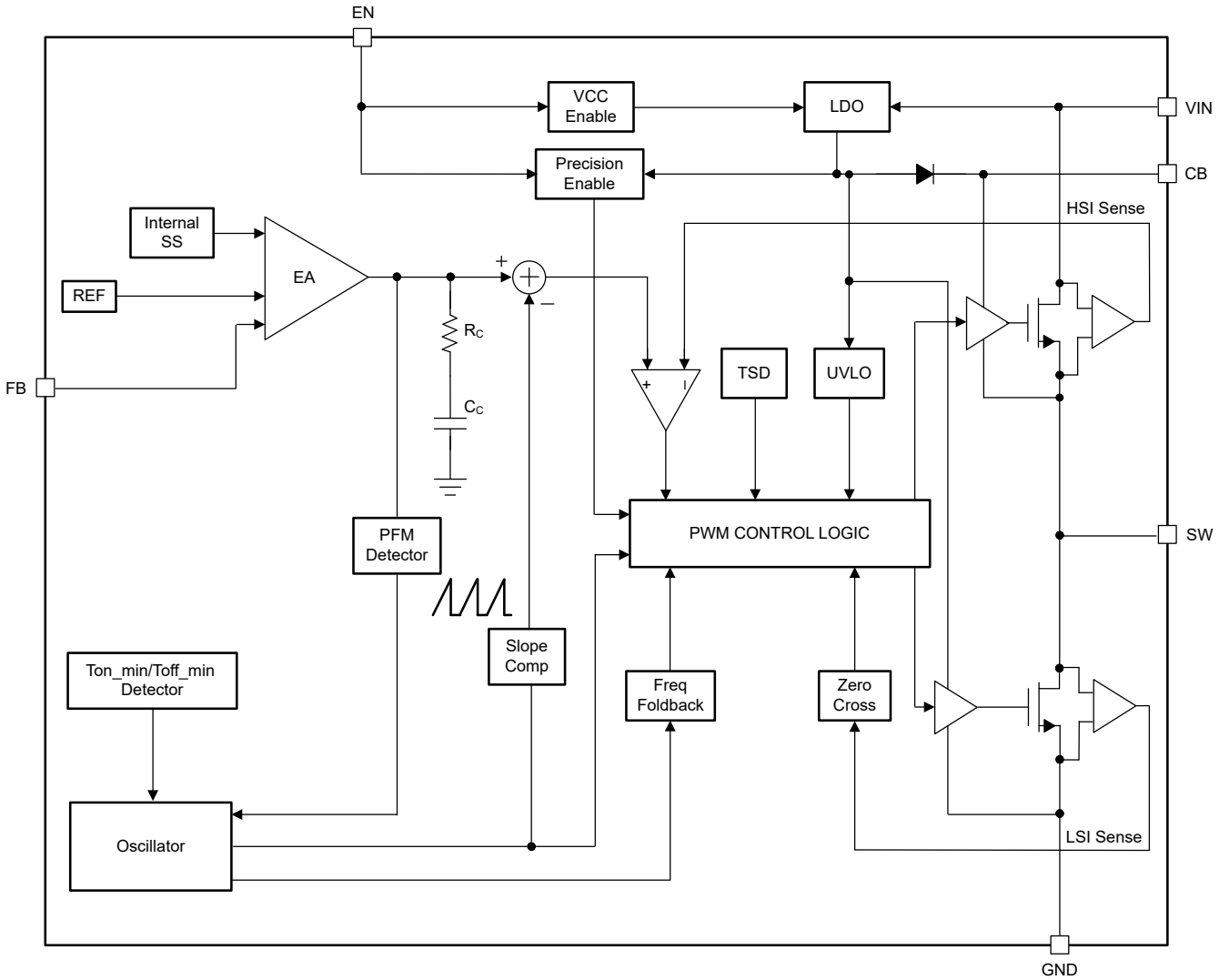
7.1 Overview

LMR70410 has a recommended maximum input voltage of 40V, 1A and is a synchronous buck switching regulator implemented in an SOT23-6 package. LMR70410 has a DC load current of up to 1A and can operate with a supply voltage as low as 4V. To support the use of smaller inductors, LMR70410 operates at a fixed 1.1MHz switching frequency.

LMR70410 implements enable UVLO, which gives the option to program the input voltage at which the device is turned on or off using a resistor divider between VIN and GND. Thermal shutdown functionality is included to turn off the LMR70410 when the junction temperature exceeds the reported thermal shutdown threshold. LMR70410 implements cycle-by-cycle overcurrent protection, which limits the maximum output current even as the output voltage falls to zero.

LMR70410 has both FPWM and PFM options, which allow for designs which call for either fixed frequency across load or higher light load efficiency. The internal soft-start time is set internally to be 1.8ms (typical).

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Fixed Frequency Peak Current Mode Control

The following operation description of the LMR70410 refers to the *Functional Block Diagram* and to the waveforms in Figure 7-1. LMR70410 is a step-down, synchronous buck regulator with integrated high-side (HS) and low-side (LS) switches (synchronous rectifier). The LMR70410 supplies a regulated output voltage by turning on the HS and LS NMOS switches with controlled duty cycle. During high-side switch ON time, the SW pin voltage swings up to approximately VIN, and the inductor current i_L increase with linear slope ($V_{IN} – V_{OUT}$) / L. When the HS switch is turned off by the control logic, the LS switch is turned on after an anti-shoot-through dead time. Inductor current discharges through the low-side switch with a slope of $–V_{OUT}$ / L. The control parameter of a buck converter is defined as Duty Cycle D = t_{ON} / T_{SW}, where t_{ON} is the high-side switch ON time and T_{SW} is the switching period. The regulator control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: D = V_{OUT} / V_{IN}.

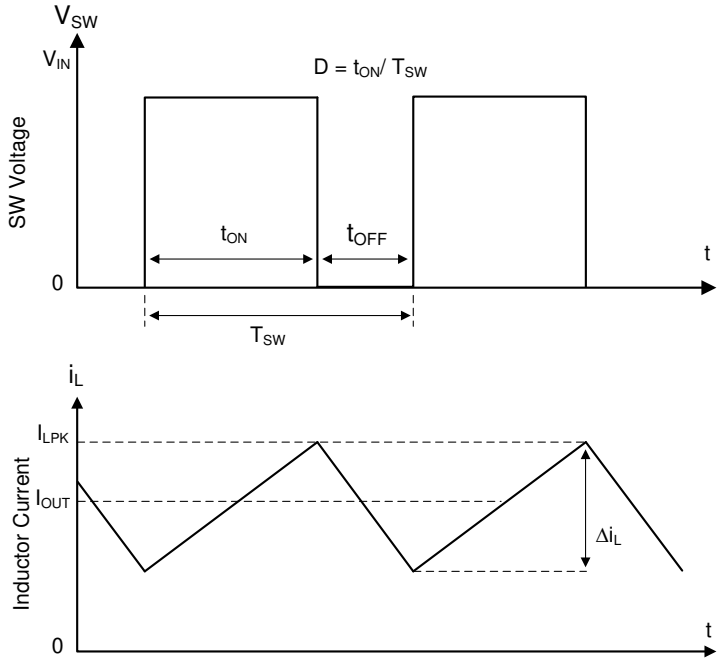

Figure 7-1. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The LMR70410 employs fixed-frequency peak-current mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak-current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current threshold to control the ON time of the high-side switch. The voltage feedback loop is internally compensated, which allows for fewer external components, making design easy and providing stable operation with almost any combination of output capacitors. The regulator operates with fixed switching frequency at normal load condition. At light-load condition, the LMR70410 operates in PFM mode to maintain high efficiency (PFM version) or in FPWM mode for low output voltage ripple, tight output voltage regulation, and constant switching frequency (FPWM version).

7.3.2 Enable and Undervoltage Lockout

LMR70410 features a precision enable and undervoltage lockout (UVLO) feature which enables the user to select the voltage level at which the device powers on and off based on the voltage present at the EN pin. To power on the device, the voltage between EN pin and GND pin must exceed the enable voltage rising threshold ($V_{EN(R)}$). After $V_{EN(R)}$ is crossed and the minimum supply voltage ($V_{IN_UVLO(R)}$) have both been satisfied, the part begins the soft-start sequence described in Section 7.3.3.

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The EN pin can be used to power down the device by reducing the voltage between EN pin and GND pin below the enable input falling threshold ($V_{EN(F)}$).

A resistor divider between VIN and GND with the center point connected to the EN pin can be used to implement the UVLO. To begin, select the input voltage at which the device must turn off, select the value of R_{ENT}, then calculate the required R_{ENB}. After R_{ENB} has been calculated, the resulting turn-on input voltage can be calculated. See Figure 7-2, Equation 1, and Equation 2 to determine the EN resistors required. If the VIN UVLO feature is not needed, the EN pin can be connected to VIN. The EN voltage must not exceed the input voltage.

$$R_{ENB} = \frac{V_{EN-TH(F)}}{\left(VIN_{turn-off} - V_{EN-TH(F)}\right)} \times R_{ENT} \quad (1)$$

$$VIN_{turn-on} = \left(1 + \frac{R_{ENT}}{R_{ENB}}\right) \times V_{EN-TH(R)} \quad (2)$$

Where:

- $VIN_{turn-off}$ represents the input voltage at which the LMR70410 turns off.
- $VIN_{turn-on}$ represents the input voltage at which the LMR70410 turns on.

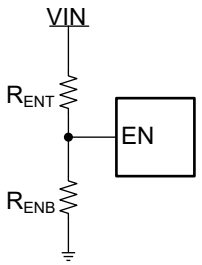

Figure 7-2. VIN UVLO Using the EN Pin

7.3.3 Soft Start and Recovery From Dropout

The LMR70410 uses soft start to prevent output voltage overshoots and large inrush currents during start-up. The soft-start time is fixed internally at 1.8ms (typical). The LMR70410 device operates correctly even if there is a voltage present on the output before activation.

To start up the LMR70410 and initiate the soft-start sequence, the voltage applied to the VIN and EN pins must exceed $VIN_{UVLO(R)}$ and $V_{EN(R)}$ respectively. After these conditions are met, the soft-start sequence initiates and the output voltage reaches the set-point in 1.8ms (typical).

Dropout occurs when the input voltage falls below the voltage level of the output voltage setpoint. After the input voltage increases, the output voltage increases with the same slope as during soft start.

7.3.4 Adjustable Output Voltage

A precision 0.8V reference voltage (V_{FB}) is used to maintain a tightly regulated output voltage over the entire operating temperature range. The output voltage is set by a resistor divider from the output voltage rail to the FB pin. TI recommends to use 1% tolerance resistors with a low temperature coefficient for the FB divider. Select the bottom-side resistor R_{FBB} for the desired divider current and use Equation 3 to calculate the top-side resistor R_{FBT}.

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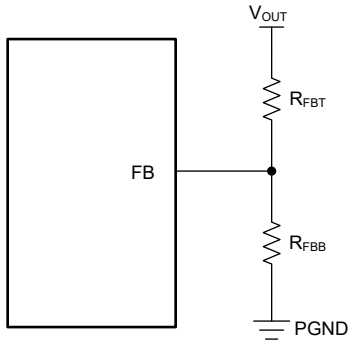

Figure 7-3. Feedback Resistor Setup for Adjustable VOUT

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (3)$$

7.3.5 Minimum ON-Time, Minimum OFF-Time and Frequency Foldback

Minimum ON-time ($t_{ON(min)}$) is the smallest duration of time that the high-side switch can be on. the minimum ON-time is typically 60ns in the LMR70410. Minimum OFF-time ($t_{OFF(min)}$) is the smallest duration that the high side switch can be off. The minimum OFF-time is typically 100ns in the LMR70410. In CCM operation, $t_{ON(min)}$ and $t_{OFF(min)}$ limit the voltage conversion range without switching frequency foldback.

The minimum duty cycle without frequency foldback allowed is:

$$D_{MIN} = T_{ON(\min)} \times f_{sw} \quad (4)$$

The maximum duty cycle without frequency foldback is:

$$D_{MAX} = 1 - T_{OFF(\min)} \times f_{sw} \quad (5)$$

Given a required output voltage, use the following equation to calculate the maximum V_{IN} without frequency foldback:

$$V_{IN_MAX} = \frac{V_{OUT}}{f_{sw} \times T_{ON(\min)}} \quad (6)$$

Use the following equation to calculate the minimum V_{IN} without frequency foldback:

$$V_{IN_MIN} = \frac{V_{OUT}}{1 - f_{sw} \times T_{OFF(\min)}} \quad (7)$$

In the LMR70410, a frequency foldback scheme is employed after the $t_{ON(min)}$ or $t_{OFF(min)}$ is triggered, which extends the maximum duty cycle or lowers the minimum duty cycle.

The on-time decreases while V_{IN} voltage increases. After the on-time decreases to $t_{ON(min)}$, the switching frequency starts to decrease while V_{IN} continues to go up, which lowers the duty cycle further to keep V_{OUT} in regulation according to Equation 4.

The frequency foldback scheme also works once larger duty cycle is needed under low V_{IN} conditions. The frequency decreases once the device hits $t_{OFF(min)}$, which extends the maximum duty cycle according to Equation 5. In such conditions, the frequency can be as low as about 100kHz (typical).

7.3.6 Bootstrap Voltage

A small capacitor between the CB and SW pins provides the gate drive voltage for the integrated high-side MOSFET. The bootstrap capacitor is refreshed when the high-side MOSFET is off and the low-side MOSFET conducts. The recommended value of the bootstrap capacitor is 0.1µF. TI recommends a ceramic capacitor with

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an X7R or X5R grade dielectric with a voltage rating of 16V or higher for stable performance overtemperature and voltage.

7.3.7 Overcurrent and Short-Circuit Protection

The LMR70410 series of devices implements a cycle-by-cycle current limit on both the high side FET and low side FET.

The high side peak current limit of the LMR70410 series of devices protects the high side FET from excessive currents by turning off the high side FET if the inductor current hits $I_{HS-PEAK}$. After this condition is triggered, the low side FET is turned on until the inductor current discharges below $I_{LS-VALLEY}$. After $I_{LS-VALLEY}$ has been crossed, the high side MOSFET is allowed to turn on again. This action effectively limits the maximum amount of DC output current to the average between the $I_{HS-PEAK}$ and $I_{LS-VALLEY}$ unless the duty factor is very high. The device operates in this mode of operation until the load is reduced, or until the junction temperature reaches the thermal shutdown limit. See also Section 7.3.8.

If the load demands more current than can be supported by the cycle-by-cycle current limit of the device, the output voltage drops in response. Even if the output voltage drops to 0V, the device continues to supply current.

Slope compensation is used to mitigate the risk of subharmonic oscillation at high duty cycle. As duty cycle increases, the effective peak current limit is reduced which can reduce the maximum amount of DC current at high duty cycles to be closer to the $I_{LS-VALLEY}$.

The low side negative current limit (I_{LS-NEG}) is used to limit the maximum amount of negative current that can flow through the low side FET. This limit is typically only seen when the device is used in Fly-Buck™ applications where the secondary side load current is reflected through the primary winding as a negative current. If the I_{LS-NEG} limit is reached during a given switching cycle, the absolute value of this negative limit reduces during the next cycle. Typically the initial low side negative current limit value is –600mA.

7.3.8 Thermal Shutdown

The LMR70410 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 165ºC (typical). Both high-side and low-side FETs stop switching in thermal shutdown. After the die temperature falls below 155ºC (typical), the device reinitiates the power-up sequence controlled by the soft-start circuitry.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control for the LMR70410. When V_{EN} is below $V_{EN(F)}$ (1V typical), the device is in shutdown mode. The LMR70410 also employs V_{IN} undervoltage lockout protection (UVLO). If V_{IN} is below $V_{IN_UVLO(F)}$ (3.1V maximum), the converter is turned off.

7.4.2 Active Mode

The LMR70410 is in active mode when both V_{EN} and VIN are above the respective operating threshold. The simplest way to enable the LMR70410 is to connect the EN pin to VIN pin. This action allows self-start-up when the input voltage is in the operating range 4V to 40V.

In active mode, depending on the load current, the LMR70410 is in one of four modes:

- Continuous conduction mode (CCM) with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple (for both PFM and FPWM versions)
- Discontinuous conduction mode (DCM) with fixed switching frequency when load current is lower than half of the peak-to-peak inductor current ripple in CCM operation (only for PFM version)
- Pulse frequency modulation mode (PFM) when switching frequency is decreased at very light load (only for PFM version)
- Forced pulse width modulation mode (FPWM) with fixed switching frequency even at light load (only for FPWM version)

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7.4.3 CCM Mode

Continuous Conduction mode (CCM) operation is employed in the LMR70410 when the load current is higher than half of the peak-to-peak inductor current. In CCM operation, the frequency of operation is fixed, output voltage ripple is at a minimum in this mode and the maximum output current can be supplied by the LMR70410.

7.4.4 Light-Load Operation (PFM Version)

For PFM versions of the LMR70410, when the load current is lower than half of the peak-to-peak inductor current in CCM, the LMR70410 operates in discontinuous conduction mode (DCM), also known as diode emulation mode (DEM). In DCM operation, the low-side switch is turned off when the inductor current drops to the zero cross detection threshold to improve efficiency. Both switching losses and conduction losses are reduced in DCM, compared to forced PWM operation at light load.

At even lighter current load, pulse frequency modulation (PFM) mode is activated to maintain high efficiency operation. When either the minimum high-side switch ON time $t_{ON(min)}$ or the minimum peak inductor current $IL_{PEAK(MIN)}$ (625mA typical) is reached, the switching frequency decreases to maintain regulation. In PFM mode, switching frequency is decreased by the control loop to maintain output voltage regulation when load current reduces. Switching loss is further reduced in PFM operation due to less frequent switching actions.

7.4.5 Light-Load Operation (FPWM Version)

For FPWM versions of LMR70410, the device is locked in PWM mode switching across the entire load range. Light load efficiency is traded off for constant switching frequency across load currents. This operation is maintained, even when there is no load present at the output, by allowing the inductor current to reverse the normal direction. The reverse current through the inductor is limited by reverse current limit circuitry. See Section 7.3.7 for more information.

Under operating conditions where the minimum on-time or minimum off-time can be exceeded, the frequency reduces even while operating in FPWM to maintain minimum timing specifications. Additionally, during soft start, the device switches in PFM mode and does not allow negative inductor current until the soft-start sequence completes.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMR70410 is a step-down DC-to-DC converter. The LMR70410 is typically used to convert a higher input voltage to a lower output DC voltage with a maximum output current of 1A. The following design procedure can be used to select components for the LMR70410.

8.2 Typical Application

The LMR70410 only requires a few external components to convert from a wide voltage range supply to a fixed output voltage. The following figure shows a basic schematic.

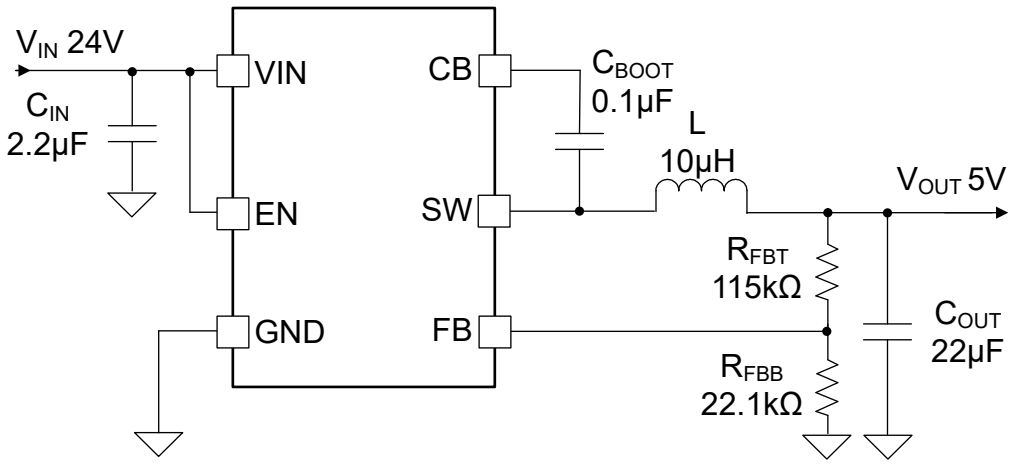

Figure 8-1. Application Circuit

The external components have to fulfill the needs of the application and the stability criteria of the control loop of the device. Use Table 8-1 to simplify the output filter component selection.

Table 8-1. L and C_{OUT} Typical Values

f_{SW}	V_{OUT} (V)	I_{OUT} (A)	L (µH)	C_{OUT}	R_{FBT} (kΩ)	R_{FBB} (kΩ)
1100kHz	3.3	1	10	22µF × 2 / 10V	69.8	22.1
	5	1	10	22µF × 1 / 10V	115	22.1
	12	1	33	10µF × 1 / 25V	309	22.1

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8.2.1 Design Requirements

The detailed design procedure is described based on a design example. For this design example, use the parameters listed in Table 8-2 as the input parameters.

Table 8-2. Design Example Parameters

PARAMETER	VALUE
Input voltage, V_{IN}	12V typical, range from 6V to 40V
Output voltage, V_{OUT}	5V ±3%
Maximum output current, I_{OUT_MAX}	1A
Output overshoot, undershoot (0.5A to 1A)	±5%
Output voltage ripple	0.5%
Operating frequency	1100kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Setpoint

The output voltage of the LMR70410 device is externally adjustable using a resistor divider network. The divider network is comprised of a top feedback resistor R_{FBT} and bottom feedback resistor R_{FBB}. Equation 8 calculates the output voltage of the converter:

$$R_{FBT} = \frac{(V_{OUT} - V_{REF})}{V_{REF}} \times R_{FBB} \tag{8}$$

Select the value of R_{FBB} to be 22.1kΩ. With the desired output voltage set to 5V and the VREF = 0.8V, use Equation 8 to calculate the R_{FBT} value. The formula yields to a value 116.025kΩ, a standard value of 115kΩ is selected.

8.2.2.2 Switching Frequency

The higher switching frequency allows for lower value inductors and smaller output capacitors, which results in smaller design size and lower component cost. However, higher switching frequency brings more switching loss, making the design less efficient and produce more heat. The switching frequency is also limited by the minimum on time of the integrated power switch, the input voltage, the output voltage, and the frequency shift limitation as mentioned in *Minimum ON Time, Minimum OFF Time, and Frequency Foldback*. For this example, a switching frequency of 2100kHz is selected.

8.2.2.3 Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current, and the RMS current. The inductance is based on the desired peak-to-peak ripple current Δi_L. Because the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L_{MIN}. Use Equation 10 to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current of the device. A reasonable value of K_{IND} must be 20% to 60% of maximum I_{OUT} supported by converter. During an instantaneous overcurrent operation event, the RMS and peak inductor current can be high. The inductor saturation current must be higher than peak current limit level.

$$\Delta i_L = \frac{V_{OUT} \times (V_{IN_MAX} - V_{OUT})}{V_{IN_MAX} \times L \times f_{SW}} \tag{9}$$

$$L_{MIN} = \frac{V_{IN_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN_MAX} \times f_{SW}} \tag{10}$$

In general, selecting lower inductance in switching power supplies is preferable because lower inductance typically corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. Too low of an inductance can generate too large of an inductor current ripple such that overcurrent protection at

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the full load can be falsely triggered. Too low of an inductance also generates more inductor core loss because the current ripple is larger. Larger inductor current ripple also implies larger output voltage ripple with the same output capacitors. With peak current mode control, TI recommends to have adequate amount of inductor ripple current. A larger inductor ripple current improves the comparator signal-to-noise ratio.

For this design example, select K_{IND} = 0.4, I_{OUT} = 1A. The minimum inductor value is calculated to be 9.9µH. Select the nearest standard 10µH ferrite inductor with a capability of 1.5A RMS current and 2.5A saturation current.

8.2.2.4 Output Capacitor Selection

The device is designed to be used with a wide variety of LC filters. Minimizing the output capacitance to keep cost and size down is generally desired. The output capacitor or capacitors, C_{OUT}, must be chosen with care because the output capacitor directly affects the steady state output voltage ripple, loop stability, and output voltage overshoot and undershoot during load current transient. The output voltage ripple is essentially composed of two parts. One part is caused by the inductor ripple current flowing through the equivalent series resistance (ESR) of the output capacitors:

$$\Delta V_{OUT_ESR} = \Delta i_L \times ESR = K_{IND} \times I_{OUT} \times ESR \quad (11)$$

The other part is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT_C} = \frac{\Delta i_L}{8 \times f_{SW} \times C_{OUT}} = \frac{K_{IND} \times I_{OUT}}{8 \times f_{SW} \times C_{OUT}} \quad (12)$$

The two components of the voltage ripple are not in-phase, therefore, the actual peak-to-peak ripple is less than the sum of the two peaks. Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation with presence of large current steps and fast slew rates. When a large load step occurs, output capacitors provide the required charge before the inductor current can slew to an appropriate level. The control loop of the converter usually requires eight or more clock cycles to regulate the inductor current equal to the new load level during this time. The output capacitance must be large enough to supply the current difference for eight clock cycles to maintain the output voltage within the specified range. Equation 13 shows the minimum output capacitance needed for a specified V_{OUT} overshoot and undershoot.

$$C_{OUT} > \frac{1}{2} \times \frac{8 \times (I_{OH} - I_{OL})}{f_{SW} \times \Delta V_{OUT_SHOOT}} \quad (13)$$

where

- K_{IND} = Ripple ratio of the inductor current (Δi_L / I_{OUT})
- I_{OL} = Low level output current during load transient
- I_{OH} = High level output current during load transient
- V_{OUT_SHOOT} = Target output voltage overshoot or undershoot

For this design example, the target output ripple is 30mV. Assuming ΔV_{OUT_ESR} = ΔV_{OUT_C} = 30mV, select K_{IND} = 0.4. Equation 11 yields ESR no larger than 75mΩ and Equation 12 yields C_{OUT} no smaller than 1.5µF. For the target overshoot and undershoot limitation of this design, ΔV_{OUT_SHOOT} = 5% × V_{OUT} = 250mV. Calculate the C_{OUT} to be no less than 7.3µF using Equation 13. In summary, the most stringent criteria for the output capacitor is 7.3µF. Considering derating, one 22µF, 10V, X7R ceramic capacitor with 10mΩ ESR is used.

8.2.2.5 Input Capacitor Selection

The LMR70410 device requires a high frequency input decoupling capacitor or capacitor. The typical recommended value for the high frequency decoupling capacitor is 2.2µF or higher. TI recommends a high-quality ceramic type X5R or X7R with sufficiency voltage rating. The voltage rating must be greater than the maximum input voltage. To compensate the derating of ceramic capacitors, TI recommends a voltage rating of twice the maximum input voltage. For this design, one 2.2µF, X7R dielectric capacitor rated for 50V is used for the input decoupling capacitor. The equivalent series resistance (ESR) is approximately 10mΩ, and the current

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rating is 1A. Include a capacitor with a value of 0.1µF for high-frequency filtering and place as close as possible to the device pins.

8.2.2.6 Bootstrap Capacitor

Every LMR70410 design requires a bootstrap capacitor, C_{BOOT}. The recommended bootstrap capacitor is 0.1µF and rated at 16V or higher. The bootstrap capacitor is located between the SW pin and the CB pin. The bootstrap capacitor must be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

8.2.2.7 Undervoltage Lockout Setpoint

The system undervoltage lockout (UVLO) is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. Use Equation 14 to determine the V_{IN} UVLO level.

$$V_{IN_RISING} = V_{EN(R)} \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \quad (14)$$

The EN rising threshold ($V_{EN(R)}$) for LMR70410 is set to be 1.2V (typical). Select a value of 200kΩ for R_{ENB} to minimize input current from the supply. If the desired V_{IN} UVLO level is at 6.0V, then use Equation 15 to calculate the value of R_{ENT}:

$$R_{ENT} = \left(\frac{V_{IN_RISING}}{V_{EN(R)}} - 1\right) \times R_{ENB} \quad (15)$$

The above equation yields a value of 800kΩ, a standard value of 796kΩ is selected. Use Equation 16 to calculate the resulting falling UVLO threshold, equal to 5V.

$$V_{IN_FALLING} = V_{EN(F)} \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \quad (16)$$

8.2.2.8 Replacing Asynchronous Converter

The LMR70410 can also be used to replace asynchronous converters such as LMR14006 or LM14010A, which need a rectifying diode in the application circuit. The design works fine with or without a rectifying diode connected to the switch node of the LMR70410 as shown in Figure 8-2

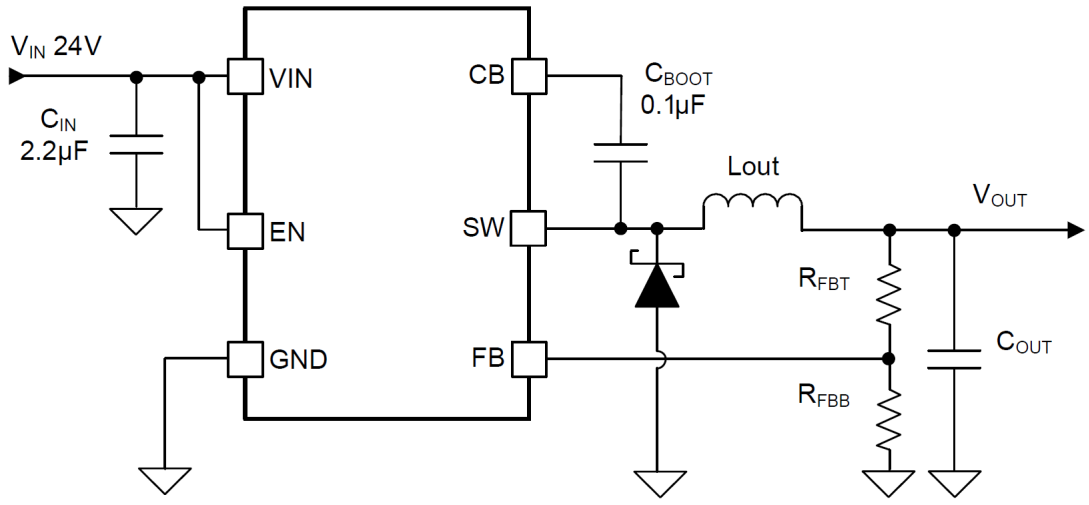

Figure 8-2. Replacing Non-Sync Buck Converter

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8.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 1.1MHz, L = 8.2µH, COUT = 66µF, TA = 25°C.

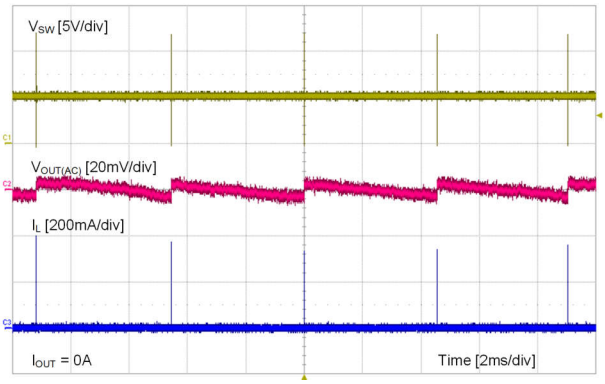

Figure 8-3. Ripple at No Load

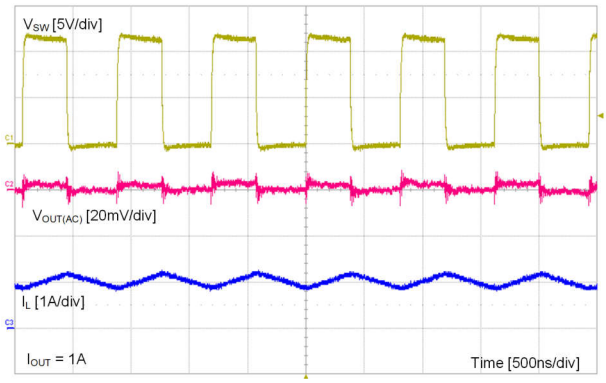

Figure 8-4. Ripple at Full Load

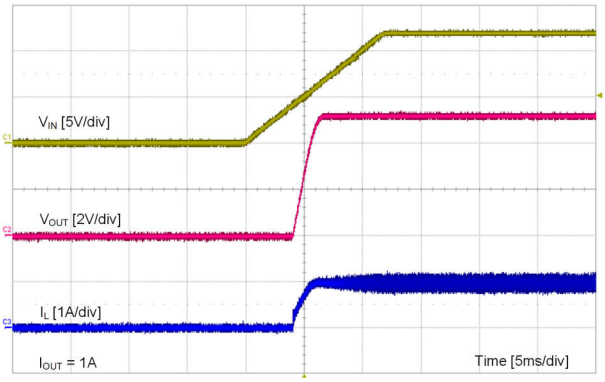

Figure 8-5. Start-Up by V_{IN}

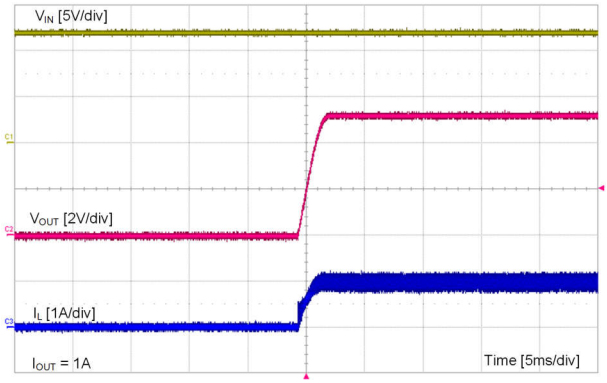

Figure 8-6. Start-Up by EN

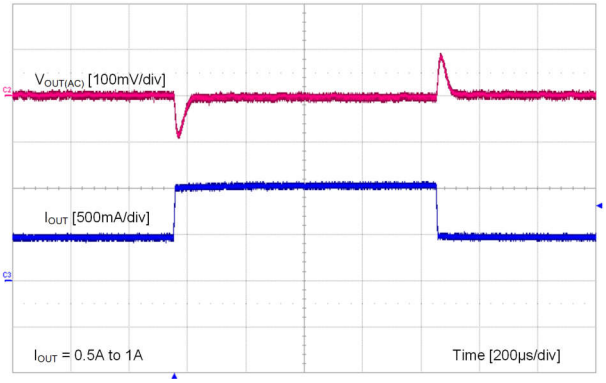

Figure 8-7. Load Transient

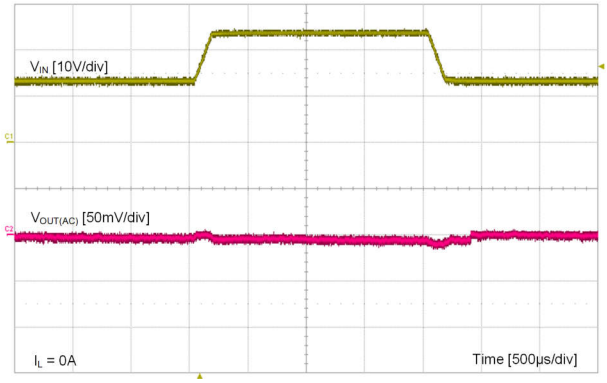

Figure 8-8. Line Transient

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8.3 Power Supply Recommendations

The LMR70410 is designed to operate from an input voltage supply range between 4V and 40V. This input supply must be well-regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LMR70410 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LMR70410, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 10µF or 22µF electrolytic capacitor is a typical choice.

8.4 Layout

8.4.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

- Place the input bypass capacitor CIN as close as possible to the VIN and GND pins. Grounding for both the input and output capacitors must consist of localized top side planes that connect to the GND pin.
- Minimize trace length to the FB pin net. Both feedback resistors, R_{FBT} and R_{FBB}, must be located close to the FB pin. If VOUT accuracy at the load is important, make sure V_{OUT} sense is made at the load. Route VOUT sense path away from noisy nodes and preferably through a layer on the other side of a shielded layer.
- Use ground plane in one of the middle layers as noise shielding and heat dissipation path if possible.
- Make V_{IN}, V_{OUT}, and ground bus connections as wide as possible. This action reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
- Provide adequate device heat-sinking. GND, VIN, and SW pins provide the main heat dissipation path and make the GND, VIN, and SW plane area as large as possible. Use an array of heat-sinking vias to connect the top side ground plane to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. Make sure enough copper area is used for heat-sinking to keep the junction temperature below 150°C.

8.4.1.1 Compact Layout for EMI Reduction

Radiated EMI is generated by the high di/dt components in pulsing currents in switching converters. The larger area covered by the path of a pulsing current, the more EMI is generated. High frequency ceramic bypass capacitors at the input side provide primary path for the high di/dt components of the pulsing current. Placing a ceramic bypass capacitor or capacitors as close as possible to the VIN and GND pins is the key to EMI reduction.

The SW pin connecting to the inductor must be as short as possible, and just wide enough to carry the load current without excessive heating. Short, thick traces or copper pours (shapes) must be used for high current conduction path to minimize parasitic resistance. Place the output capacitors close to the VOUT end of the inductor and closely grounded to GND pin.

8.4.1.2 Feedback Resistors

To reduce noise sensitivity of the output voltage feedback path, place the resistor divider close to the FB pin, rather than close to the load. The FB pin is the input to the error amplifier, so the pin is a high impedance node and very sensitive to noise. Placing the resistor divider closer to the FB pin reduces the trace length of FB signal and reduces noise coupling. The output node is a low impedance node, so the trace from VOUT to the resistor divider can be long if short path is not available.

If voltage accuracy at the load is important, make sure voltage sense is made at the load. Doing so corrects for voltage drops along the traces and provides the best output accuracy. The voltage sense trace from the load to the feedback resistor divider must be routed away from the SW node path and the inductor to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This action is most important when high value resistors are used to set the output voltage. TI recommends to route the voltage sense trace and place the resistor divider on a different layer than the inductor and SW node path, such that there is a ground plane in between the feedback trace and inductor/SW node polygon. This action provides further shielding for the voltage feedback path from EMI noises.

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8.4.2 Layout Example

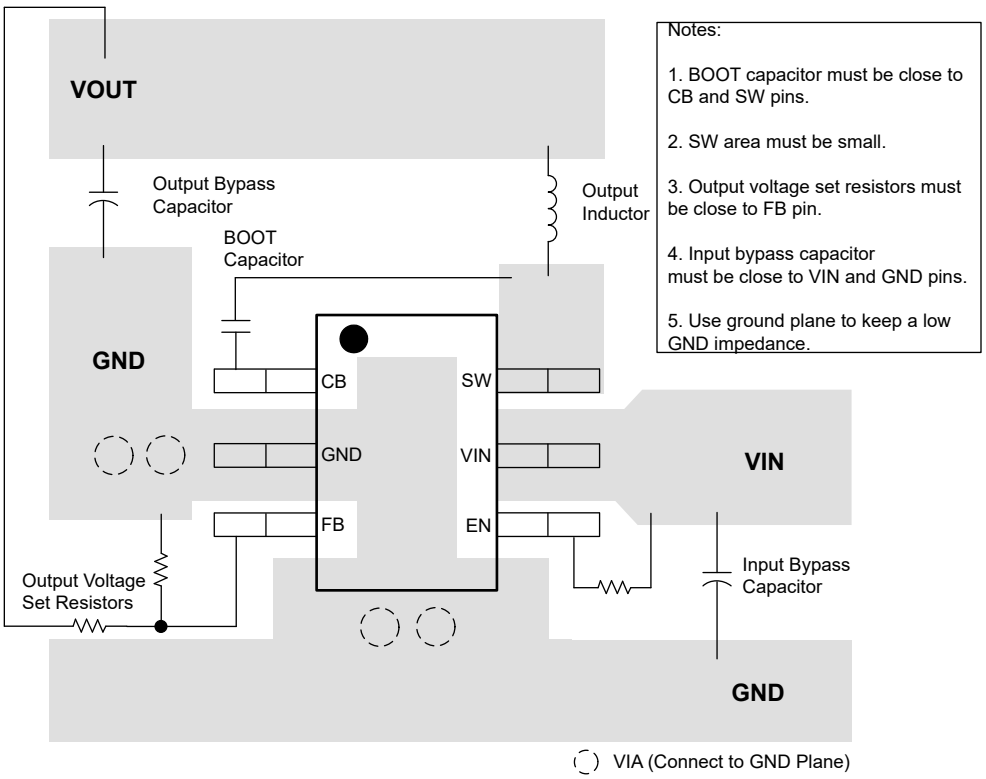

Figure 8-9. Layout

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
October 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, see also the left-hand navigation.

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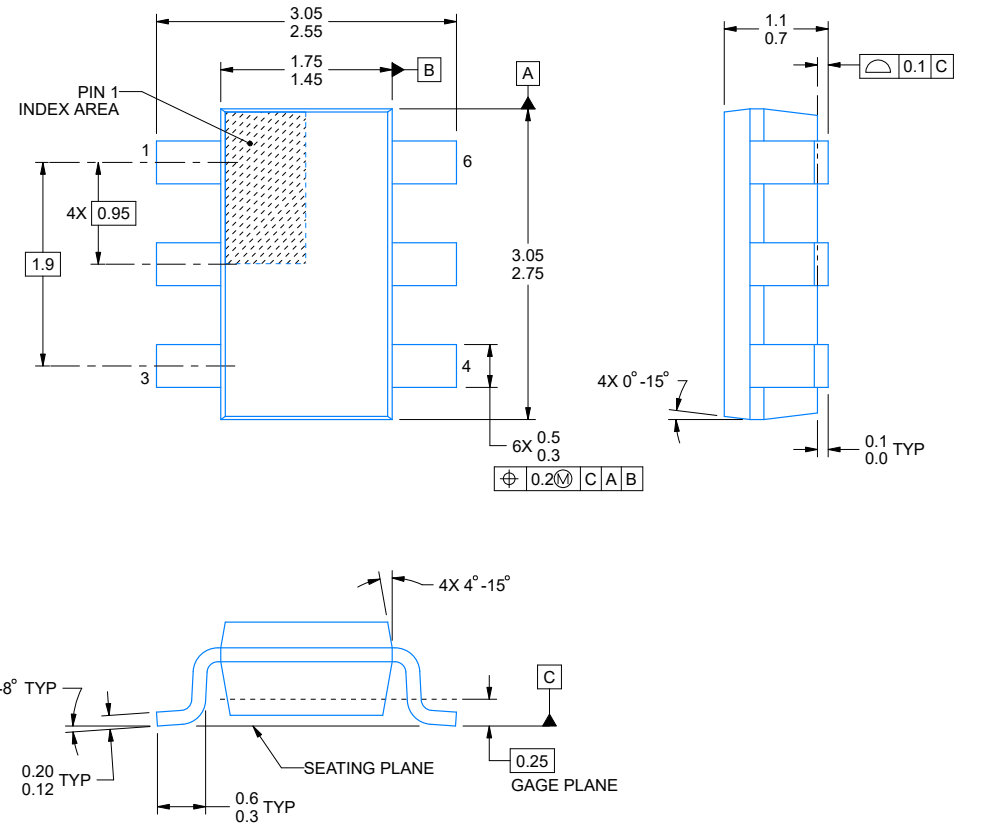
11.1 Mechanical Data

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.

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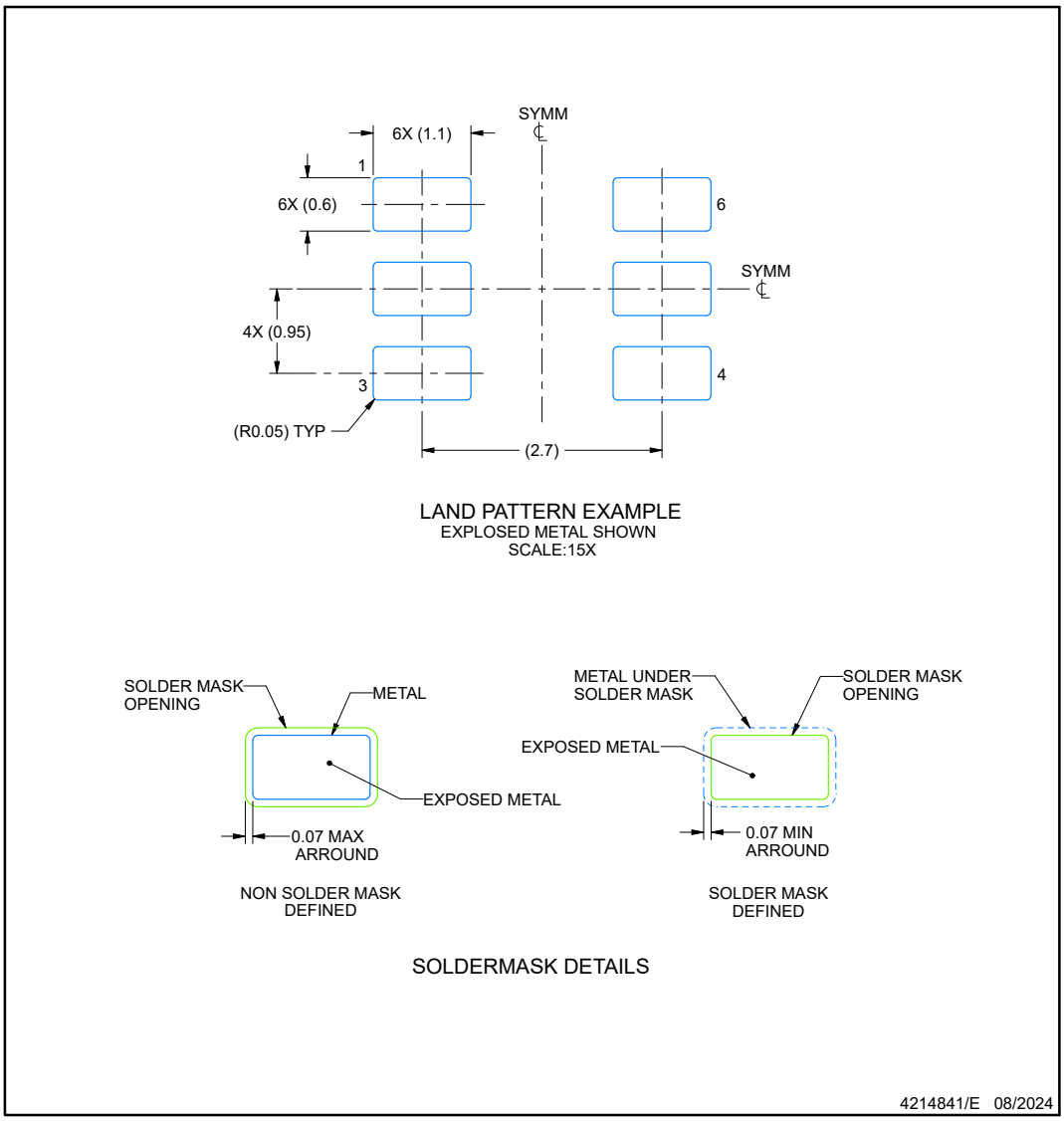
EXAMPLE BOARD LAYOUT

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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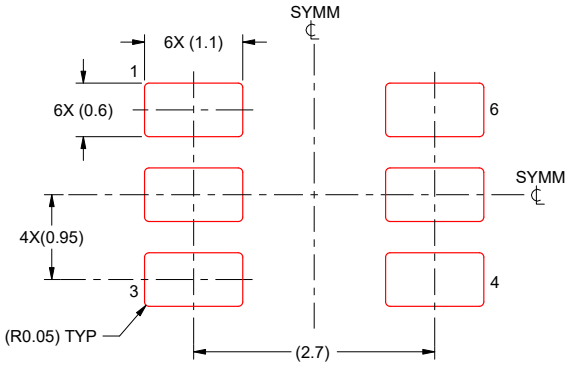
EXAMPLE STENCIL DESIGN

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PLMR70410YAFDDCR	Active	Preproduction	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 150	
PLMR70410YAPDDCR	Active	Preproduction	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 150	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMR70410 :

- Automotive : LMR70410-Q1

NOTE: Qualified Version Definitions:

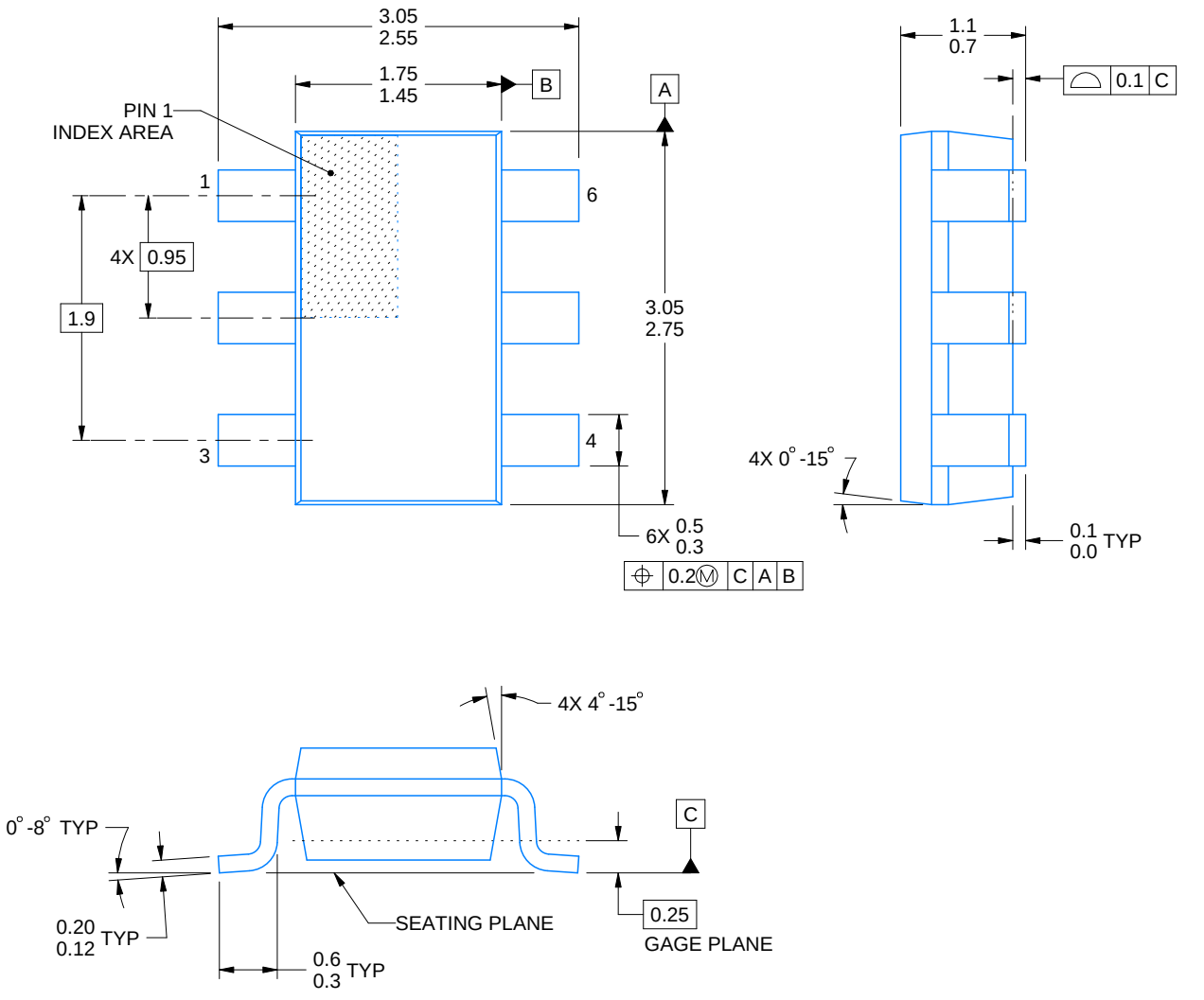
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



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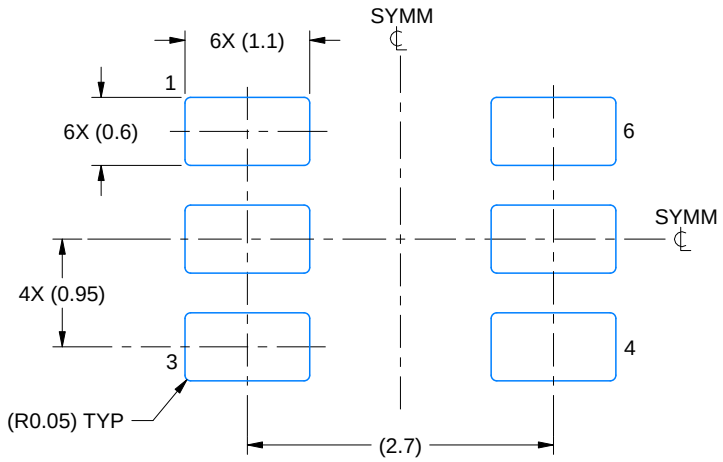
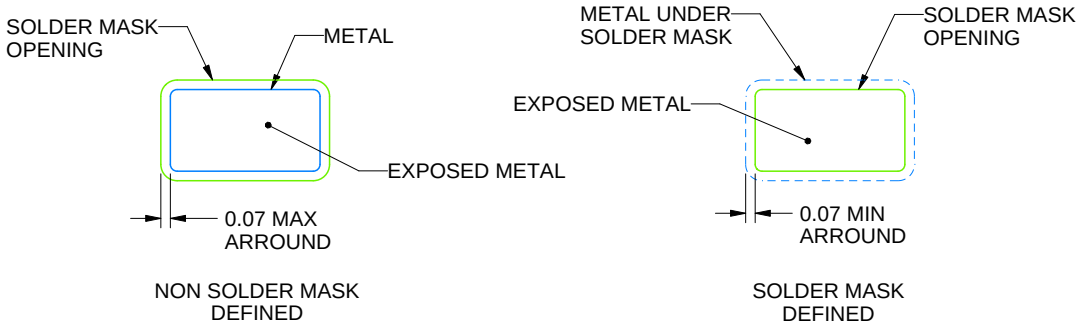
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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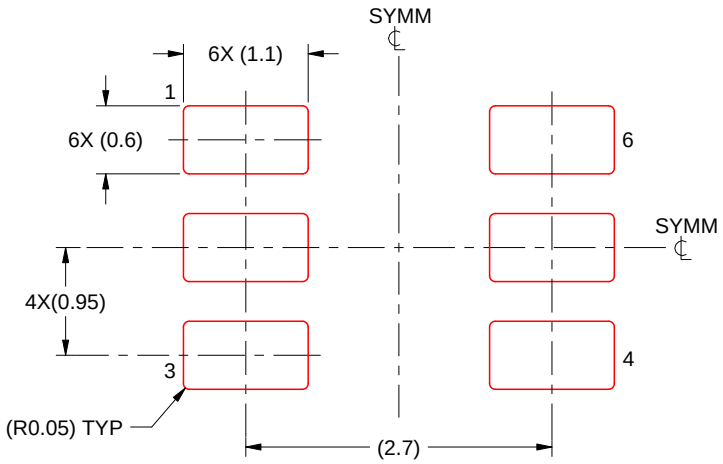
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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