LMS1225 22.5V, 270μΩ, MOSFET With Integrated Driver and Dead Time Compensation

1 Features

- Integrated synchronous rectifier FET and driver: 0.27mΩ
- Operates from 5V external bias supply
- Dead-time compensation (DTC) works with digital power controllers:
  - Automatic or manual dead-time adjustment of gate turn-on edges
- Ideal diode mode (IDM) for autonomous turn-on edge optimization by sensing 3rd quadrant conduction
- body-diode conduction sensing threshold: –250mV
- Detection times of body diode conduction: as low as 4ns
- High frequency operation: up to 5MHz
- V_{CC} undervoltage lockout (UVLO)
- 3.3V or 5V input logic levels, 3.3V output logic level
- 5mm × 6mm QFN package
  - Top-side exposed die for excellent thermal path top side
  - Large thermal pads for low thermal resistance bottom side
  - Large drain and source pads and corner pins for improved board level reliability (BLR) performance

2 Applications

- Server power: 6V PSU
- Server power: 6/5/4V brick applications
- Center-tapped LLC converters
- Digital power-control applications
- TV power supply

3 Description

The LMS1225 device is an industry-first 22.5V, synchronous-rectification power stage with an integrated gate driver and a MOSFET. The device provides body-diode conduction sensing and reporting and integrates a high performance driver that allows any digital PWM controller to achieve advanced synchronous-rectification (SR) control. The device contains a high-speed gate driver, a body-diode conduction-sensing circuit, an autonomous turn-on and dead time reporting features. The device is designed for high-efficiency center-tapped LLC applications, where SR dead-time optimization is desired.

The LMS1225 device offers efficient operation at high frequencies up to 5MHz. The gate drive control turns on through PWM signal in standard operation or autonomously turns on in IDM operation. In IDM operation an internal high-speed comparator with a –250mV threshold detects the body-diode conduction and autonomously switches on the MOSFET at the turn-on edge if the PWM signal is already high. The device is capable of sensing body-diode conduction time as low as 4ns. In both operation modes, turn-off control relies on PWM falling edge.

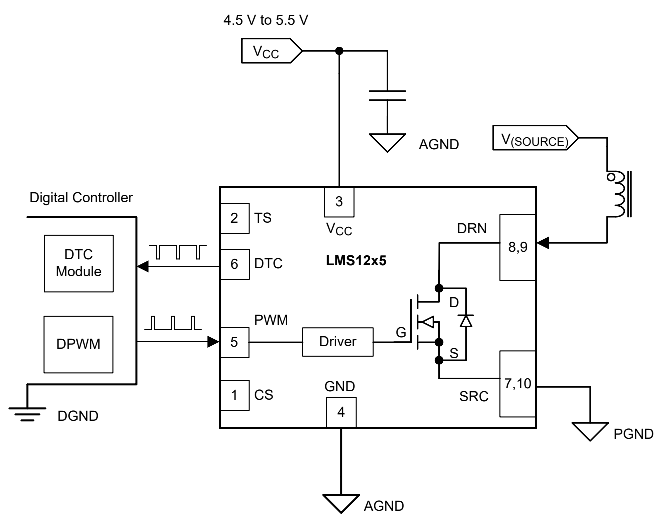
The LMS1225 internal high-speed comparator with a –250mV threshold detects the body-diode conduction and reports the information to the digital-power controller through the DTC pin. The device senses body-diode conduction time as low as 4ns. The SR turn-on and turn-off edge is optimized by the digital-power controller which analyzes the body-diode conduction information reported by the LMS1225 DTC pin.

The benefits of the chipset include maximizing system efficiency by minimizing body-diode conduction time, robust and fast bi-directional current sensing. The integrated approach promotes high power density with a layout which is optimized by as much as 30% in comparison to discrete solutions.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMS1225	VEU (QFN, 10)	5mm × 6mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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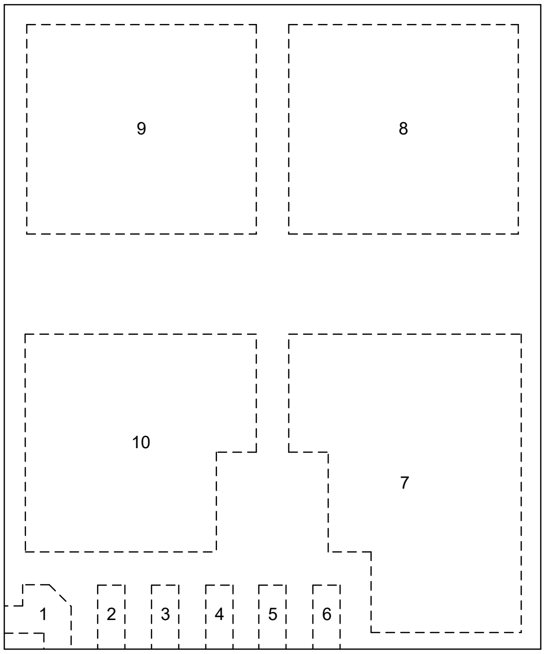
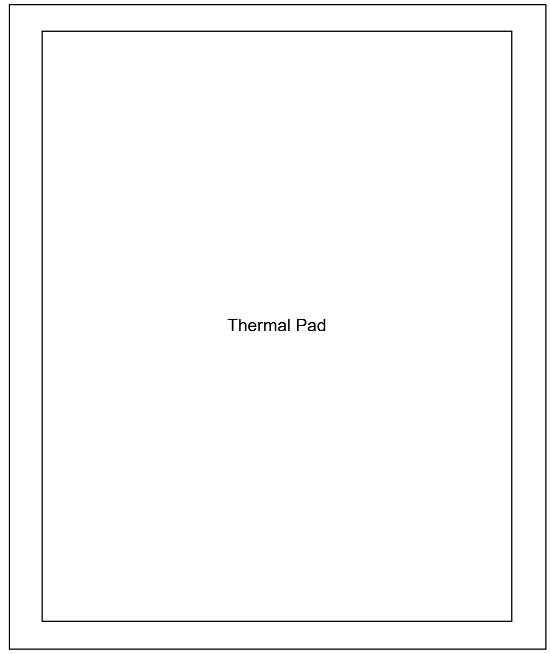
4 Pin Configuration and Functions



Transparent Top View
(Shows Pin Locations)



Top View
(Shows Exposed Si
for heatsink connection)

Figure 4-1. VEU Package, 10-Pin QFN With Exposed Thermal Pad (Top View)

Table 4-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
CS	1	O	Current sense emulation output: Outputs scaled current of the MOSFET current. Feed output current into a resistor to create a current sense voltage signal. Reference the resistor to a voltage source (V_{CS}) for negative current sense. This function replaces the external current sense resistor that is used in series with the FET source. If not used, short CS pin to GND
TS	2	O	Temperature sense: Outputs an analog voltage signal that correlates to the internal temperature measured on the FET die. If not used, leave TS pin floating.
V_{cc}	3	P	IC supply: External bias supply input. The supply range is 4.5V to 5.5V
GND	4	G	Analog ground; internally shorted to source
PWM	5	I	Input: Gate driver input. This pin is PWM signal input to control the integrated gate driver.
DTC	6	IO	Dead time compensation (DTC): Standard digital IO. Output is set low when the body diode is conducting. Connect this pin to the Input pin of the Digital PWM controller. If not used, leave DTC pin floating. Ideal diode mode (IDM): Connect this pin to ground using a pull-down resistor of 22kΩ to enable autonomous rising edge optimization when not using the DTC mode. Leave this pin floating to disable autonomous rising edge optimization.
SRC	7, 10	P	Source of MOSFET
DRN	8, 9	P	Drain of MOSFET
—	Thermal Pad	—	Exposed thermal pad: The exposed pad on the top of the package enhances the thermal performance of the device. This pad is electrically connected to source.

(1) I = input, O = output, I/O = bidirectional, P = power, G = ground

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5 Specifications

5.1 Absolute Maximum Ratings

Unless otherwise noted: voltages are respect to GND(1)

			MIN	MAX	UNIT
V_{DS}	Drain-source (D to S) voltage, FET off			22.5	V
	Pin voltage	VCC	-0.5	5.5	V
		PWM	-0.5	5.5	V
		TS	-0.5	5.5	V
		CS	-0.5	5.5	V
		IDM/DTC	-0.5	5.5	V
$I_{S(cnts)}$	Source (S to D) continuous current, FET on, T_C = 25℃			1000	A
	Source (S to D) continuous current, FET on, T_C = 125℃			450	A
T_J	Operating junction temperature		-40	175	°C
T_{stg}	Storage temperature		-40	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic Discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Supply voltage		4.5	5	5.25	V
	Input voltage	PWM	-0.3		5.25	
I_s	Diode continuous forward current	T_C = 25°C			704	A
f_{MAX}	Maximum switching frequency				5	MHz

5.4 Thermal Information

THERMAL METRIC [(1)]		LMS1225	UNIT
		QFN	
		9 PINS	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.3	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	1.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

Unless otherwise noted: voltage, resistance, and capacitance are respect to GND; –40°C ≤ T_J ≤ 150°C; 4.5V ≤ V_{VCC} ≤ 5.5V; V_{PWM} = 0V; R_{CS} = 100Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER TRANSISTOR						
$R_{DS(on)}$	Drain-source on resistance	I_{DS} = 10A, V_{VCC} = 5V, T_J=25°C		0.27	0.32	mΩ
		I_{DS} = 10A, V_{VCC} = 5V, T_J=150°C		0.41	0.50	
I_{DS}	Drain-source Leakage	V_{DS} = 16V, PWM = 0V, T_J=25°C		0.3	5	uA
I_{DS}	Drain-source Leakage	V_{DS} = 16V, PWM = 0V, T_J=150°C		270		uA
C_{OSS}	Output capacitance	V_{DS} = 16V, V_{GS} = 0V, 1MHz		3.2		nF
$C_{OSS(er)}$	Energy related effective output capacitance	V_{DS} = 0V to 16V, V_{GS} = 0V		4.6		nF
$C_{OSS(tr)}$	Time related effective output capacitance	V_{DS} = 0V to 16V, V_{GS} = 0V		6.3		nF
Q_{G_eq} (soft-switching)	Total gate charge, equivalent	V_{DS} = 0V, V_{GS} = 0V to 5V		45	70	nC
Q_{OSS}	Output charge	V_{DS} = 0V to 16V		101		nC
V_{SD}	Diode forward voltage	I_{SD} = 0.1A, T_J = 25°C		0.57		V
		I_{SD} = 40A, T_J = 25°C		0.73		
t_{RR}	Reverse recovery time	V_{DS} = 16V, I_{SD} = 10A, dI_{SD}/dt = 400A/µs				ns
$V_{DS(clamp)}$	V_{DS} voltage clamping	I_{DS} = 1A		17.5		V
VCC						
$V_{VCC,T+}$ (UVLO)	UVLO – positive-going threshold voltage		3.8	4.1	4.35	V
	UVLO – negative-going threshold voltage		3.7	3.8	4.15	V
	UVLO threshold hysteresis			270		mV
	VCC Quiescent Current	V_{VCC} = 5V		1	1.5	mA
	VCC Quiescent Current	V_{VCC} = V_{PWM} = 5V		1.4	3.2	mA
	VCC Operating Current	f_{PWM} = 1MHz, 50% Duty cycle, V_{DS} = 0V, I_{DS}=0		45	70	mA
PWM						
$V_{PWM,IT+}$	Positive-going input threshold voltage		1.7	1.9	2.1	V
$V_{PWM,IT-}$	Negative-going input threshold voltage		0.97	1.05	1.25	V
	Input threshold voltage hysteresis			0.85		V
R_I	Input pull down resistance		200	250	300	kΩ
CS						

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Unless otherwise noted: voltage, resistance, and capacitance are respect to GND; –40°C ≤ T_J ≤ 150°C; 4.5V ≤ V_{VCC} ≤ 5.5V; V_{PWM} = 0V; R_{CS} = 100Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CS_{gain}	Current Sense Gain			10		µA/A
$CS_{(Acc-PL)}$	Accuracy of current Sense output at 100A load	I_{SD} = 100A;	9.7	10	10.3	µA/A
$CS_{(Acc-HL)}$	Accuracy of current Sense output at 20A load	I_{SD} = 20A;	9.65	10	10.35	µA/A
$CS_{(Acc-LL)}$	Accuracy of current Sense output at 5A load	I_{SD} = 5A;	9	10	11	µA/A
$CS_{(Acc-LL)}$	Accuracy of current Sense output at -10A load	I_{SD} = -10A;	9	10	11	µA/A
$CS_{(ratio)}$	Difference of CS output in two consecutive switching cycles		-90	0	90	uA
$V_{C\ S}$	Maximum voltage output from CS pin	I_{CS} = 2.6mA source current.	2.8	3.1	3.6	V
TS						
$TS_{(slope)}$	Slope of Temperature sense curve	T_J = 25ºC to 175ºC		13.5		mV/℃
$TS_{(Acc)}$	Accuracy of Temp. Sense output		-3	0	3	℃
V_{MT}	Voltage output from the TS at T_J = 175℃	Tj =175℃	2.45	2.5	2.65	V
V_{TS}	Minimum voltage output from TS pin		0.17	0.3	0.35	V
DTC						
$V_{OL(DTC)}$	Low level output voltage	I_{DTC} = -4mA			0.25	V
$V_{OH(DTC)}$	High level output voltage	I_{DTC} = 4mA	2.48			V
V_{DTC}	DTC pin output voltage	I_{DTC} = 0A	2.9	3.2	3.5	V
V_{TH}	Body diode conduction sensing threshold		-320	-250	-190	mV

5.6 Switching Characteristics

Unless otherwise noted: voltage, resistance, and capacitance are respect to GND; –40°C ≤ T_J ≤ 150°C; 4.5V ≤ V_{VCC} ≤ 5.5V; V_{PWM} = 0V; R_{CS} = 100Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER TRANSISTOR						
$t_{d(on)}$	Turn-on propagation delay	I_{DS} = -40A, V_{PWM} > $V_{PWM,IT+}$ to V_{DS} > -0.3V		10	25	ns
$t_{d(off)}$	Turn-off propagation delay	I_{DS} = -40A, V_{PWM} < $V_{PWM,IT-}$ to V_{DS} < -0.3V		25	37	ns
t_{PW}	Minimum LHL input pulse width for FET turn-on	V_{PWM} rise/fall times < 1ns, V_{DS} increase to > -0.3V, I_{DS} = -20A		15	24	ns
VCC						
t_{PWUP}	Power up time	V_{VCC} > $V_{VCC,T+(UVLO)}$ to FET on		35	70	µs
CS						
DTC						
$t_{d(COMP)}$	Body-diode conduction detection-comparator controlled-turnon propagation delay	Turn-on optimization is enabled. From V_{PWM} = 5V, V_{DS} falling below -0.25V to V_{DS} rising above -0.25V, I_{DS} = -30A		20	30	ns
$t_{d(DTC)}$	Rising edge propagation delay	V_{DS} > -0.25V to V_{DTC} > 1.8V		8	13	ns
$t_{d(DTC)}$	Falling edge propagation delay	V_{DS} < -0.25V to V_{DTC} < 1.8V		8	15	ns
$t_{w(VD)}$	Minimum diode conduction time that changes the DTC output state	Duration of VDS below -0.25V	4	7		ns

6 Detailed Description

6.1 Overview

The LMS1225 is a low-side integrated device with a 22.5V FET and a high-performance driver for secondary-side synchronous rectification with body-diode conduction sensing. The device is designed for high-power high-efficiency center-tapped LLC converter applications where dead-time optimization is desired. The body-diode conduction is sensed and a pulse is sent to the a digital-power controller through one digital IO pin. The digital controller can adjust the dead-time setting based on this information. At the turn-on edge, in the IDM mode, the gate driver in the LMS1225 optimizes the dead time by turning the gate on when the diode conduction is detected. The benefits of this driver to the system include, but are not limited to, improved efficiency, improved reliability, and ease of design.

The internal gate driver is a single-channel, high-speed gate driver designed for a 5V drive. The package and pin configuration provide minimum parasitic inductances to reduce rise and fall times and to limit ringing. Additionally, the short propagation delay with minimized tolerances and variations allows efficient operation at high frequencies.

The internal body-diode conduction detector is a high-speed comparator with 4ns propagation delay. The DTC output is internally pulled high by default. When sensing a body-diode conduction, the DTC pin drives low.

6.2 Functional Block Diagram

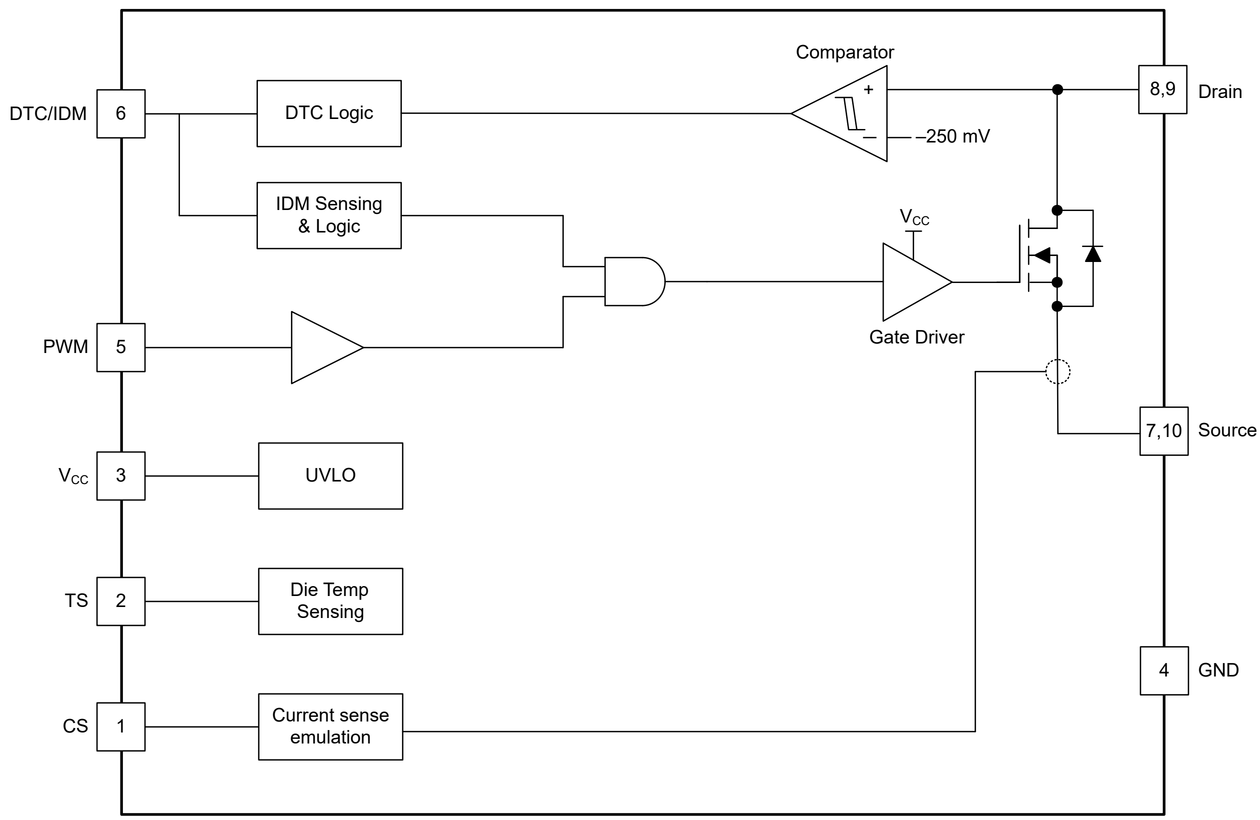

Figure 6-1. Functional Block Diagram

6.3 Feature Description

6.3.1 V_{CC} and Undervoltage Lockout

The LMS1225 has an internal undervoltage-lockout (UVLO) protection feature based on the V_{CC} pin voltage. When the VCC voltage is below the threshold voltage the gate drive output is low. After V_{CC} goes above rising UVLO limit, the gate drive output follows the PWM signal command. After the positive-going UVLO is cleared, if

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the V_{CC} falls below the negative-going UVLO limit, the gate drive output goes low until the positive-going UVLO is cleared again.

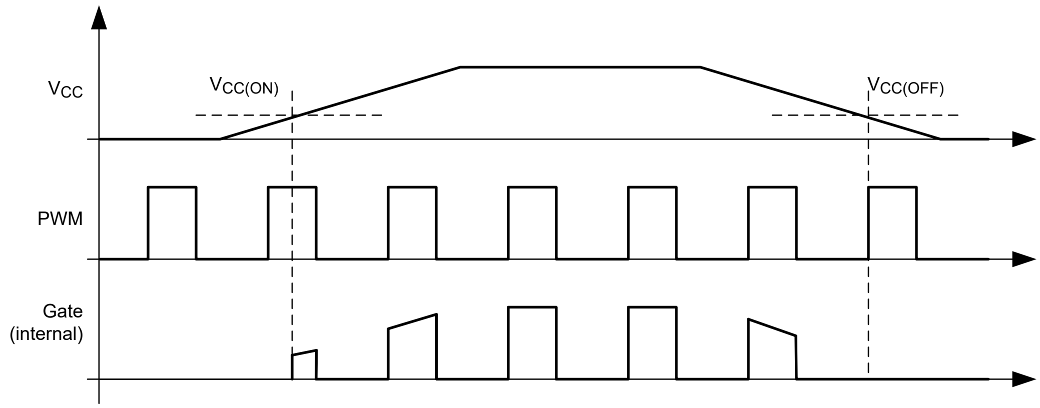

Figure 6-2. Device Power Up and Power Down

6.3.2 Current Sense

The LMS1225 includes current sense emulation, which is output on the CS pin. The current sense emulation function creates a replica of the current through the MOSFET. Current sense emulation on the LMS1225 is able to represent both positive and negative current by sourcing and sinking current from the CS pin. When device is conducting current from source to drain, the CS pin sources current out of the CS pin. When the device is conducting current from drain to source, the CS pin sinks current into the CS pin.

Connect the CS pin to a voltage source, V_{Ref}, through a resistor (R_{CS}). Read the voltage across the resistor to calculate the current through the resistor. The current through the resistor represents the current through the FET with a gain of 10µA/A. The V_{Ref} voltage source is from 0.9V to 2.1V.

If the V_{Ref} voltage source is unregulated, best practice is to use a differential ADC. If the voltage source is regulated, use a single ended ADC.

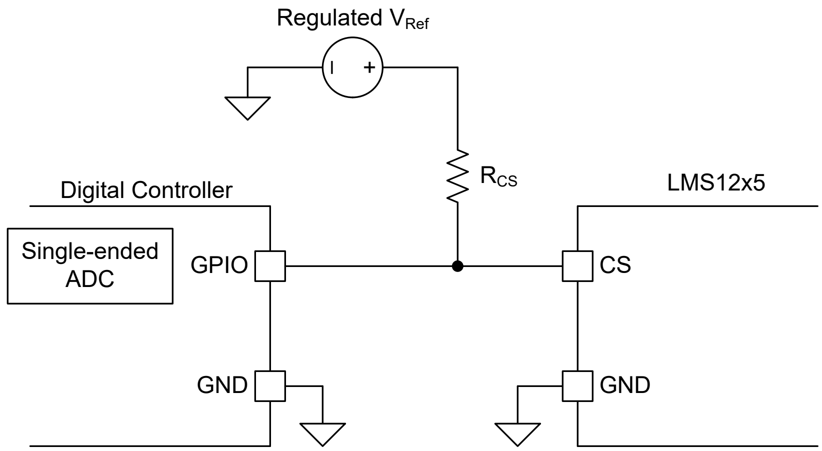

Figure 6-3. Current Sense Implementation With Regulated Voltage Source

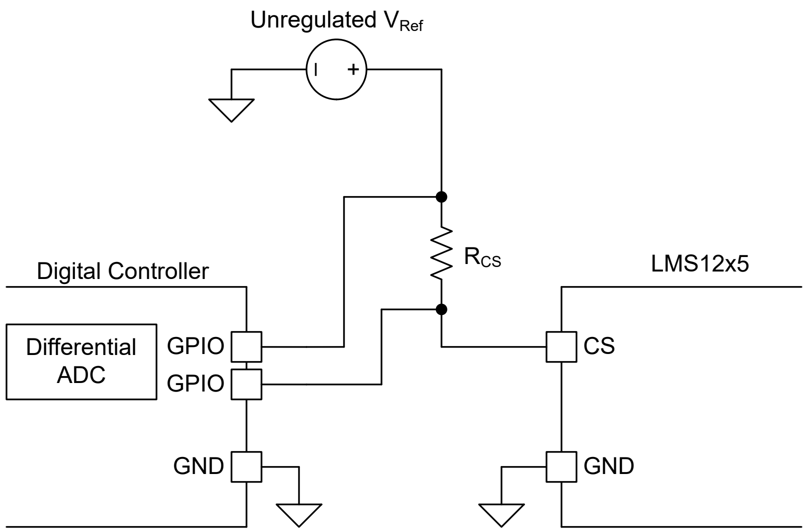

Figure 6-4. Current Sense Implementation With Unregulated Voltage Source

6.3.3 Temperature Sensing and Reporting

The LMS1225 device includes integrated temperature sensing and reporting. The temperature sense element is integrated into the same die at the MOSFET to provide the best accuracy. The temperature is reported out on the TS pin in a voltage signal from 0V to 3.3V. The signal has a linear correlation with 0.25V representing 27°C and 2.55V representing 175°C.

6.3.4 Dead Time Compensation

In Figure 6-5, V_{DS} is the drain-to-source voltage which is connected to the drain pin. PWM is the gate-driver input-command signal from digital controller on the PWM pin. DTC is the signal from the DTC pin on LMS1225. The DTC pin outputs an active low pulse that occurs after the drain to source voltage goes beyond the –250mV threshold. The pulse is a fixed length pulse with duration according to the switching characteristics table. The GATE (internal) signal is the gate-driver output and describes when the device is driven on. The body-diode conduction detection comparator has a –250mV threshold.

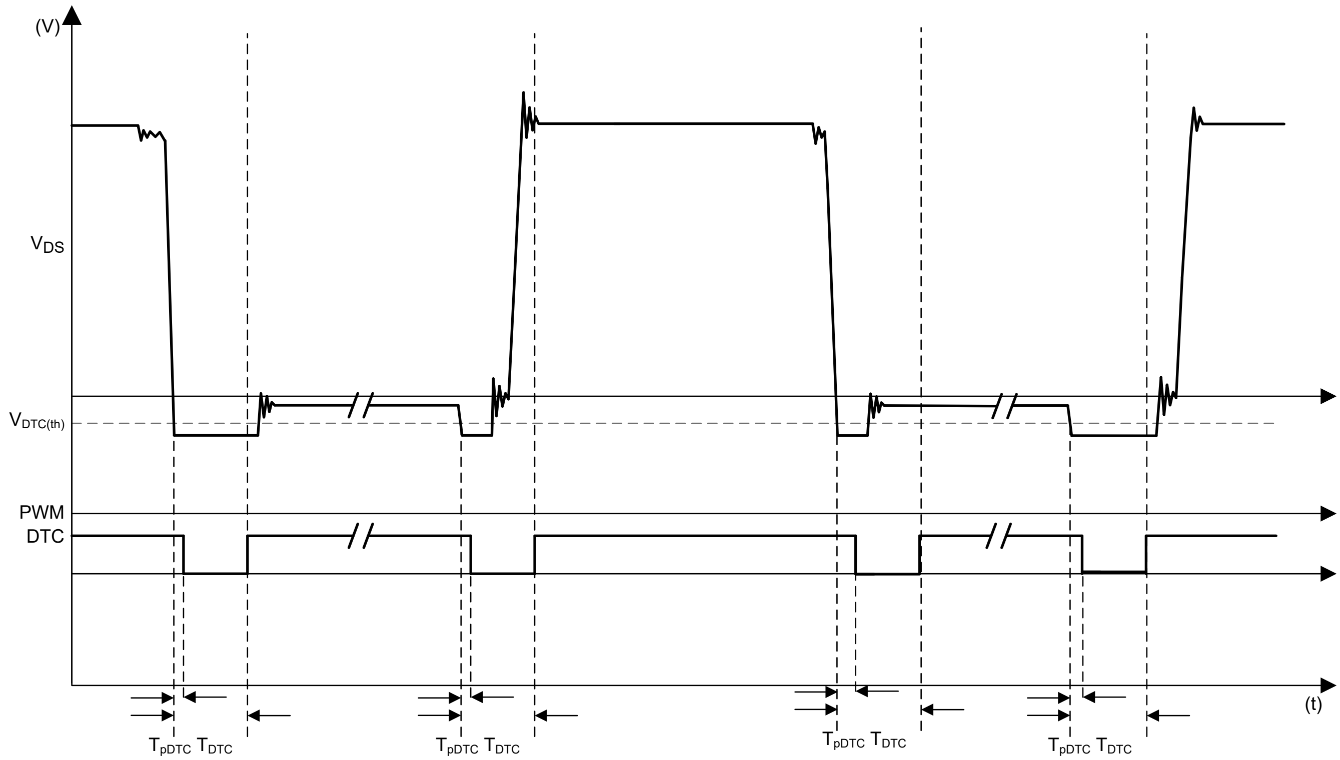

Figure 6-5. Input-Output Timing Diagram (Turn-On Optimization is Enabled)

To improve noise immunity, the comparator output DTC blanks when the gate driver output, GATE (internal), is high. The DTC signal always outputs high when OUT is high.

6.3.5 Ideal Diode Mode

To operate the LMS1225 device in ideal diode mode, connect a 22kΩ pulldown resistor from DTC (pin 6) to Source. When the LMS1225 device is in ideal diode mode, the MOSFET turn-on is controlled by a combination of the PWM signal and the internal body-diode conduction sensing circuit. If the PWM signal is high and body-diode conduction is sensed, the gate driver turns the MOSFET on. Turn-off is controlled only by the falling edge of the PWM signal.

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.3 Trademarks

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7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

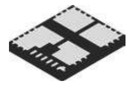
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2026	*	Initial Release

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

9.1 Mechanical Data

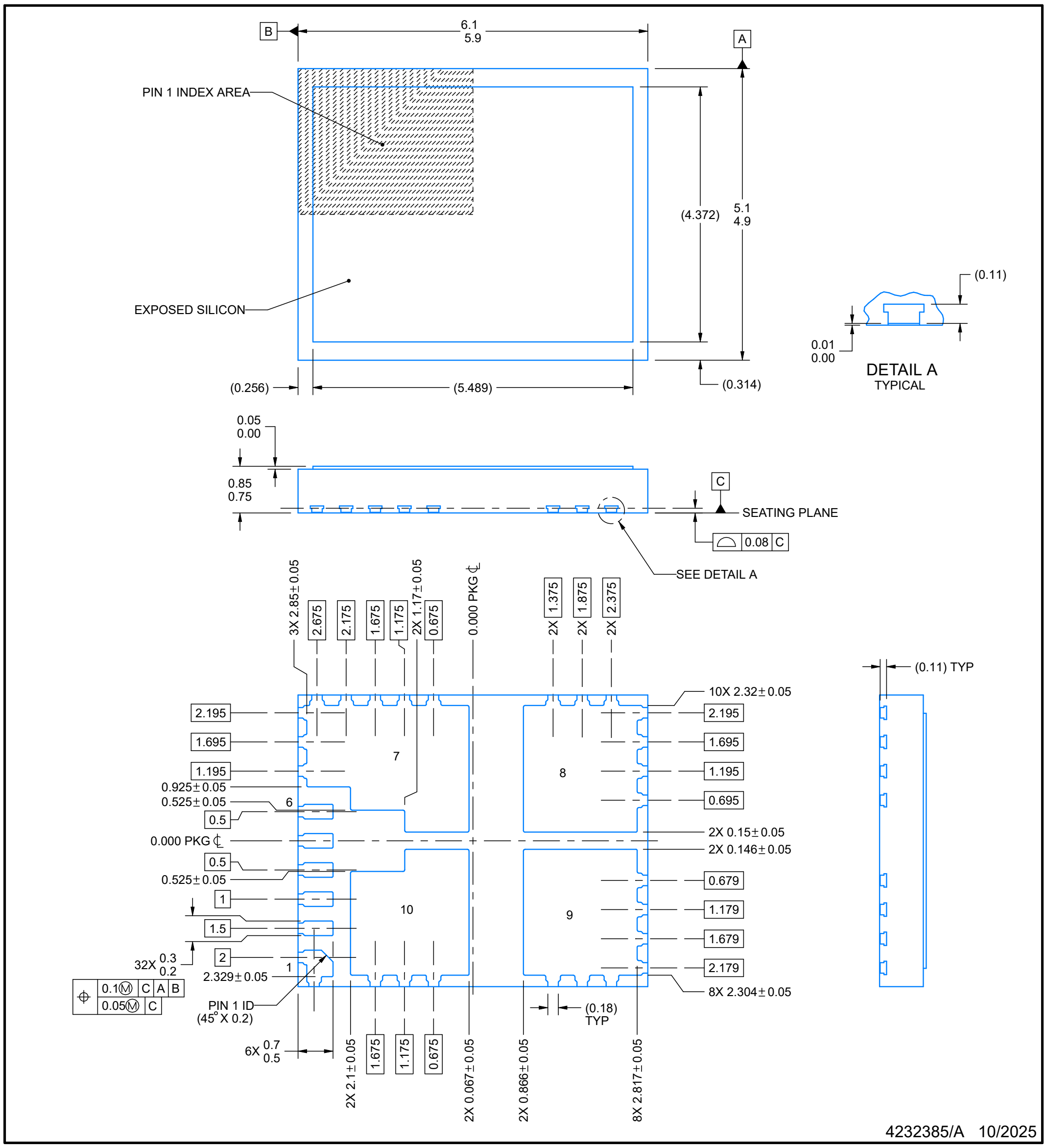


PACKAGE OUTLINE

VEU0010A

VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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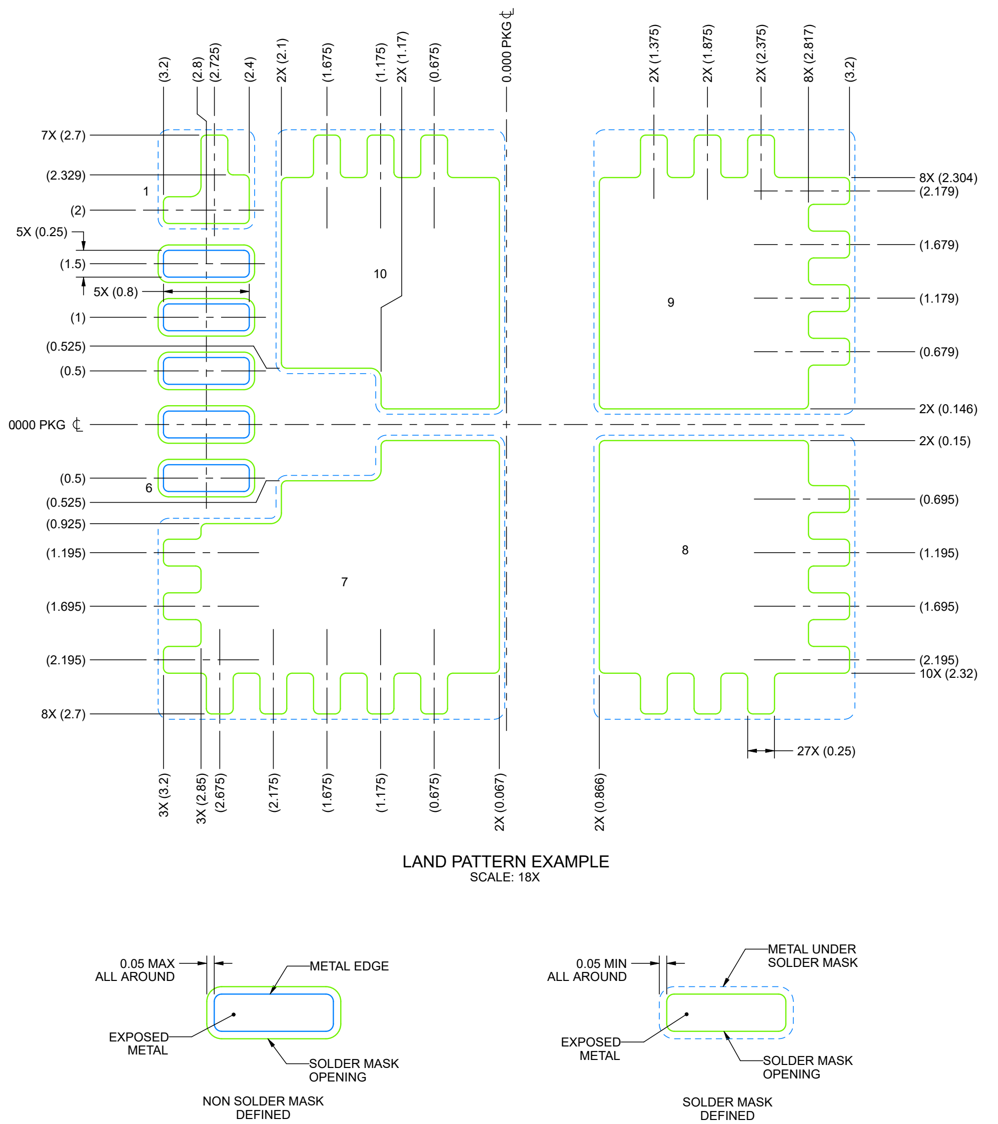
EXAMPLE BOARD LAYOUT

VEU0010A

VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE: 18X

SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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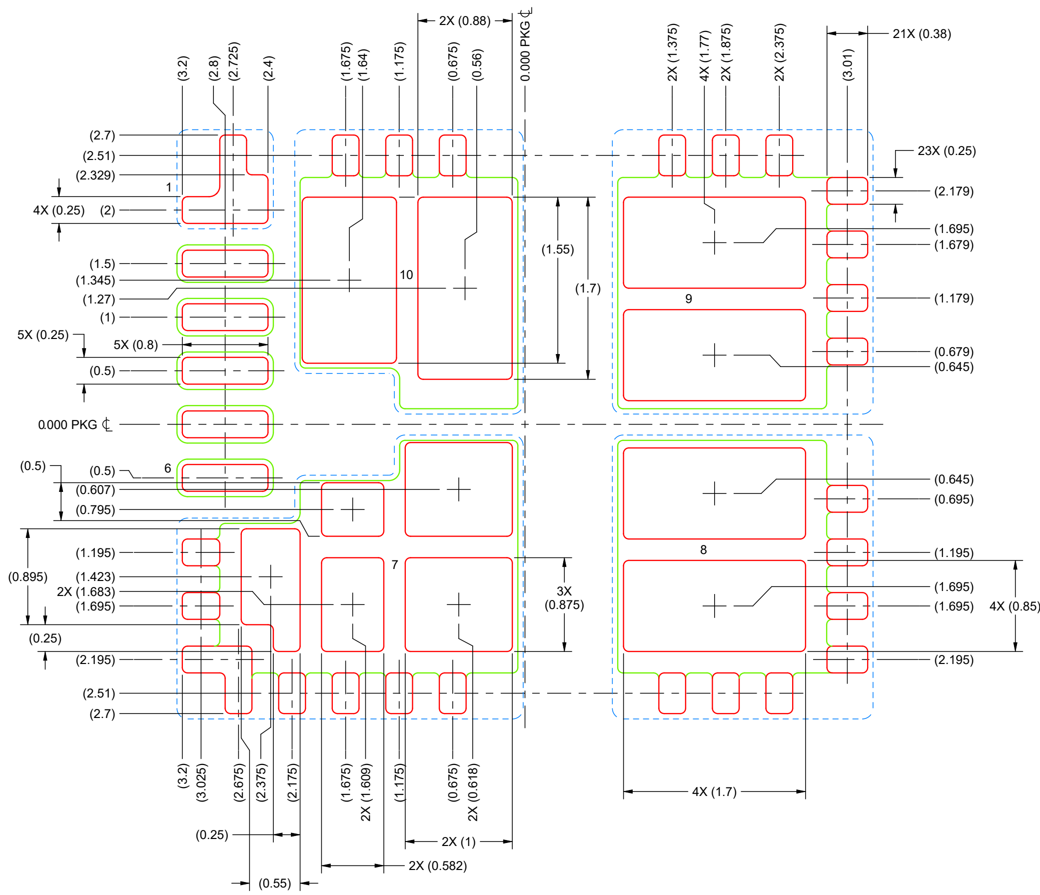
EXAMPLE STENCIL DESIGN

VEU0010A **VQFN-FCRLF - 0.85 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 18X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 7: 67%
PADS 8 -10: 72%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.