LMV61x Single, Dual, and Quad, 1.4-MHz, Low-Power, General-Purpose 1.8-V Operational Amplifiers

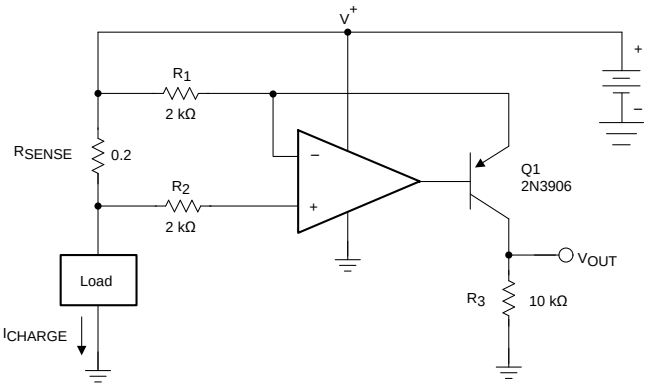
1 Features

- Supply Values: 1.8 V (Typical)
- Ensured 1.8-V, 2.7-V, and 5-V Specifications
- Output Swing:
  - 80 mV From Rail With 600-Ω Load
  - 30 mV From Rail With 2-kΩ Load
- V_{CM} = 200 mV Beyond Rails
- 100-µA Supply Current (Per Channel)
- 1.4-MHz Gain Bandwidth Product
- Maximum V_{OS} = 4 mV
- Temperature Range: −40°C to +125°C
- Create a Custom Design Using the LMV61x With the WEBENCH® Power Designer

2 Applications

- Consumer Communication
- Consumer Computing
- PDAs
- Audio Pre-Amplifiers
- Portable or Battery-Powered Electronic Equipment
- Supply Current Monitoring
- Battery Monitoring

Typical Application



$$V_{OUT} = \frac{R_{SENSE} \bullet R_3}{R_1} \bullet I_{Charge} = 1\,\Omega \bullet I_{Charge}$$

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3 Description

The LMV61x devices are single, dual, and quad low-voltage, low-power operational amplifiers (op amps). They are designed specifically for low-voltage, general-purpose applications. Other important product characteristics are, rail-to-rail input or output, low supply voltage of 1.8 V and wide temperature range. The LMV61x input common mode extends 200 mV beyond the supplies and the output can swing rail-to-rail unloaded and within 30 mV with 2-kΩ load at 1.8-V supply. The LMV61x achieves a gain bandwidth of 1.4 MHz while drawing 100-µA (typical) quiescent current.

The industrial-plus temperature range of −40°C to 125°C allows the LMV61x to accommodate a broad range of extended environment applications.

The LMV611 is offered in the tiny 5-pin SC70 package, the LMV612 in space-saving 8-pin VSSOP and SOIC packages, and the LMV614 in 14-pin TSSOP and SOIC packages. These small package amplifiers offer an ideal solution for applications requiring minimum PCB footprint. Applications with area constrained PCB requirements include portable and battery-operated electronics.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV611	SOT-23 (5)	2.92 mm × 1.60 mm
	SC70 (5)	2.00 mm × 1.25 mm
LMV612	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	4.90 mm × 3.91 mm
LMV614	TSSOP (14)	5.00 mm × 4.40 mm
	SOIC (14)	8.64 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2016) to Revision D — **Page**

- Added links for WEBENCH ... 1
- Changed Slew Rate vs Supply title to reflect LMV611 and LMV614 only ... 13
- Added Slew Rate vs Supply Graph for LMV612 only ... 13

Changes from Revision B (March 2013) to Revision C — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed values in the *Thermal Information* table to align with JEDEC standards ... 5

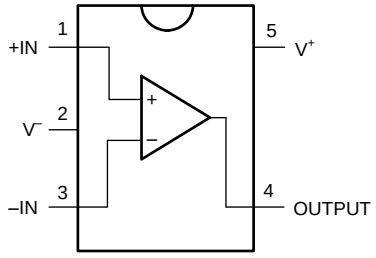
Changes from Revision A (March 2012) to Revision B — **Page**

- Changed layout of National Semiconductor data sheet to TI format ... 1

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5 Pin Configuration and Functions

DCK and DBV Packages
5-Pin SC70 and SOT-23
Top View

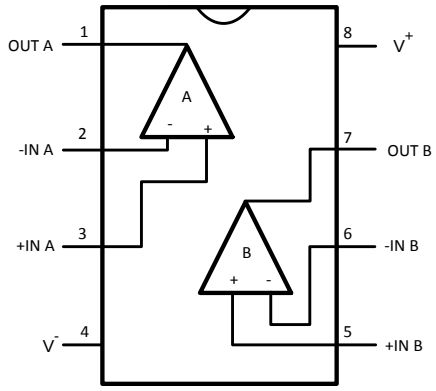


Pin Functions – LMV611

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	+IN	I	Noninverting input
2	V–	P	Negative supply input
3	–IN	I	Inverting input
4	OUTPUT	O	Output
5	V+	P	Positive supply input

(1) I = Input, O = Output, and P = Power

DGK and D Packages
8-Pin VSSOP and SOIC
Top View



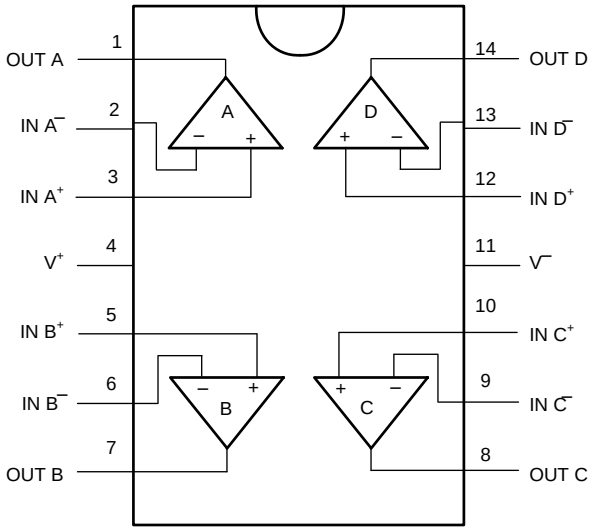
Pin Functions – LMV612

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	OUT A	O	Output A
2	–IN A	I	Inverting input A
3	+IN A	I	Noninverting input A
4	V–	P	Negative supply input
5	+IN B	I	Noninverting input B
6	–IN B	I	Inverting input B
7	OUT B	O	Output B
8	V+	P	Positive supply input

(1) I = Input, O = Output, and P = Power

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PW and D Packages
14-Pin TSSOP and SOIC
Top View



Pin Functions – LMV614

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	OUT A	O	Output A
2	IN A−	I	Inverting input A
3	IN A+	I	Noninverting input A
4	V+	P	Positive supply input
5	IN B+	I	Noninverting input B
6	IN B−	I	Inverting input B
7	OUT B	O	Output B
8	OUT C	O	Output C
9	IN C−	I	Inverting input C
10	IN C+	I	Noninverting input C
11	V−	P	Negative supply input
12	IN D+	I	Noninverting input D
13	IN D−	I	Inverting input D
14	OUT D	O	Output D

(1) I = Input, O = Output, and P = Power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
Differential input voltage	±Supply voltage		
Supply voltage (V^+–V^-)		6	V
Voltage at input or output pin	V^- – 0.3	V^+ + 0.3	V
Junction temperature, T_{JMAX}(4)		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Soldering specifications for all packages available at www.ti.com and *Absolute Maximum Ratings for Soldering*.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Machine model (MM)(2)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Machine model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage	1.8	5.5	V
Temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMV611		LMV612		LMV614		UNIT
		DBV (SOT-23)	DCK (SC70)	D (SOIC)	DGK (VSSOP)	D (SOIC)	PW (TSSOP)	
		5 PINS	5 PINS	8 PINS	8 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	197.2	285.9	125.9	184.5	94.4	124.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	156.7	115.9	70.2	74.3	52.5	51.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.6	63.7	66.5	105.1	48.9	67.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	41.4	4.5	19.8	13.1	14.3	6.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55	62.9	65.9	103.6	48.6	66.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics – 1.8 V (DC)

All limits ensured for T_J = 25°C, V^+ = 1.8 V, V^- = 0 V, V_{CM} = V^+/ 2, V_O = V^+/ 2, and R_L > 1 MΩ (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OS}	Input offset voltage	LMV611 (single)			1	4	mV
		LMV612 (dual) and LMV614 (quad)			1	5.5	
TCV_{OS}	Input offset voltage average drift				5.5		µV/°C
I_B	Input bias current				15		nA
I_{OS}	Input offset current				13		nA
I_S	Supply current (per channel)				103	185	µA
CMRR	Common-mode rejection ratio	LMV611, 0 V ≤ V_{CM} ≤ 0.6 V, 1.4 V ≤ V_{CM} ≤ 1.8 V(4)		60	78		dB
		LMV612 and LMV614, 0 V ≤ V_{CM} ≤ 0.6 V, 1.4 V ≤ V_{CM} ≤ 1.8 V(4)		55	76		
		−0.2 V ≤ V_{CM} ≤ 0 V, 1.8 V ≤ V_{CM} ≤ 2 V		50	72		
PSRR	Power supply rejection ratio	1.8 V ≤ V^+ ≤ 5 V			100		dB
CMVR	Input common-mode voltage	For CMRR range ≥ 50 dB	V^-, T_A = 25°C	V^- – 0.2	–0.2		V
			V^+, T_A = 25°C		2.1	V^+ + 0.2	
			T_A = −40°C to 85°C	V^-		V^+	
			T_A = 125°C	V^- + 0.2		V^+ – 0.2	
A_V	Large signal voltage gain LMV611 (single)	R_L = 600 Ω to 0.9 V, V_O = 0.2 V to 1.6 V, V_{CM} = 0.5 V		77	101		dB
		R_L = 2 kΩ to 0.9 V, V_O = 0.2 V to 1.6 V, V_{CM} = 0.5 V		80	105		
	Large signal voltage gain LMV612 (dual) and LMV614 (quad)	R_L = 600 Ω to 0.9 V, V_O = 0.2 V to 1.6 V, V_{CM} = 0.5 V		75	90		
		R_L = 2 kΩ to 0.9 V, V_O = 0.2 V to 1.6 V, V_{CM} = 0.5 V		78	100		
V_O	Output swing	R_L = 600 Ω to 0.9 V		1.65	1.72		V
		V_{IN} = ±100 mV			0.077	0.105	
		R_L = 2 kΩ to 0.9 V		1.75	1.77		
		V_{IN} = ±100 mV			0.024	0.035	
I_O	Output short-circuit current(5)	Sourcing, V_O = 0 V, V_{IN} = 100 mV			8		mA
		Sinking, V_O = 1.8 V, V_{IN} = –100 mV			9		

(1) Electrical characteristics values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. See *Application and Implementation* for information of temperature derating of the device. *Absolute Maximum Ratings* indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depends on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) For specified temperature ranges, see Input common mode voltage specifications.
(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.

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6.6 Electrical Characteristics – 1.8 V (AC)

All limits ensured for T_J = 25°C, V^+ = 1.8 V, V^- = 0 V, V_{CM} = V^+/ 2, V_O = V^+/ 2, and R_L > 1 MΩ (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
SR	Slew rate(4)			0.35		V/µs
GBW	Gain-bandwidth product			1.4		MHz
Φ_m	Phase margin			67		°
G_m	Gain margin			7		dB
e_n	Input-referred voltage noise	f = 10 kHz, V_{CM} = 0.5 V		60		nV/√Hz
i_n	Input-referred current noise	f = 10 kHz		0.08		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = +1, R_L = 600 Ω, V_{IN} = 1 V_{PP}		0.023%		
	Amp-to-amp isolation(5)			123		dB

(1) Electrical characteristics values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. See *Application and Implementation* for information of temperature derating of the device. *Absolute Maximum Ratings* indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depends on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.
(5) Input-referred, R_L = 100 kΩ connected to V^+ / 2. Each amp excited in turn with 1 kHz to produce V_O = 3 V_{PP} (for supply voltages < 3 V, V_O = V^+).

6.7 Electrical Characteristics – 2.7 V (DC)

All limits ensured for T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = V^+/ 2, V_O = V^+/ 2, and R_L > 1 MΩ (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OS}	Input offset voltage	LMV611 (single)		1	4	mV
		LMV612 (dual) and LMV614 (quad)		1	5.5	
TCV_{OS}	Input offset voltage average drift			5.5		µV/°C
I_B	Input bias current			15		nA
I_{OS}	Input offset current			8		nA
I_S	Supply current (per channel)			105	190	µA
CMRR	Common-mode rejection ratio	LMV611, 0 V ≤ V_{CM} ≤ 1.5 V, 2.3 V ≤ V_{CM} ≤ 2.7 V(4)	60	81		dB
		LMV612 and LMV614, 0 V ≤ V_{CM} ≤ 1.5 V, 2.3 V ≤ V_{CM} ≤ 2.7 V(4)	55	80		
		−0.2 V ≤ V_{CM} ≤ 0 V, 2.7 V ≤ V_{CM} ≤ 2.9 V	50	74		
PSRR	Power supply rejection ratio	1.8 V ≤ V^+ ≤ 5 V, V_{CM} = 0.5 V		100		dB

(1) Electrical characteristics values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. See *Application and Implementation* for information of temperature derating of the device. *Absolute Maximum Ratings* indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depends on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) For specified temperature ranges, see input common mode voltage specifications.

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Electrical Characteristics – 2.7 V (DC) (continued)

All limits ensured for T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = V^+/ 2, V_O = V^+/ 2, and R_L > 1 MΩ (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
V_{CM}	Input common-mode voltage	For CMRR range ≥ 50 dB	V^-, T_A = 25°C	V^- – 0.2	–0.2		V
			V^+, T_A = 25°C		3	V^+ + 0.2	
			T_A = –40°C to 85°C	V^-		V^+	
			T_A = 125°C	V^- + 0.2		V^+ – 0.2	
A_V	Large signal voltage gain LMV611 (single)	R_L = 600 Ω to 1.35 V, V_O = 0.2 V to 2.5 V		87	104		dB
		R_L = 2 kΩ to 1.35 V, V_O = 0.2 V to 2.5 V		92	110		
	Large signal voltage gain LMV612 (dual) and LMV614 (quad)	R_L = 600 Ω to 1.35 V, V_O = 0.2 V to 2.5 V		78	90		
		R_L = 2 kΩ to 1.35 V, V_O = 0.2 V to 2.5 V		81	100		
V_O	Output swing	R_L = 600 Ω to 1.35 V		2.55	2.62		V
		V_{IN} = ±100 mV			0.083	0.11	
		R_L = 2 kΩ to 1.35 V		2.65	2.675		
		V_{IN} = ±100 mV			0.025	0.04	
I_O	Output short-circuit current(5)	Sourcing, V_O = 0 V, V_{IN} = 100 mV			30		mA
		Sinking, V_O = 0 V, V_{IN} = –100 mV			25		

(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.

6.8 Electrical Characteristics – 2.7 V (AC)

All limits ensured for T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = 1 V, V_O = 1.35 V, and R_L > 1 MΩ (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
SR	Slew rate(4)			0.4		V/µs
GBW	Gain-bandwidth product			1.4		MHz
Φ_m	Phase margin			70		°
G_m	Gain margin			7.5		dB
e_n	Input-referred voltage noise	f = 10 kHz, V_{CM} = 0.5 V		57		nV/√Hz
i_n	Input-referred current noise	f = 10 kHz		0.08		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = +1, R_L = 600 Ω, V_{IN} = 1 V_{PP}		0.022%		
	Amp-to-amp isolation(5)			123		dB

(1) Electrical characteristics values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. See *Application and Implementation* for information of temperature derating of the device. *Absolute Maximum Ratings* indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depends on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.
(5) Input-referred, R_L = 100 kΩ connected to V^+ / 2. Each amp excited in turn with 1 kHz to produce V_O = 3 V_{PP} (for supply voltages < 3 V, V_O = V^+).

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6.9 Electrical Characteristics – 5 V (DC)

All limits ensured for T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V^+/ 2, V_O = V^+/ 2, and R_L > 1 MΩ (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OS}	Input offset voltage	LMV611 (single)			1	4	mV
		LMV612 (dual) and LMV614 (quad)			1	5.5	
TCV_{OS}	Input offset voltage average drift				5.5		µV/°C
I_B	Input bias current				14	35	nA
I_{OS}	Input offset current				9		nA
I_S	Supply current (per channel)				116	210	µA
CMRR	Common-mode rejection ratio	0 V ≤ V_{CM} ≤ 3.8 V, 4.6 V ≤ V_{CM} ≤ 5 V(4)		60	86		dB
		–0.2 V ≤ V_{CM} ≤ 0 V 5 V ≤ V_{CM} ≤ 5.2 V		50	78		
PSRR	Power supply rejection ratio	1.8 V ≤ V^+ ≤ 5 V, V_{CM} = 0.5 V			100		dB
CMVR	Input common-mode voltage	For CMRR range ≥ 50 dB	V^-, T_A = 25°C	V^- – 0.2	–0.2		V
			V^+, T_A = 25°C		5.3	V^+ + 0.2	
			T_A = –40°C to 85°C	V^-		V^+	
			T_A = 125°C	V^- + 0.3		V^+ – 0.3	
A_V	Large signal voltage gain LMV611 (single)	R_L = 600 Ω to 2.5 V, V_O = 0.2 V to 4.8 V		88	102		dB
		R_L = 2 kΩ to 2.5 V, V_O = 0.2 V to 4.8 V		94	113		
	Large signal voltage gain LMV612 (dual) and LMV614 (quad)	R_L = 600 Ω to 2.5 V, V_O = 0.2 V to 4.8 V		81	90		
		R_L = 2 kΩ to 2.5 V, V_O = 0.2 V to 4.8 V		85	100		
V_O	Output swing	R_L = 600 Ω to 2.5 V		4.855	4.89		V
		V_{IN} = ±100 mV			0.12	0.16	
		R_L = 2 kΩ to 2.5 V		4.945	4.967		
		V_{IN} = ±100 mV			0.037	0.065	
I_O	Output short-circuit current(5)	LMV611, Sourcing, V_O = 0 V, V_{IN} = 100 mV			100		mA
		Sinking, V_O = 5 V, V_{IN} = –100 mV			65		

(1) Electrical characteristics values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. See *Application and Implementation* for information of temperature derating of the device. *Absolute Maximum Ratings* indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depends on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) For specified temperature ranges, see Input common mode voltage specifications.
(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.

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6.10 Electrical Characteristics – 5 V (AC)

All limits ensured for T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V^+/ 2, V_O = 2.5 V, and R_L > 1 MΩ (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
SR	Slew rate(4)			0.42		V/µs
GBW	Gain-bandwidth product			1.5		MHz
Φ_m	Phase margin			71		°
G_m	Gain margin			8		dB
e_n	Input-referred voltage noise	f = 10 kHz, V_{CM} = 1 V		50		nV/√Hz
i_n	Input-referred current noise	f = 10 kHz		0.08		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = +1, R_L = 600 Ω, V_O = 1 V_{PP}		0.022%		
	Amp-to-amp isolation(5)			123		dB

(1) Electrical characteristics values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. See *Application and Implementation* for information of temperature derating of the device. *Absolute Maximum Ratings* indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depends on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.
(5) Input-referred, R_L = 100 kΩ connected to V^+ / 2. Each amp excited in turn with 1 kHz to produce V_O = 3 V_{PP} (for supply voltages < 3 V, V_O = V^+).

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6.11 Typical Characteristics

V_S = 5 V, single supply, T_A = 25°C (unless otherwise noted)

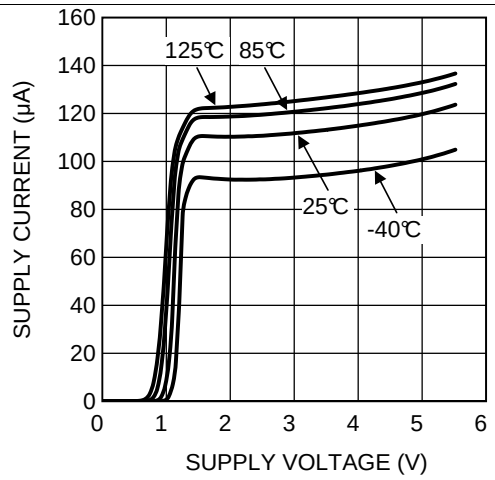


Figure 1. Supply Current vs Supply Voltage (LMV611)

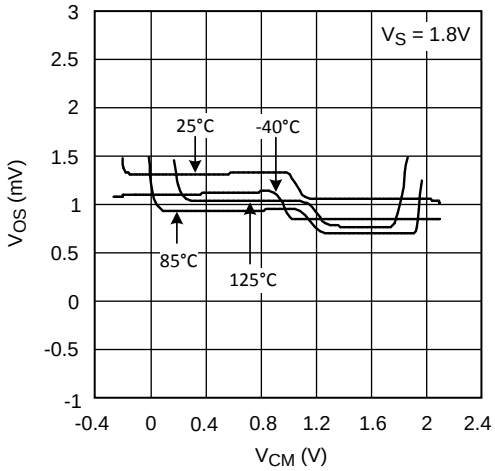


Figure 2. Offset Voltage vs Common-Mode Range

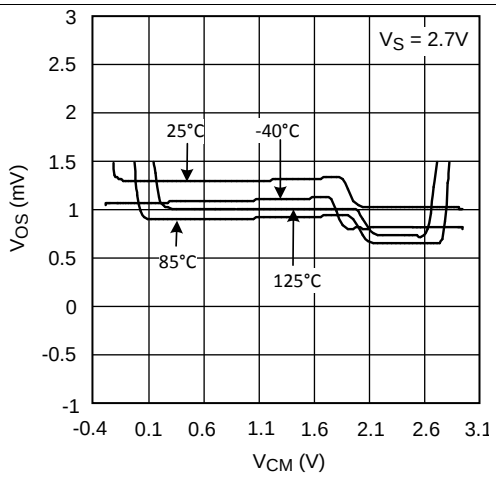


Figure 3. Offset Voltage vs Common-Mode Range

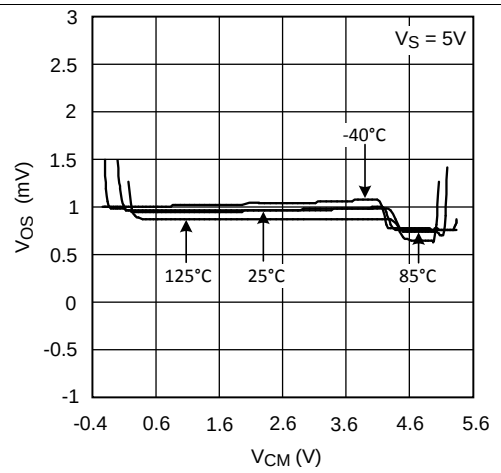


Figure 4. Offset Voltage vs Common-Mode Range

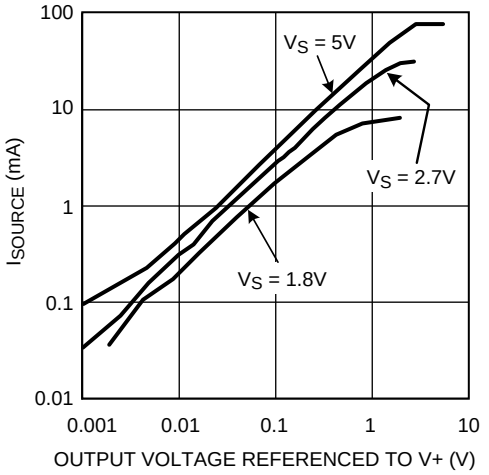


Figure 5. Sourcing Current vs Output Voltage

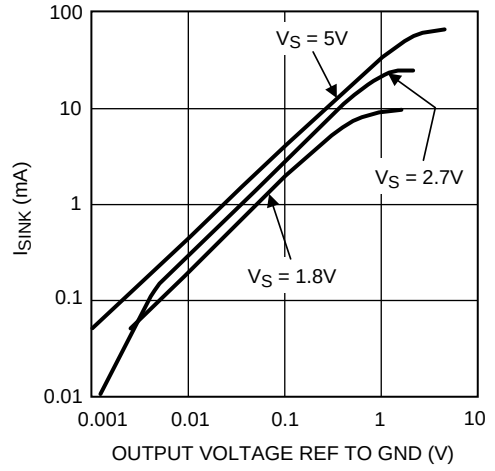


Figure 6. Sinking Current vs Output Voltage

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Typical Characteristics (continued)

V_S = 5 V, single supply, T_A = 25°C (unless otherwise noted)

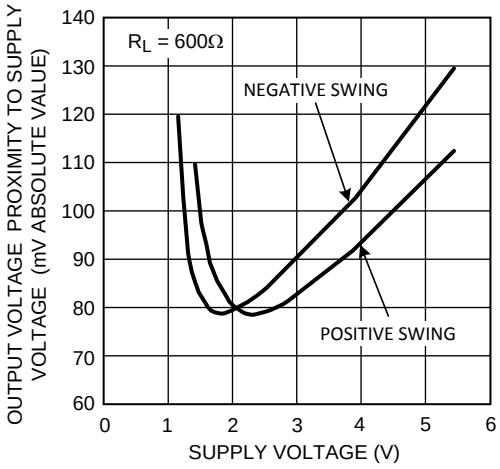


Figure 7. Output Voltage Swing vs Supply Voltage

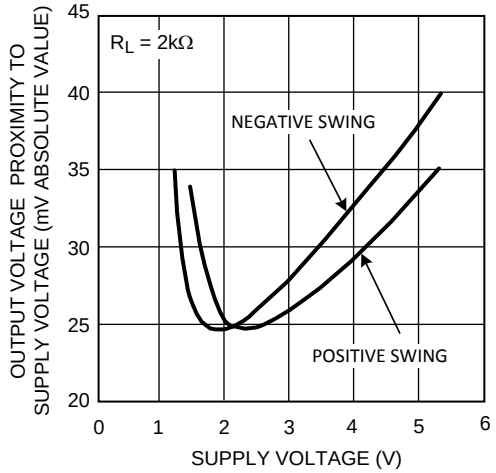


Figure 8. Output Voltage Swing vs Supply Voltage

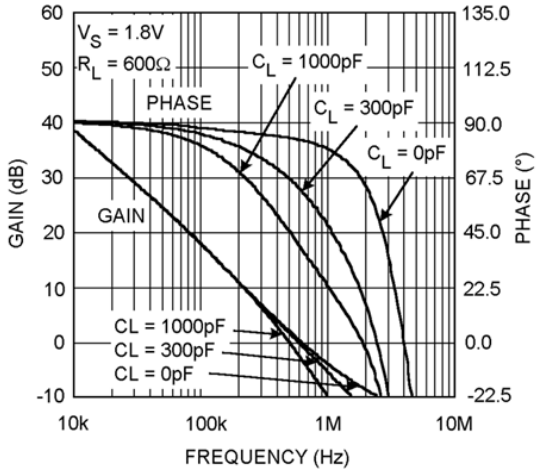


Figure 9. Gain and Phase vs Frequency

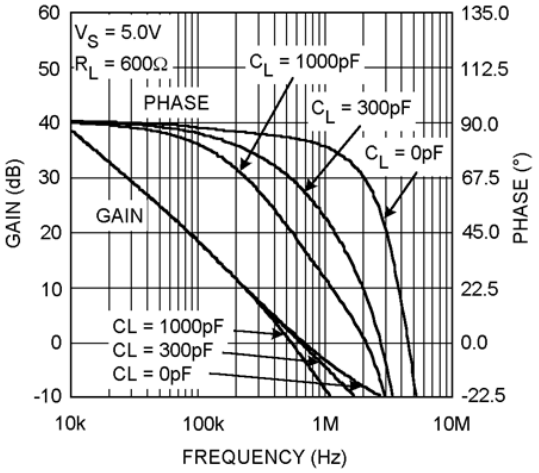


Figure 10. Gain and Phase vs Frequency

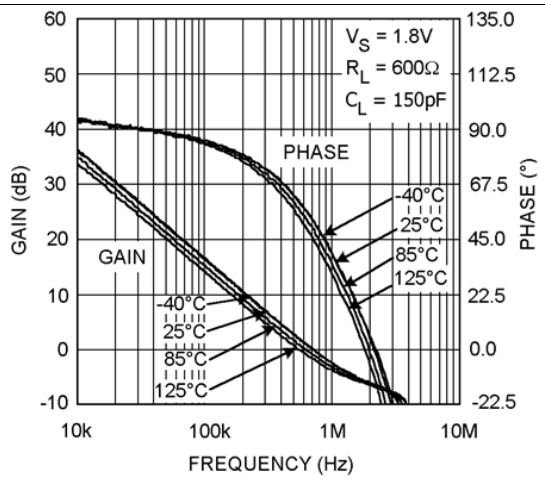


Figure 11. Gain and Phase vs Frequency

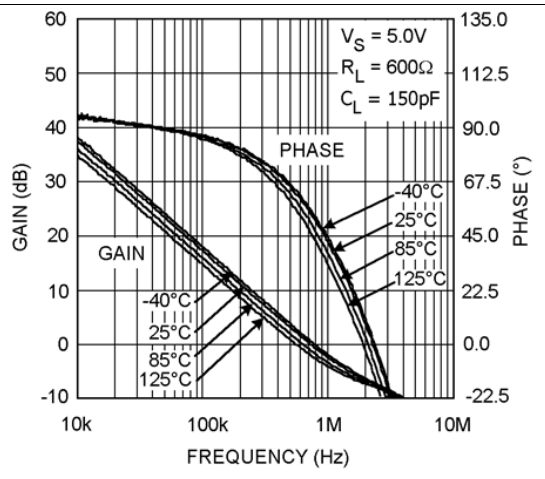


Figure 12. Gain and Phase vs Frequency

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Typical Characteristics (continued)

V_S = 5 V, single supply, T_A = 25°C (unless otherwise noted)

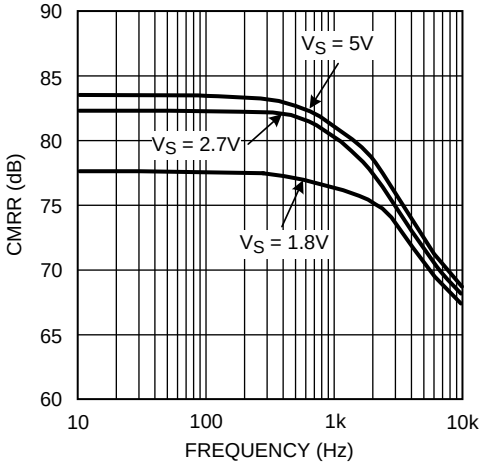


Figure 13. CMRR vs Frequency

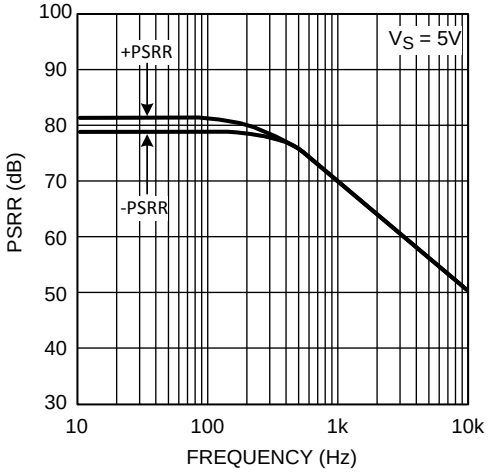


Figure 14. PSRR vs Frequency

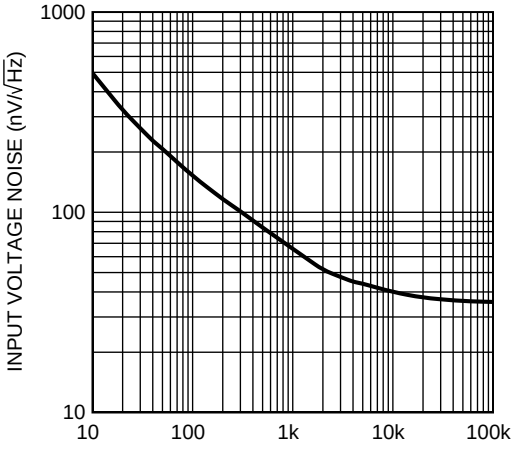


Figure 15. Input Voltage Noise vs Frequency

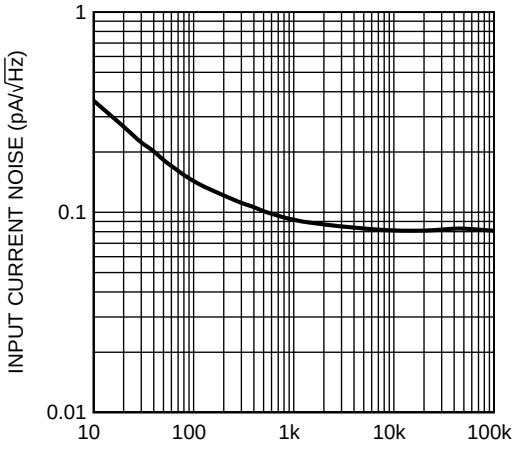


Figure 16. Input Current Noise vs Frequency

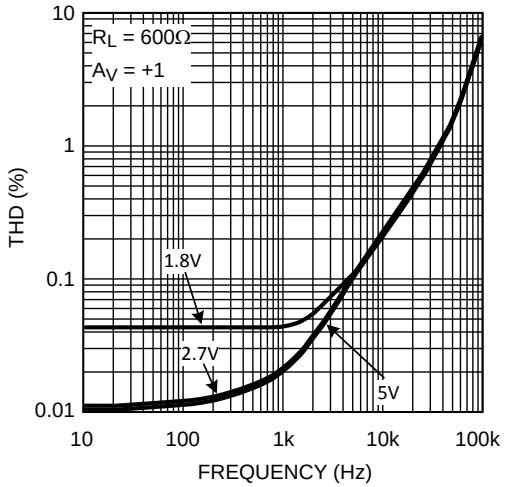


Figure 17. THD vs Frequency

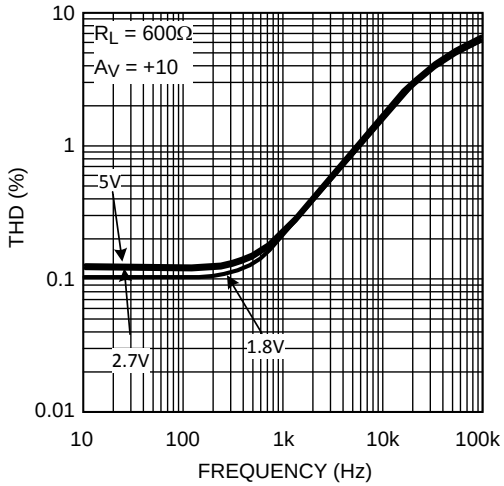


Figure 18. THD vs Frequency

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Typical Characteristics (continued)

V_S = 5 V, single supply, T_A = 25°C (unless otherwise noted)

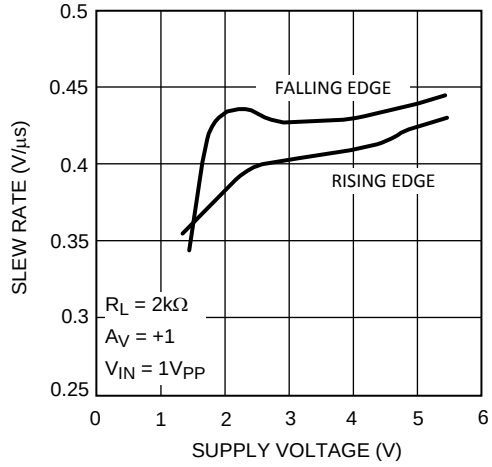


Figure 19. Slew Rate vs Supply Voltage LMV611 and LMV614

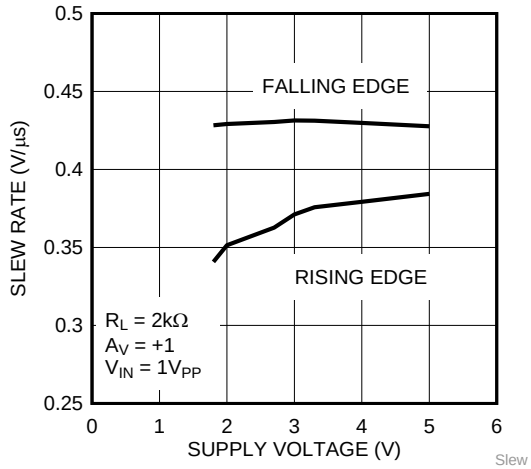


Figure 20. Slew Rate vs Supply Voltage LMV612 Only

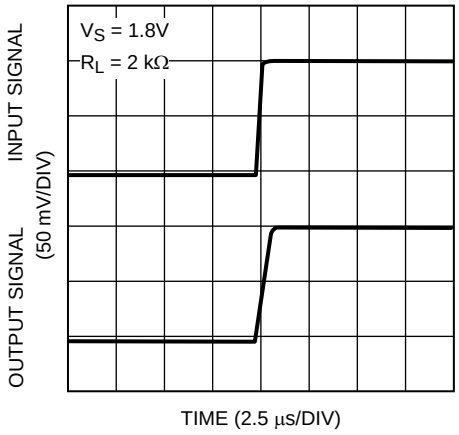


Figure 21. Small Signal Noninverting Response

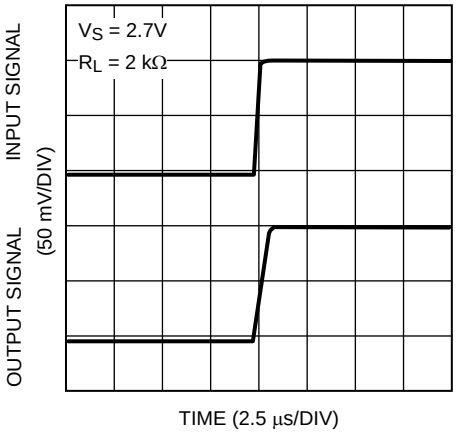


Figure 22. Small Signal Noninverting Response

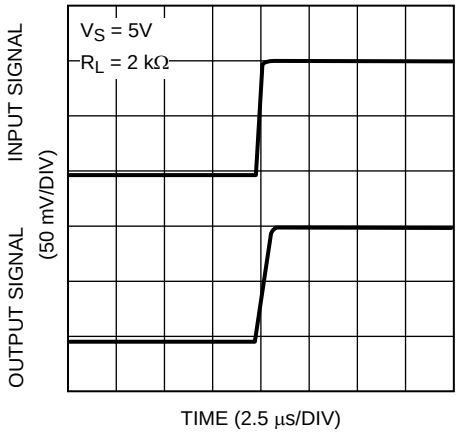


Figure 23. Small Signal Noninverting Response

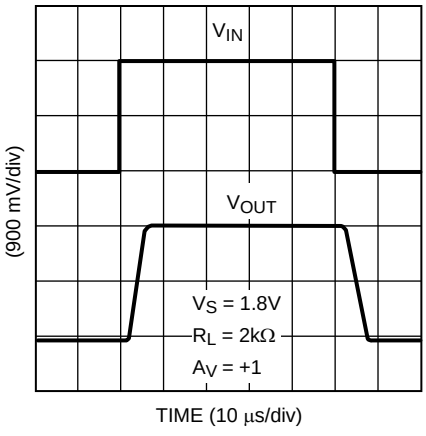


Figure 24. Large Signal Noninverting Response

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Typical Characteristics (continued)

V_S = 5 V, single supply, T_A = 25°C (unless otherwise noted)

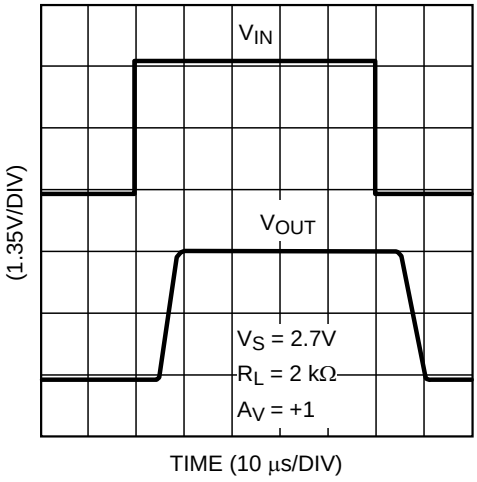


Figure 25. Large Signal Noninverting Response

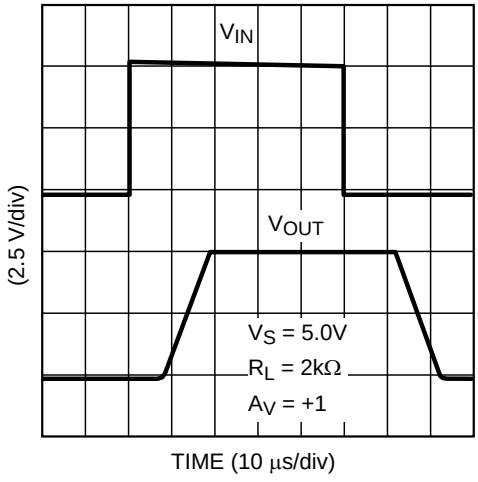


Figure 26. Large Signal Noninverting Response

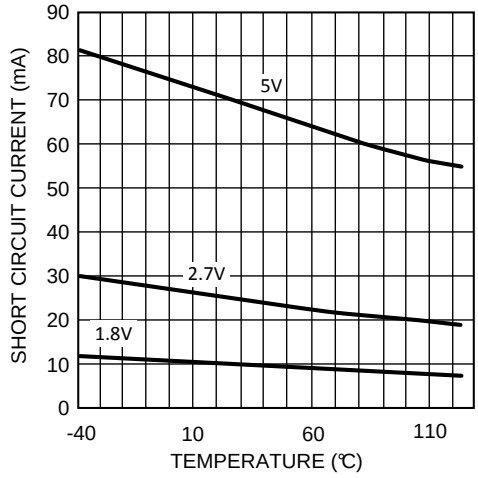


Figure 27. Short-Circuit Current vs Temperature (Sinking)

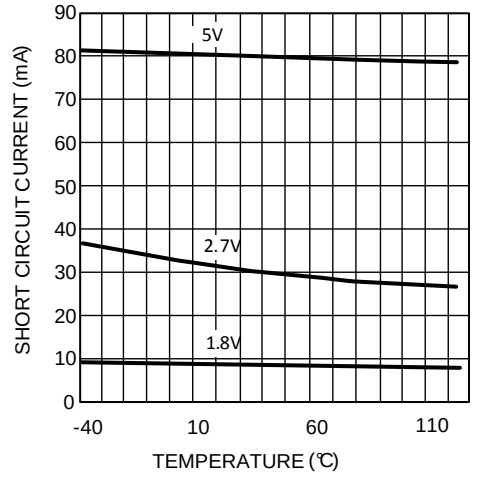


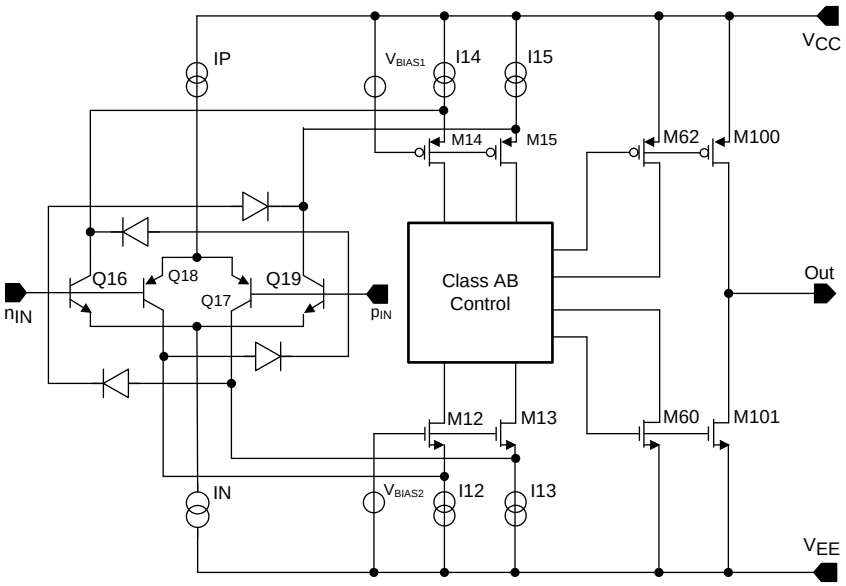
Figure 28. Short-Circuit Current vs Temperature (Sourcing)

7 Detailed Description

7.1 Overview

The LMV61x devices achieve a gain bandwidth of 1.4 MHz while drawing 100-µA (typical) quiescent current. They also provide a rail-to-rail input with a maximum input offset voltage of 4 mV. Lastly, the LMV61x input common mode extends 200 mV beyond the supplies and the output can swing rail-to-rail unloaded and within 30 mV with 2-kΩ load at 1.8-V supply.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Input and Output Stage

The rail-to-rail input stage of this family provides more flexibility for the designer. The LMV61x use a complimentary PNP and NPN input stage in which the PNP stage senses common-mode voltage near V^- and the NPN stage senses common-mode voltage near V^+. The transition from the PNP stage to NPN stage occurs 1 V below V^+. Because both input stages have their own offset voltage, the offset of the amplifier becomes a function of the input common-mode voltage and has a crossover point at 1 V below V^+.

This V_{OS} crossover point can create problems for both DC- and AC-coupled signals if proper care is not taken. Large input signals that include the V_{OS} crossover point causes distortion in the output signal. One way to avoid such distortion is to keep the signal away from the crossover. For example, in a unity-gain buffer configuration and with V_S = 5 V, a 5-V peak-to-peak signal contains input-crossover distortion while a 3-V peak-to-peak signal centered at 1.5 V does not contain input-crossover distortion as it avoids the crossover point. Another way to avoid large signal distortion is to use a gain of −1 circuit which avoids any voltage excursions at the input terminals of the amplifier. In that circuit, the common-mode DC voltage can be set at a level away from the V_{OS} crossover point. For small signals, this transition in V_{OS} shows up as a V_{CM} dependent spurious signal in series with the input signal and can effectively degrade small signal parameters such as gain and common-mode rejection ratio. To resolve this problem, the small signal must be placed such that it avoids the V_{OS} crossover point. In addition to the rail-to-rail performance, the output stage can provide enough output current to drive 600-Ω loads. Because of the high current capability, take care to not exceed the 150°C maximum junction temperature specification.

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7.4 Device Functional Modes

7.4.1 Input Bias Current Consideration

The LMV61x family has a complementary bipolar input stage. The typical input bias current (I_B) is 15 nA. The input bias current can develop a significant offset voltage. This offset is primarily due to I_B flowing through the negative feedback resistor, R_F. For example, if I_B is 50 nA and R_F is 100 kΩ, then an offset voltage of 5 mV develops ($V_{OS} = I_B \times R_F$). Using a compensation resistor (R_C), as shown in Figure 29, cancels this effect. But the input offset current (I_{OS}) still contributes to an offset voltage in the same manner.

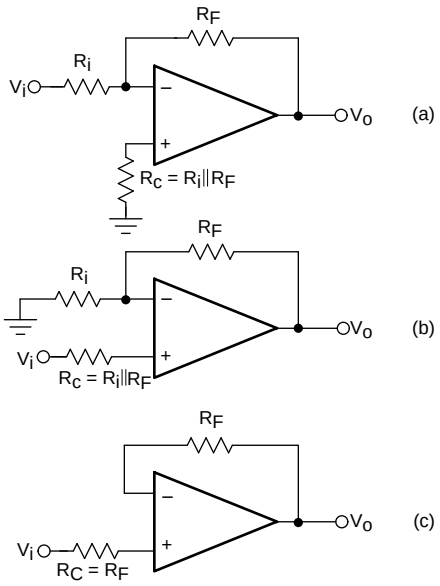


Figure 29. Canceling Offset Voltage Due to Input Bias Current

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMV61x devices bring performance, economy, and ease-of-use to low-voltage, low-power systems. They provide rail-to-rail input and rail-to-rail output swings into heavy loads.

8.1.1 Half-Wave Rectifier With Rail-to-Ground Output Swing

Because the LMV61x input common-mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half-wave rectifier functions in either direction is an easy task. All that is needed are two external resistors; there is no need for diodes or matched resistors. The half wave rectifier can have either positive or negative going outputs, depending on the way the circuit is arranged.

In Figure 30 the circuit is referenced to ground, while in Figure 31 the circuit is biased to the positive supply. These configurations implement the half-wave rectifier because the LMV61x can not respond to one-half of the incoming waveform. It can not respond to one-half of the incoming because the amplifier can not swing the output beyond either rail. Therefore, the output disengages during this half cycle. During the other half cycle, however, the amplifier achieves a half wave that can have a peak equal to the total supply voltage. R_I must be large enough not to load the LMV61x.

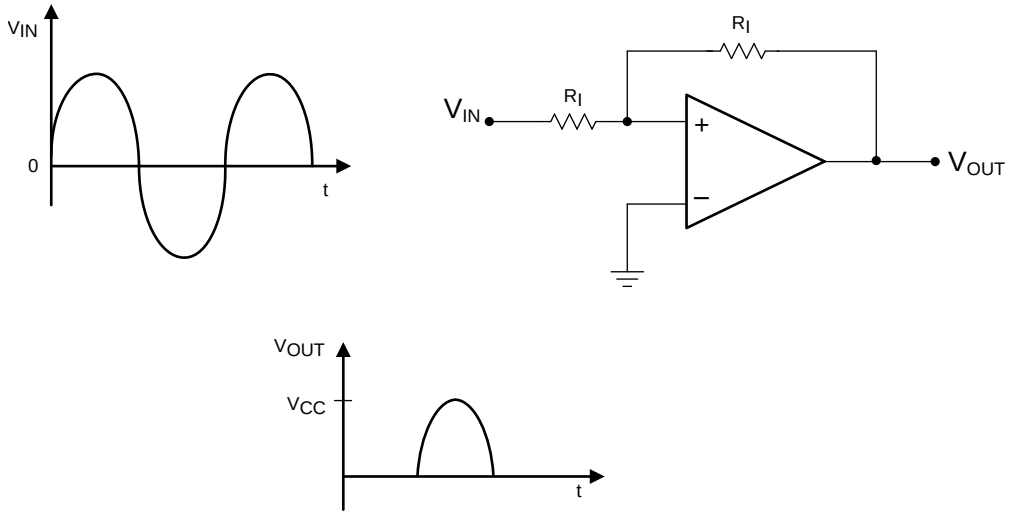


Figure 30. Half-Wave Rectifier With Rail-to-Ground Output Swing Referenced to Ground

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Application Information (continued)

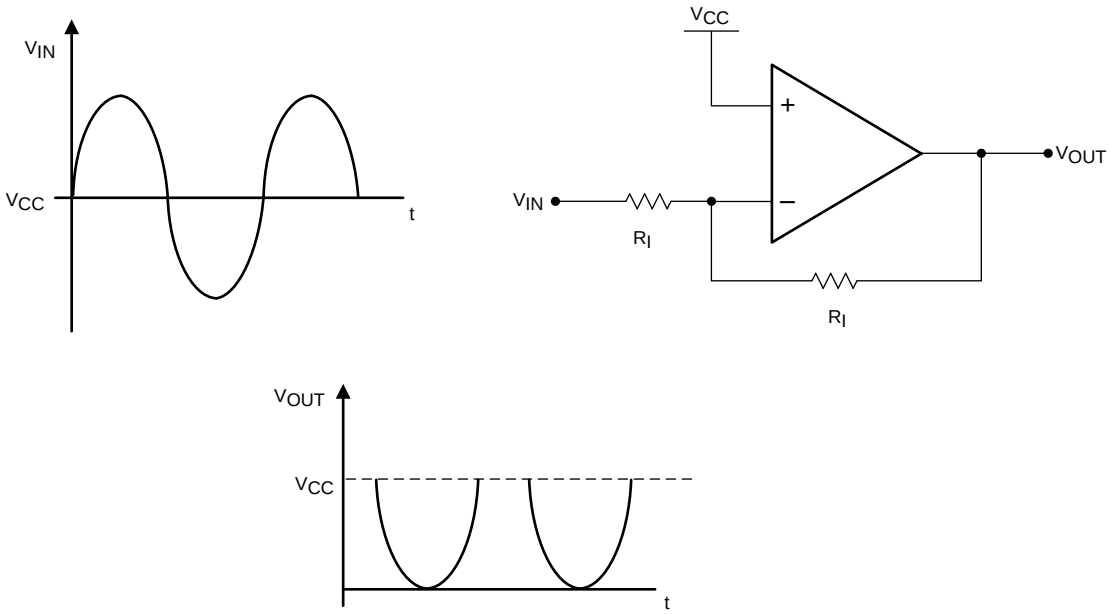


Figure 31. Half-Wave Rectifier With Negative-Going Output Referenced to V_{CC}

8.1.2 Instrumentation Amplifier With Rail-to-Rail Input and Output

Some manufactures make rail-to-rail op amps out of op amps that are otherwise non-rail-to-rail by using a resistive divider on the inputs. The resistors divide the input voltage to get a rail-to-rail input range. The problem with this method is that it also divides the signal, so to get the obtained gain, the amplifier must have a higher closed-loop gain. This raises the noise and drift by the internal gain factor and lowers the input impedance. Any mismatch in these precision resistors reduces the CMRR, as well. The LMV61x is rail-to-rail and therefore doesn't have these disadvantages.

Using three of the LMV61x amplifiers, an instrumentation amplifier with rail-to-rail inputs and outputs can be made as shown in Figure 32.

In this example, amplifiers on the left side act as buffers to the differential stage. These buffers assure that the input impedance is very high and require no precision matched resistors in the input stage. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMRR set by the matching R_1-R_2 with R_3-R_4. The gain is set by the ratio of R_2/R_1 and R_3 must equal R_1 and R_4 equal R_2. With both rail-to-rail input and output ranges, the input and output are only limited by the supply voltages. Remember that even with rail-to-rail outputs, the output can not swing past the supplies so the combined common-mode voltages plus the signal must not be greater that the supplies or limiting occurs.

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Application Information (continued)

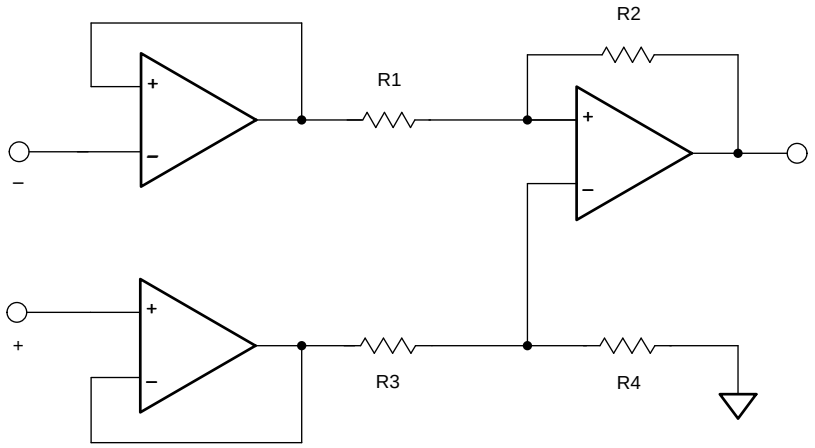
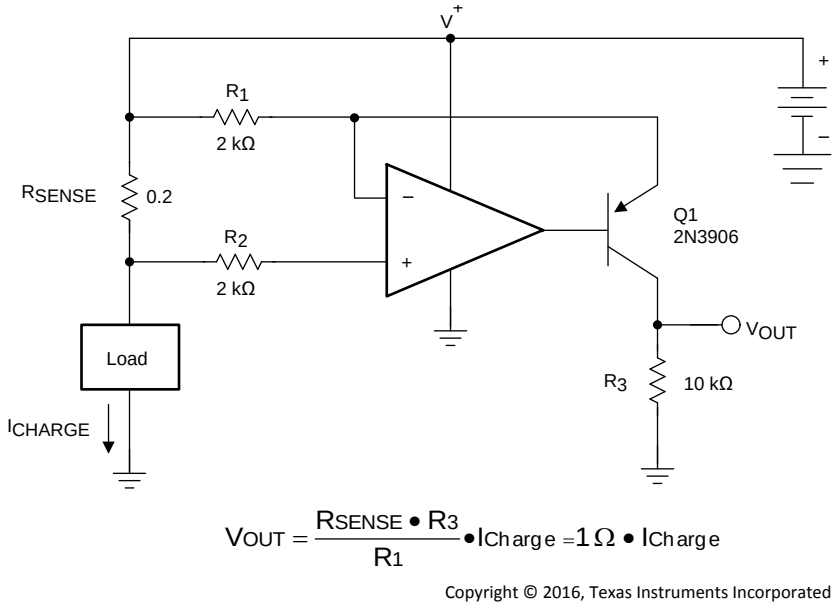


Figure 32. Rail-to-Rail Instrumentation Amplifier

8.2 Typical Applications

8.2.1 High-Side Current Sensing



$$V_{OUT} = \frac{R_{SENSE} \bullet R3}{R1} \bullet I_{Charge} = 1\,\Omega \bullet I_{Charge}$$

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Figure 33. High-Side, Current-Sensing Schematic

8.2.1.1 Design Requirements

The high-side, current-sensing circuit (Figure 33) is commonly used in a battery charger to monitor charging current to prevent overcharging. A sense resistor R_{SENSE} is connected to the battery directly. This system requires an op amp with rail-to-rail input. The LMV61x are ideal for this application because its common-mode input range goes up to the rail.

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Typical Applications (continued)

8.2.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMV61x devices with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2 Detailed Design Procedure

As seen in (Figure 33), the I_{CHARGE} current flowing through sense resistor R_{SENSE} develops a voltage drop equal to V_{SENSE}. The voltage at the negative sense point is now less than the positive sense point by an amount proportional to the V_{SENSE} voltage.

The low-bias currents of the LMV61x cause little voltage drop through R_2, so the negative input of the LMV61x amplifier is at essentially the same potential as the negative sense input.

The LMV61x detects this voltage error between its inputs and servo the transistor base to conduct more current through Q1, increasing the voltage drop across R_1 until the LMV61x inverting input matches the noninverting input. At this point, the voltage drop across R_1 now matches V_{SENSE}.

I_G, a current proportional to I_{CHARGE}, flows according to Equation 1.

$$I_G = V_{RSENSE} / R_1 = (R_{SENSE} \times I_{CHARGE}) / R_1 \quad (1)$$

I_G also flows through the gain resistor R_3 developing a voltage drop equal to Equation 2.

$$V_3 = I_G \times R_3 = (V_{RSENSE} / R_1) \times R_3 = ((R_{SENSE} \times I_{CHARGE}) / R_2) \times R_3 \quad (2)$$

$$V_{OUT} = (R_{SENSE} \times I_{CHARGE}) \times G$$

where

- $G = R_3 / R_1$ (3)

The other channel of the LMV61x may be used to buffer the voltage across R3 to drive the following stages.

8.2.1.2.1 Application Curve

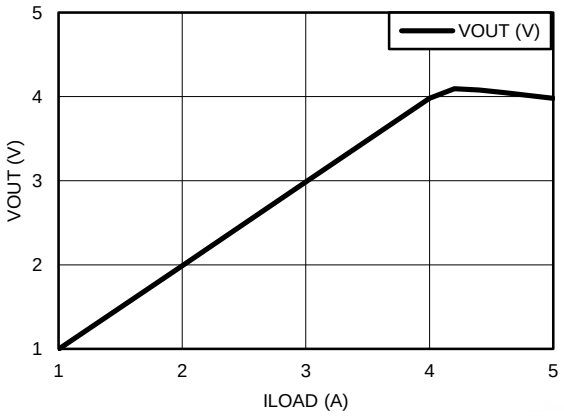


Figure 34. High-Side, Current-Sensing Results

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9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines, TI recommends that 10-nF capacitors be placed as close as possible to the op amp power supply pins. For single-supply, place a capacitor between V^+ and V^- supply leads. For dual supplies, place one capacitor between V^+ and ground, and one capacitor between V^- and ground.

10 Layout

10.1 Layout Guidelines

To properly bypass the power supply, several locations on a printed-circuit board must be considered. A 6.8-µF or greater tantalum capacitor must be placed at the point where the power supply for the amplifier is introduced onto the board. Another 0.1-µF ceramic capacitor must be placed as close as possible to the power supply pin of the amplifier. If the amplifier is operated in a single power supply, only the V^+ pin must be bypassed with a 0.1-µF capacitor. If the amplifier is operated in a dual power supply, both V^+ and V^- pins must be bypassed.

It is good practice to use a ground plane on a printed-circuit board to provide all components with a low inductive ground connection.

TI recommends surface-mount components in 0805 size or smaller in the LMV611-N application circuits. Designers can take advantage of the VSSOP miniature sizes to condense board layout to save space and reduce stray capacitance.

10.2 Layout Example

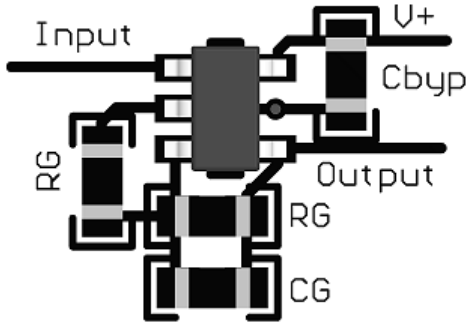


Figure 35. SOT-23 Layout Example

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For development support see the following:

- LMV611 SPICE Model
- LMV612 SPICE Model
- LMV614 SPICE Model
- SPICE-based analog simulation program, TINA-TI
- DIP adapter evaluation module, DIP Adapter EVM
- TI universal operational amplifier evaluation module, Op Amp EVM
- TI software, FilterPro

11.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMV61x devices with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Absolute Maximum Ratings for Soldering*
- *AN-29 IC Op Amp Beats FETs on Input Current*
- *AN-31 Op Amp Circuit Collection*
- *AN-71 Micropower Circuits Using the LM4250 Programmable Op Amp*
- *AN-127 LM143 Monolithic High Voltage Operational Amplifier Applications*

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV611	Click here	Click here	Click here	Click here	Click here
LMV612	Click here	Click here	Click here	Click here	Click here
LMV614	Click here	Click here	Click here	Click here	Click here

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11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.6 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV611MF/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AE9A
LMV611MF/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AE9A
LMV611MFX/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AE9A
LMV611MFX/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AE9A
LMV611MG/NOPB	Active	Production	SC70 (DCK) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AVA
LMV611MG/NOPB.A	Active	Production	SC70 (DCK) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AVA
LMV611MGX/NOPB	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AVA
LMV611MGX/NOPB.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AVA
LMV612MA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV6 12MA
LMV612MA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV6 12MA
LMV612MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV6 12MA
LMV612MAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV6 12MA
LMV612MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	AD9A
LMV612MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AD9A
LMV612MMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	AD9A
LMV612MMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AD9A
LMV614MA/NOPB	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV614MA
LMV614MA/NOPB.A	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV614MA
LMV614MAX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV614MA
LMV614MAX/NOPB.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV614MA
LMV614MT/NOPB	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LMV61 4MT
LMV614MT/NOPB.A	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV61 4MT
LMV614MTX/NOPB	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LMV61 4MT

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV614MTX/NOPB.A	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV61 4MT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

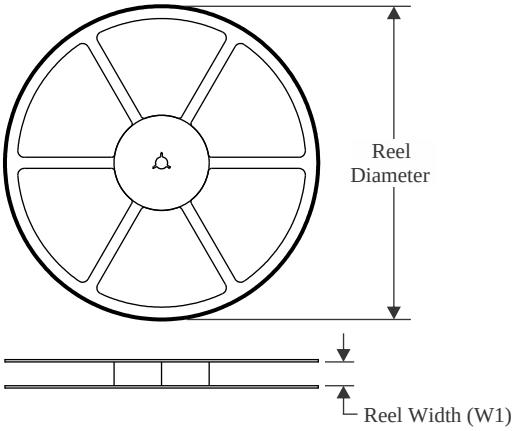
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

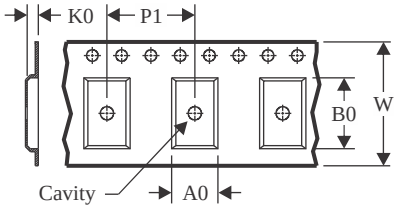
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

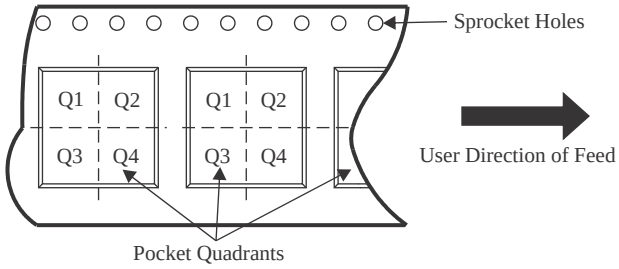


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

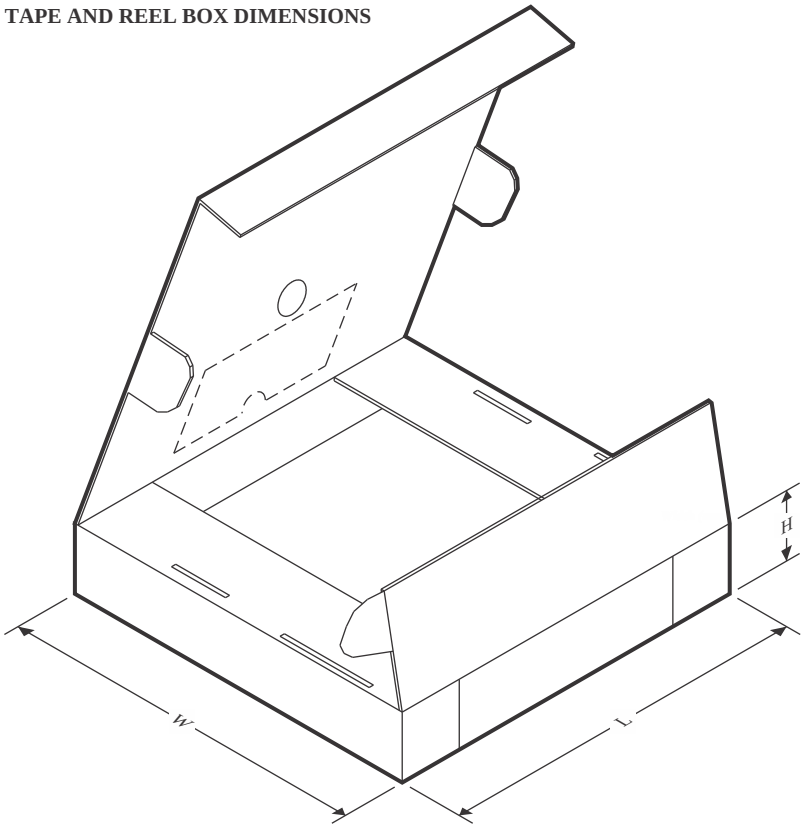
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV611MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV611MF/NOPB	SOT-23	DBV	5	1000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV611MFX/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV611MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV611MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV611MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV612MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV612MM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV612MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV614MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMV614MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV614MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

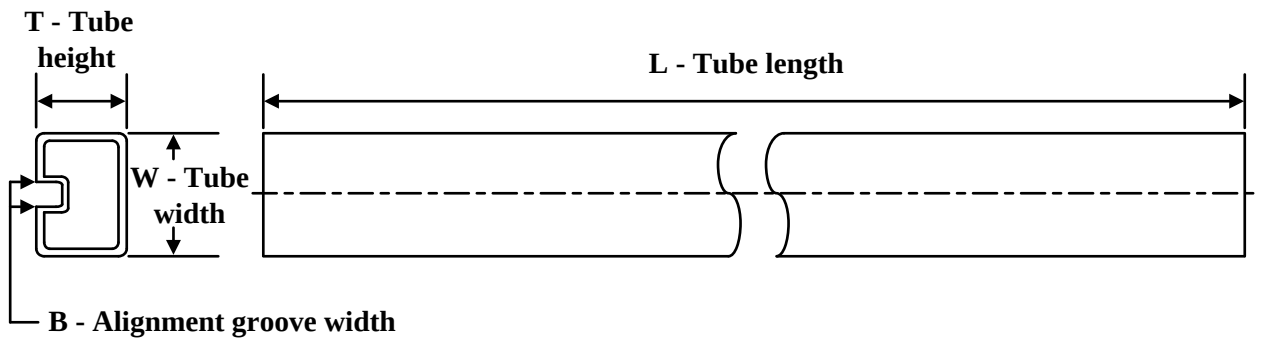
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV611MF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV611MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV611MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV611MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMV611MG/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
LMV611MGX/NOPB	SC70	DCK	5	3000	208.0	191.0	35.0
LMV612MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV612MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMV612MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV614MAX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMV614MTX/NOPB	TSSOP	PW	14	2500	353.0	353.0	32.0
LMV614MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

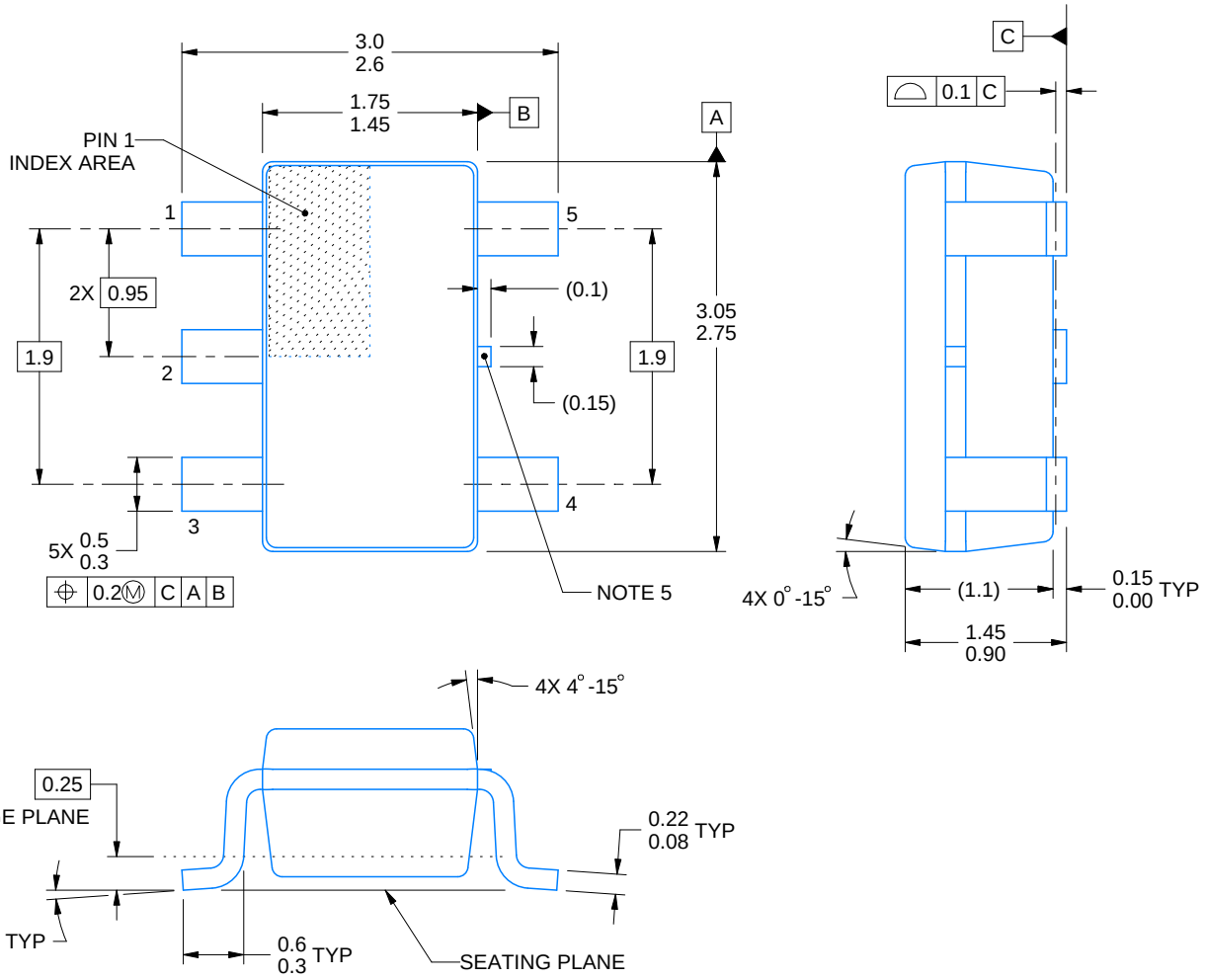
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMV612MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMV612MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LMV614MA/NOPB	D	SOIC	14	55	495	8	4064	3.05
LMV614MA/NOPB.A	D	SOIC	14	55	495	8	4064	3.05
LMV614MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06
LMV614MT/NOPB	PW	TSSOP	14	94	530	10.2	3600	3.5
LMV614MT/NOPB.A	PW	TSSOP	14	94	530	10.2	3600	3.5
LMV614MT/NOPB.A	PW	TSSOP	14	94	495	8	2514.6	4.06

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

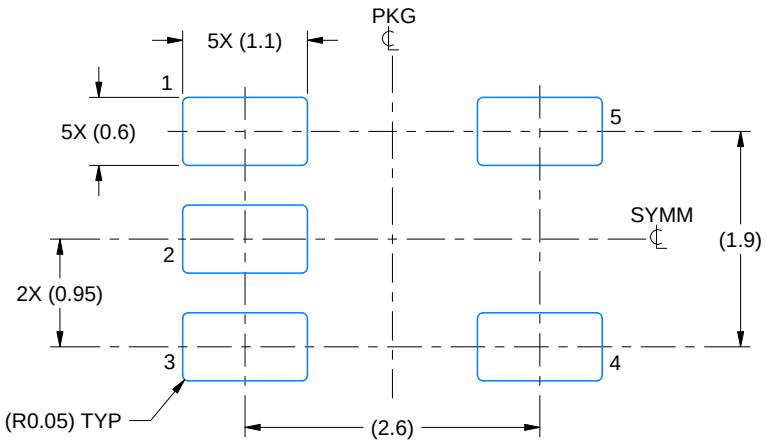
SMALL OUTLINE TRANSISTOR



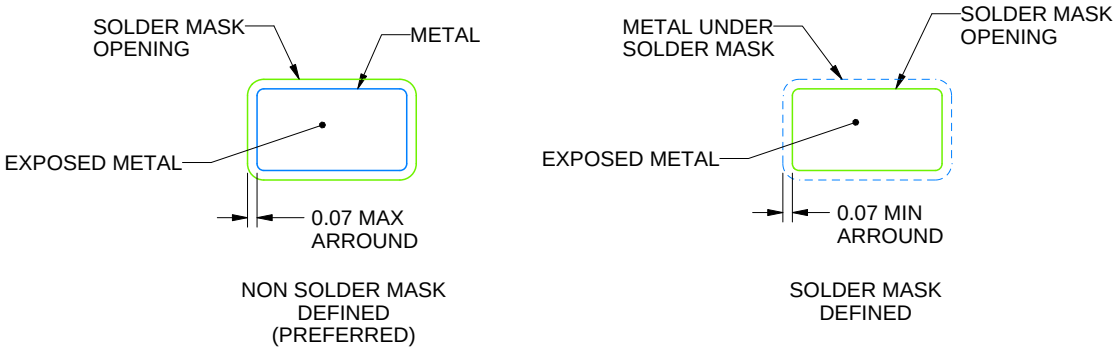
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

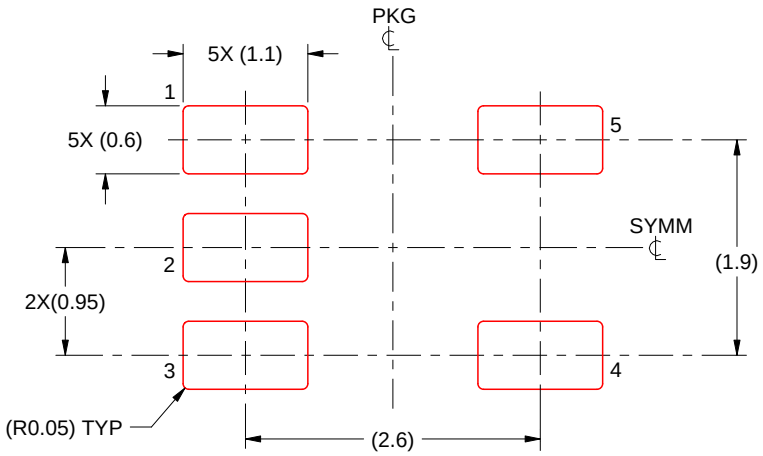


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

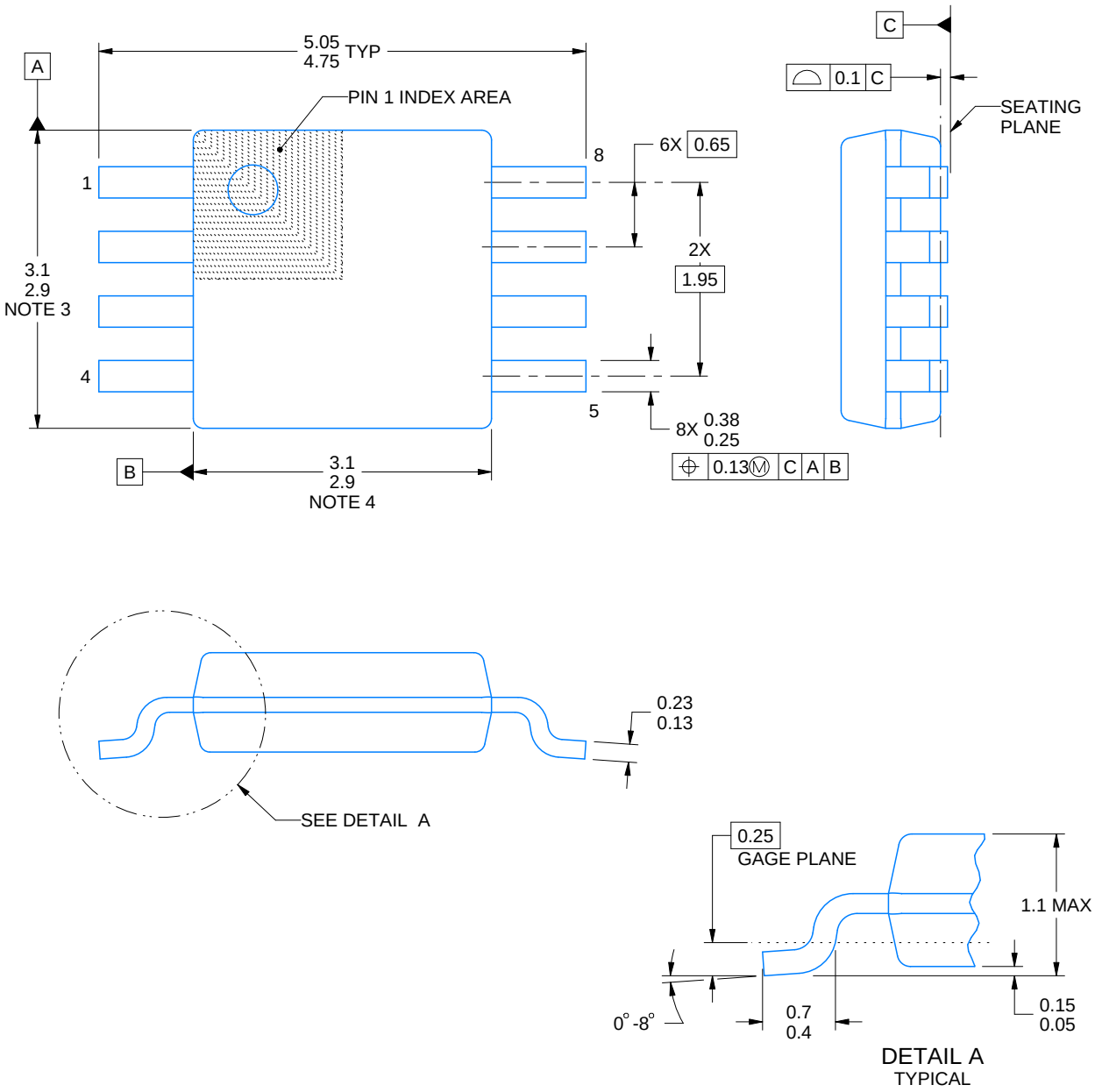
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

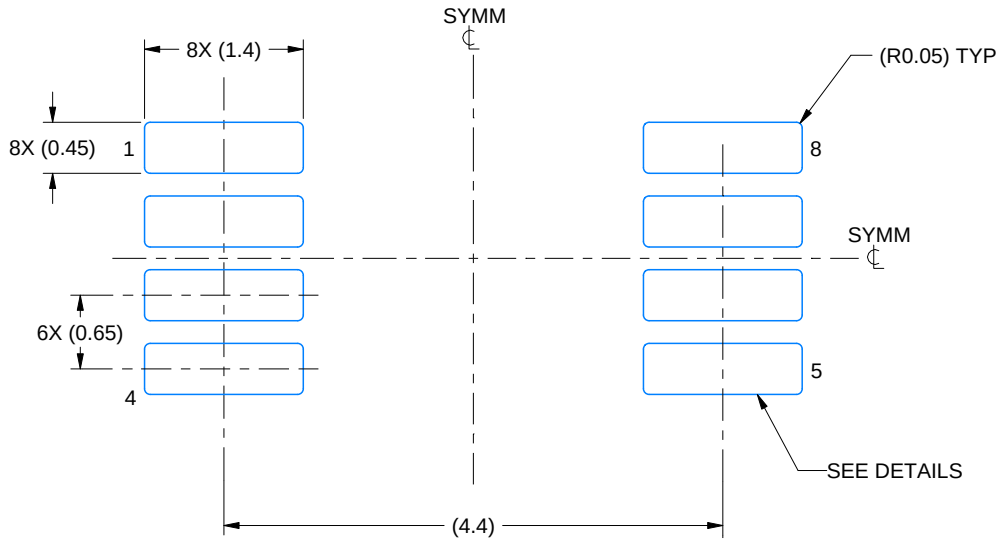
SMALL OUTLINE PACKAGE



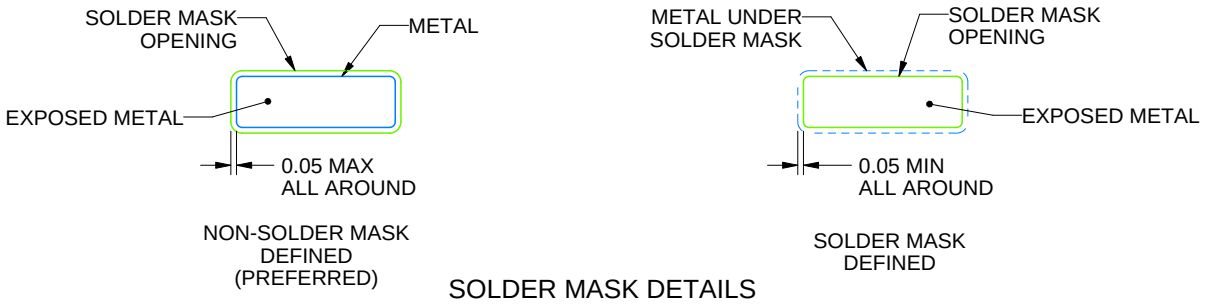
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

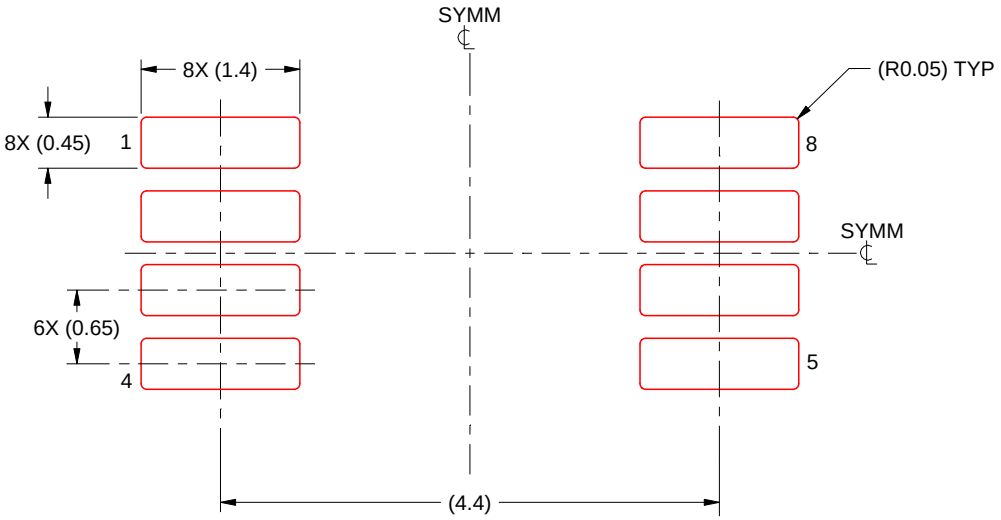


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

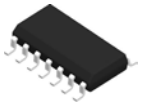


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

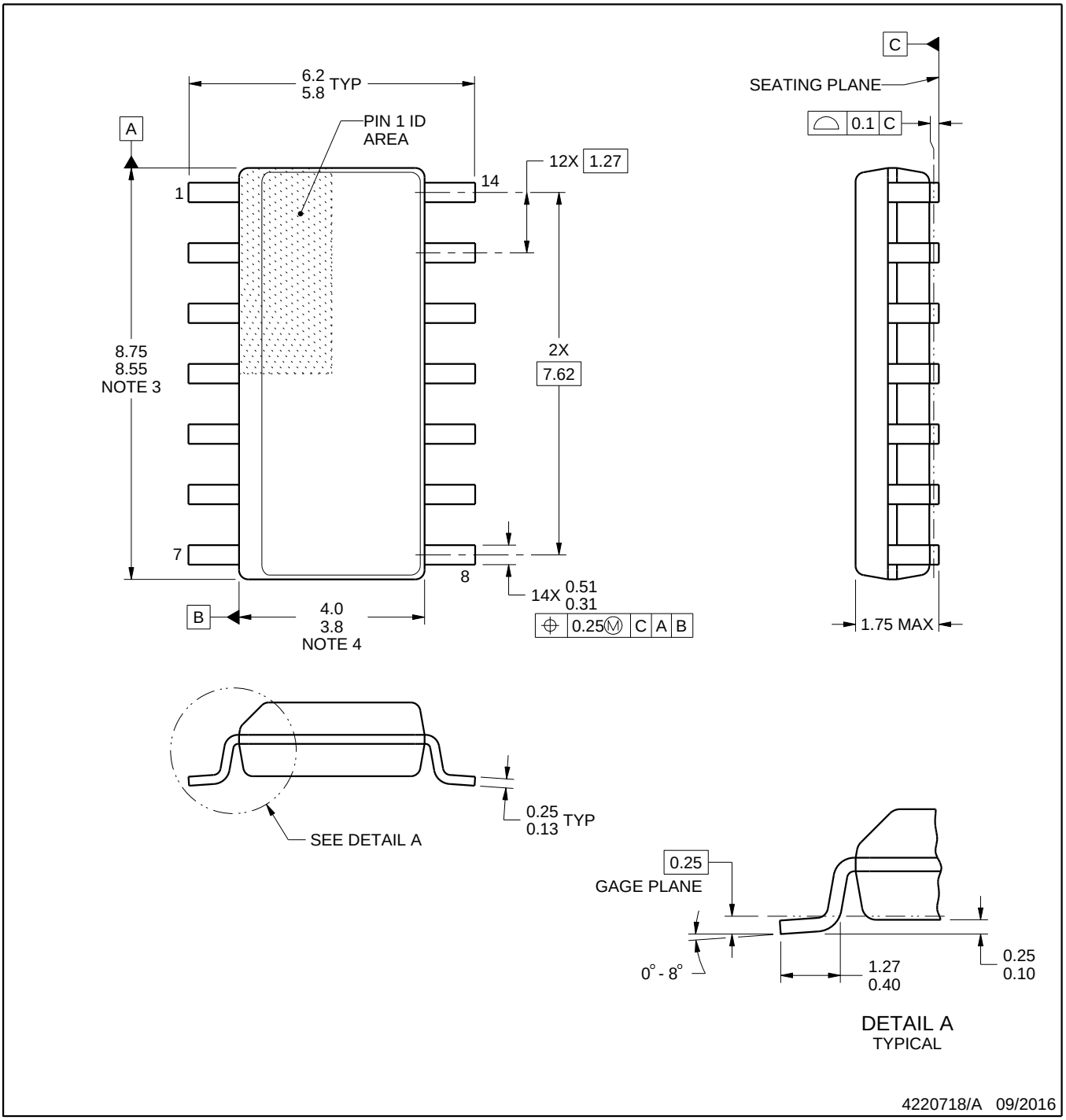


PACKAGE OUTLINE

D0014A

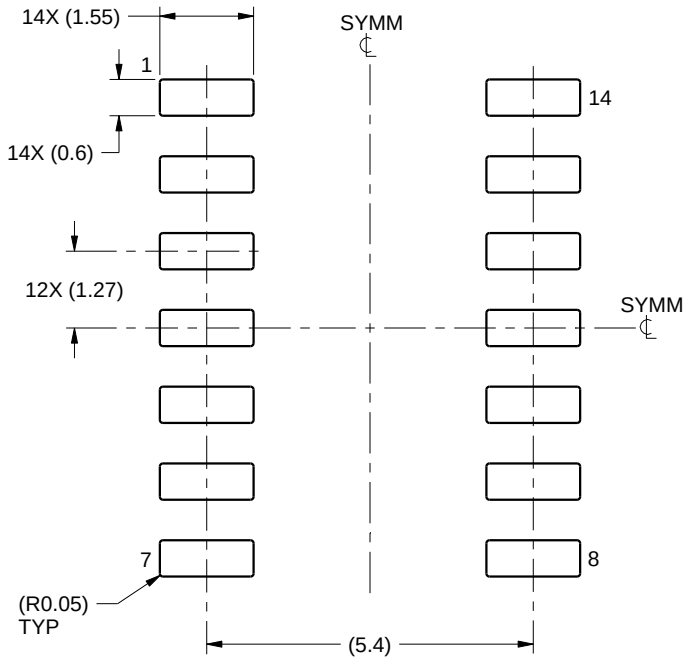
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

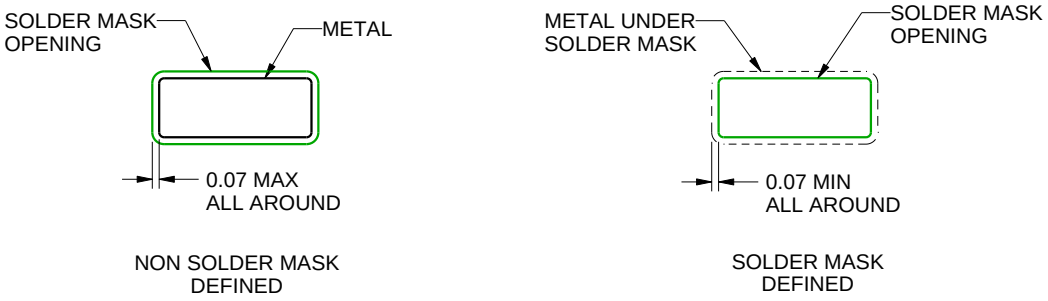


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

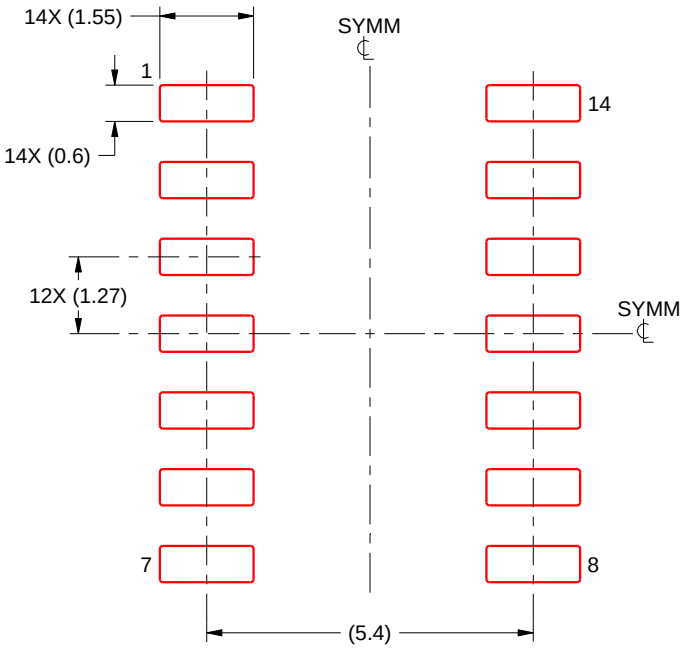
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

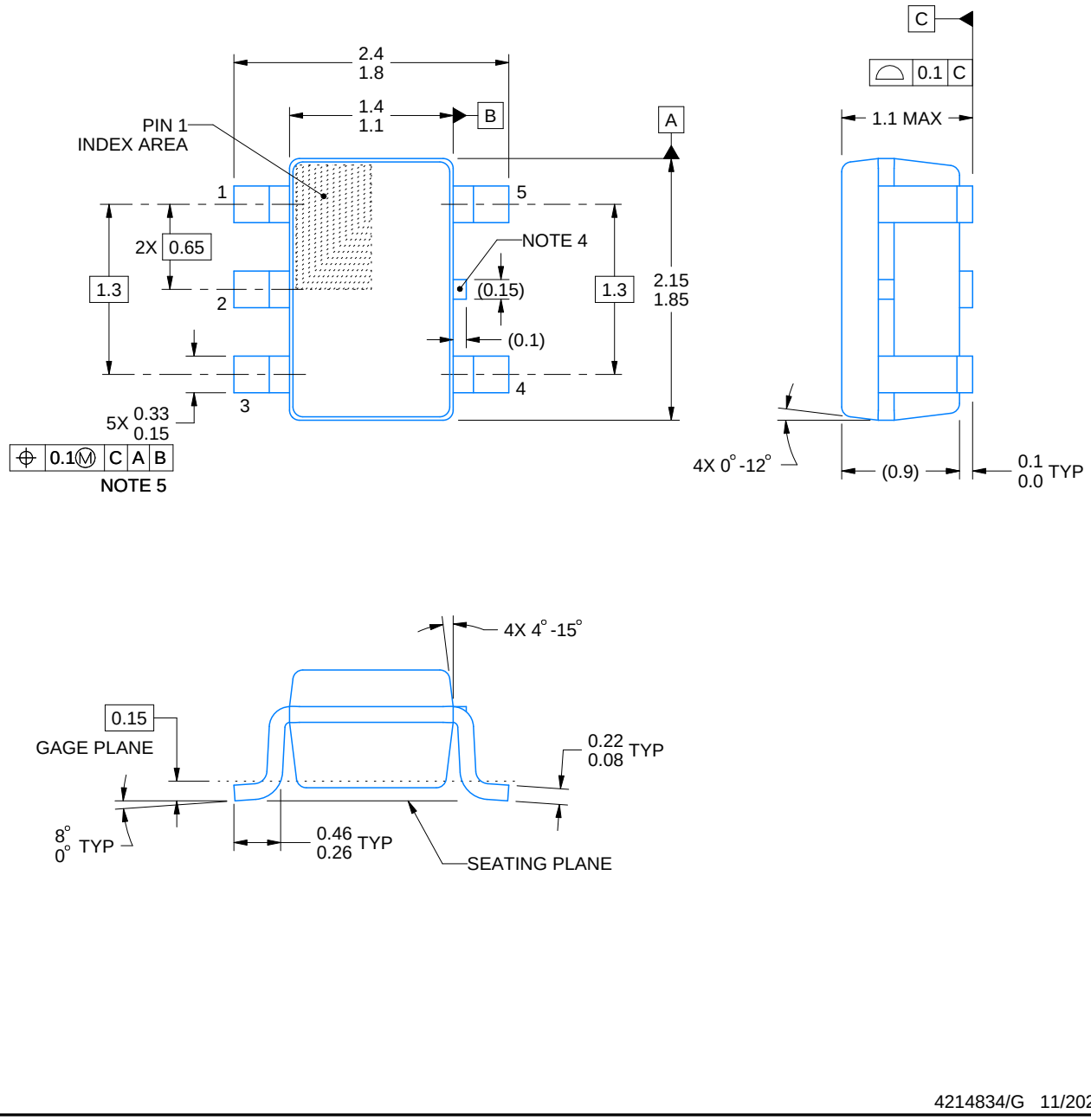
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

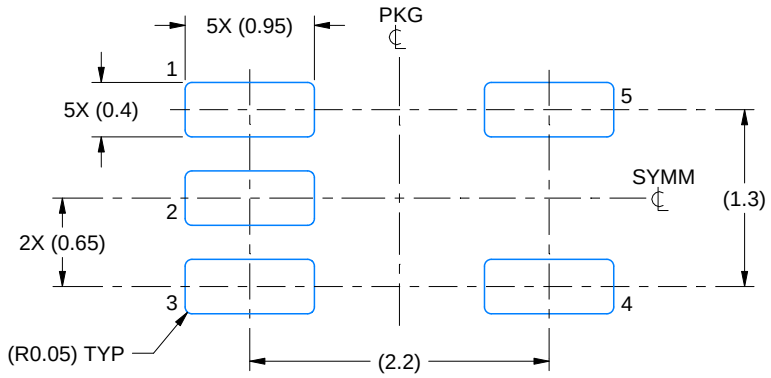
SMALL OUTLINE TRANSISTOR



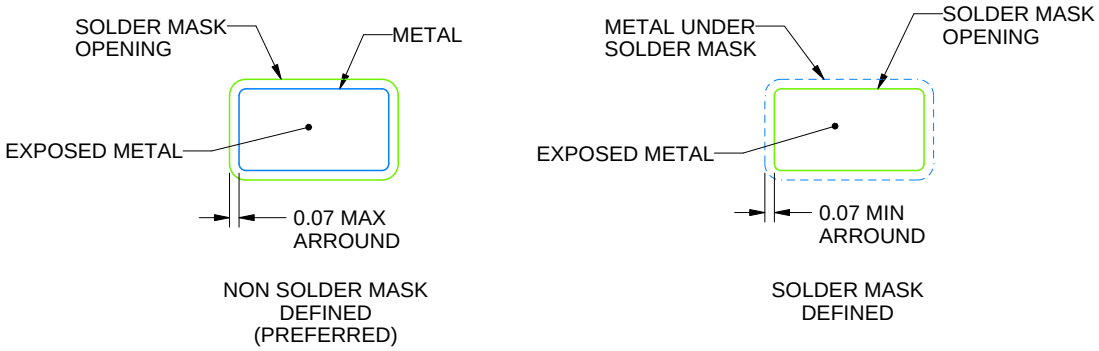
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

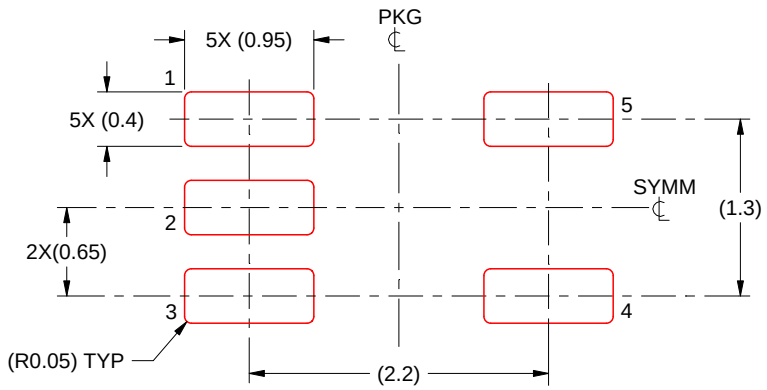


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

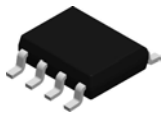


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

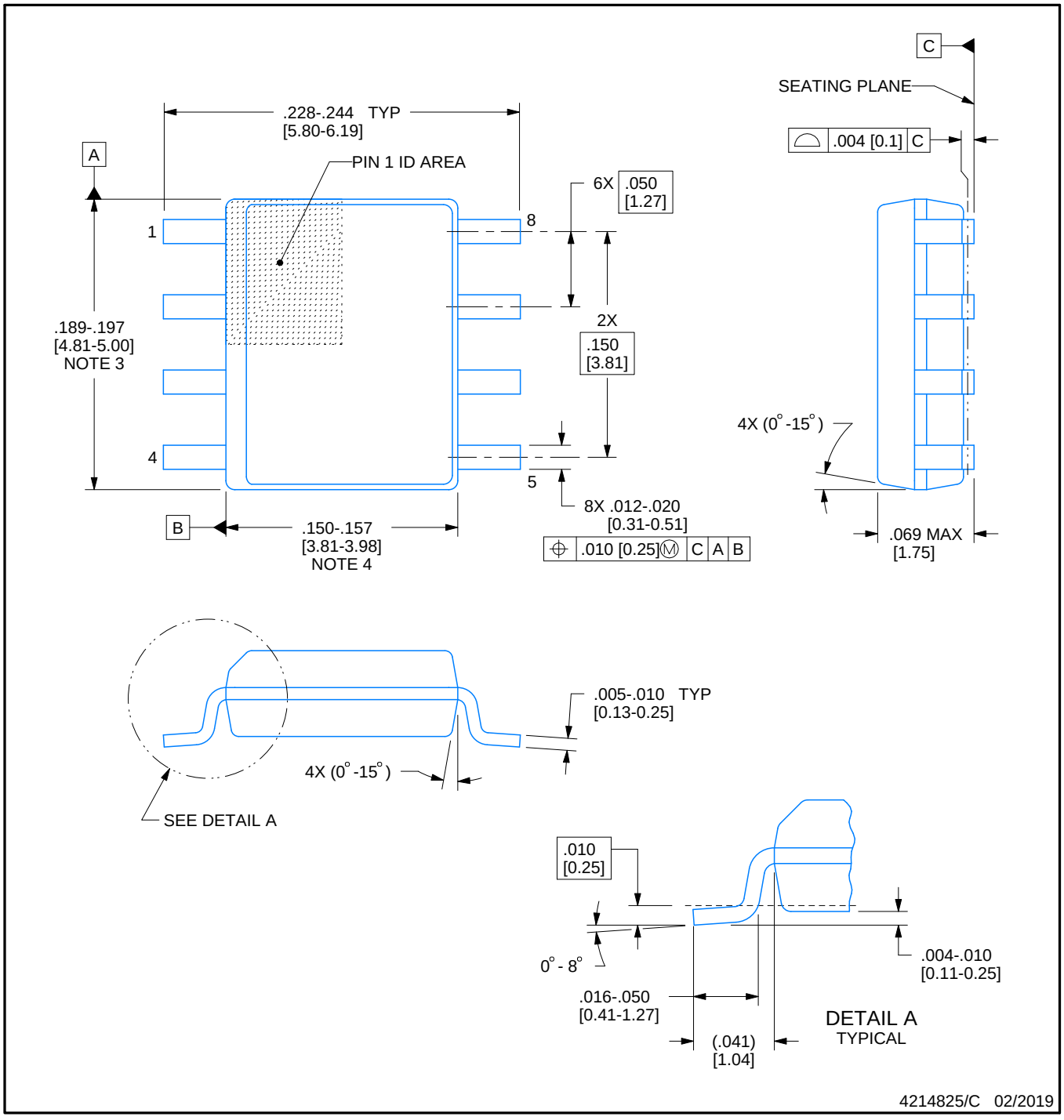


PACKAGE OUTLINE

D0008A

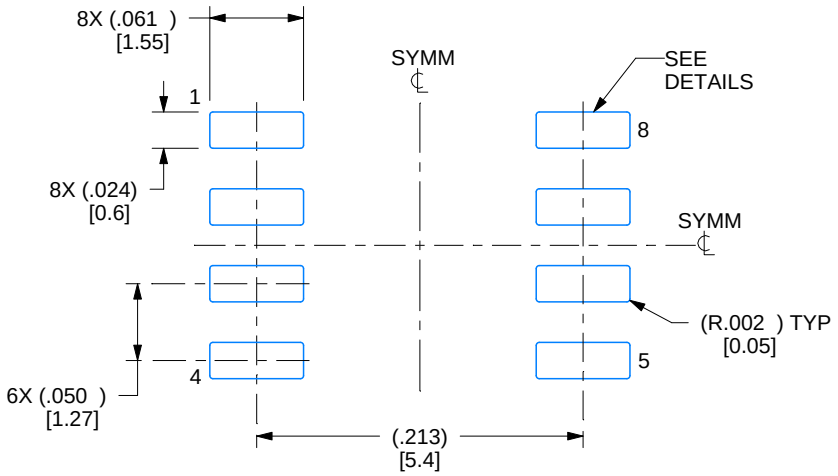
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

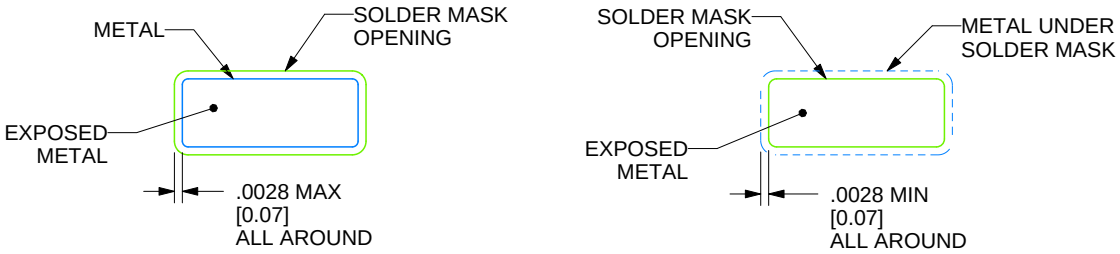


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

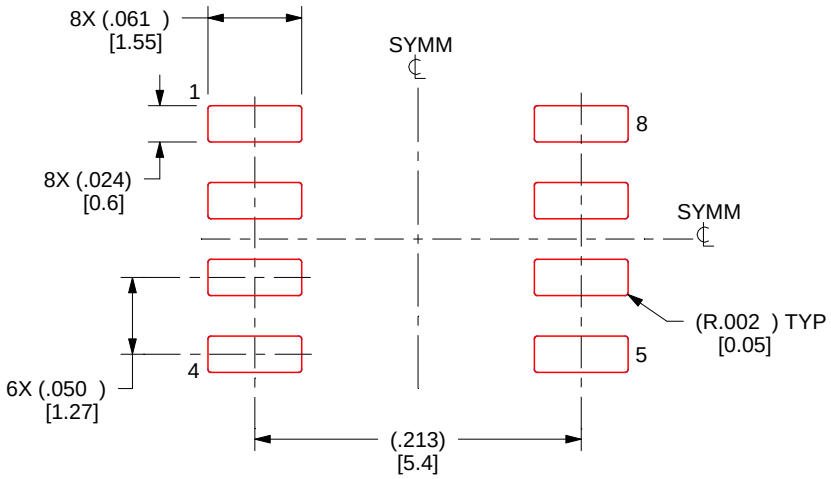
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

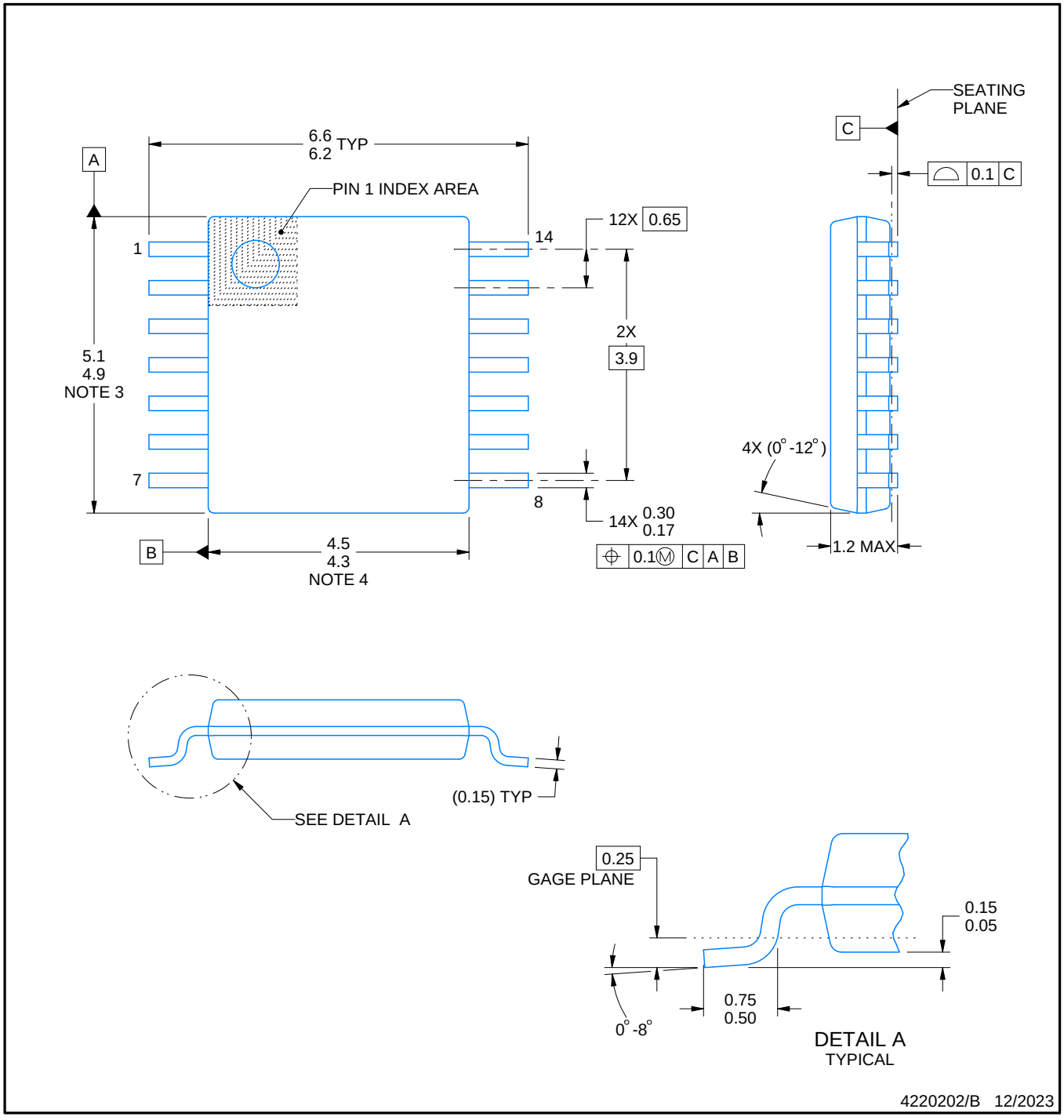
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

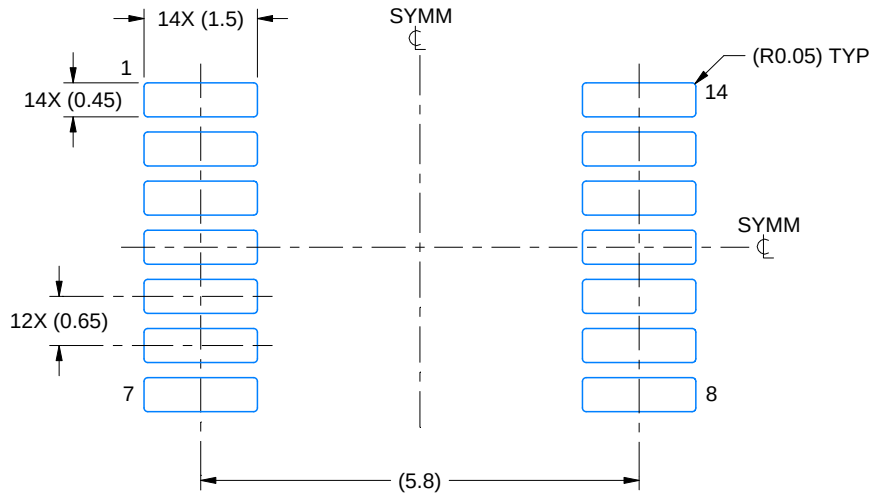
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

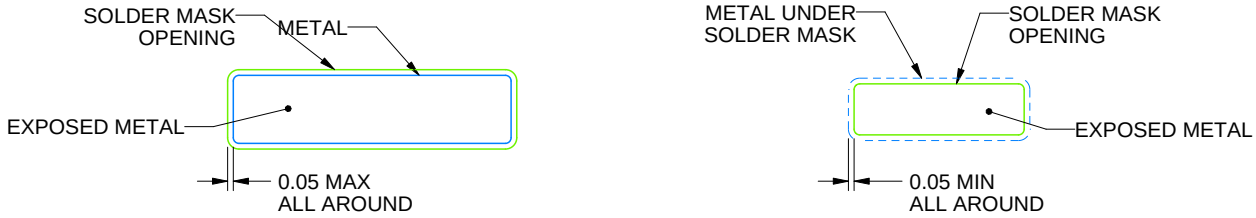


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

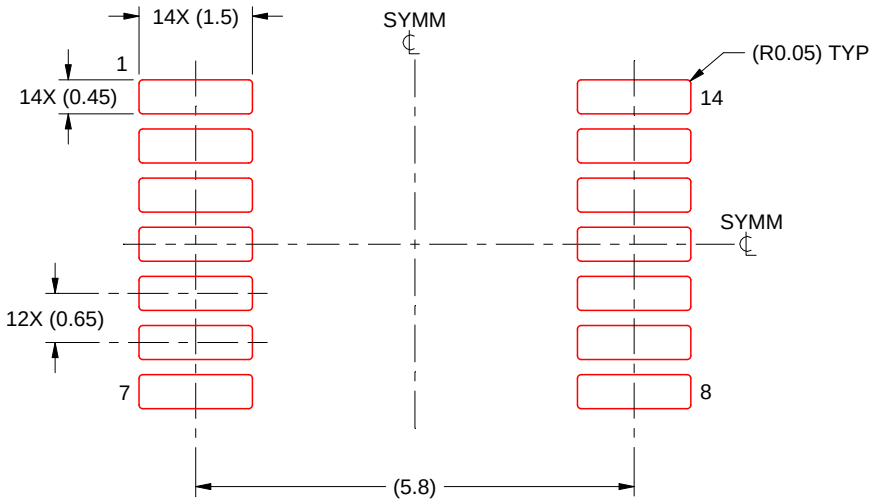


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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