LMX5453 Micro-Module Integrated Bluetooth®2.0 Baseband Controller and Radio

Check for Samples: LMX5453

FEATURES

The LMX5453 is a drop in replacement for the LMX5452. The LMX5453 has new features added:

- **eSCO**
- **eSCO over USB HCI transport**
- **Enhanced scatternet**
- **Interlaced scan**
- **Flushing**
- **Audio PCM slave mode support**
- **Generic PCM configuration**
- **Compliant with the Bluetooth 2.0 Core Specification**
- **Better than -80 dBm input sensitivity**
- **Class 2 operation**
- **Low power consumption:**
- **Accepts external clock or crystal input:**
  - **Clocking option 12/13 MHz with PLL bypass mode for power reduction**
  - **10-20 MHz external clock or crystal network**
  - **Secondary 32.768 kHz oscillator for low-power modes**
  - **Advanced power management features**
- **High integration:**
  - **Implemented in 0.18 µm CMOS technology**
  - **RF includes on-chip antenna filter and switch**
- **On-chip firmware with complete HCI**
- **Embedded ROM (200K) and Patch RAM (16.6K) memory**
- **Up to 7 Asynchronous Connection Less (ACL) links**
- **Support for two simultaneous voice or Extended Synchronous Connection Oriented (eSCO) and Synchronous Connection Oriented (SCO) and links.**
- **Enhanced scatternet**
- **Interlaced scan**
- **Flushing**
- **Audio PCM slave mode support**
- **Generic PCM configuration**
- **Fractional-N Sigma/Delta modulator**
- **Operating voltage range 2.5–3.6V**
- **I/O voltage range 1.6–3.6V**
- **60-pad micro-module BGA package (6.1 mm × 9.1 mm × 1.2 mm)**

APPLICATIONS

- **Mobile Handsets**
- **USB Dongles**
- **Stereo Headsets**
- **Personal Digital Assistants**
- **Personal Computers**
- **Automotive Telematics**

DESCRIPTION

The LMX5453 is a highly integrated Bluetooth 2.0 compliant solution. The integrated baseband controller and 2.4 GHz radio combine to form a complete, small form-factor (6.1 mm × 9.1 mm × 1.2 mm) Bluetooth node.

The on-chip memory, ROM, and Patch RAM provide lowest cost and minimize design risk with the flexibility of firmware upgrades.

The firmware supplied in the on-chip ROM supports a complete Bluetooth Link Manager and HCI with communication through a UART or USB interface. This firmware features point-to-point and point-to-multipoint link management, supporting data rates up to 723 kbps.

The radio employs an integrated antenna filter and switch to minimize the number of external components.

The radio has a heterodyne receiver architecture with a low intermediate frequency (IF), which enables the IF filters to be integrated on-chip. The transmitter uses direct IQ-modulation with Gaussian-filtered bit-stream data, a voltage-controlled oscillator (VCO) buffer, and a power amplifier.

The LMX5453 module is lead free and RoHS (Restriction of Hazardous Substances) compliant. For more information on those quality standards, please visit our green compliance website at ** http://www.national.com/quality/green/

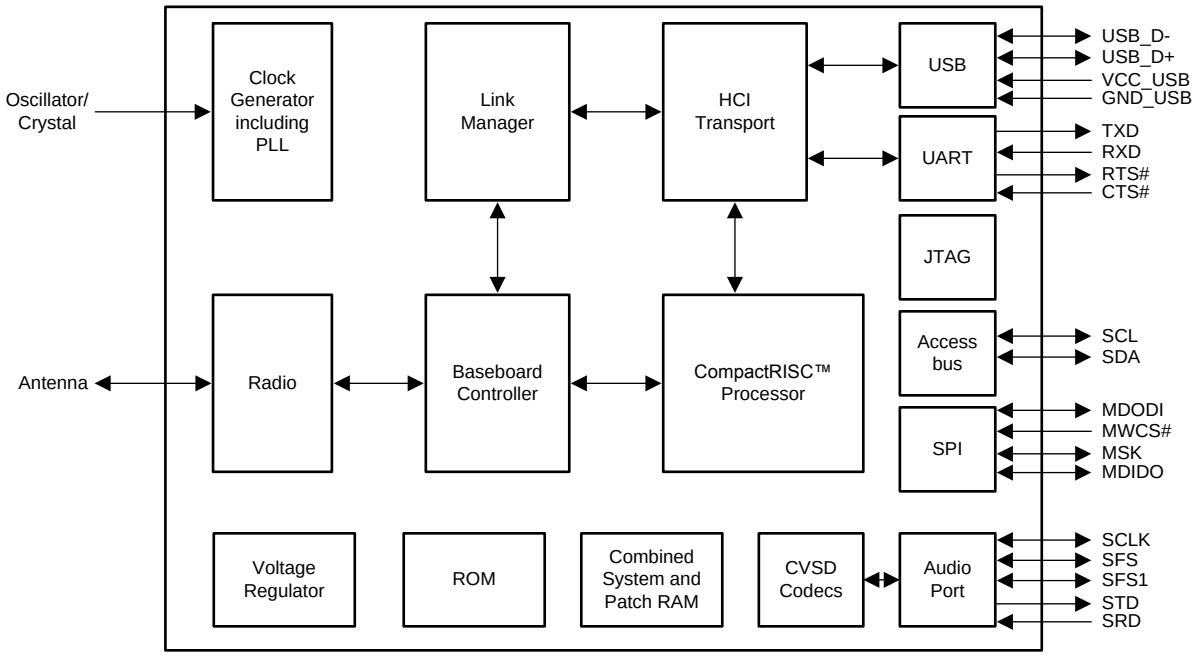
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Functional Block Diagram



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

INTERFACES

- **Full-duplex UART supporting transfer rates up to 921.6 kbps including baud rate detection for HCI**
- **Full speed (12 Mbps) USB 2.0 for HCI**
- **ACCESS.bus and SPI/Microwire for interfacing with external non-volatile memory**
- **Advanced Audio Interface (AAI) for interfacing with external 8-kHz PCM codec**
- **Up to 3 GPIO port pins (OP4/PG4, PG6, PG7) controllable by HCI commands**
- **JTAG based serial on-chip debug interface**
- **Single Rx/Tx-pad radio interface**

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CONNECTION DIAGRAM

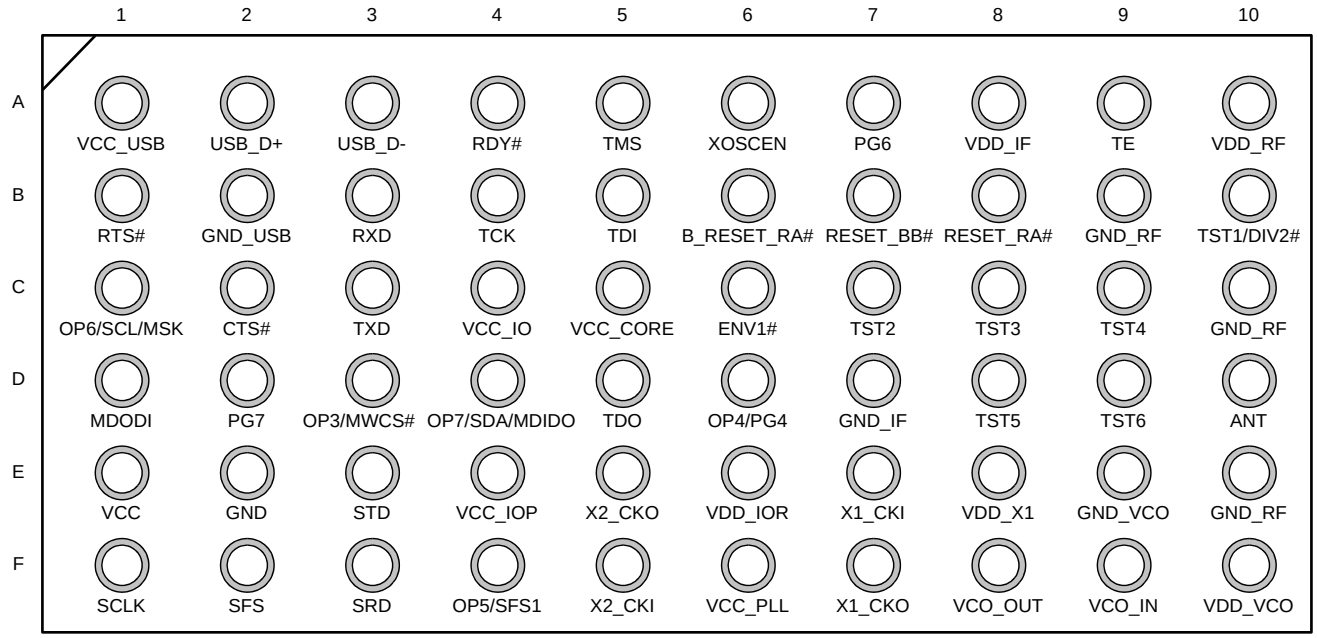


Figure 1. X-ray - Top View

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SIGNAL DESCRIPTIONS

Table 1. Signal Descriptions

Pad Name	Pad Location	Type	Default Layout	Description
X1_CKO	F7	O		Crystal 10-20 MHz
X1_CKI	E7	I		Crystal or External Clock 10-20 MHz
X2_CKI	F5	I	GND **(if not used)**	32.768 kHz Crystal Oscillator
X2_CKO	E5	O	NC **(if not used)**	32.768 kHz Crystal Oscillator
RESET_RA#	B8	I		Radio Reset Input (active low)
B_RESET_RA#	B6	O		Buffered Radio Reset Output (active low)
RESET_BB#	B7	I		Baseband Controller Reset (active low)
ENV1	C6	I	NC	ENV1: Environment Select used for manufacturing test only
TE	A9	I	GND	Test Enable - Used for manufacturing test only
TST1/DIV2#	B10	I	NC	TST1: Test Mode. Leave not connected to permit use with VTune automatic tuning algorithm. DIV2#: No longer supported
TST2	C7	I	GND	Test Mode, Connect to GND
TST3	C8	I	GND	Test Mode, Connect to GND
TST4	C9	I	GND	Test Mode, Connect to GND
TST5	D8	I	GND	Test Mode, Connect to GND
TST6	D9	I	VCO_OUT	Test Input, Connect to VCO_OUT through a zero-ohm resistor to permit use with VTune automatic tuning algorithm
USB_D-	A3	I		USB Data (negative)
USB_D+	A2	I		USB Data (positive)
MDODI(1)	D1	I/O		SPI Master Data Out/Slave Data In
OP6/SCL/MSK	C1	**OP6: I** **SCL/MSK:** I/O	See Table 20	**OP6:** Pin checked during the start-up sequence for configuration option **SCL:** ACCESS.Bus Clock **MSK:** SPI Shift
OP7/SDA/MDIDO	D4	**OP7: I** **SDA/MDIDO:** I/O	See Table 20	**OP7:** Pin checked during the start-up sequence for configuration option **SDA:** ACCESS.Bus Serial Data **MDIDO:** SPI Master Data In/Slave Data Out
OP3/MWCS#	D3	I	See Table 20 and Table 21	**OP3:** Pin checked during the start-up sequence for configuration option **MWCS#:** SPI Slave Select Input (active low)
OP4/PG4	D6	**OP4: I** **PG4:** I/O	See Table 20 and Table 21	**OP4:** Pin checked during the start-up sequence for configuration option **PG4:** GPIO
OP5/SFS1	F4	I/O	See Table 20 and Table 21	**OP5:** Pin checked during the start-up sequence for configuration option **SFS1:** Audio PCM Interface - Frame Synchronization for second codec
SCLK	F1	I/O		Audio PCM Interface Clock
SFS	F2	I/O		Audio PCM Interface Frame Synchronization
SRD	F3	I		Audio PCM Interface Receive Data Input
STD	E3	O		Audio PCM Interface Transmit Data Output
XOSCEN	A6	O		Clock Request. Toggles with X2 (LP0) crystal enable/disable
PG6	A7	O	See NVS Table 21	GPIO - Default setup USB status indication
PG7	D2	O	See NVS Table 21	GPIO - Default setup TL (Transport Layer) traffic LED indication

(1) Must use 1k ohm pull up

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Table 1. Signal Descriptions (continued)

Pad Name	Pad Location	Type	Default Layout	Description
CTS#(2)	C2	I	GND **(if not used)**	Host Serial Port Clear To Send (active low)
RXD	B3	I		Host Serial Port Receive Data
RTS#(3)	B1	O	NC **(if not used)**	Host Serial Port Request To Send (active low)
TXD	C3	O		Host Serial Port Transmit Data
RDY#	A4	I	NC	JTAG Ready Output (active low)
TCK	B4	I	NC	JTAG Test Clock Input
TDI	B5	I	NC	JTAG Test Data Input
TDO	D5	O	NC	JTAG Test Data Output
TMS	A5	I	NC	JTAG Test Mode Select Input
VCO_OUT	F8	O		Charge Pump Output, connect to loop filter
VCO_IN	F9	I		VCO Tuning Input, feedback from loop filter
ANT	D10	O		RF Antenna, 50-ohm nominal impedance
VCC_PLL	F6	O		1.8V Core Logic Power Supply Output
VCC_CORE	C5	O		1.8V Voltage Regulator Output
VDD_X1	E8	I		Power Supply Crystal Oscillator
VDD_VCO	F10	I		Power Supply VCO
VDD_RF	A10	I		Power Supply RF
VDD_IOR	E6	I		Power Supply I/O Radio/BB
VDD_IF	A8	I		Power Supply IF
VCC_USB	A1	I		Power Supply USB Transceiver
VCC_IOP	E4	I		Power Supply Audio Interface
VCC_IO	C4	I		Power Supply I/O
VCC	E1	I		Voltage Regulator Input
GND_VCO	E9			Ground
GND_USB	B2			Ground
GND_RF	B9, C10, E10			Ground
GND_IF	D7			Ground
GND	E2			Ground

(2) Connect to GND if CTS is not used
(3) Treat as No Connect if RTS is not used. Pad required for mechanical stability

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Electrical Specifications

Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. This device is ESD sensitive. Handling and assembly of this device should be performed at ESD-free workstations. All pads are rated 2 kV. This device operates between -40 and +85°C.

Absolute Maximum Ratings

	Parameter	Min	Max	Units
VCC	Power Supply Voltage	–0.2	4.0	V
V_I	Voltage on any pad with GND = 0V	–0.2	VCC + 0.2	V
VDD_RF	Supply Voltage Radio	0.2	3.3	V
VDD_IF				
VDD_X1				
VDD_VCO				
$P_{IN}RF$	RF Input Power		0	dBm
V_{ANT}	Applied Voltage to ANT pad		1.95	V
T_S	Storage Temperature Range	–65	+150	°C
T_L	Lead Temperature (1) (solder 4 sec)		225	°C
T_{LNOPB}	Lead Temperature NOPB (1)(2) (solder 40 sec)		260	°C
ESD_{HBM}	ESD - Human Body Model		2000	V
ESD_{MM}	ESD - Machine Model		200	V
ESD_{CDM}	ESD - Charged Device Model		1000	V

(1) Reference IPC/JEDEC J-STD-020C spec.
(2) NOPB = No Pb (No Lead)

Recommended Operating Conditions

	Parameter	Min	Typ	Max	Units
VCC	Module Power Supply Voltage	2.5	2.75	3.6	V
T_R	Module Power Supply Rise Time			10	µS
T_A	Ambient Opoerating Temperature Range Fully Functional Bluetooth Node	–40	+25	+85	°C
VCC_IO	Supply Voltage Digital I/O	1.6	3.3	3.6	V
VCC_USB	Supply Voltage USB	2.97	3.3	3.63	V
VCC_PLL	Internally connected to VCC_Core				
VDD_RF	Supply Voltage Radio	2.5	2.75	3.0	V
VDD_IF					
VDD_X1					
VDD_VCO					
VDD_IOR	Supply Voltage Radio I/O	1.6	2.75	VDD_RF	V
VCC_IOP	Supply Voltage PCM Interface	1.6	3.3	3.6	V
VCC_CORE	Supply Voltage Output		1.8		V
VCC_CORE_{MAX}	Supply Voltage Output Max Load		5		mA
VCC_CORE_{SHORT}	When used as supply input (VCC grounded)	1.6	1.8	2.0	V

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Power Supply Requirements(1)(2)

	Parameter	Min	Typ	Max	Units
I_{RXDM5}	During Receive DM5		26		mA
I_{TXDM5}	During Transmit DM5		27		mA
I_{RXDH5}	During Receive DH5		26		mA
I_{TXDH5}	During Transmit DH5		27		mA
I_{RXHV1}	During Receive HV1		12		mA
I_{TXHV1}	During Transmit HV1		12		mA
I_{CC-RX}	Receive Power Supply Current (Receive in Continuous Mode)			65	mA
I_{CC-TX}	Transmit Power Supply Current (Transmit in Continuous Mode)			65	mA
$I_{CC-PWDN}$	Power-down Current (Standby, XO off)		34		µA
I_{ACTIVE}	Active Mode - Page/Inquiry Scan Enabled		6		mA
I_{SNIFF}	Sniff Mode - Sniff Interval 1.28 sec.		5		mA

(1) Power supply requirements are based on Class 2 output power.
(2) VCC = 2.75V, T_A = +25°C

DC Characteristics

	Parameter	Condition	Min	Max	Units
V_{IH}	Logical 1 Input Voltage High (except oscillator I/O)	1.6V **≤ VCC_IO ≤ 3.0** **3.0V ≤ VCC_IO ≤ 3.6**	0.7 x VCC_IO 2.0	VCC_IO + 0.2 VCC_IO + 0.2	V
V_{IL}	Logical 1 Input Voltage Low (except oscillator I/O)	1.6V **≤ VCC_IO ≤ 3.0** **3.0V ≤ VCC_IO ≤ 3.6**	-0.2 -0.2	0.25 x VCC_IO 0.8	V
I_{OH}(1)	Logical 1 Output Current	V_{OH} = 2.4V, VCC_IO = 3.0V	-10		mA
I_{OL}(1)	Logical 0 Output Current	V_{OL} = 0.4V, VCC_IO = 3.0V	10		mA

(1) Maximum current is 50mA per VCC_IO/GND pair.

USB Transceiver

	Parameter	Condition	Min	Typ	Max	Units
VCC_USB	USB Power Supply Voltage		2.97	3.3	3.63	V
V_{DI}	Differential Input Sensitivity	(D+) - (D-)	-0.2		+0.2	V
V_{CM}	Differential Common Mode Range		0.8		2.5	V
V_{SE}	Siungle Ended Received Threshold		0.8		2.0	V
V_{OL}	Output Low Voltage	R_L = 1.5k, to 3.6V			0.3	V
V_{OH}	Output High Voltage		2.8			V
I_{OZ}	TRI-STATE Data Line Leakage	0V < V_{IN} < 3.3V	-10		+10	µA
C_{TRN}	Transceiver Capacitance				20	pF

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RF Characteristics

	Parameter	Condition		Min	Typ (1)	Max	Units
RX_{sense}	Receive Sensitivity	BER < 0.001	2.402 GHz		–80	–76	dBm
			2.441 GHz		–80	–76	dBm
			2.480 GHz		–80	–76	dBm
PinRF	Maximum Input Level			–10	0		dBm
IMP (2), (3)	Intermodulation Performance	F_1 = + 3 MHz, F_2 = + 6 MHz, $P_{in}RF$ = –64 dBm		–38	-36		dBm
RSSI	RSSI Dynamic Range at LNA Input			–72		–52	dBm
Z_{RFIN} (3)	Input Impedance of RF Port (RF_inout)	Single input impedance F_{in} = 2.5 GHz			32		Ω
Return Loss (3)	Return Loss					–8	dB
OOB (2), (3)	Out of Band Blocking Performance	$P_{in}RF$ = -10 dBm, 30 MHz < F_{CWI} < 2 GHz, BER < 0.001		–10			dBm
		$P_{in}RF$ = -27 dBm, 2000 MHz < F_{CWI} < 2399 MHz, BER < 0.001		–27			dBm
		$P_{in}RF$ = -27 dBm, 2498 MHz < F_{CWI} < 3000 MHz, BER < 0.001		–27			dBm
		$P_{in}RF$ = -10 dBm, 3000 MHz < F_{CWI} < 12.75 GHz, BER < 0.001		–10			dBm

(1) Typical operating conditions are at 2.75V operating voltage and 25°C ambient temperature.
(2) The f_0 = –64 dBm Bluetooth modulated signal, f_1 = -39 dbm sine wave, f_2 = -39 dBm Bluetooth modulated signal, $f_0 = 2f_1 - f_2$, and $|f_2 - f_1| = n \times 1$ MHz, where n is 3, 4, or 5. For the typical case, n = 3.
(3) Not tested in production.

Transmitter Characteristics

	Parameter	Condition	Min	Typ (1)	Max	Units
$P_{OUT}2 \times f_o{}^{d(2)}$	PA 2nd Harmonic Suppression	Maximum gain setting: f_0 = 2402 MHz, P_{out} = 4804 MHz			–30	dBm
$Z_{RFOUT}\theta$	RF Output Impedance/Input Impedance of RF Port (RF_inout)	P_{out} @ 2.5 GHz		47		Ω

(1) Typical operating conditions are at 2.75V operating voltage and 25°C ambient temperature.
(2) Out-of-Band spurs only exist at 2nd and 3rd harmonics of the CW frequency for each channel.

Synthesizer Characteristics

	Parameter	Condition	Min	Typ	Max	Units
f_{VCO}	VCO Frequency Range		2402		2480	MHz
t_{LOCK}	Lock Time	f_0 ± 20 kHz		120		µs
Δf_0offset (1)	Initial Carrier Frequency Tolerance	During preamble	–75	0	75	kHz
Δf_0drift (1)	Initial Carrier Frequency Drift	DH1 data packet	–25	0	25	kHz
		DH3 data packet	–40	0	40	kHz
		DH5 data packet	–40	0	40	kHz
		Drift Rate	–20	0	20	kHz/50 µs
t_D-Tx	Transmitter Delay Time	From Tx data to antenna		4		µs

(1) Frequency accuracy is dependent on crystal oscillator chosen. The crystal must have a cumulative accuracy of <20 ppm to meet Bluetooth specifications.

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Crystal Requirements

The LMX5453 provides an on-chip driver that may be used with an external crystal and capacitors to form an oscillator. Figure 2 shows the recommended crystal circuit. Table 5 specifies the system clock requirements.

The RF local oscillator and internal digital clocks for the LMX5453 are derived from the reference clock at the CLK+ input. This reference may come from either an external clock signal or the oscillator using the on-chip driver.

When the on-chip driver is used, the board- and design dependent capacitance must be considered in tuning the crystal circuit. Equations that provide a close approximation of the crystal tuning capacitance are used as a starting point, but the optimal values will vary with the capacitive properties of the circuit board. As a result, fine tuning of the crystal circuit must be performed experimentally, by testing different values of load capacitance.

Many different crystals can be used with the LMX5453. A key requirement from the Bluetooth specification is a cumulative accuracy of <20 ppm. Additionally, ESR (Equivalent Series Resistance) must be carefully considered. The LMX5453 can support a maximum ESR of 230Ω, but it is recommended to stay <100Ω for best performance over voltage and temperature. See Figure 3 for ESR as part of the crystal circuit for more information. The ESR of the crystal also has an impact on the start-up time of the crystal oscillator circuit. See ** Section 15.0 and Table 18 for system start-up timing.

Crystal

The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors. The resonant frequency may be trimmed with the crystal load capacitance.

Load Capacitance

For resonance at the correct frequency, the crystal should be loaded with its specified load capacitance. Load capacitance is a parameter specified by the crystal vendor, typically expressed in pF. The crystal circuit shown in Figure 3 is composed of:

- C1 (motional capacitance)
- R1 (motional resistance)
- L1 (motional inductance)
- C0 (static or shunt capacitance)

The LMX5453 provides some of the load with internal capacitors C_{int} and XOC_{TUNE}. The remainder must come from the external capacitors labeled Ct1 and Ct2 shown in Figure 2. For best noise performance, Ct1 and Ct2 should have the same the value.

The value of XOC_{TUNE} can be programmed in register 2. There are 7 bits of tuning for XOC_{TUNE}. The default value is 0028h, which results in an additional 2.6 pF internal capacitance. This register can be used in production testing for additional tuning, if necessary. See Table 19 for the range of XOC_{TUNE} values.

The crystal load capacitance (C_L) is calculated as:

$$C_L = C_{int} + XOC_{TUNE} + Ct1 // Ct2 \quad (1)$$

The C_L above does not include the crystal internal self capacitance C_0 as shown in Figure 3, so the total capacitance is:

$$C_{total} = C_L + C_0 \quad (2)$$

Based on the crystal specification and equation:

$$C_L = C_{int} + XOC_{TUNE} + Ct1 // Ct2 \quad (3)$$

$$C_L = 8\ pF + 2.6\ pF + 6\ pF = 16.6\ pF \quad (4)$$

16.6 pF is very close to the TEW crystal requirement of 16 pF load capacitance. With the internal shunt capacitance C_{total}:

$$C_{total} = 16.6\ pF + 5\ pF = 21.6\ pF \quad (5)$$

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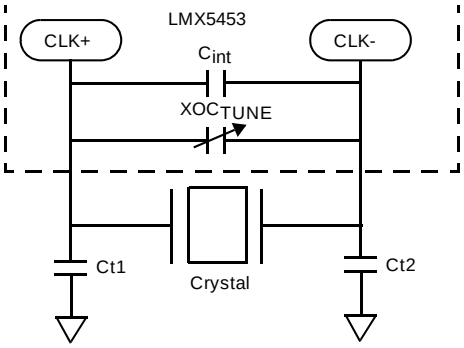


Figure 2. Recommended Crystal Circuit

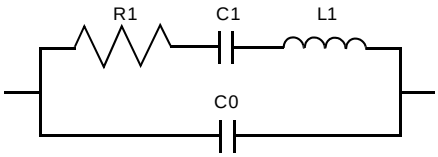


Figure 3. Crystal Equivalent Circuit

Crystal Pullability

Pullability is another important crystal parameter, which is the change in frequency of a crystal with units of ppm/pF, either from the natural resonant frequency to a load resonant frequency, or from one load resonant frequency to another. The frequency can be pulled in a parallel resonant circuit by changing the value of load capacitance. A decrease in load capacitance causes an increase in frequency, and an increase in load capacitance causes a decrease in frequency.

Frequency Tuning

Frequency tuning is performed by adjusting the crystal load capacitance with external capacitors. It is a Bluetooth requirement that the frequency is always within 20 ppm. The crystal/oscillator must have cumulative accuracy specifications of **15 ppm** to provide margin for frequency drift with aging and temperature.

TEW Crystal

The LMX5453 has been tested with the TEW TAS-4025A crystal (see Table 3). Because the internal capacitance of the crystal circuit is 8 pF and the load capacitance is 16 pF, 12 pF is a good starting point for both Ct1 and Ct2. The 2480 MHz RF frequency offset is then tested. Figure 5 shows the RF frequency offset test results.

Figure 5 shows the results are -20 kHz off the center frequency, which is –1 ppm. The pullability of the crystal is 2 ppm/pF, so the load capacitance must be decreased by about 1.0 pF. By changing Ct1 or Ct2 to 10 pF, the total load capacitance is decreased by 1.0 pF. Figure 6 shows the frequency offset test results. The frequency offset is now zero with Ct1 = 10 pF and Ct2 = 10 pF.

See Table 3 for crystal tuning values used on the Phoenix Development Board with the TEW crystal.

Table 2. TEW TAS-4025A

Specification	Value
Package	4.0 × 2.5 × 0.65 mm - 4 pads
Frequency	13.000 MHz
Mode	Fundamental
Stability	<15ppm @ –40 to +85°C
CL Load Capacitance	16 pF
ESR	80Ω max
CO Shunt Capacitance	5 pF

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Table 2. TEW TAS-4025A (continued)

Specification	Value
Drive Level	50 ± 10uV
Pullability	2 ppm/pF (minimum)
Storage Temperature	–40 to +85°C

Table 3. TEW on Phoenix Board

Specification	Value
Ct1	10 pF
Ct2	10 pF

TCXO (Temperature Compensated Crystal Oscillator)

The LMX5453 also can operate with an external TCXO (Temperature Compensated Crystal Oscillator). The TCXO signal is directly connected to the CLK+.

1. Input Impedance

The LMX5453 CLK+ pin has in input impedance of 2pF capacitance in parallel with >400kΩ resistance

Optional 32 KHZ Oscillator

A second oscillator is provided (see Figure 4) that is tuned to provide optimum performance and low-power consumption while operating with a 32.768 kHz crystal. An external crystal clock network is required between the 32kHz_CLKI clock input (pad B13) and the 32kHz_CLKO clock output (pad C13) signals. The oscillator is built in a Pierce configuration and uses two external capacitors. Figure 4 provides the oscillator's specifications.

In case the 32Khz is placed optionally, it is recommended to remove C2 and replace C1 with a zero ohm resistor.

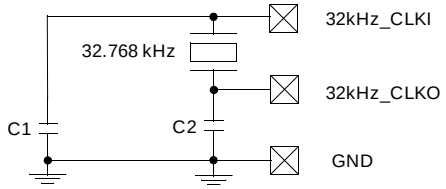


Figure 4. 32.768 kHz Oscillator

Table 4. 32.768 kHz Oscillator Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		1.62	1.8	1.98	V
I_{DDACT}	Supply Current (Active)			2		µA
f	Nominal Output Frequency			32.768		kHz
V_{PPOSC}	Oscillating Amplitude			1.8		V
	Duty Cycle		40		60	%

Table 5. System Clock Requirements

Symbol	Parameter	Min	Typ	Max	Unit
C_{REF}	External Reference Clock Frequency(1)	10	13	20	MHz
C_{TOL}	Frequency Tolerance (over full operating temperature and aging)	–20	15	20	ppm
XOC_{TUNE}	Digital Crystal Tuning Load Range		8		pF
C_{OSC}	Crystal Oscillator	10	13	20	MHz

(1) Frequencies supported: 10.00, 10.368, 12.00, 12.60, 12.80, 13.00, 13.824, 14.40, 15.36, 16.00, 16.20, 16.80, 19.20, 19.44, 19.68, and 19.80 MHz

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Table 5. System Clock Requirements (continued)

Symbol	Parameter	Min	Typ	Max	Unit
C_{ESR}	Crystal Serial Resistance			230	Ω
C_{REF-PS}	External Reference Clock Power Swing (peak to peak)	100	200	400	mV
C_{int}	Internal Load Capacitance		8		pF
C_{AGE}	Aging			1	ppm/year

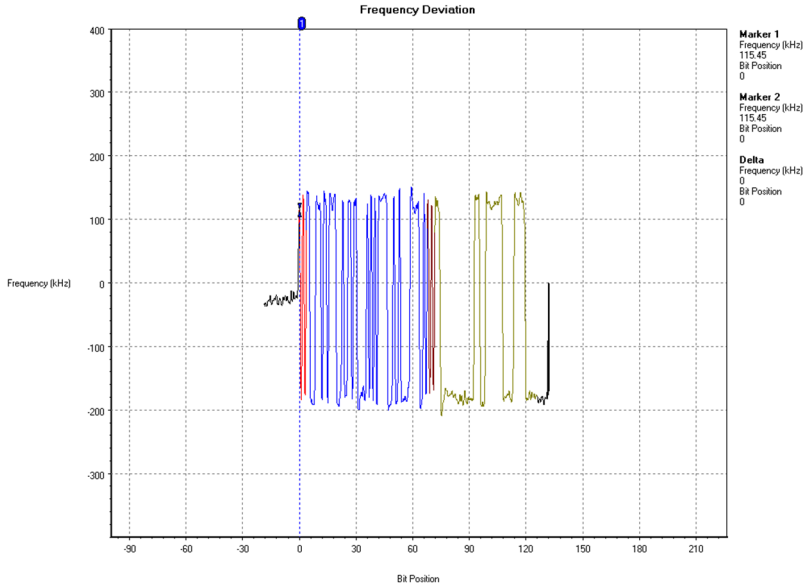


Figure 5. Frequency Offset with 12 pF//12 pF Capacitors

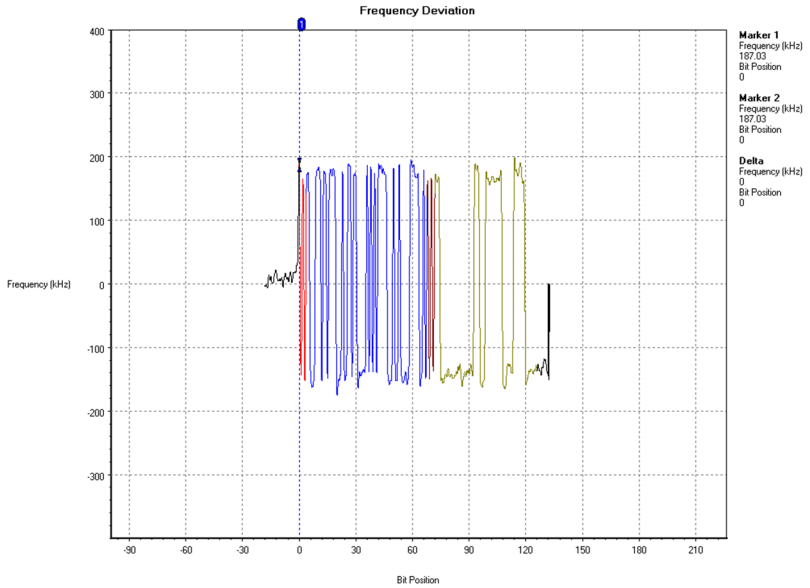


Figure 6. Frequency Offset with 10 pF//10 pF Capacitors

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Table 6. Register 2: XOCTUNE Tuning Load Range

Binary Value	Hex Value	Value	Units
000 0000	00	0	pF
010 1000	28(1)	2.6	pF
111 1111	7F	8	pF

(1) Default value for RF initialization register 2.

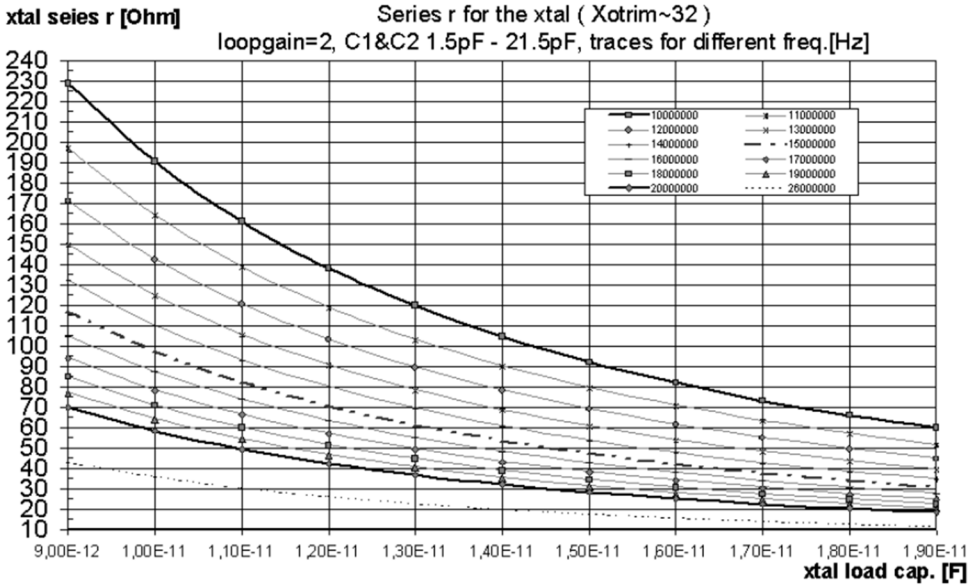


Figure 7. ESR vs. Load Capacitance for the Crystal

Antenna Matching and Front-End Filtering

Figure 8 shows the recommended component layout to be used between RF output and antenna input. Allows for versatility in the design such that the match to the antenna maybe improved and/or the blocking margin increased by addition of a LC filter. Refer to antenna application note for further details.

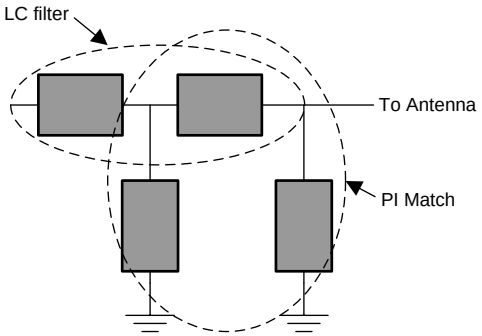


Figure 8. Front End Layout

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Loop Filter Design

Since the LMX5453 has an external loop filter that determines the performance of the device to a great extent, it is important that it is designed correctly. Texas Instruments will provide the starting component values but the end customer may have to make adjustments to optimize the performance. Please refer to Loop Filter application note and also Texas Instrument's Webench design tool for detailed information.

Component Calculations

The following parameters are required for component value calculation of a third order passive loop filter.

symbol?	Phase Margin: Phase of the open loop transfer function
F_c	Loop Bandwidth
F_{comp}	Comparison Frequency: Phase detector frequency
KVOC	VCO gain: Sensitivity of the VCO to control volts
K symbol?	Charge Pump gain: Magnitude of the alternating current during lock
F_{OUT}	Mean RF output frequency
T31	Ratio of the poles T3 to T1 in a 3rd order filter
symbol?	Gamma optimization parameter

The third order loop filter being defined has the topology shown in Figure 10.

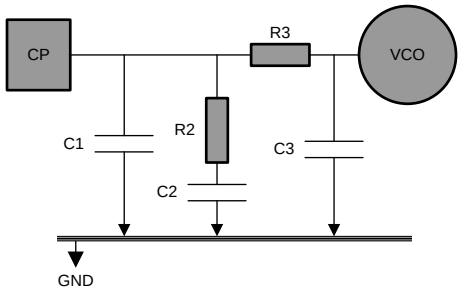


Figure 9. Third Order Loop Filter

$$\phi = \tan^{-1}\left(\frac{\gamma}{\omega_C \cdot T1 \cdot T1 + T31}\right) - \tan^{-1}(\omega_C \cdot T1) - \tan^{-1}(\omega_C \cdot T1 \cdot T31) \quad (6)$$

Calculate the poles and zeros. Use exact method to solve for T1 using numerical methods.

$$T3 = T31 \times T1 \qquad T2 = \frac{\gamma}{\omega_C \cdot (T1 + T3)} \quad (7)$$

$$A0 = \frac{K\phi \cdot K_{vco}}{\omega_C{}^2 \cdot N} \cdot \sqrt{\frac{1 + \omega_C{}^2 \cdot T2^2}{(1 + \omega_C{}^2 \cdot T1^2)(1 + \omega_C{}^2 \cdot T3^2)}} \quad (8)$$

Calculate the loop filter coefficients,

$$A1 = A0 \cdot (T1 + T3) \qquad A2 = A0 \cdot T1 \cdot T3 \quad (9)$$

$$C1 = \frac{A2}{T2^2} \cdot \left(1 + \sqrt{1 + \left(\frac{T2 \cdot A0 - T2 \cdot A1}{A2}\right)}\right) \quad (10)$$

Summary:

Symbol	Description	Units
η	N counter value	None
	Loop Bandwidth	rad/s
T1	Loop filter pole	S

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Symbol	Description	Units
T2	Loop filter zero	S
T3	Loop filter zero	S
A0	Total capacitance	nF
A1	First order loop filter coefficient	nFs
A2	Second order loop filter coefficients	nFs2

Components can then be calculated from loop filter coefficients

$$C3 = \frac{1 \cdot T2^2 \cdot C1^2 + T2 \cdot A1 \cdot C1 - A2 \cdot A0}{T2^2 \cdot C1 - A2} \qquad C2 = A0 - C1 - C3 \tag{11}$$

$$R2 = \frac{T2}{C2} \qquad R3 = \frac{A2}{C1 \cdot C3 \cdot T2} \tag{12}$$

$$LT = \frac{400}{F_C}(1 - \log_{10} \Delta F) \qquad \text{where } \Delta F = \frac{\text{Frequency} - \text{tolerance}}{\text{Frequency} - \text{jump}} \tag{13}$$

Some typical values for the LMX5453 are:

Symbol	Description	Units
Comparison Frequency	13	MHz
Phase Margin	48	PI rad
Loop bandwidth	100	kHz
T3 or T1 ratio	40	%
Gamma	1.0	
VCO gain	120	MHz per V
Charge pump gain	0.6	mA
Fout	2441	MHz

Which give the following component values:

Symbol	Description	Units
C1	0.17	nF
C2	2.38	nF
C3	0.04	nF
R2	1737	ohms
R3	7025	ohms

Phase Noise and Lock-Time Calculations

Phase noise has three sources, the VCO, crystal oscillator and the rest of the PLL consisting of the phase detector, dividers, charge pump and loop filter. Assuming the VCO and crystal are very low noise, it is possible to put down approximate equations that govern the phase noise of the PLL.

Phase noise (in-band) = PN1Hz + 20Log[N] + 10Log [F_{comp}]

Where PH1Hz is the PLL normalized noise floor in 1 Hz resolution bandwidth.

Further out from the carrier, the phase noise will be affected by the loop filter roll-off and hence its bandwidth.

As a rule-of-thumb; Δ Phase noise = 40Log [Δ F_c]

Where Fc is the relative change in loop BW expressed as a fraction.

For example if the loop bandwidth is reduced from 100kHz to 50kHz or by one half, then the change in phase noise will be -12dB. Loop BW in reality should be selected to meet the lower limit of the modulation deviation, this will yield the best possible phase noise.

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Even further out from the carrier, the phase noise will be mainly dominated by the VCO noise assuming the crystal is relatively clean.

Lock-time is dependent on three factors, the loop bandwidth, the maximum frequency jump that the PLL must make and the final tolerance to which the frequency must settle. As a rule-of-thumb it is given by:

$$LT = \frac{400}{F_C}(1 - \log_{10} \Delta F) \qquad \text{where } \Delta F = \frac{\text{Frequency} - \text{tolerance}}{\text{Frequency} - \text{jump}} \tag{14}$$

These equations are approximations of the ones used by Webench to calculate phase noise and lock-time.

Practical Optimisation

In an example where frequency drift and drift rate can be improved though loop filter tweaks, consider the results taken below. The drift rate is 26.1 kHz per 50us and the maximum drift is 25 kHz for DH1 packets, both of which are exceeding or touching the Bluetooth pass limits. These measurements are taken with component values shown above.

Table 7. TRM/CA/09/C (Carrier Drift)
Hopping On - Low Channel

	DH1	DH3	DH5
Drift Rate / 50us	26, 1 kHz	N/A	–30,5 kHz
Max Drift	25 kHz	N/A	36 kHz
Average Drift	–1 kHz	N/A	12 kHz
Packets Tested	10	N/A	10
Packets Failed	2	N/A	10
Overall Result	Failed	N/A	Failed

Results below were taken on the same board with three loop filter values changed. C2 and R2 have been increased in value and C1 has been reduced. The drift rate has improved by 13 kHz per 50 µs and the maximum drift has improved by 10 kHz.

Table 8. TRM/CA/09/C (Carrier Drift)
Hopping On - Low Channel

	DH1	DH3	DH5
Drift Rate / 50us	–13,6 kHz	N/A	15,6 kHz
Max Drift	15 kHz	N/A	21 kHz
Average Drift	3 kHz	N/A	1 kHz
Packets Tested	10	N/A	10
Packets Failed	0	N/A	0
Overall Result	Passed	N/A	Passed

The effect of changing these three components is to reduce the loop bandwidth which reduces the phase noise. The reduction in this noise level corresponds directly to the reduction of noise in the payload area where drift is measured. This noise reduction comes at the expense of locktime which can be increased to 120 µs without suffering any ill effects, however if we continue to reduce the loop BW further the lock-time will increase such that the PLL does not have time to lock before data transmission and the drift will again increase. Before the lock-time goes out of spec, the modulation index will start to fall since it is being cut by the reducing loop BW. Therefore a compromise has to be found between lock-time, phase noise and modulation, which yields best performance.

Note// The values shown on the LMX5453 datasheet are the best case optimized values that have been shown to produce the best overall results and are recommended as a starting point for all designs.

Another example of how the loop filter values can affect frequency drift rate, these results below show the DUT with maximum drift on mid and high channels failing. Adjusting the loop bandwidth as shown provides the improvement required to pass qualification.

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Table 9. Original results:

Hopping OFF - Low Channel				
	DH1	**DH3**	**DH5**	**Limits**
Drift Rate / 50us	–15.00 kHz	–28.10 kHz	–19.10 kHz	+/– 20 kHz
Maximum Drift	–19 kHz	–37 kHz	–20 kHz	DH1: +/– 25 kHz
Average Drift	–11 kHz	–32 kHz	–10 kHz	DH3: +/– 40 kHz
Packets Tested	10	10	10	DH5: +/– 40 kHz
Packets Failed	0	1	0	
Result	Pass	Fail	Pass	

Hopping OFF - Med Channel				
	DH1	**DH3**	**DH5**	**Limits**
Drift Rate / 50us	–18.60 kHz	16.30 kHz	–18.00 kHz	+/– 20 kHz
Maximum Drift	–29 kHz	–44 kHz	–28 kHz	DH1: +/– 25 kHz
Average Drift	–19 kHz	–37 kHz	–19 kHz	DH3: +/– 40 kHz
Packets Tested	10	10	10	DH5: +/– 40 kHz
Packets Failed	2	2	0	
Result	Fail	Fail	Pass	

Hopping OFF - High Channel				
	DH1	**DH3**	**DH5**	**Limits**
Drift Rate / 50us	–16.30 kHz	16.80 kHz	–17.70 kHz	+/– 20 kHz
Maximum Drift	–36 kHz	–61 kHz	–38 kHz	DH1: +/– 25 kHz
Average Drift	–31 kHz	–48 kHz	–29 kHz	DH3: +/– 40 kHz
Packets Tested	10	10	10	DH5: +/– 40 kHz
Packets Failed	10	8	0	
Result	Fail	Fail	Pass	

Table 10. New Results:

Hopping OFF - Low Channel				
	DH1	**DH3**	**DH5**	**Limits**
Drift Rate / 50us	–12.00 kHz	–15.10 kHz	18.80 kHz	+/– 20 kHz
Maximum Drift	–15 kHz	–35 kHz	–19 kHz	DH1: +/– 25 kHz
Average Drift	–6 kHz	–25 kHz	–9 kHz	DH3: +/– 40 kHz
Packets Tested	10	10	10	DH5: +/– 40 kHz
Packets Failed	0	0	0	
Result	Pass	Pass	Pass	

Hopping OFF - Med Channel				
	DH1	**DH3**	**DH5**	**Limits**
Drift Rate / 50us	–14.20 kHz	–16.10 kHz	17.20 kHz	+/– 20 kHz
Maximum Drift	–16 kHz	–34 kHz	–22 kHz	DH1: +/– 25 kHz
Average Drift	–11 kHz	–27 kHz	–9 kHz	DH3: +/– 40 kHz
Packets Tested	10	10	10	DH5: +/– 40 kHz
Packets Failed	0	0	0	
Result	Pass	Pass	Pass	

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Hopping OFF - High Channel				
	DH1	DH3	DH5	Limits
Drift Rate / 50us	–12.70 kHz	–17.40 kHz	–16.50 kHz	+/– 20 kHz
Maximum Drift	–23 kHz	–29 kHz	–25 kHz	DH1: +/– 25 kHz
Average Drift	–12 kHz	–25 kHz	–16 kHz	DH3: +/– 40 kHz
Packets Tested	10	10	10	DH5: +/– 40 kHz
Packets Failed	0	0	0	
Result	Pass	Pass	Pass	

Reference Starting Values

Recommended starting values for the LMX5453 as also stated in the reference design towards the end of this datasheet are a as shown in Table 11. These values have been optimized through testing to yield the best results from the design. However minor changes to the layout could mean the values need re-optimization.

Table 11. Loop Filter Values

Device	C1	C2	C3	R2	R3
LMX5453	220 pF	2200 pF	39 pF	4.7k	10k

Functional Blocks

Baseband Processor And Link Management Processor

Baseband and lower link control functions are implemented using a combination of a CompactRISC 16-bit processor and the Bluetooth Lower Link Controller (LLC). These processors operate from integrated ROM memory and RAM. They execute on-board firmware implementing all Bluetooth functions.

Bluetooth Lower Link Controller

The integrated Bluetooth Lower Link Controller complies with the Bluetooth Specification version 2.0 and implements the following functions:

- Faster connection
- Interlaced Scanning
- Adaptive frequency hopping (AFH)
- Enhanced Error detection
- Support for 1-, 3-, and 5-slot packet types
- 79 channel hop-frequency generation circuitry
- Fast frequency hopping at 1600 hops per second
- Power management control
- Access code correlation and slot timing recovery

Memory

The LMX5453 provides 16K of combined system and Patch RAM memory that can be used for data and/or code upgrades of the ROM-based firmware. Due to the flexible startup used for the LMX5453, operating parameters like the Bluetooth Device Address (BD_ADDR) are defined during boot time. This allows reading the parameters from an external EEPROM or programming them directly over HCI.

External Memory Interfaces

Because the LMX5453 is a ROM-based device with no onchip non-volatile storage, the operation parameters will be lost after a power cycle or hardware reset. To avoid reinitializing operation parameters, patches, or user data, the LMX5453 offers two options for connecting with an external EEPROM:

- Microwire/SPI
- ACCESS.bus (I^2C compatible)

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The interface is selected during start-up, based on states sampled from the option pins. See Table 20 for the option pin descriptions.

Microwire/SPI Interface

If the configuration selected by the option pins uses a Microwire/SPI interface, the LMX5453 activates that interface and attempts to read the EEPROM. The external memory must be compatible with the features listed in Table 12.

The largest size EEPROM supported is limited by the addressing format of the selected EEPROM. The device must have a page size equal to N x 32 bytes.

The LMX5453 firmware requires that the EEPROM supports page write. The clock must be high when idle.

Table 12. M95640-S EEPROM 8K × 8

Parameter	Value
Supplier	ST Microelectronics
Supply Voltage (1)	1.8 - 3.6 V
Interface	SPI compatible (positive clock SPI modes)
Memory Size	8K x 8 (64 Kbits)
Clock Rate (1)	2 MHz
Access	Byte and page write (up to 32 bytes)

(1) Parameter range reduced to requirements of Texas Instruments' reference design.

ACCESS.bus Interface

If the configuration selected by the option pins uses an ACCESS.bus or I2C-compatible interface, the LMX5453 activates that interface and attempts to read the EEPROM. The external memory must be compatible with the features listed in Table 13.

The largest size EEPROM supported is limited by the addressing format of the selected EEPROM. The device must have a page size equal to N x 32 bytes. The device uses a 16-bit address format. The device address must be 000.

Table 13. 24C64 EEPROM 8K × 8

Parameter	Value
Supplier	Atmel
Supply Voltage (1)	2.7 - 5.5 V
Interface	2-wire serial interface
Memory Size	8K x 8 (64 Kbits)
Clock Rate (1)	100 kHz
Access	32-byte page-write mode

(1) Parameter range reduced to requirements of Texas Instruments' reference design.

Host Controller Interface Port

UART Interface

The LMX5453 provides one Universal Asynchronous Receiver Transmitter (UART). It supports 8-bit data with or without parity, and with one or two stop bits. The UART can operate at standard baud rates from 300 baud up to a maximum of 921.6 kbaud. DMA transfers are supported to allow for fast processor-independent receive and transmit operation. The UART implements flow-control signals (RTS# and CTS#) for hardware handshaking.

The reference clock and UART baud rate are configured during start-up by sampling option pins OP3, OP4, and OP5. If the auto baud rate detect option is selected, the firmware checks an area in non-volatile storage (NVS) for a valid UART baud rate stored during a previous session. If no value was saved, the LMX5453 will switch to auto baud rate detection and wait for an incoming reference signal.

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The UART can detect a BREAK signal, which forces the LMX5453 to reset. This is useful when the only connection between the LMX5453 and the host system is the HCI port.

The UART offers wake-up from low-power modes through its Multi-Input Wake-Up module (MIWU). When the LMX5453 is in a low-power mode, RTS# and CTS# can function as Host_WakeUp and Bluetooth_WakeUp, respectively. Table 14 represents the operational modes supported by the LMX5453 firmware for implementing the HCI transport port with the UART.

Table 14. UART Operation Modes

Modes	Range	Default at Power-Up	With Auto Baud Detect
Baud Rate	0.3 to 921.6 kbaud	Configured by option pins, NVS parameter, or auto baud rate detection	0.3 to 921.6 kbaud
Flow Control	RTS#/CTS# or None	RTS#/CTS#	RTS#/CTS#
Parity	Odd, Even, or None	None	None
Stop Bits	1 or 2	1	1
Data Bits	8	8	8

USB Interface

The LMX5453 USB node controller features enhanced DMA support with many automatic data handling features. It is certifiable to USB specification version 2.0. The USB interface is the standard 12 Mbit/s. An internal PLL provides the necessary 48 MHz clock.

The USB node controller integrates the required USB transceiver, a Serial Interface Engine (SIE) and USB endpoint FIFOs. Seven endpoint pipelines are supported: one for the mandatory control endpoint and six to support interrupt, bulk, and isochronous endpoints. Each endpoint pipeline has a dedicated FIFO (8 bytes for the control endpoint, and 64 bytes for the other endpoints).

Audio Port

Advanced Audio Interface

The Advanced Audio Interface (AAI) is an advanced version of the Synchronous Serial Interface (SSI) that provides a full-duplex communications port to a variety of industry-standard 13/14/15/16-bit linear or 8-bit log PCM codecs, DSPs, and other serial audio devices.

The interface supports up to two codecs or interfaces. The firmware selects the desired audio path and interface configuration using a parameter in RAM (imported from nonvolatile storage or programmed during boot-up). The audio path options include 16-bit two's complement linear audio through the HCI transport, the Motorola MC145483 codec, and the OKI MSM7717 codec through the AAI, or No Audio. See NVS Table 21.

If an external codec or DSP is used, the LMX5453 audio interface generates the necessary bit and frame clock for driving the interface.

Table 15 summarizes the audio path selection and the configuration of the audio interface at the specific modes.

The LMX5453 supports two simultaneous SCO links.

Table 15. Audio Path configuration

Audio setting	Interface	Freq	Format	AAI Bit Clock	AAI Frame Clock	AAI Frame Sync Pulse Length
OKI MSM7717	Advanced audio interface	ANY (1)	8-bit log PCM (a-law only)	480 KHz	8 KHz	14 Bits
Motorola MC145483 (2)	Advanced audio interface		13-bit linear	480 KHz	8 KHz	13 Bits

(1) For supported frequencies see Table 5

(2) Due to internal clock divider limitations the optimum of 512KHz, 8KHz can not be reached. The values are set to the best possible values. The clock mismatch does not result in any discernible loss in audio quality.

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Table 15. Audio Path configuration (continued)

Audio setting	Interface	Freq	Format	AAI Bit Clock	AAI Frame Clock	AAI Frame Sync Pulse Length
OKI MSM7717	Advanced audio interface	13MHz	8-bit log PCM (a-law only)	520 KHz	8 KHz	14 Bits
Motorola MC145483(3)	Advanced audio interface		13-bit linear	520 KHz	8 KHz	13 Bits
Winbond W681310	Advanced audio interface	13MHz	8 bit log PCM A-law and u-law	520 KHz	8 KHz	14 Bits
Winbond W681360	Advanced audio interface	13MHz	13-bit linear	520 KHz	8 KHz	13 Bits
PCM slave(4)	Advanced audio interface	ANY(1)	8/16 bits	128 - 1024 KHz	8 KHz	8/16 Bits
Audio over HCI	HCI Transport		16-Bit Two's Complement Linear	--	--	--

(3) Due to internal clock divider limitations the optimum of 512KHz, 8KHz can not be reached. The values are set to the best possible values. The clock mismatch does not result in any discernible loss in audio quality.
(4) In PCM slave mode, parameters are stored in NVS. Bit clock and frame clock must be generated by the host interface.

PCM slave configuration example: PCM slave uses the slot 0, 1 slot per frame, 16 bit linear mode, long frame sync, normal frame sync. In this case, 0x03E0 should be stored in NVS. See ** "LMX5453 Software User's Guide" for more details.

Auxiliary Ports

RESET#

There are two reset inputs: RESET_RA# for the radio and RESET_BB# for the baseband. Both are active low.

There is also a reset output, B_RESET_RA# (Buffered Radio Reset), which is also active low. This output follows input RESET_RA#. When RESET_RA# is released, going high, B_RESET_RA# stays low until the clock has started.

See ** Section 15.0 for details and Section 16.0 for schematics.

General Purpose I/O Ports

The LMX5453 provides 3 GPIO ports which either can be used as indication and configuration pins or can be used for general-purpose functionality. The states which select these options are sampled during the start-up sequence.

In a general-purpose configuration, the pins are controlled by hardware-specific HCI commands. These commands provide the ability to set the direction of the pin, drive the pin high or low, and enable a weak pull-up on the pin.

In the alternate-function configuration, the pins have predefined indication functions. See Table 16 for a description of the alternate-function configuration.

Table 16. Alternate GPIO Pin Configuration

Pin	Description
OP4/PG4	Operation mode pin to configure transport layer settings during boot-up
PG6	USB status indication
PG7	TL (Transport Layer) traffic indication

System Power-Up

To power-up the LMX5453 the following sequence must be performed:

1. Apply VCC_IO and VCC to the LMX5453.
2. The RESET_RA# should be driven high.

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3. Then RESET_BB# should be driven high at a recommended time of 1ms after the LMX5453 voltage rails are high. The LMX5453 is properly reset. (See Figure 10).

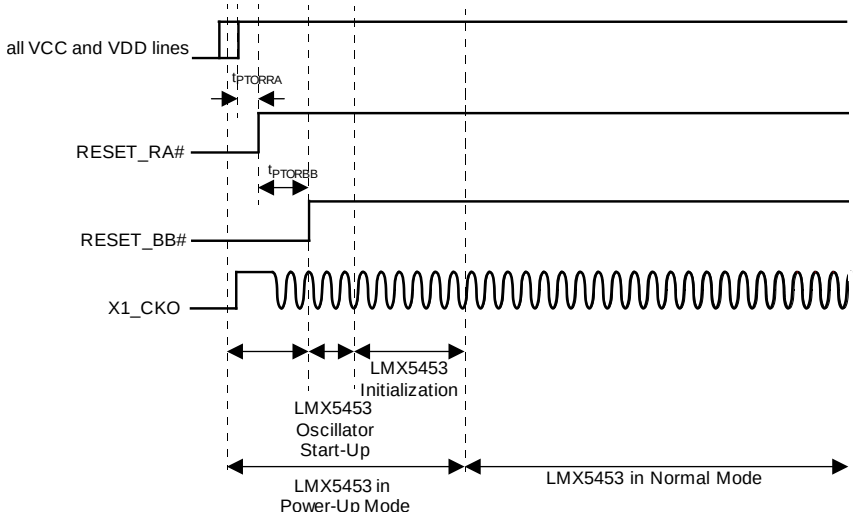


Figure 10. LMX5453 Power-On Reset Timing

Table 17. LMX5453 Power to Reset Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{PTORRA}	Power to Reset	VCC and VCC_IO at operating voltage level to valid reset	<500 (1)			µs
t_{PTORBB}	Reset to Reset	VCC and VCC_IO at operating voltage level to valid reset	1 (2)			ms

(1) Rise time on power must switch on fast, rise time <500 µs
(2) Recommended value.

Table 18. ESR vs. Start-Up Time

ESR (Ω)	Typical (1)(2)	Units
10	12	ms
25	13	ms
40	16	ms
50	24	ms
80	30	ms

(1) Frequency, loading caps, and ESR all must be considered for determining the start-up time.
(2) For reference only, must be tested on each system to accurately determine the start-up time.

Start-Up Sequence

During start-up, the LMX5453 samples the option inputs OP3 to OP7 for configuration, external clock source, HCI transport layer, and available non-volatile storage EEPROM interface. The start-up options are described in Table 20.

Options Register

The states sampled from the OP inputs listed in Table 20 are latched in this register at the end of reset. The Options register can be read by the LMX5453 firmware at any time.

All pads are inputs with weak on-chip pull-up/down resistors during reset. The resistors are disconnected at the end of RESET_BB#.

1 = Pull-up resistor connected in application

0 = Pull-down resistor connected in application

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x = Don't care

Start-Up With External EEPROM

To read information from an external EEPROM, the OP inputs have to be strapped according to Table 20.

The start-up sequence performs these operations:

1. From the Options register bits OP6 and OP7, the firmware checks whether a serial EEPROM is available to use (ACCESS.bus or Microwire/SPI).
2. If a serial EEPROM is available, the permanent parameter block, patch block, and non-volatile storage (NVS) are initialized from it.
3. From the Options register bits OP3, OP4, and OP5, the firmware checks for clocking information and transport layer settings. If the NVS information are not sufficient, the firmware will send the Await Initialization event on the TL and wait for additional information (see ** Section 15.1.3)
4. The firmware compensates the UART for new BBCLK information from the NVS.
5. The firmware starts up the Bluetooth core.

Start-Up Without External EEPROM

The following sequence will take place if OP6 and OP7 have selected No external memory, as described in Table 20.

The start-up sequence performs these operations:

1. From the Options registers OP6 and OP7, the firmware checks if an EEPROM is available to use.
2. From the Options register OP3, OP4 and OP5, the firmware checks the clocking mode and transport layer settings.
3. The firmware sends the Await Initialization event on the transport layer and waits for NVS configuration commands. The configuration is finalized by sending the Enter Bluetooth Mode command.
4. The firmware compensates the UART for new BBCLK information from the NVS.
5. The firmware starts up the Bluetooth core.

Table 19. Start-Up Sequence Options(1)

Package Pad						Description
OP3	OP4	OP5	OP6	OP7	ENV1#	
PD	PD	PD	PD	PD	PU	PD = Internal pull-down during reset PU = Internal pull-up during reset
x	x	x	Open (0)	Open (0)	Open (1) BBCLK	No serial memory
x	x	x	1	Open (0)	Open (1) BBCLK	TBD
x	x	x	Open (0)	1	Open (1) BBCLK	Microwire serial memory
x	x	x	1	1	Open (1) BBCLK	ACCESS.bus serial memory
T_SCLK	x	x	T_RFDATA	T_RFCE	0 BBCLK/US BCLK	Test mode

(1) I/O pull-up/down resistor connected in application.

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Table 20. Fixed Frequencies

Osc Freq (MHz)	BBLCK (MHz)	PLL (48 MHz)	OP3	OP4	OP5	Description
12	12	Off	0	0	0	HCI UART transport layer with baud rate detection
13	13	Off	1	0	0	
10-20	10-20(1)	On	0	1	0	
13	13	Off	1	1	0	HCI UART transport layer 115.2 kbaud
12	12	On	0	0	1	HCI USB transport layer
13	13	On	1	0	1	
10-20	10-20(1)	On	0	1	1	
13	13	Off	1	1	1	HCI UART transport layer 921.6 kbaud

(1) See Table 5 for supported frequencies.

Configuring the LMX5453 Through the Transport Layer

As described in Section 15.0, the LMX5453 checks the Options register during start-up to determine whether an external EEPROM is available. If the EEPROM information is incomplete or no EEPROM is installed, the LMX5453 will boot into the initialization mode. The mode is confirmed by the Await Initialization event.

The following information is needed to enter Bluetooth mode:

- Bluetooth Device Address (BD_ADDR)
- External clock source (only if 10–20 MHz has been selected)
- UART baud rate (only needed if auto baud rate detection has been selected)

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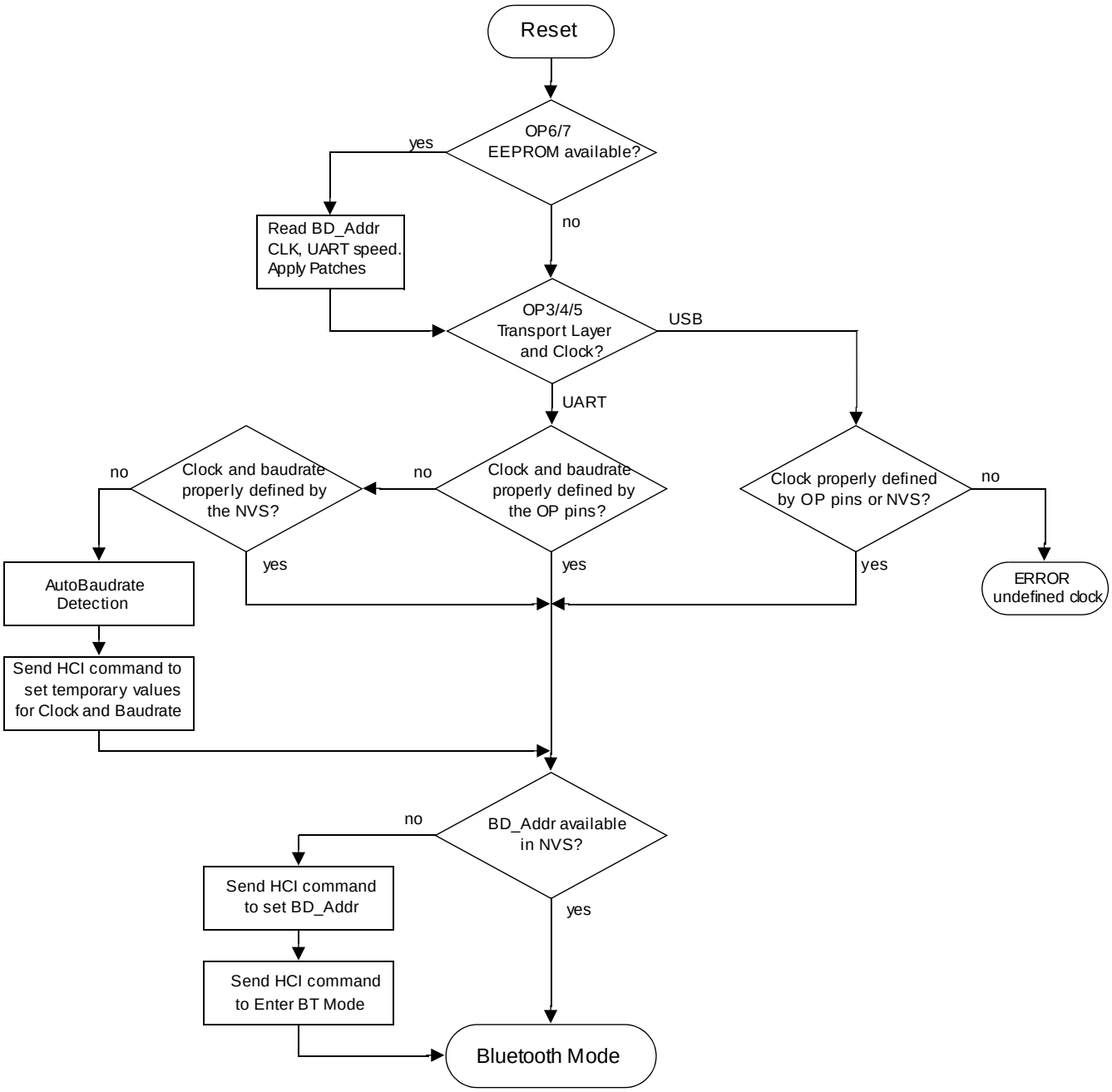


Figure 11. Flow Chart for the Start-Up Sequence

In general, the following procedure will initialize the LMX5453:

1. Wait for the Await initialization event. The event will only appear if the transport layer speed is set or after successful baud rate detection.
2. Send Set Clock and Baudrate command for temporary clock frequency and UART configuration.
3. Send Write BD_Addr to configure local Bluetooth device address.
4. Send Enter Bluetooth Mode. The LMX5453 will use the configured clock frequency and UART baud rate to start the HCI transport layer interface.

Note: These clock and baud rate settings are only valid until the next power-on or hardware reset.

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Auto Baud Rate Detection

The LMX5453 supports an auto baud rate detection in case the external clock is different from 12, 13 MHz or the range 10-20 MHz or the baud rate is different from 115.2 or 921.6 kbaud.

The baud rate detection is based on the measurement of a single character. The following issues need to be considered:

- The flow control pin CTS# must be low, otherwise the host is held in flow stop mode.
- The auto baud rate detector measures the length of the 0x01 character from the positive edge of bit 0 to the positive edge of the stop bit.
- Therefore, the very first received character must always be 0x01.
- The host can restrict itself to send only a 0x01 character or it can send an HCI command.
- If an HCI command is used for baud rate detection, the second received character must be 0x00.
- The host must flush the TX buffer within 50–100 milliseconds, depending on the clock frequency of the host controller.
- After 50–100 milliseconds, the UART is about to be initialized. Then, the host should receive an Await Initialization event or a Command Status event.

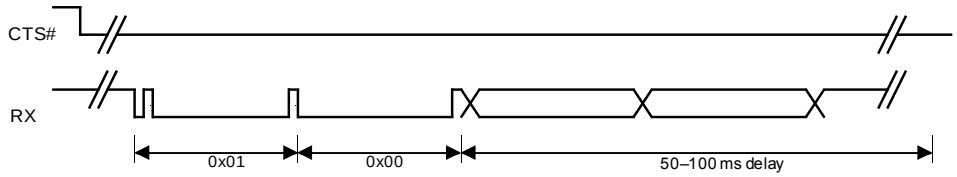


Figure 12. Auto Baud Rate Detection

Using an External EEPROM for Nonvolatile Storage

The LMX5453 offers two interfaces for connecting to external EEPROM used for non-volatile storage (NVS). The interface is selected by the states sampled from the option inputs during the start-up sequence. See Table 20 for the available options.

The external memory is used to store mandatory parameters such as the Bluetooth device address (BD_ADDR) as well as many optional parameters such as link keys or user data.

The firmware uses fixed addresses to reference the parameters, which allows the EEPROM to be preprogrammed with default parameters in manufacturing. See Table 21 for the organization of the NVS parameter map.

If the EEPROM is empty, during the first start-up the LMX5453 will behave as though no memory is connected. (see ** Section 15.1.3). During the start-up sequence, parameters can be written directly to the EEPROM so that they can be used during subsequent sessions. Patches supplied over the transport layer will be stored automatically into the EEPROM.

Table 21. Non Volatile Storage Map

Address	Name	Description
00-05 (1)	BD_ADDR	Bluetooth Device Address LAP(lsb), LAP, UAP, NAP, NAP (msb)
06	Audio Path Selection	0x00: One motorola MC145483 codec 0x01: Two motorola MC145483 codecs 0x02: One OKI MSM7717 codec 0x03: Two OKI MSM7717 codecs 0x04: Generic PCM Slave. For this setting the generic slave configuration and the generic slave frame clock prescaler must also be set to correct values in the NVS. 0x05 0xFE: No audio path 0xFF: HCI used for SCO transfer
07-0A	Baudrate	

(1) Parameters located at these addresses are requested by the Bluetooth Core for proper operation.

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Table 21. Non Volatile Storage Map (continued)

Address	Name	Description
0B	Frame settings(2)	
0C-0D	USB Vid	
0E-0F	USB PID	
10	USB Self powered	
11	USB max power	
12-15	Frequency(3)	
Core parameters		
16-BD(1)	Link Keys	Internal use, 24 bytes per key
BE(1)	Local Name Length	Length of Local Device Name
BF-1B6(1)	Local Device Name	Friendly bluetooth name of the bluetooth device
1B7(1)	Link Key Type	
1B8(1)	Unit Key Present	
1B9-1C8(1)	Unit Key	
Debugging info		
1C9-1D7	Assert Information	Internal use only.
1D8-1E9	Runtime Information	Internal use only.
Reserved		
1EA	Options	**Bit 0: Reserved** **Bit 1: Low power operation** 0: Disable low power operation 1: Enable low power operation **Bit 2: Traffic LED Indication** 0: Enable traffic LED indication on PG7 1: Disable traffic LED indication on PG7 **Bit 3: USB status** 0: Enable USB status on PG6 1: Disable USB status on PG6 **Bit 4: TLKAS (Transport Layer Keep Alive during Scans)** 0: Normal TL power off 1: Only power off TL if page/inquiry scans disabled Bit4 has no effect on USB TL. The USB TL will always use halt in order to comply with USB power constraints. This option does not affect the protocol for TL power management, only the internal operation of the firmware. TLKAS == 0 requires a stable clock when exiting from HALT mode.ormal TL power off **Bit 5-7: Unused**
1EB	Vtune_Desired_Threshold	Internal use only.
1EC	Vtune_on	Internal use only.
1ED	Vtune_enable	Internal use only.
1EE	AclAndScoBufferMode	0: 8 339 byte ACL buffers, 2 SCO buffers 1: 8 ACL 339 bytes, 1 eSCO/SCO 2: 4 339 byte ACL, 2 eSCO/SCO 0xFF: specifies same set-up as 1.

(2) This parameter can only be used with a pre-programming external EEPROM.
(3) The frequency parameter is only needed when the firmware starts up in a mode with unknown crystal frequency (10- 20MHz). FSEL pins are used to determine if the crystal frequency is unknown. Reference Table 5 for supported frequencies.

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Table 21. Non Volatile Storage Map (continued)

Address	Name	Description
1F1-1F2	Generic PCM slave config	This 16-bit value (LSB first) is used to store the PCM format configuration for the PCM generic slave. The Fcprs value must also be set in order to use the generic PCM slave. Attention: Some values are not mapped directly to the parameter values, because we want 0xFF to select the default behavior. **Bit 0-1: Slot selection:** 11: use slot 0 00: use slot 1 01: use slot 2 10: use slot 3 **Bit 2-3: Number of slots per frame:** 11: 1 slot 00: 2 slots 01: 3 slots 10: 4 slots **Bit 4-6: PCM data format:** 000: 8 bit A-law 001: 8 bit u-law 010: 13 bit linear 011: 14 bit linear 100: 15 bit linear 101: 16 bit linear 110: 16 bit linear 111: 16 bit linear **Bit 7: Frame sync length:** 0: short frame sync 1: long frame sync **Bit 8: Data word length:** 0: 8-bit data word length 1: 16-bit data word length **Bit 9: Frame sync polarity:** 0: use normal frame sync 1: use inverted frame sync **Bit 10-15: Unused, set to 1**
1F3	Generic PCM slave Fcprs	Frame clock prescaler for generic PCM slave. The ratio between the bit clock and the frame clock must be written into this register for the generic PCM slave to operate correctly. **BIT0-6: Fcprs** This value is an unsigned integer indicating the prescaler. The following equation must be true: bit_clock/(Fcprs + 1) = frame_clock. Example: bit clock = 480000, frame sync rate = 8000, Fcprs must be set to 59 since 480000/(59 + 1) = 8000 **BIT7: Unused, set to 1**
Production Parameters		
1F0 (4)	XOC_{TUNE}	
1F4-1F7	RfReg4	
1F8-1FB	RfReg15	
1FC-1FF	Unused	
Reserved for RF development		
200-2FF	RF Development	Internal use only.
Patch Code Area		
300-1CFF	Patch code	Space for Patch code, activated during startup
Application Data		
1D00-2000	User Data	Available space if 8K EEPROM is used
1D00-4000	User Data	Available space if 16K EEPROM is used
1D00-8000	User Data	Available space if 32K EEPROM is used

(4) Reference Section 11.0 "Crystal Requirements" on page 12 for details on crystal tuning.

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Low-Power Operation

The LMX5453 provides low-power modes which cover the main usage scenarios in a Bluetooth environment. Each of the low-power modes is optimized for minimal power consumption in that particular scenario. The modular structure of the LMX5453 allows the firmware to power down unused modules or to switch to a low-speed clock. Because the LMX5453 firmware supports these modes transparently, no power-control mechanisms need to be implemented by application code to use these modes.

To reduce power consumption, the LMX5453 can disable the UART transport layer, which switches off the UART module and enables a wake-up mechanism triggered by the UART interface.

Power Modes

The LMX5453 has six operating power modes, which are selected by the activity level of the HCI transport layer and the Bluetooth baseband processor. Mode switching is triggered by a change in the baseband processor activity or by enabling/disabling the UART transport layer.

The baseband processor activity depends on application requirements and is defined by standard Bluetooth operations such as inquiry/page scanning and link establishment.

A remote device establishing or disconnecting a link may also indirectly change the baseband processor activity and therefore the power mode.

The HCI transport layer is enabled on device power-up by default. To disable the transport layer, the vendor-specific HCI command HCI_DISABLE_TL is used. Therefore, only the host side of the HCI can disable the transport layer. Reenabling the transport layer is controlled by the hardware wake-up signalling. This can be performed from either the host or the LMX5453 side of the interface. See Section 15.5 for detailed information.

Note: The HCI_Disable_TL command is only supported with the UART transport layer. The Main clock can disabled for PM0. The Main clock itself may be 12, 13, or 10-20 MHz. The PLL will always be enabled if the transport layer is USB or if the transport layer is UART but the Main clock is not 12 or 13 MHz. Also, in PM2, the Main and System clocks will be disabled by Host Controller when not needed by the Lower Link Controller.

Table 22. LMX5453 Power Modes

Power Mode	UART Mode	Baseband Activity	Description
PM0	Disabled Wake-Up Trigger Enabled	None	Standby mode.
PM1	Enabled	None	Transport layer ready to receive commands, no baseband processor activity.
PM2	Disabled Wake-Up Trigger Enabled	Scanning	LMX5453 discoverable/connectable for other devices. UART disabled. Wake-up trigger enabled to wake-up host on incoming connection.
PM3	Enabled	Scanning	LMX5453 discoverable/connectable for other devices. UART enabled.
PM4	Disabled Wake-Up Trigger Enabled	Active Link	LMX5453 handling at least one link. UART disabled. Wake-up trigger enabled to wake-up host on incoming data or connections.
PM5	Enabled	Active Link	Standard active mode. LMX5453 handling at least one link.

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The LMX5453 switches between power modes in response to certain changes in activity. Because any of the parameters can be changed dynamically, there is no limitation on which mode can be reached from another. Figure 13 shows an overview of the power modes and the transitions between modes.

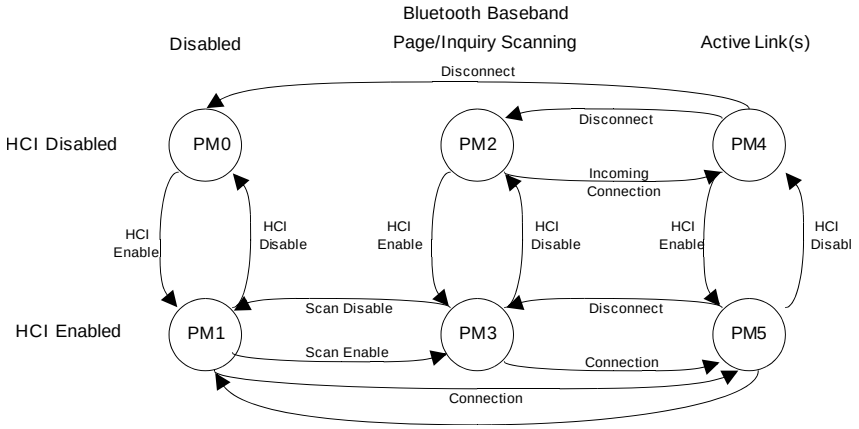


Figure 13. LMX5453 Power Modes

Controlling the UART

Hardware Wake-Up Function

In certain usage scenarios, the host may switch off the transport layer of the LMX5453 to reduce power consumption. Then, both devices are able to shut down their UART interfaces. In this mode, the firmware will configure the UART interface to enable a hardware wake-up trigger.

The hardware interface between the host and the UART interface on the LMX5453 is shown in Figure 14.

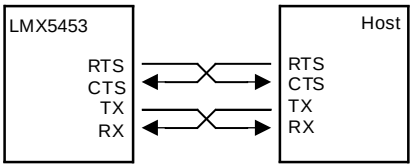


Figure 14. UART Null Modem Connections

Disabling the UART

The host can disable the UART transport layer by sending the Disable Transport Layer command. In response, the LMX5453 will empty its buffers, send the confirmation event, and disable its UART interface. Then, the UART interface will be reconfigured to wake-up the LMX5453 when a rising edge occurs on the CTS# input.

When the HCI transport layer is disabled, both the host and the LMX5453 will drive RTS=0, because they will be in a Not Ready to Receive mode. The hardware wake-up signal is then defined as a falling edge on the CTS input i.e. a device wakes up the other device by asserting its own Ready to Receive output (i.e. Setting RTS active).

If the LMX5453 redefines the CTS input from flow-control input to wake-up input when the UART has shifted out the last byte of the HCI_COMMAND_COMPLETE (for HCI_DISABLE_TL) event and the host redefines its RTS output when it has received the last byte of the HCI_COMMAND_COMPLETE event there will be a short period of time during which the signalling is ambiguous. To avoid this, delays are introduced as illustrated in Figure 15.

LMX5453 To Host Wake-Up and UART Enable

Because the transport layer can be disabled in any situation, the LMX5453 must first verify that the transport layer is enabled before sending data to the host. Possible scenarios in which the LMX5453 must wake up the host include incoming data or incoming link indicators. If the UART is not enabled, the LMX5453 assumes that it must wake up the host by asserting RTS#. To respond to this assertion, the host must monitor its CTS# input.

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When CTS# is asserted, the host must wake up its UART interface and confirm the UART status by sending the HCI_RTX_WAKEUP_COMPLETE event. This event should not be sent until the HCI transport layer is ready for transferring data. When the host receives the HCI_RTX_WAKEUP_COMPLETE debug event, both sides know that the HCI transport layer is enabled.

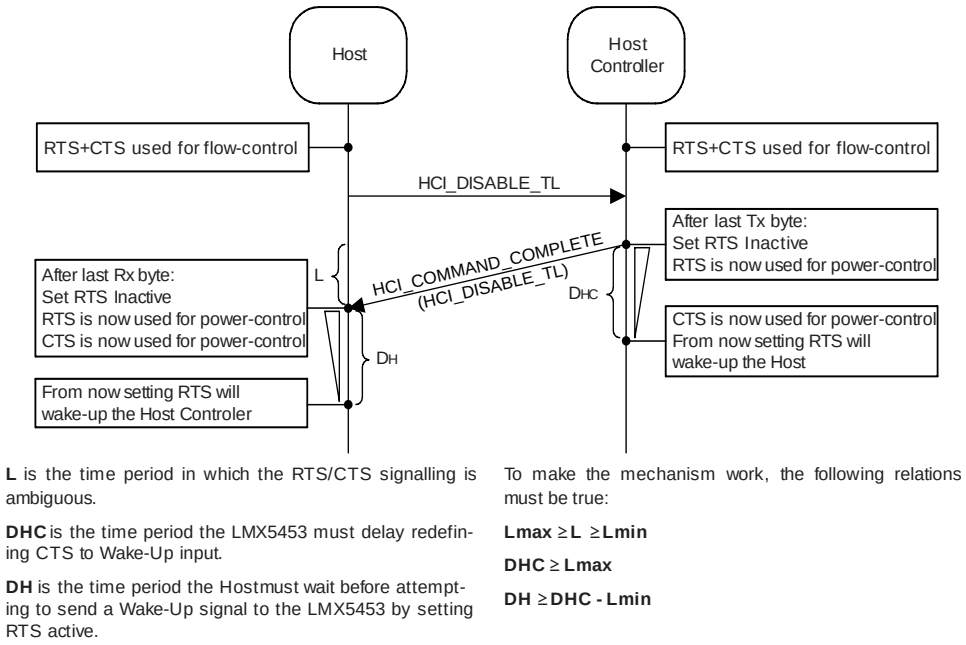


Figure 15. Disabling the UART Transport Layer

The LMX5453 should now send the pending HCI events that triggered the wake-up. See Figure 16 for the complete process.

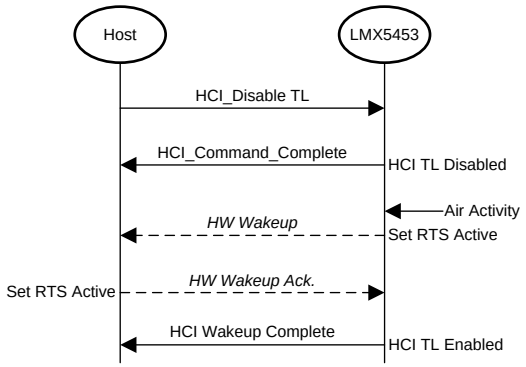


Figure 16. LMX5453 Wake-Up to Host

Host to LMX5453 Wake-Up and UART Enable

If the host needs to send data or commands to the LMX5453 while the UART transport layer is disabled, it must first assume that the LMX5453 is sleeping and wake it up by asserting its RTS signal.

When the LMX5453 detects the wake-up signal, it enables the UART and acknowledges the wake-up signal by asserting its RTS signal. Additionally, the wake up will be confirmed by a confirmation event. When the host has received this HCI_WAKEUP_COMPLETE event, the LMX5453 is ready to receive commands. The host may now send the pending HCI events that triggered the wakeup. See Figure 17 for the complete process.

Note: Even though the LMX5453 sets RTS active (indicating Ready to Receive mode), the host must not send any HCI commands to the LMX5453 before receiving the HCI_WAKEUP_COMPLETE event.

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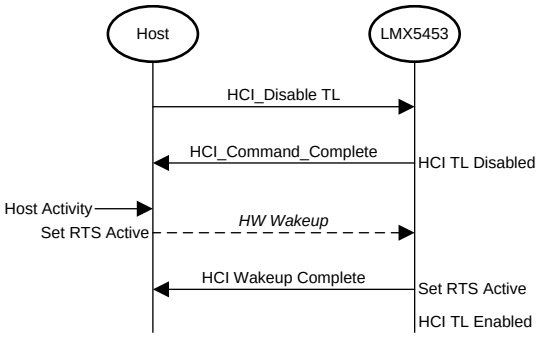
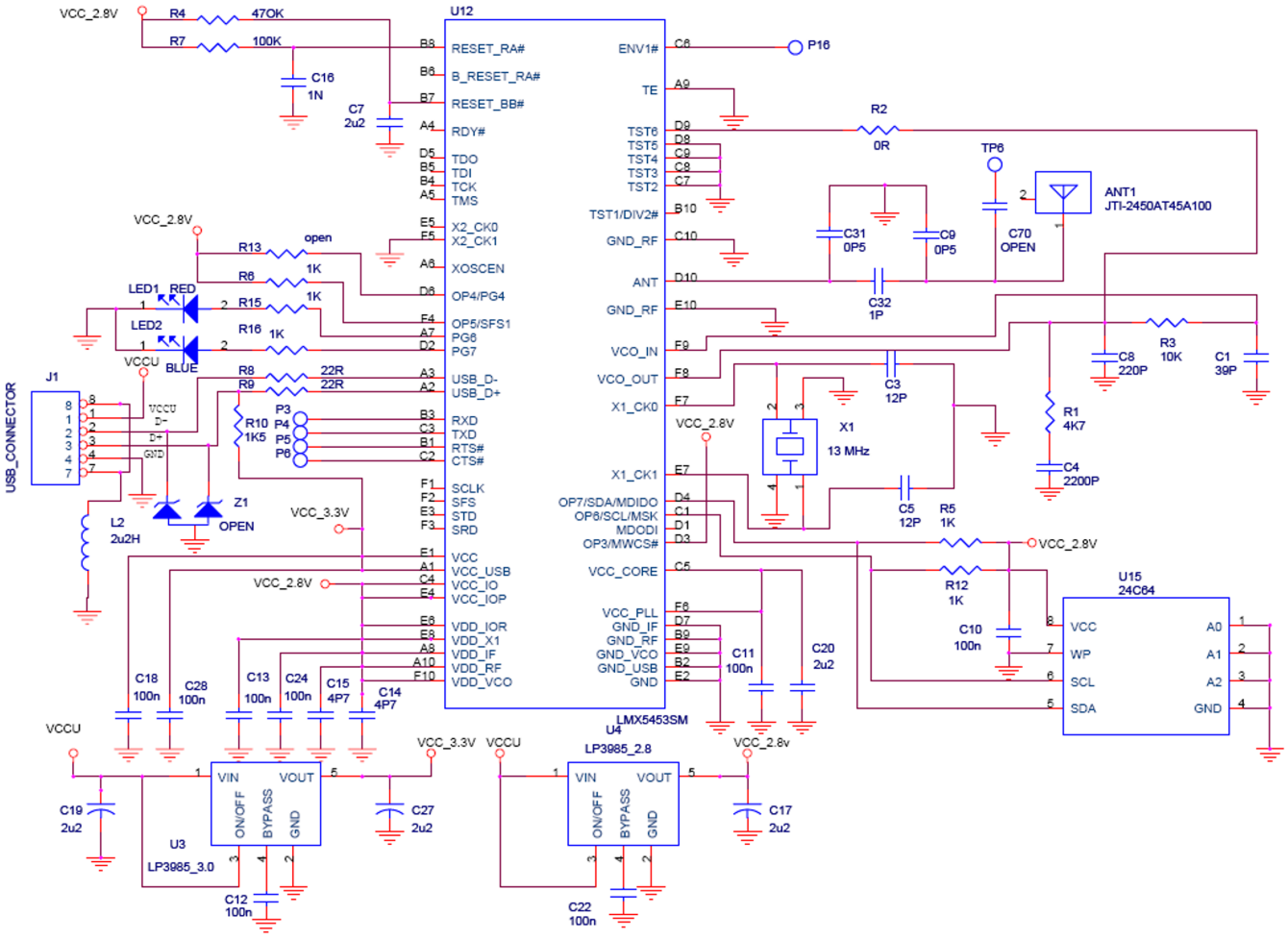


Figure 17. Host Wake-Up to LMX5453

Applications Information

USB Dongle Reference Schematic



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Soldering

The LMX5453 bumps are composed of a solder alloy and reflow (melt and reform) during the Surface Mount Assembly (SMA) process. In order to ensure reflow of all solder bumps and maximum solder joint reliability while minimizing damage to the package, recommended reflow profiles should be used. Table 23, Table 24, and Figure 18 provide the soldering details required to properly solder the LMX5453 to standard PCBs. The illustration serves only as a guide and Texas Instruments is not liable if a selected profile does not work.

Table 23. Soldering Details

Parameter	Value
PCB Land Pad Diameter	13 mil
PCB Solder Mask Opening	19 mil
PCB Finish	Defined by customer or manufacturing facility
Stencil Aperture	17 mil
Stencil Thickness	5 mil
Solder Paste Used	Defined by customer or manufacturing facility
Flux Cleaning Process	Defined by customer or manufacturing facility

Table 24. Classification Reflow Profiles (1)(2)

Profile Feature	NOPB Assembly
Average Ramp-Up Rate (TsMAX to Tp)	
Preheat: Temperature Min (Ts_{MIN}) Temperature Max (Ts_{MAX}) Time (ts_{MIN} to ts_{MAX})	150°C 200°C 60–180 seconds
Time maintained above: Temperature (T_L) Time (t_L)	217°C 60–150 seconds
Peak/Classification Temperature (Tp)	260 + 0°C
Time within 5°C of actual Peak Temperature (tp)	20–40 seconds
Ramp-Down Rate	6°C/second maximum
Time 25°C to Peak Temperature	8 minutes maximum
Reflow Profiles	See Figure 18

(1) See ** IPC/JEDEC J-STD-020C, July 2004.
(2) All temperatures refer to the top side of the package, measured on the package body surface.

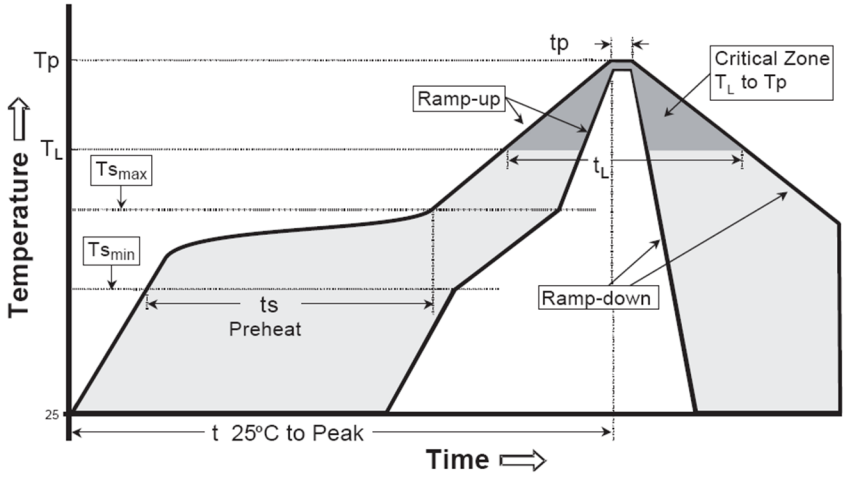


Figure 18. Typical Reflow Profiles

REVISION HISTORY

Changes from Revision C (June 2013) to Revision D	Page
• Added data to Recommended Operating Conditions because data was missing from old National version	6

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMX5453SM/NOPB	NRND	Production	NFBGA (NZB) | 60	320 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-4-260C-72 HR	-40 to 85	5453SM
LMX5453SM/NOPB.A	NRND	Production	NFBGA (NZB) | 60	320 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-4-260C-72 HR	-40 to 85	5453SM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

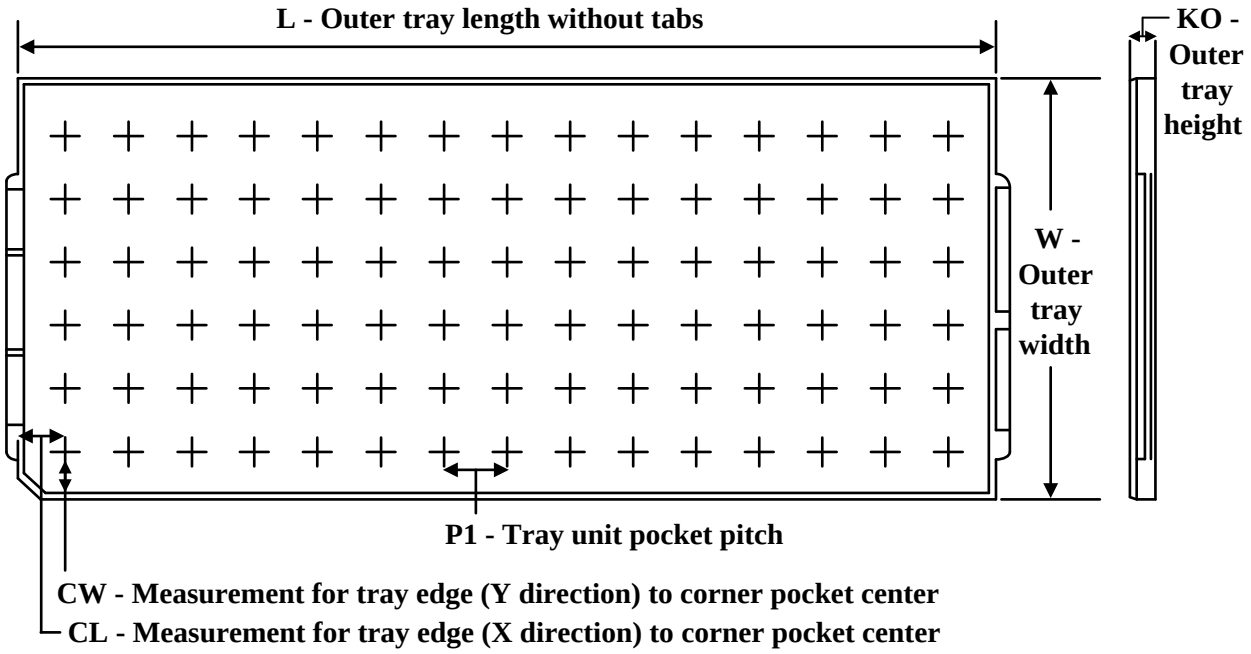
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TRAY

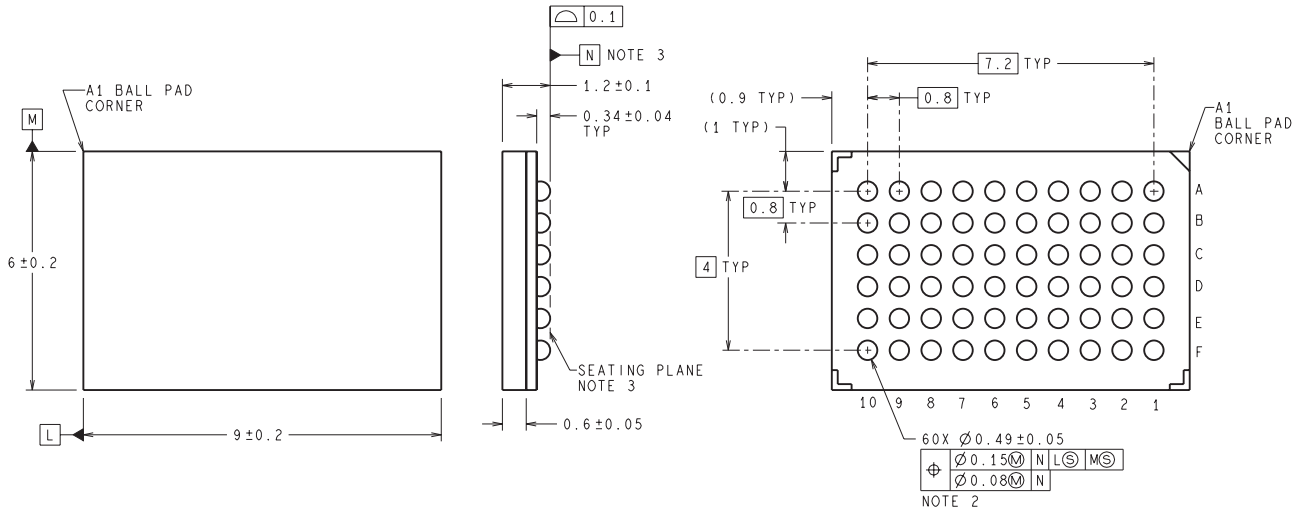


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
LMX5453SM/NOPB	NZB	NFBGA	60	320	10 X 32	150	322.6	135.9	7620	9.4	11.8	16.65
LMX5453SM/NOPB.A	NZB	NFBGA	60	320	10 X 32	150	322.6	135.9	7620	9.4	11.8	16.65

NZB0060A



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