



LMZ31530 30-A Power Module With 3-V to 14.5-V Input in QFN Package

1 Features

- Complete Integrated Power Solution; Smaller than a Discrete Design
- 15 mm × 16 mm × 5.8 mm Package Size
- Pin Compatible with LMZ31520
- Ultra-Fast Load Step Response
- Efficiencies Up To 96%
- Wide-Output Voltage Adjust
0.6 V to 3.6 V, with 1% Reference Accuracy
- Optional Split Power Rails Allows Input Voltage Down to 3 V
- Selectable Switching Frequency;
(300 kHz to 850 kHz)
- Selectable Slow-Start
- Adjustable Over Current Limit
- Power Good Output
- Output Voltage Sequencing
- Over Temperature Protection
- Pre-bias Output Start-up
- Operating Temperature Range: –40°C to 85°C
- Enhanced Thermal Performance: 8.6°C/W
- Meets EN55022 Class A Emissions
- Integrated Shielded Inductor
- Create a Custom Design Using the LMZ31530 With the [WEBENCH® Power Designer](#)

2 Applications

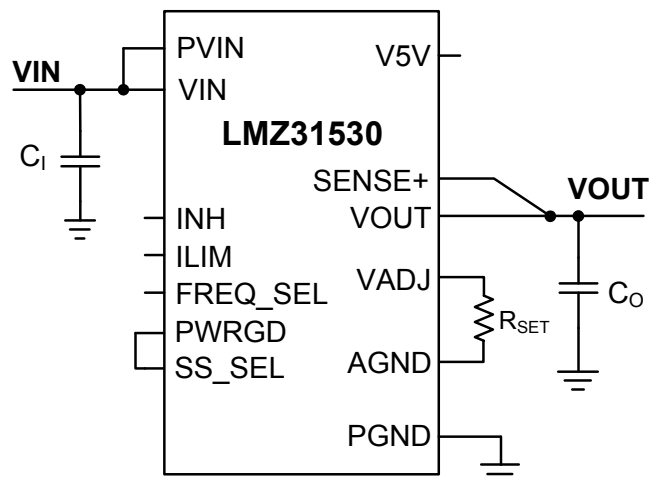
- Broadband and Communications Infrastructure
- DSP and FPGA Point of Load Applications
- High Density Power Systems

3 Description

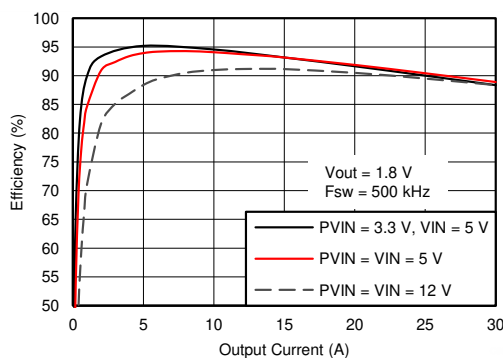
The LMZ31530 power module is an easy-to-use integrated power solution that combines a 30-A DC/DC converter with power MOSFETs, a shielded inductor, and passives into a low profile, QFN package. This total power solution allows as few as three external components and eliminates the loop compensation and magnetics part selection process.

The 15 × 16 × 5.8 mm, QFN package is easy to solder onto a printed circuit board and allows a compact point-of-load design. Achieves greater than 95% efficiency, has ultra-fast load step response and excellent power dissipation capability with a thermal impedance of 8.6°C/W. The LMZ31530 offers the flexibility and the feature-set of a discrete point-of-load design and is ideal for powering a wide range of ICs and systems. Advanced packaging technology affords a robust and reliable power solution compatible with standard QFN mounting and testing techniques.

Simplified Application



Efficiency



4 Specifications

4.1 Absolute Maximum Ratings⁽¹⁾

over operating temperature range (unless otherwise noted)

| | | VALUE | | UNIT |
|--|---|-------|--------------------|------|
| | | MIN | MAX | |
| Input Voltage | V _{IN} , P _{VIN} | −0.3 | 20 | V |
| | INH, V _{ADJ} , P _{WRGD} , P _{WRGD_PU} , I _{LIM} , FREQ_SEL, SS_SEL, V _{5V} | −0.3 | 7 | V |
| Output Voltage | PH | −1 | 25 | V |
| | PH 10ns Transient | −2 | 27 | |
| | V _{OUT} | −0.3 | 6 | V |
| V _{DIFF} (GND to exposed thermal pad) | | | ±200 | mV |
| Operating Junction Temperature | | −40 | 125 ⁽²⁾ | °C |
| Storage Temperature | | −55 | 150 | °C |
| Peak Reflow Case Temperature ⁽³⁾ | | | 245 ⁽⁴⁾ | °C |
| Maximum Number of Reflows Allowed ⁽³⁾ | | | 3 ⁽⁴⁾ | |
| Mechanical Shock | Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted | | 250 | G |
| Mechanical Vibration | Mil-STD-883D, Method 2007.2, 20-2000Hz | | 20 | |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) See the temperature derating curves in the Typical Characteristics section for thermal information.

(3) For soldering specifications, refer to the [Soldering Requirements for BQFN Packages](#) application note.

(4) Devices with a date code prior to week 14 2018 (1814) have a peak reflow case temperature of 240°C with a maximum of one reflow

4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------|-------------------------|-----|------|------|
| PV _{IN} | Input Switching Voltage | | 14.5 | V |
| V _{IN} | Input Bias Voltage | 4.5 | 14.5 | V |
| V _{OUT} | Output Voltage | 0.6 | 3.6 | V |
| f _{SW} | Switching Frequency | 300 | 850 | kHz |

4.3 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | | LMZ31530 | UNIT |
|-------------------------------|---|--------------------|----------|------|
| | | | RLG | |
| | | | 72 PINS | |
| θ_{JA} | Junction-to-ambient thermal resistance ⁽²⁾ | Natural Convection | 8.6 | °C/W |
| $\theta_{JA(100LFM)}$ | Junction-to-ambient thermal resistance ⁽³⁾ | 100 LFM | 7.8 | °C/W |
| ψ_{JT} | Junction-to-top characterization parameter ⁽⁴⁾ | | 1.6 | °C/W |
| ψ_{JB} | Junction-to-board characterization parameter ⁽⁵⁾ | | 4.2 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) The junction-to-ambient thermal resistance, θ_{JA} , applies to devices soldered directly to a 100 mm x 100 mm, 6-layer PCB with 1 oz. copper and natural convection cooling. Additional airflow reduces θ_{JA} .
- (3) The junction-to-ambient thermal resistance, θ_{JA} , applies to devices soldered directly to a 100 mm x 100 mm, 6-layer PCB with 1 oz. copper and 100 LFM forced air cooling. Additional airflow reduces θ_{JA} .
- (4) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature, T_J , of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JT} * P_{dis} + T_T$; where P_{dis} is the power dissipated in the device and T_T is the temperature of the top of the device.
- (5) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature, T_J , of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} * P_{dis} + T_B$; where P_{dis} is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

4.4 Package Specifications

| LMZ31530 | | UNIT |
|-----------------------------|---|------------|
| Weight | | 4.96 grams |
| Flammability | Meets UL 94 V-O | |
| MTBF Calculated reliability | Per Bellcore TR-332, 50% stress, $T_A = 40^\circ\text{C}$, ground benign | 26.5 Mhrs |

4.5 Electrical Characteristics

 $T_A = -40^\circ\text{C}$ to 85°C , $P_{VIN} = V_{IN} = 12\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 30\text{ A}$
 $C_{IN} = 2 \times 22\text{ }\mu\text{F}$ ceramic and $330\text{ }\mu\text{F}$ bulk, $C_{OUT} = 4 \times 100\text{ }\mu\text{F}$ ceramic (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|--------------------------------|---|------------------|--------------|----------------------------|------|
| I_{OUT} | Output current | | 0 | | 30 | A |
| V_{IN} | Input bias voltage range | Over I_{OUT} range | 4.5 | | 14.5 | V |
| P_{VIN} | Input switching voltage range | Over I_{OUT} range | 3 ⁽¹⁾ | | 14.5 | V |
| UVLO | VIN Undervoltage lockout | V_{IN} Increasing | 4.0 | 4.2 | 4.33 | V |
| | | Hysteresis | | 0.25 | | |
| $V_{OUT(adj)}$ | Output voltage adjust range | Over I_{OUT} range | 0.6 | | 3.6 | V |
| V_{OUT} | Set-point voltage tolerance | | | | $\pm 1.0\%$ ⁽²⁾ | |
| | Temperature variation | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ | | $\pm 0.25\%$ | | |
| | Load regulation | Over I_{OUT} range | | $+0.4\%$ | | |
| | Total output voltage variation | Includes set-point, load, and temperature variation | | | $\pm 2.0\%$ ⁽²⁾ | |
| Line regulation | | $P_{VIN} \pm 10\%$ | | $\pm 0.1\%$ | | |
| | | Over P_{VIN} range | | $\pm 0.7\%$ | | |

(1) The minimum P_{VIN} voltage is 3.0V or ($V_{OUT} + 1.1\text{V}$), whichever is greater. See [VIN and PVIN Input Voltage](#) for more details.

(2) The stated limit of the set-point voltage tolerance includes the tolerance of both the internal voltage reference and the internal adjustment resistor. The overall output voltage tolerance will be affected by the tolerance of the external R_{SET} resistor.

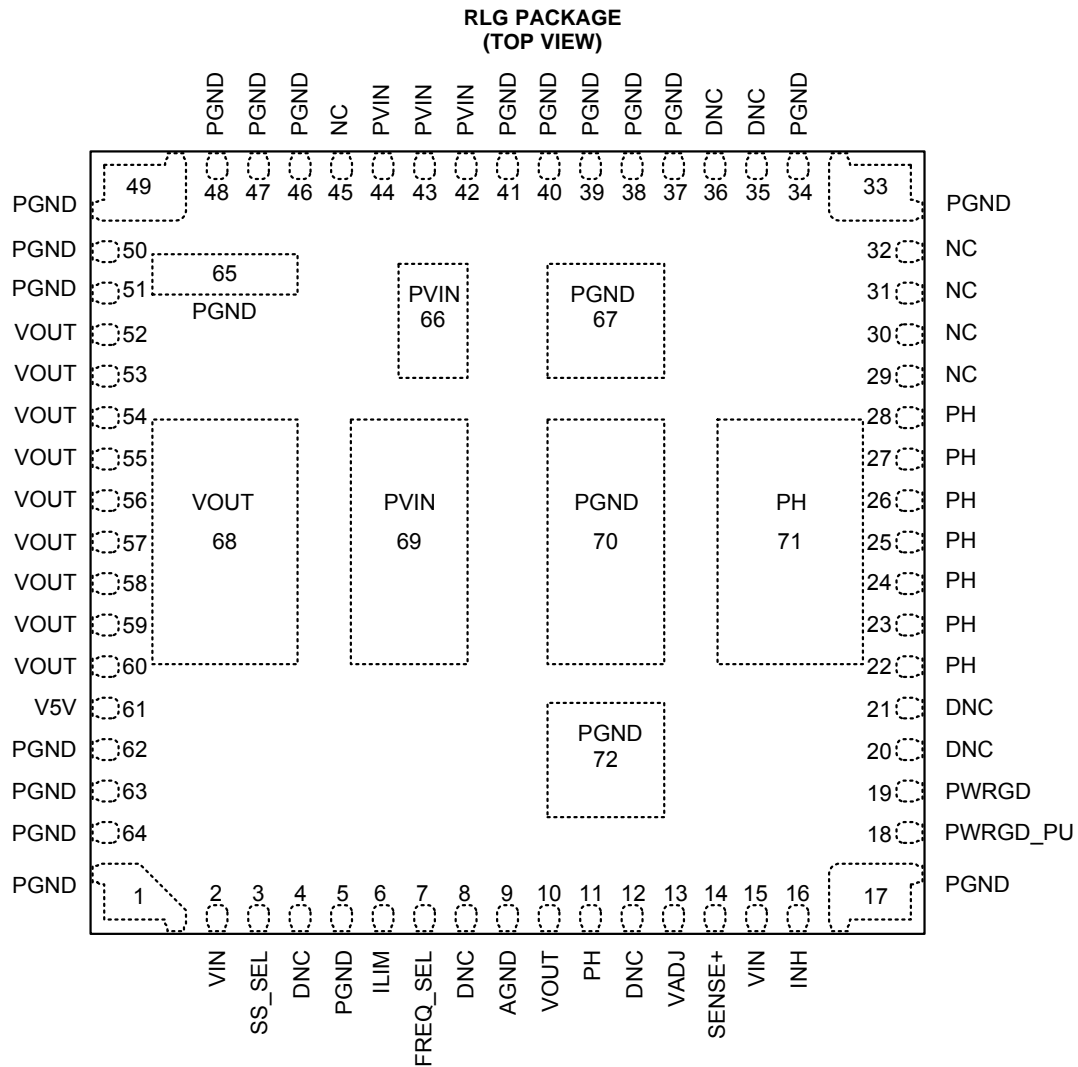
Electrical Characteristics (continued)

 $T_A = -40^{\circ}\text{C}$ to 85°C , $P_{VIN} = V_{IN} = 12\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 30\text{ A}$
 $C_{IN} = 2 \times 22\text{ }\mu\text{F}$ ceramic and $330\text{ }\mu\text{F}$ bulk, $C_{OUT} = 4 \times 100\text{ }\mu\text{F}$ ceramic (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------------------|---------------------------------|---|--|--------------------|-----|---------------------|--------------------|
| η | Efficiency | $P_{VIN} = V_{IN} = 12\text{ V}$ $I_O = 15\text{ A}$ | $V_{OUT} = 3.3\text{ V}, f_{SW} = 500\text{kHz}$ | | 94 | | % |
| | | | $V_{OUT} = 1.8\text{ V}, f_{SW} = 500\text{kHz}$ | | 92 | | |
| | | | $V_{OUT} = 1.2\text{ V}, f_{SW} = 500\text{kHz}$ | | 88 | | |
| | | | $V_{OUT} = 0.9\text{ V}, f_{SW} = 500\text{kHz}$ | | 86 | | |
| | | | $V_{OUT} = 0.6\text{ V}, f_{SW} = 500\text{kHz}$ | | 82 | | |
| | | $P_{VIN} = V_{IN} = 5\text{ V}$ $I_O = 15\text{ A}$ | $V_{OUT} = 3.3\text{ V}, f_{SW} = 500\text{kHz}$ | | 96 | | % |
| | | | $V_{OUT} = 1.8\text{ V}, f_{SW} = 500\text{kHz}$ | | 94 | | |
| | | | $V_{OUT} = 1.2\text{ V}, f_{SW} = 500\text{kHz}$ | | 91 | | |
| | | | $V_{OUT} = 0.9\text{ V}, f_{SW} = 500\text{kHz}$ | | 88 | | |
| | | | $V_{OUT} = 0.6\text{ V}, f_{SW} = 500\text{kHz}$ | | 85 | | |
| Output voltage ripple | | 20 MHz bandwidth | | | 1% | | VOUT |
| I_{LIM} | Current limit threshold | | | | 40 | | A |
| Transient response | | 2.5 A/ μs load step from 25 to 75% $I_{OUT(max)}$ | Recovery time | | 30 | | μs |
| | | | VOUT over/undershoot | | 30 | | mV |
| V_{INH} | Inhibit Control | Inhibit High Voltage | | 1.8 | | Open ⁽³⁾ | V |
| | | Inhibit Low Voltage | | -0.3 | | 0.6 | V |
| $I_{IN(stby)}$ | VIN standby current | INH pin to AGND | $V_{IN} = 5\text{ V}$ | | 0.5 | 0.7 | mA |
| | | | $V_{IN} = 12\text{ V}$ | | 1.2 | 1.5 | mA |
| Power Good | PWRGD Thresholds | V_{OUT} rising | Good | | 95 | | % |
| | | | Fault | | 115 | | |
| | | V_{OUT} falling | Fault | | 90 | | |
| | | | Good | | 110 | | |
| | | PWRGD Low Voltage | $I(PWRGD) = 2\text{ mA}$ | | | 0.2 | 0.3 |
| f_{SW} | Switching frequency | FREQ_SEL pin OPEN, $I_{OUT} = 10\text{ A}$ | | 470 | 520 | 570 | kHz |
| f_{SEL} | Frequency Select ⁽⁴⁾ | 66 k Ω resistor between FREQ_SEL pin and PGND | | | 300 | | kHz |
| | | FREQ_SEL pin connected to V5V (pin 61) | | | 850 | | kHz |
| Thermal Shutdown | | Thermal shutdown | | | 145 | | $^{\circ}\text{C}$ |
| | | Thermal shutdown hysteresis | | | 10 | | $^{\circ}\text{C}$ |
| C_{IN} | External input capacitance | Ceramic | | 44 ⁽⁵⁾ | 94 | | μF |
| | | Non-ceramic | | | 330 | | |
| C_{OUT} | External output capacitance | | | 100 ⁽⁶⁾ | 400 | 5000 | μF |

- (3) This pin has an internal pull-up. If this pin is left open circuit, the device operates when a valid input voltage is applied. A small, low-leakage (<300nA) MOSFET is recommended for control.
- (4) See the [Frequency Select](#) section for more information on selecting the frequency.
- (5) A minimum of 44 μF (2x 22 μF) of external ceramic capacitance is required across the input (P_{VIN}/V_{IN} and PGND connected) for proper operation. Locate the capacitor close to the device. See [Table 3](#) for more details. When operating with split VIN and P_{VIN} rails, place 4.7 μF of ceramic capacitance directly at the VIN pin to PGND.
- (6) A minimum of 100 μF of ceramic capacitance is required at the output. Locate the capacitance close to the device. Adding additional capacitance close to the load improves the response of the regulator to load transients and reduces ripple. See [Table 3](#) for more details.

5 Device Information



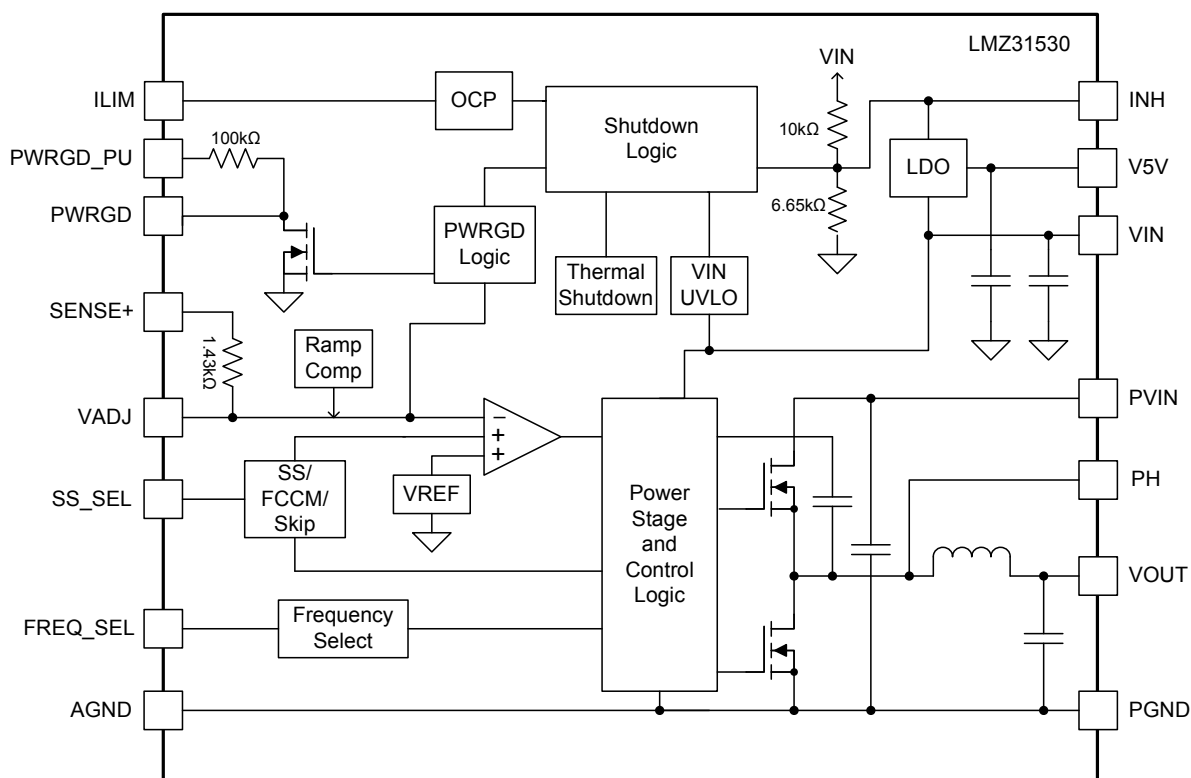
Pin Functions

| TERMINAL | | DESCRIPTION |
|----------|-----|---|
| NAME | NO. | |
| AGND | 9 | This pin is connected internally to the power ground of the device. This pin should only be used as the zero volt ground reference for connecting the voltage setting resistor (R_{SET}). Do not connect AGND to PGND. See Layout Recommendations. |
| DNC | 4 | Do Not Connect. Do not connect these pins to AGND, to another DNC pin, or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad. |
| | 8 | |
| | 12 | |
| | 20 | |
| | 21 | |
| | 35 | |
| | 36 | |
| FREQ_SEL | 7 | Frequency Select pin. Leave this pin open (floating) to select 500 kHz (typ) operating frequency. Connect this pin to V5V pin to select 850 kHz (typ) operating frequency. Connect a 66 k Ω resistor between this pin and PGND to select 300 kHz (typ) operating frequency. See Table 2 for more info. |
| ILIM | 6 | Current limit setting pin. Connecting a resistor between this pin and PGND sets the current limit. When left open, refer to the Electrical Characterization table for current limit value. |
| INH | 16 | Inhibit pin. Use an open drain or open collector logic device to ground this pin to control the INH function. |
| NC | 29 | Not Connected. These pins are internally isolated from any signal and all other pins. Each pin must be soldered to a pad on the PCB. These pins can be left isolated, connected to one another, or connected to any signal on the PCB. |
| | 30 | |
| | 31 | |
| | 32 | |
| | 45 | |
| PGND | 1 | This is the return current path for the power stage of the device. Connect these pins to the load and to the bypass capacitors associated with VIN and VOUT. Pads 65, 67, 70, and 72 should be connected to PCB ground planes using multiple vias for good thermal performance. Not all pins are connected together internally. All pins must be connected together externally with a copper plane or pour directly under the device. |
| | 5 | |
| | 17 | |
| | 33 | |
| | 34 | |
| | 37 | |
| | 38 | |
| | 39 | |
| | 40 | |
| | 41 | |
| | 46 | |
| | 47 | |
| | 48 | |
| | 49 | |
| | 50 | |
| | 51 | |
| | 62 | |
| | 63 | |
| | 64 | |
| | 65 | |
| | 67 | |
| | 70 | |
| | 72 | |

Pin Functions (continued)

| TERMINAL | | DESCRIPTION |
|----------|-----|--|
| NAME | NO. | |
| PH | 11 | Phase switch node. Do not place any external component on these pins or tie them to a pin of another function. Connect these pins using a copper area beneath pad 71. |
| | 22 | |
| | 23 | |
| | 24 | |
| | 25 | |
| | 26 | |
| | 27 | |
| | 28 | |
| | 71 | |
| PVIN | 42 | Input switching voltage pin. This pin supplies voltage to the power switches of the converter. |
| | 43 | |
| | 44 | |
| | 66 | |
| | 69 | |
| PWRGD | 19 | Power Good flag pin. This open drain output asserts low if the output voltage is more than approximately $\pm 6\%$ out of regulation. |
| PWRGD_PU | 18 | Power Good pull-up pin. This pin is connected to a 100k Ω resistor which is tied to the PWRGD pin internally. Connect this pin to V5V or to any voltage between 1.3V and 6.5V. |
| SENSE+ | 14 | Remote sense connection. Connect this pin to VOUT at the load for improved regulation. This pin must be connected to VOUT at the load, or at the module pins. |
| SS_SEL | 3 | Slow-start select pin. Connect a resistor between this pin and PWRGD (or PGND) to select the slow-start time. See the SS_SEL section of the datasheet for slow-start times and corresponding resistor values. Connect the SS_SEL pin to PGND to select Auto-skip Eco-mode or to the PWRGD pin (pin 19) to select FCCM. |
| V5V | 61 | 5V regulator pin. This regulator supplies the internal circuitry. |
| VADJ | 13 | Output voltage adjust pin. Connecting a resistor between this pin and AGND sets the output voltage. |
| VIN | 2 | Input bias voltage pins. Supplies the control circuitry of the power converter. |
| | 15 | |
| VOUT | 10 | Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external bypass capacitors between these pins and PGND. |
| | 52 | |
| | 53 | |
| | 54 | |
| | 55 | |
| | 56 | |
| | 57 | |
| | 58 | |
| | 59 | |
| | 60 | |
| | 68 | |

Functional Block Diagram



6 Typical Characteristics (PVIN = VIN = 12 V)

The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3. The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm six-layer PCB with 1 oz. copper. Applies to Figure 4, Figure 5, and Figure 6.

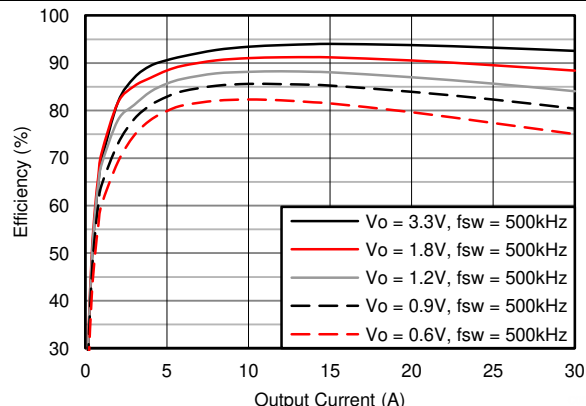


Figure 1. Efficiency vs. Output Current

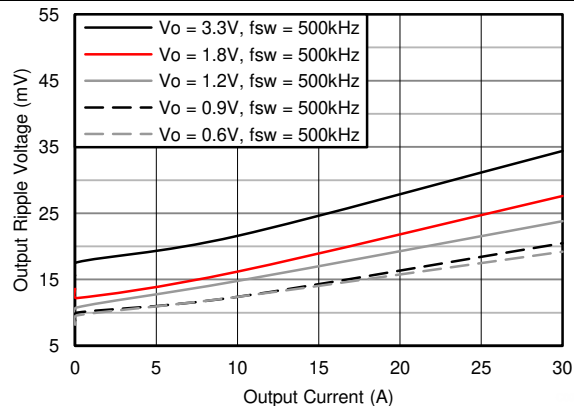


Figure 2. Voltage Ripple vs. Output Current

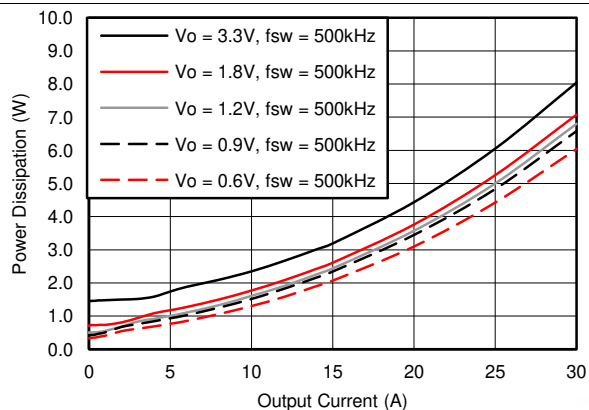


Figure 3. Power Dissipation vs. Output Current

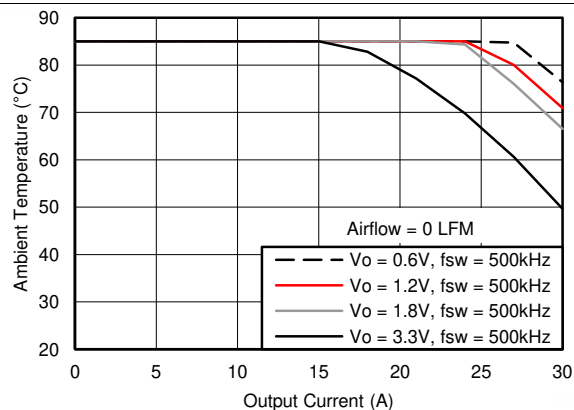


Figure 4. Safe Operating Area (0 LFM)

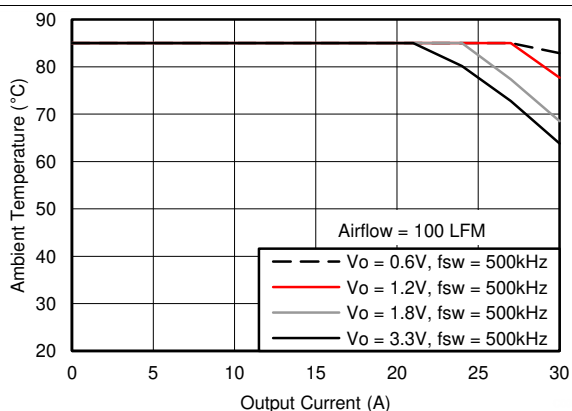


Figure 5. Safe Operating Area (100 LFM)

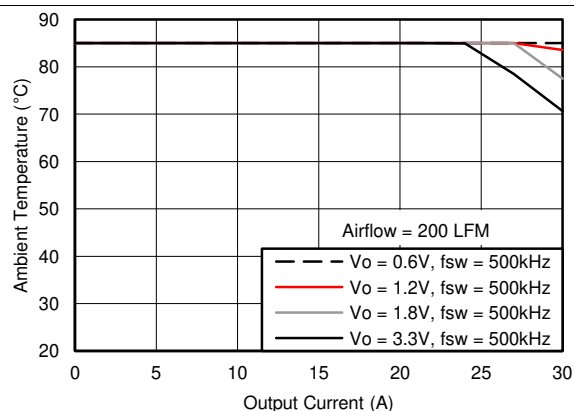
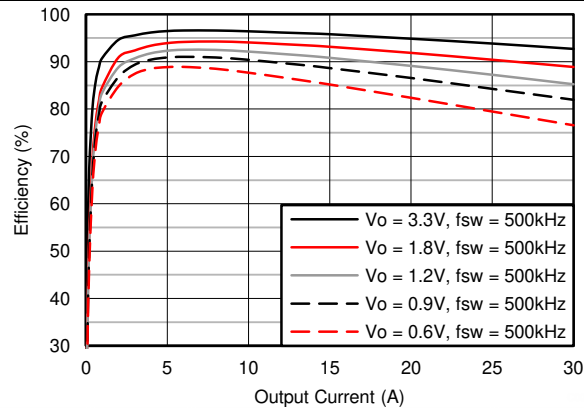
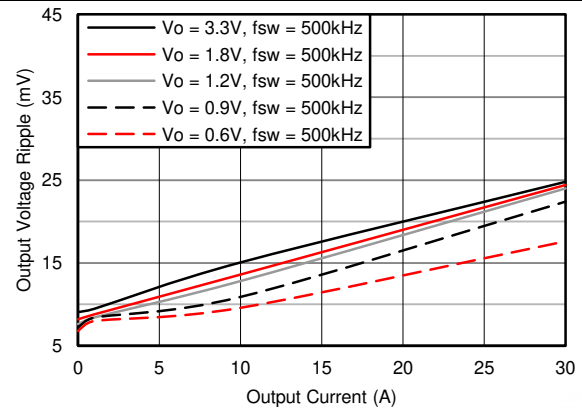
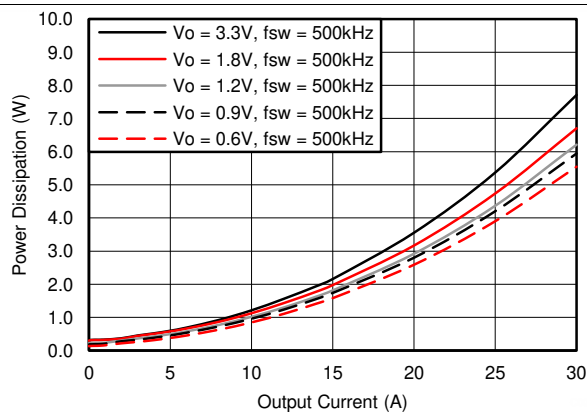
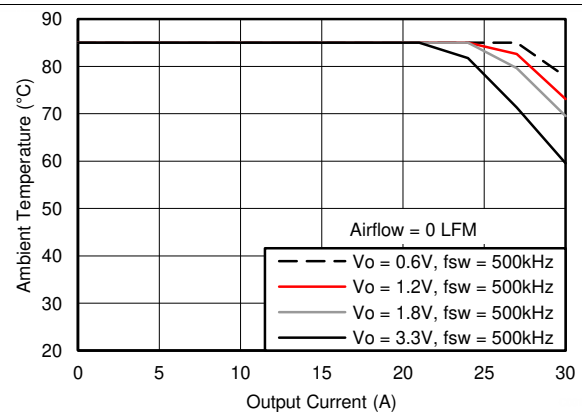
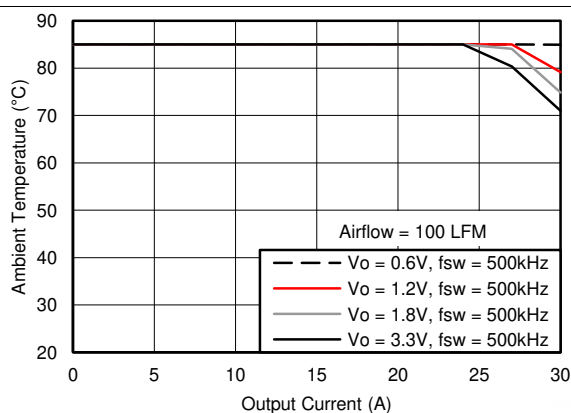
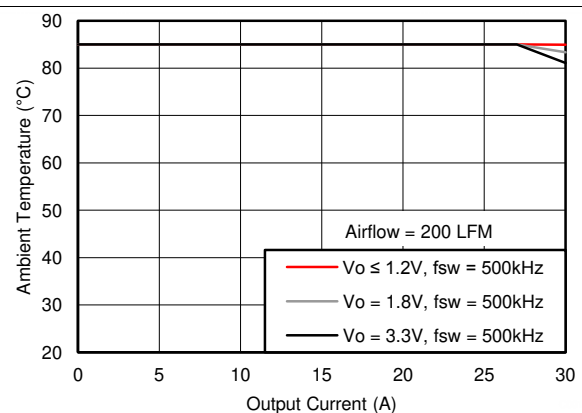


Figure 6. Safe Operating Area (200 LFM)

7 Typical Characteristics (P_{VIN} = V_{IN} = 5 V)

The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to [Figure 7](#), [Figure 8](#), and [Figure 9](#). The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm six-layer PCB with 1 oz. copper. Applies to [Figure 10](#), [Figure 11](#), and [Figure 12](#).


Figure 7. Efficiency vs. Output Current

Figure 8. Voltage Ripple vs. Output Current

Figure 9. Power Dissipation vs. Output Current

Figure 10. Safe Operating Area (0 LFM)

Figure 11. Safe Operating Area (100 LFM)

Figure 12. Safe Operating Area (200 LFM)

8 Application Information

8.1 Adjusting the Output Voltage

The VADJ control sets the output voltage of the LMZ31530. The output voltage adjustment range is from 0.6V to 3.6V. The adjustment method requires the addition of R_{SET} , which sets the output voltage, and the connection of SENSE+ to VOUT. The R_{SET} resistor must be connected directly between the VADJ (pin 13) and AGND (pin 9). The SENSE+ pin (pin 14) must be connected to VOUT either at the load for improved regulation or at VOUT of the device.

The LMZ31530 relies on a precision trimmed 0.6 V reference for the feedback voltage regulation and operates by regulating the valley of the voltage ripple appearing at the VADJ pin. The voltage ripple is a function of the input voltage and the output voltage, therefore the R_{SET} resistor will change based on the input voltage. [Table 1](#) gives the calculated external R_{SET} resistor for a number of common bus voltages for PVIN of 12 V, 5 V, and 3.3 V. The recommended switching frequency is 500 kHz which can be configured by leaving the FREQ_SEL pin open. To adjust the frequency, see [Table 2](#).

Table 1. R_{SET} Resistor Values

| V_{OUT} (V) | R_{SET} (Ω) | | | V_{OUT} (V) | R_{SET} (Ω) | | |
|---------------|------------------------|------------|--------------|---------------|------------------------|------------|--------------|
| | PVIN = 12 V | PVIN = 5 V | PVIN = 3.3 V | | PVIN = 12 V | PVIN = 5 V | PVIN = 3.3 V |
| 0.60 | open | open | open | 2.15 | 566 | 563 | 560 |
| 0.65 | 18787 | 18681 | 18588 | 2.20 | 548 | 545 | 542 |
| 0.70 | 9024 | 8993 | 8966 | 2.25 | 532 | 528 | 525 |
| 0.75 | 5939 | 5923 | 5908 | 2.30 | 516 | 513 | 510 |
| 0.80 | 4427 | 4416 | 4406 | 2.35 | 502 | 498 | 495 |
| 0.85 | 3529 | 3521 | 3513 | 2.40 | 488 | 484 | 481 |
| 0.90 | 2934 | 2927 | 2921 | 2.45 | 475 | 471 | 468 |
| 0.95 | 2511 | 2505 | 2500 | 2.50 | 462 | 459 | 456 |
| 1.00 | 2195 | 2190 | 2185 | 2.55 | 451 | 447 | 444 |
| 1.05 | 1950 | 1945 | 1941 | 2.60 | 439 | 436 | 433 |
| 1.10 | 1754 | 1749 | 1745 | 2.65 | 429 | 425 | 422 |
| 1.15 | 1594 | 1589 | 1586 | 2.70 | 419 | 415 | 412 |
| 1.20 | 1460 | 1456 | 1453 | 2.75 | 409 | 405 | 402 |
| 1.25 | 1348 | 1344 | 1341 | 2.80 | 400 | 396 | 393 |
| 1.30 | 1251 | 1248 | 1244 | 2.85 | 391 | 387 | 384 |
| 1.35 | 1168 | 1164 | 1161 | 2.90 | 382 | 379 | 375 |
| 1.40 | 1095 | 1091 | 1088 | 2.95 | 374 | 370 | 367 |
| 1.45 | 1031 | 1027 | 1024 | 3.00 | 367 | 363 | 359 |
| 1.50 | 973 | 970 | 968 | 3.05 | 359 | 355 | 352 |
| 1.55 | 922 | 919 | 916 | 3.10 | 352 | 348 | 345 |
| 1.60 | 876 | 873 | 870 | 3.15 | 345 | 341 | 338 |
| 1.65 | 834 | 831 | 828 | 3.20 | 339 | 335 | 331 |
| 1.70 | 797 | 793 | 790 | 3.25 | 332 | 328 | 325 |
| 1.75 | 762 | 759 | 756 | 3.30 | 326 | 322 | 318 |
| 1.80 | 730 | 727 | 724 | 3.35 | 320 | 316 | 312 |
| 1.85 | 701 | 698 | 695 | 3.40 | 315 | 310 | 307 |
| 1.90 | 674 | 671 | 668 | 3.45 | 309 | 305 | 301 |
| 1.95 | 650 | 646 | 643 | 3.50 | 304 | 300 | 296 |
| 2.00 | 626 | 623 | 620 | 3.55 | 299 | 294 | 291 |
| 2.05 | 605 | 602 | 599 | 3.60 | 294 | 289 | 286 |
| 2.10 | 585 | 581 | 578 | | | | |

8.2 Frequency Select

The LMZ31530 switching frequency can be selected from several values as shown in [Table 2](#). To select a switching frequency, a resistor (R_{FREQ}) must be connected between the FREQ_SEL pin and either PGND or V5V (pin 61) as shown in [Table 2](#). For all output voltages, the recommended switching frequency is 500 kHz which can be configured by leaving the FREQ_SEL pin open. [Table 2](#) also shows the output voltage range for each frequency.

Table 2. Frequency Selection

| Frequency Select (kHz) | R_{FREQ} (k Ω) | Connect To | V _{OUT} RANGE (V) | |
|------------------------|--------------------------|------------|----------------------------|-----|
| | | | MIN | MAX |
| 300 | 66 | PGND | 0.6 | 3.6 |
| 400 | 498 | PGND | 0.6 | 3.6 |
| 500 | open | - | 0.6 | 3.6 |
| 650 | 745 | V5V | 0.8 | 3.6 |
| 750 | 188 | V5V | 1.0 | 3.6 |
| 850 | short | V5V | 1.2 | 3.6 |

8.3 Capacitor Recommendations for the LMZ31530 Power Supply

8.3.1 Capacitor Technologies

8.3.1.1 Electrolytic, Polymer-Electrolytic Capacitors

Aluminum electrolytic capacitors provide adequate decoupling over the frequency range of 2 kHz to 150 kHz. When using electrolytic capacitors, high-quality, polymer-electrolytic capacitors are recommended. Polymer-electrolytic type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Panasonic OS-CON capacitor series is suggested due to the lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size.

8.3.1.2 Ceramic Capacitors

The performance of ceramic capacitors is most effective above 150 kHz. Multilayer ceramic capacitors have a low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output.

8.3.1.3 Tantalum, Polymer-Tantalum Capacitors

Polymer-tantalum type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Panasonic POSCAP series and Kemet T530 capacitor series are recommended rather than many other tantalum types due to their lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

8.3.2 Input Capacitor

The LMZ31530 requires a minimum input capacitance of 44 μ F of ceramic type. The voltage rating of input capacitors must be greater than the maximum input voltage. The input RMS ripple current is a function of the output current and the duty cycle for any application. The input capacitor must be rated for the application's RMS ripple current. [Table 3](#) includes a preferred list of capacitors by vendor.

8.3.3 Output Capacitor

The required output capacitance of the LMZ31530 can be comprised of either all ceramic capacitors, or a combination of ceramic and bulk capacitors. The required output capacitance must include at least 100 μ F of ceramic type. When adding additional non-ceramic bulk capacitors, low-ESR devices like the ones recommended in [Table 3](#) are required. The required capacitance above the minimum is determined by actual transient deviation requirements. See [Table 4](#) for typical transient response values for several output voltage, input voltage and capacitance combinations. [Table 3](#) includes a preferred list of capacitors by vendor.

Capacitor Recommendations for the LMZ31530 Power Supply (continued)

Table 3. Recommended Input/Output Capacitors⁽¹⁾

| VENDOR | SERIES | PART NUMBER | CAPACITOR CHARACTERISTICS | | |
|-----------|--------|--------------------|---------------------------|------------------|-------------------------|
| | | | WORKING VOLTAGE (V) | CAPACITANCE (μF) | ESR ⁽²⁾ (mΩ) |
| Murata | X5R | GRM32ER61E226K | 25 | 22 | 2 |
| TDK | X5R | C3216X5R1E476M | 25 | 47 | 2 |
| TDK | X5R | C3216X5R1C476M | 16 | 47 | 2 |
| Murata | X5R | GRM32ER61C476M | 16 | 47 | 2 |
| TDK | X5R | C3225X5R0J107M | 6.3 | 100 | 2 |
| Murata | X5R | GRM32ER60J107M | 6.3 | 100 | 2 |
| TDK | X5R | C3225X5R0J476K | 6.3 | 47 | 2 |
| Murata | X5R | GRM32ER60J476M | 6.3 | 47 | 2 |
| Panasonic | EEH-ZA | EEH-ZA1E101XP | 25 | 100 | 30 |
| Kemet | T520 | T520V107M010ASE025 | 10 | 100 | 25 |
| Panasonic | POSCAP | 6TPE100MI | 6.3 | 100 | 25 |
| Panasonic | POSCAP | 2R5TPE220M7 | 2.5 | 220 | 7 |
| Kemet | T530 | T530D227M006ATE006 | 6.3 | 220 | 6 |
| Kemet | T530 | T530D337M006ATE010 | 6.3 | 330 | 10 |
| Panasonic | POSCAP | 2TPF330M6 | 2.0 | 330 | 6 |
| Panasonic | POSCAP | 6TPE330MFL | 6.3 | 330 | 15 |

(1) **Capacitor Supplier Verification, RoHS, Lead-free and Material Details**

Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.

(2) Maximum ESR @ 100kHz, 25°C.

8.4 Transient Response

The LMZ31530 is designed to have an ultra-fast load step response with minimal output capacitance. [Table 4](#) shows the voltage deviation and recovery time for several different transient conditions. Several waveforms are shown in [Application Curves](#).

Table 4. Output Voltage Transient Response

| C _{IN1} = 3 x 47 μF CERAMIC | | | | | | |
|--------------------------------------|---------------------|---------------------------|------------------------|--------------------------|--------------------------|--------------------|
| V _{OUT} (V) | V _{IN} (V) | C _{OUT1} Ceramic | C _{OUT2} BULK | VOLTAGE DEVIATION (mV) | | RECOVERY TIME (μs) |
| | | | | 10 A LOAD STEP, (1 A/μs) | 15 A LOAD STEP, (1 A/μs) | |
| 0.6 | 5 | 500 μF | - | 15 | 18 | 35 |
| | 12 | 500 μF | - | 15 | 20 | 35 |
| 0.9 | 5 | 500 μF | - | 15 | 18 | 40 |
| | | 500 μF | 470 μF | 12 | 15 | 40 |
| | 12 | 500 μF | - | 20 | 25 | 40 |
| | | 500 μF | 470 μF | 16 | 22 | 40 |
| 1.2 | 5 | 500 μF | - | 20 | 25 | 40 |
| | | 500 μF | 330 μF | 15 | 22 | 40 |
| | 12 | 500 μF | - | 20 | 25 | 40 |
| | | 500 μF | 330 μF | 16 | 24 | 40 |
| 1.8 | 5 | 500 μF | - | 20 | 30 | 40 |
| | | 500 μF | 330 μF | 16 | 25 | 40 |
| | 12 | 500 μF | - | 20 | 30 | 40 |
| | | 500 μF | 330 μF | 16 | 25 | 45 |
| 3.3 | 5 | 500 μF | - | 25 | 40 | 50 |
| | 12 | 500 μF | - | 25 | 35 | 50 |

8.5 Application Curves

Device configured for FCCM mode of operation, (pin 3 connected to pin 19).

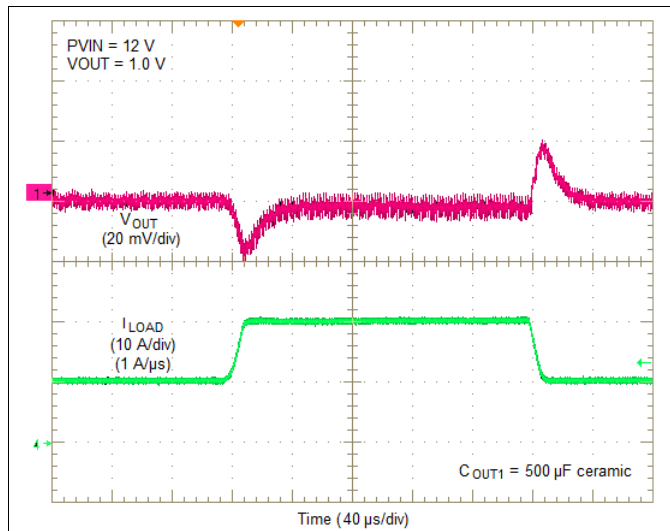


Figure 13. P_{VIN} = 12V, V_{OUT} = 1.0V, 10A Load Step

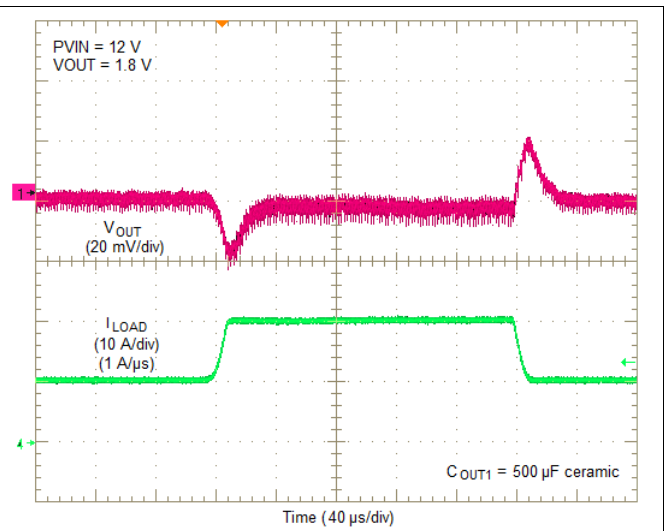


Figure 14. P_{VIN} = 12V, V_{OUT} = 1.8V, 10A Load Step

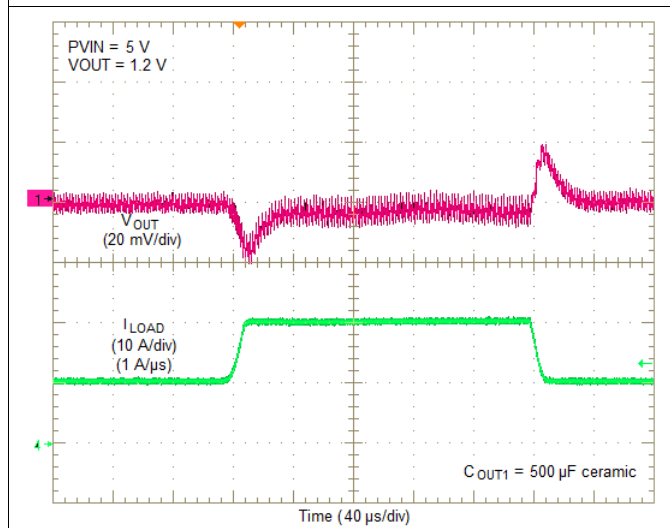


Figure 15. P_{VIN} = 5V, V_{OUT} = 1.2V, 10A Load Step

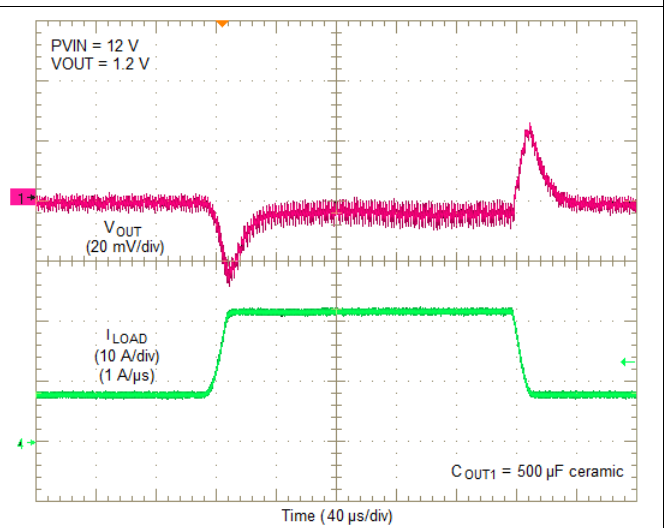


Figure 16. P_{VIN} = 12V, V_{OUT} = 1.2V, 5A Load Step

8.6 Application Schematics

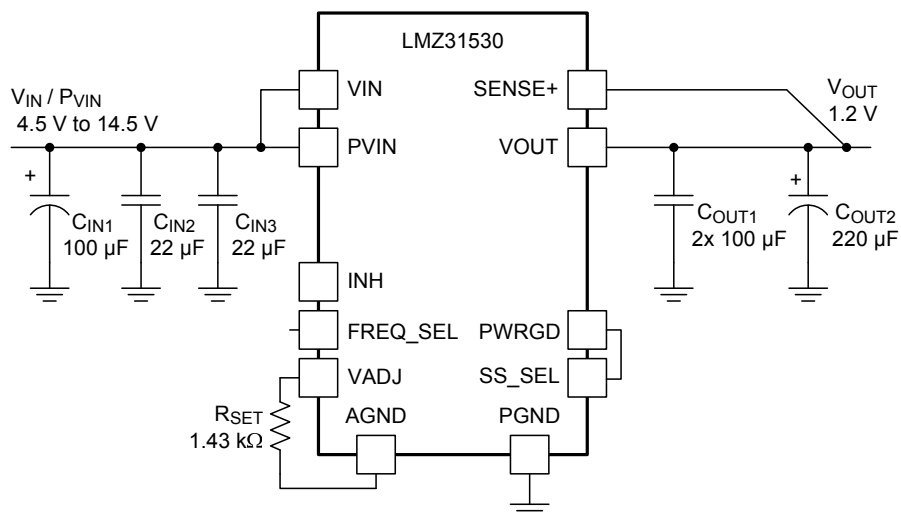


Figure 17. Typical Schematic
PVIN = VIN = 4.5 V to 14.5 V, VOUT = 1.2 V

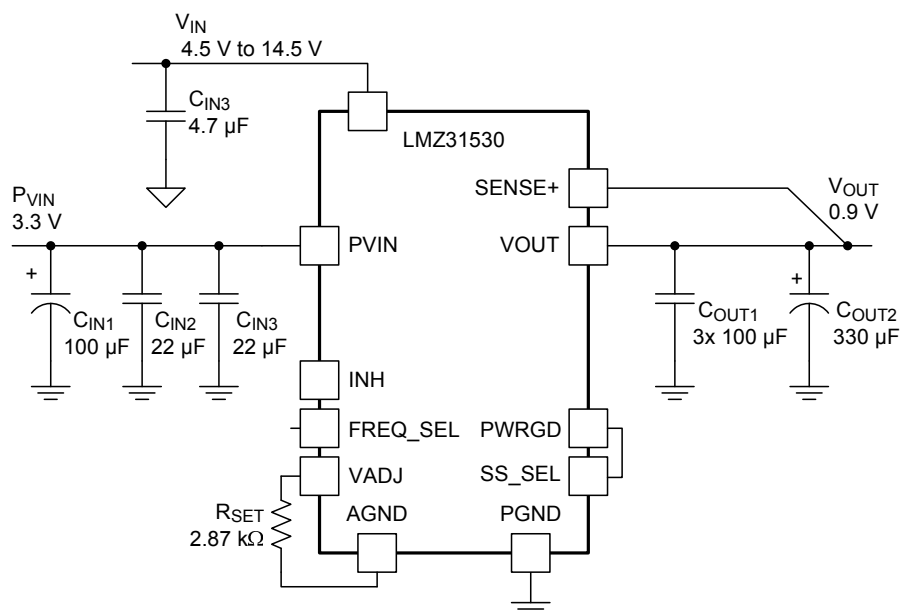


Figure 18. Typical Schematic
PVIN = 3.3 V, VIN = 4.5 V to 14.5 V, VOUT = 0.9 V

8.7 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the LMZ31530 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.8 VIN and PVIN Input Voltage

The LMZ31530 allows for a variety of applications by using the VIN and PVIN pins together or separately. The VIN voltage supplies the internal control circuits of the device. The PVIN voltage provides the input voltage to the power converter system.

If tied together, the input voltage for the VIN pin and the PVIN pin can range from 4.5 V to 14.5 V. If using the VIN pin separately from the PVIN pin, the VIN pin must be greater than 4.5 V, and the PVIN pin can range from as low as 3.0 V to 14.5 V. When operating from a split rail, it is recommended to supply VIN from 5 V to 12 V, for best performance.

8.9 3.3 V PVIN Operation

Applications operating from a PVIN of 3.3 V must provide at least 4.5 V for VIN. It is recommended to supply VIN from 5 V to 12 V, for best performance. See application note, [SNVA692](#) for help creating 5 V from 3.3 V using a small, simple charge pump device.

8.10 Power Good (PWRGD)

The PWRGD pin is an open drain output. Once the voltage on the SENSE+ pin is between 90% and 115% of the set voltage, the PWRGD pin pull-down is released and the pin floats. The recommended pull-up resistor value is between 10 k Ω and 100 k Ω to a voltage source that is less than 7 V. An internal 100 k Ω pull-up resistor is provided internal to the device between the PWRGD pin (pin 19) and PWRGD_PU pin (pin 18). The PWRGD_PU pin can be connected to a voltage source less than 7 V or connected directly to V5V (pin 61), which is an internal 5V regulator. The PWRGD pin is in a defined state once VIN is greater than 1.0 V. The PWRGD pin is pulled low when the voltage on SENSE+ is lower than 90% or greater than 115% of the nominal set voltage. Also, the PWRGD pin is pulled low if the input UVLO or thermal shutdown is asserted or the INH pin is pulled low.

8.11 Slow Start (SS_SEL)

Connecting the SS_SEL pin to PWRGD or PGND sets the slow start interval of approximately 0.7 ms. The connection to either PWRGD or PGND determines the mode of the LMZ31530 as described in [Auto-Skip Eco-mode™ / Forced Continuous Conduction Mode](#). Adding a resistor between SS_SEL pin and PWRGD or PGND increases the slow start time. Increasing the slow start time will reduce inrush current. [Table 5](#) shows a resistor connected between SS_SEL pin and PWRGD to select FCCM and [Figure 20](#) shows a resistor between SS_SEL pin and PGND to select Auto-skip mode. See [Table 5](#) below for SS resistor values and timing interval.

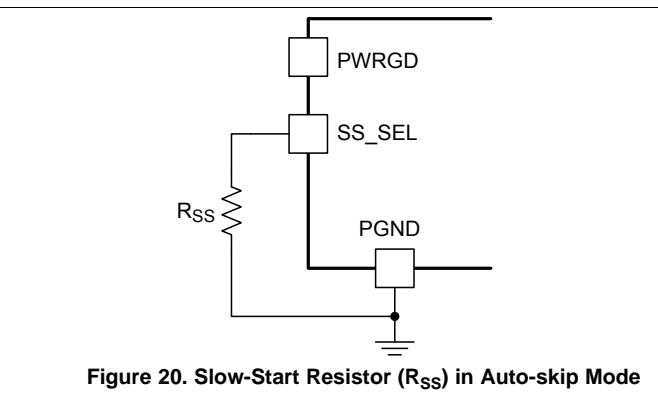
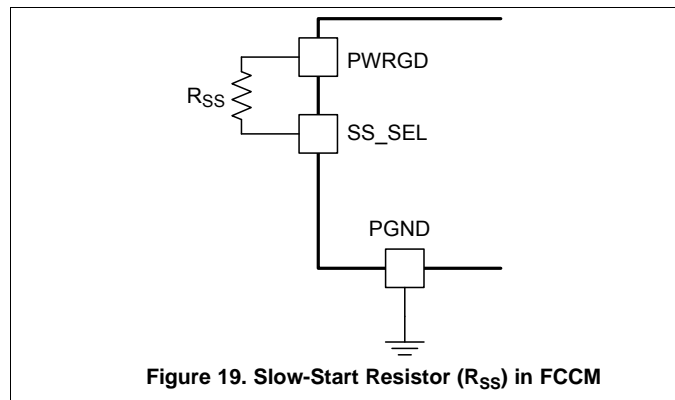


Table 5. Slow-Start Resistor Values and Slow-Start Time

| R_{SS} (k Ω) | short | 61.9 | 161 | 436 |
|------------------------|-------|------|-----|-----|
| SS Time (msec) | 0.7 | 1.4 | 2.8 | 5.6 |

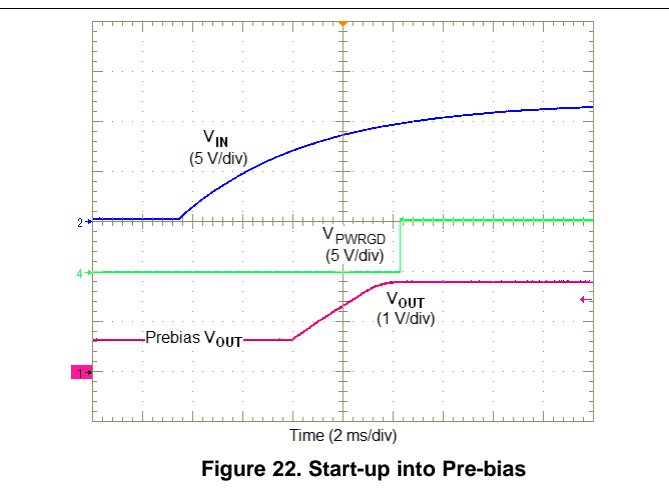
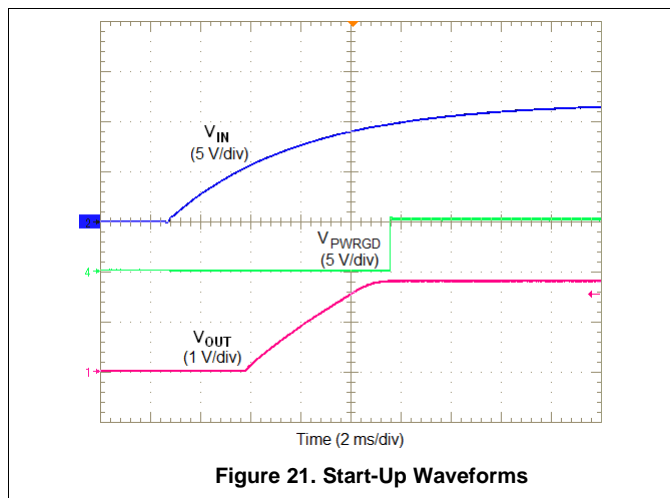
8.12 Auto-Skip Eco-mode™ / Forced Continuous Conduction Mode

Auto-skip Eco-mode or Forced Continuous Conduction Mode (FCCM) can be selected using the SS_SEL pin (pin 3). Connect the SS_SEL pin to PGND to select Auto-skip Eco-mode or to the PWRGD pin to select FCCM.

In Auto-skip Eco-mode, the LMZ31530 automatically reduces the switching frequency at light load conditions to maintain high efficiency. In FCCM, the controller keeps continuous conduction mode in light load condition and the switching frequency is kept almost constant over the entire load range. Transient performance is best in FCCM.

8.13 Power-Up Characteristics

When configured as shown in the front page schematic, the LMZ31530 produces a regulated output voltage following the application of a valid input voltage. During the power-up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of in-rush current that can be drawn from the input source. [Figure 21](#) shows the start-up waveforms for a LMZ31530, operating from a 12-V input ($P_{VIN}=V_{IN}$) and with the output voltage adjusted to 1.8 V. [Figure 22](#) shows the start-up waveforms for a LMZ31530 starting up into a pre-biased output voltage. The waveforms were measured with a 15-A constant current load.



8.14 Pre-Biased Start-Up

The LMZ31530 has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During pre-biased startup, the low-side MOSFET does not turn on until the high-side MOSFET has started switching. The high-side MOSFET does not start switching until the slow start voltage exceeds the voltage on the V_ADJ pin. Refer to [Figure 22](#).

8.15 Remote Sense

The SENSE+ pin must be connected to V_{OUT} at the load, or at the device pins.

Connecting the SENSE+ pin to V_{OUT} at the load improves the load regulation performance of the device by allowing it to compensate for any I-R voltage drop between its output pins and the load. An I-R drop is caused by the high output current flowing through the small amount of pin and trace resistance. This should be limited to a maximum of 300 mV.

NOTE

The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the SENSE+ connection, they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

8.16 Output On/Off Inhibit (INH)

The INH pin provides electrical on/off control of the device. Once the INH pin voltage exceeds the threshold voltage, the device starts operation. If the INH pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.

The INH pin has an internal pull-up current source, allowing the user to float the INH pin for enabling the device. If an application requires controlling the INH pin, use an open drain/collector device, or a suitable logic gate to interface with the pin.

Figure 23 shows the typical application of the inhibit function. The Inhibit control has its own internal pull-up to VIN potential. An open-collector or open-drain device is recommended to control this input.

Turning Q1 on applies a low voltage to the inhibit control (INH) pin and disables the output of the supply, shown in Figure 24. If Q1 is turned off, the supply executes a soft-start power-up sequence, as shown in Figure 25. The waveforms were measured with a 12-A constant resistance load.

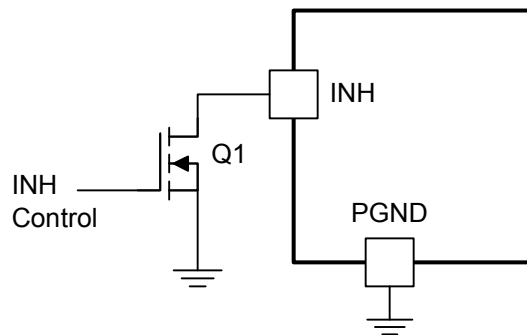
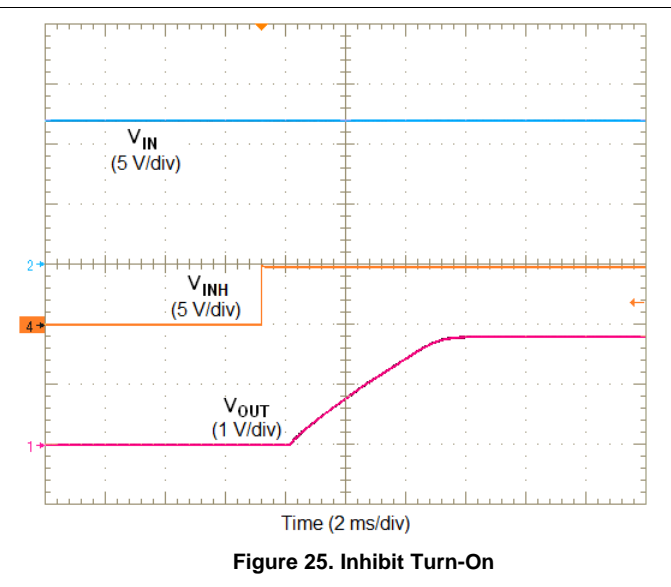
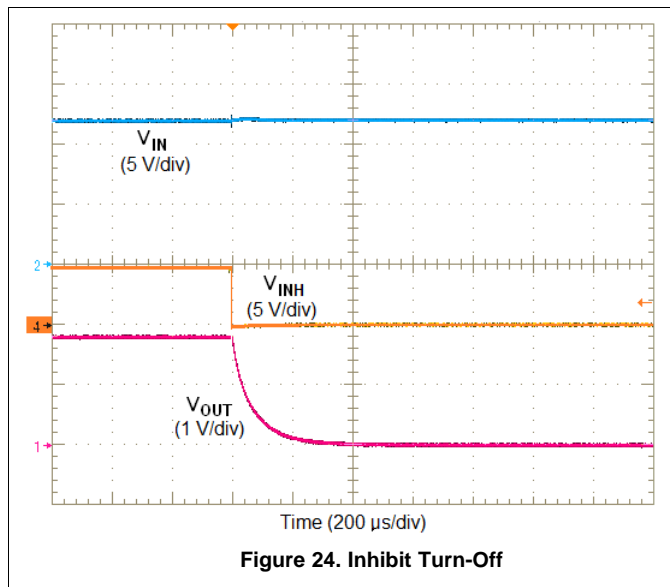
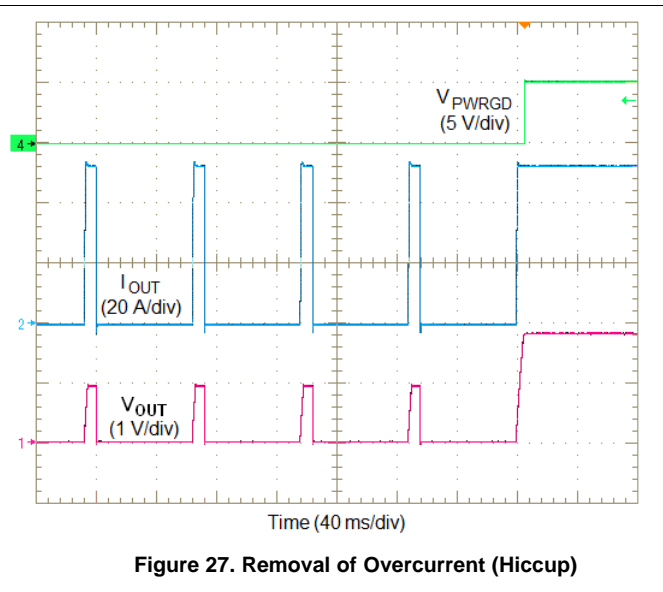
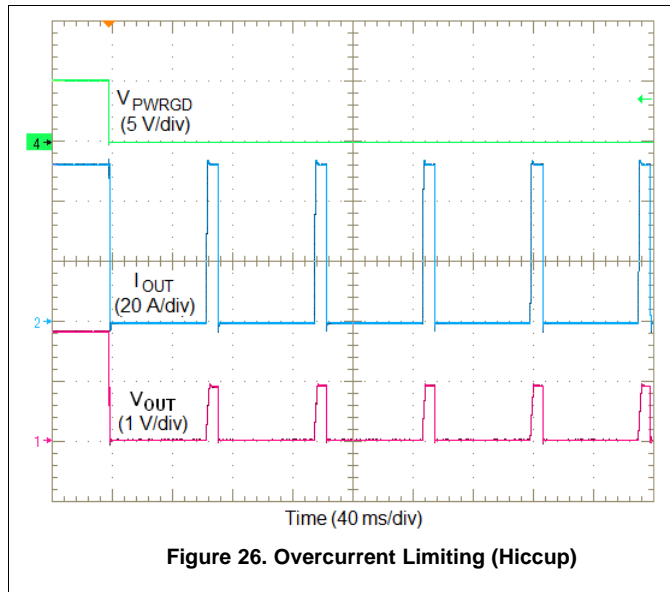


Figure 23. Typical Inhibit Control



8.17 Overcurrent Protection

For protection against load faults, the LMZ31530 incorporates cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the OFF state and the controller maintains the OFF state during the period in that the inductor current is larger than the overcurrent trip level. In cycle-by-cycle mode, applying a load that exceeds the regulator's overcurrent threshold limits the output current and reduces the output voltage as shown in Figure 26. If the overcurrent condition remains and the output voltage drops below 70% of the set-point, the LMZ31530 shuts down. Following shutdown, the module periodically attempts to recover by initiating a soft-start power-up as shown in Figure 26. This is described as a hiccup mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced which reduces power dissipation. Once the fault is removed, the module automatically recovers and returns to normal operation as shown in Figure 27.



8.18 Current Limit (ILIM) Adjust

The current limit of this device can be adjusted lower by connecting a resistor, R_{ILIM} , between the ILIM pin (pin 6) and PGND. To adjust the typical current limit threshold, as listed in the electrical characteristics table, refer to Table 6.

Table 6. Current Limit Adjust Resistor

| Current Limit Reduction | $R_{ILIM}(k\Omega)$ |
|-------------------------|---------------------|
| 10 % | 825 |
| 20 % | 487 |
| 30 % | 324 |

8.19 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 145°C typically. The device reinitiates the power up sequence when the junction temperature drops below 135°C typically.

8.20 Layout Considerations

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. [Figure 28](#) thru [Figure 33](#), shows a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (PVIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Keep AGND and PGND separate from one another. AGND should only be used as the return for R_{SET} .
- Place R_{SET} , R_{FREQ} , and R_{SS} as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

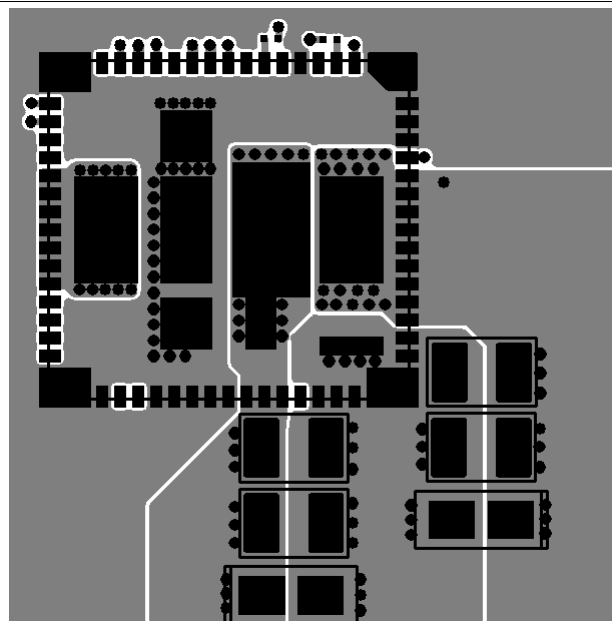


Figure 28. Typical Top Layer Layout

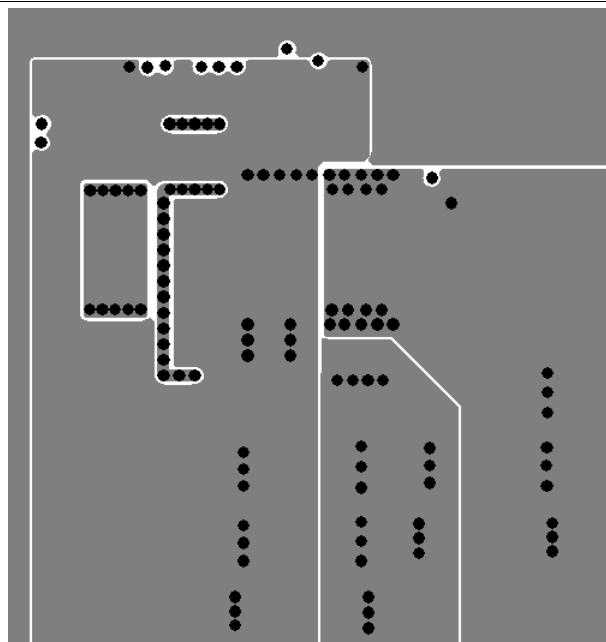


Figure 29. Typical Layer 2 Layout

Layout Considerations (continued)

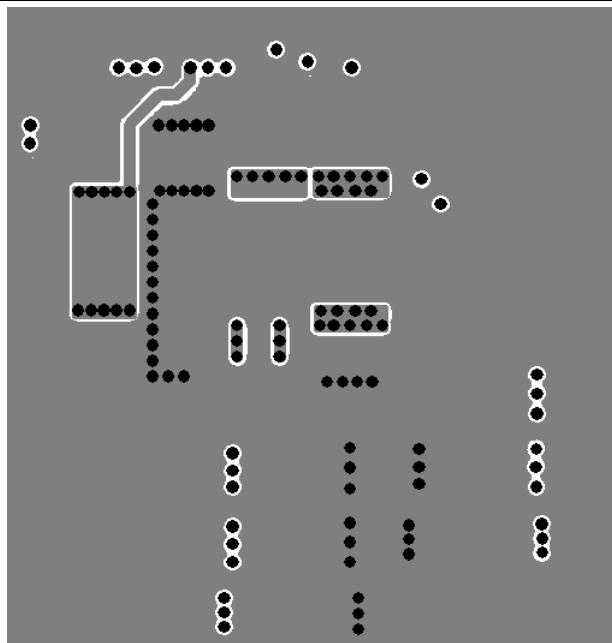


Figure 30. Typical Layer 3 Layout

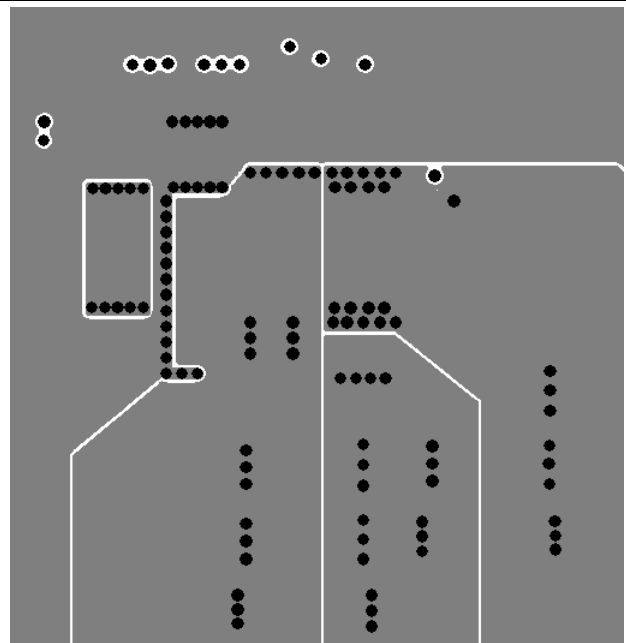


Figure 31. Typical Layer 4 Layout

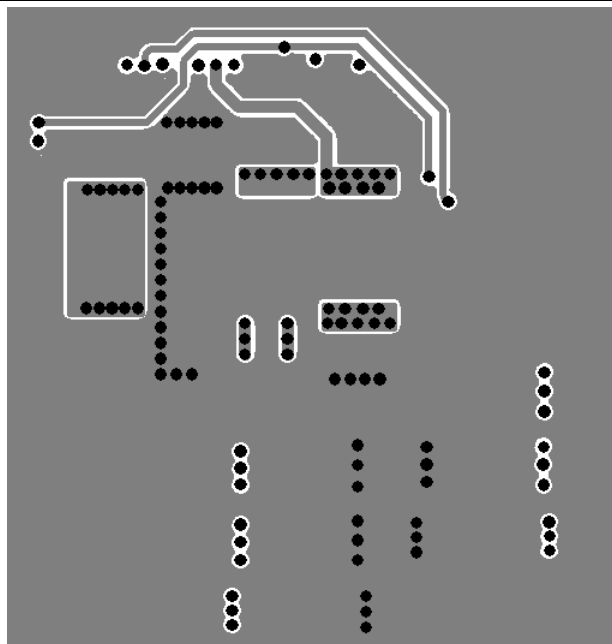


Figure 32. Typical Layer 5 Layout

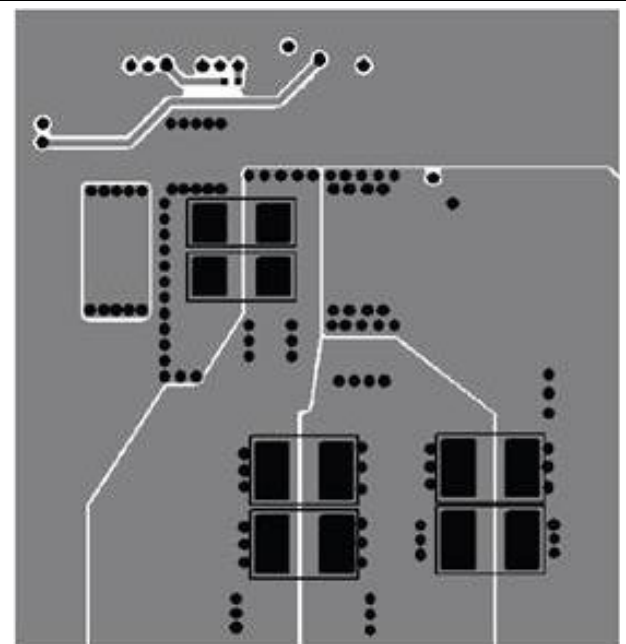
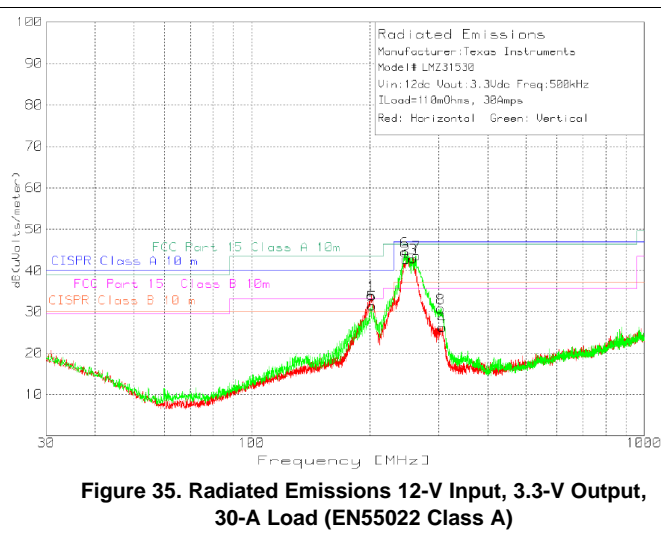
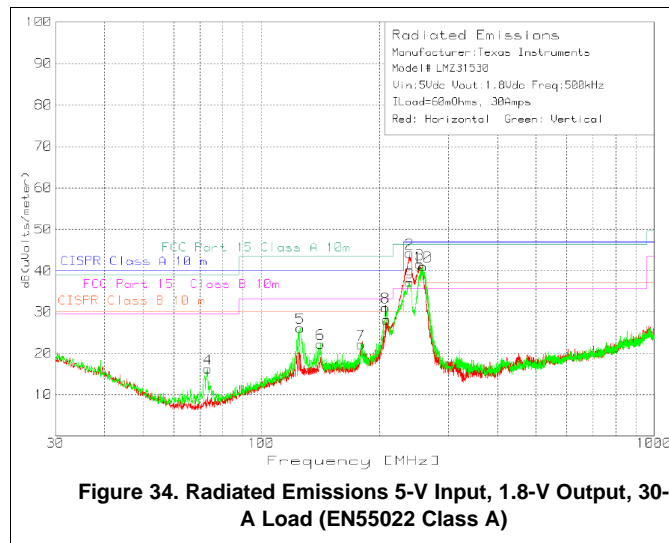


Figure 33. Typical Bottom Layer Layout

8.21 EMI

The LMZ31530 is compliant with EN55022 Class A radiated emissions. [Figure 34](#) and [Figure 35](#) show typical examples of radiated emissions plots for the LMZ31530 operating from 5V and 12V respectively. Both graphs include the plots of the antenna in the horizontal and vertical positions.



9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April 2018) to Revision E Page

- Updated PCB Typical Bottom Layer Layout [21](#)

Changes from Revision C (June 2017) to Revision D Page

- Added WEBENCH® design links for the LMZ31530..... [1](#)
- Increased the peak reflow temperature and maximum number of reflows to JEDEC specifications for improved manufacturability..... [2](#)
- Added *Device Support* section [25](#)
- Added *Mechanical, Packaging, and Orderable Information* section [26](#)

Changes from Revision B (December 2013) to Revision C Page

- Added peak reflow and maximum number of reflows information [2](#)

Changes from Revision A (December 2013) to Revision B Page

- Added additional capacitors to the recommended capacitor table..... [13](#)

Changes from Original (October 2013) to Revision A Page

- Changed status from Preview to Production [1](#)

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.1.1.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the LMZ31530 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

[Soldering Requirements for BQFN Packages](#)

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Community Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.5 Trademarks

Eco-mode, E2E are trademarks of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

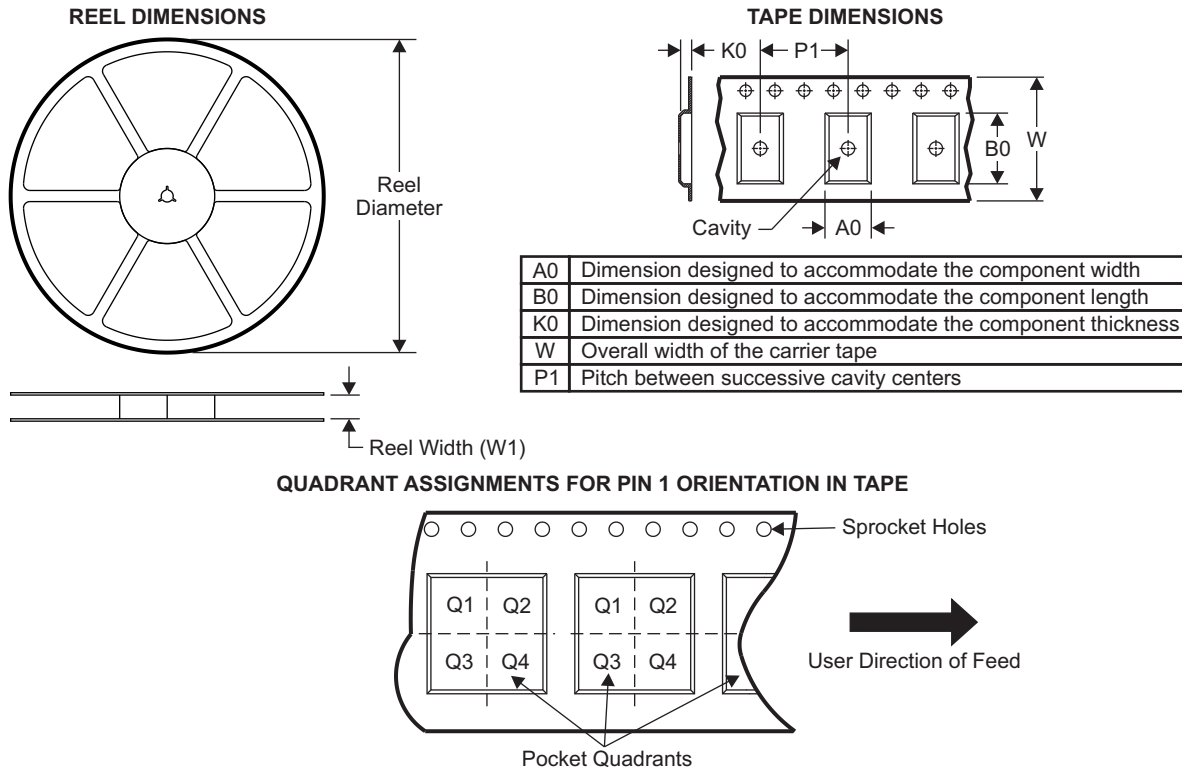
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

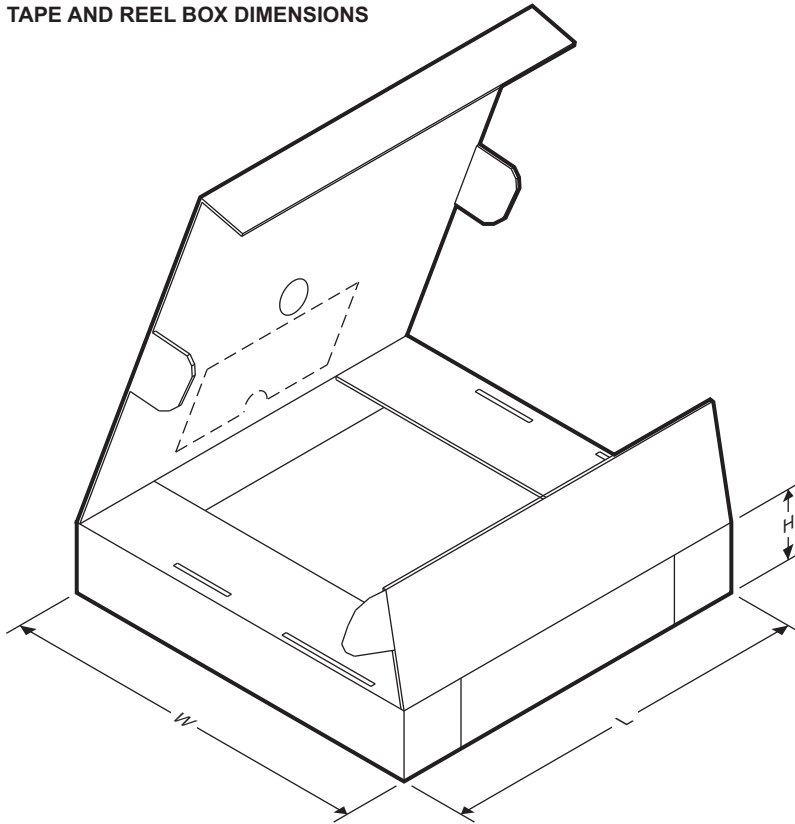
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information



| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMZ31530RLGT | BQFN | RLG | 72 | 250 | 330.0 | 24.4 | 15.35 | 16.35 | 6.1 | 20.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|-----|-------------|------------|-------------|
| LMZ31530RLGT | BQFN | RLG | 72 | 250 | 383.0 | 353.0 | 58.0 |

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| LMZ31530RLGT | Active | Production | BQFN (RLG) 72 | 250 SMALL T&R | Exempt | NIPDAU | Level-3-245C-168 HR | -40 to 85 | LMZ31530 |
| LMZ31530RLGT.A | Active | Production | BQFN (RLG) 72 | 250 SMALL T&R | Exempt | NIPDAU | Level-3-245C-168 HR | -40 to 85 | LMZ31530 |
| LMZ31530RLGTG4 | Active | Production | BQFN (RLG) 72 | 250 SMALL T&R | Yes | NIPDAU | Level-3-245C-168 HR | -40 to 85 | LMZ31530 |
| LMZ31530RLGTG4.A | Active | Production | BQFN (RLG) 72 | 250 SMALL T&R | Yes | NIPDAU | Level-3-245C-168 HR | -40 to 85 | LMZ31530 |
| LMZ31530RLGTG4.B | Active | Production | BQFN (RLG) 72 | 250 SMALL T&R | Yes | NIPDAU | Level-3-245C-168 HR | -40 to 85 | LMZ31530 |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

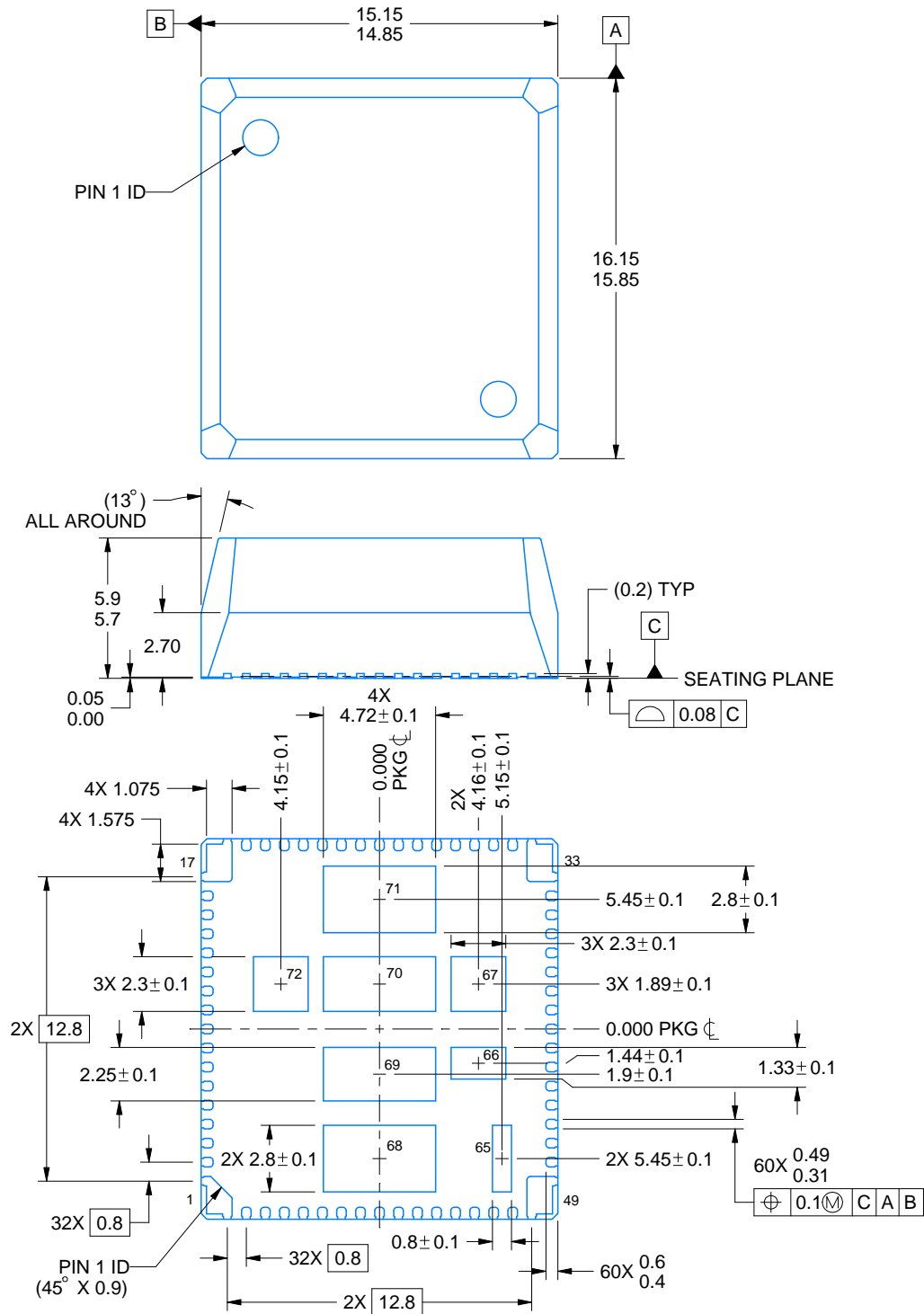
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

RLG0072A

B4QFN - 5.9 mm max height

EXTREMELY THICK QUAD FLATPACK - NO LEAD



4226426/A 12/2020

NOTES:

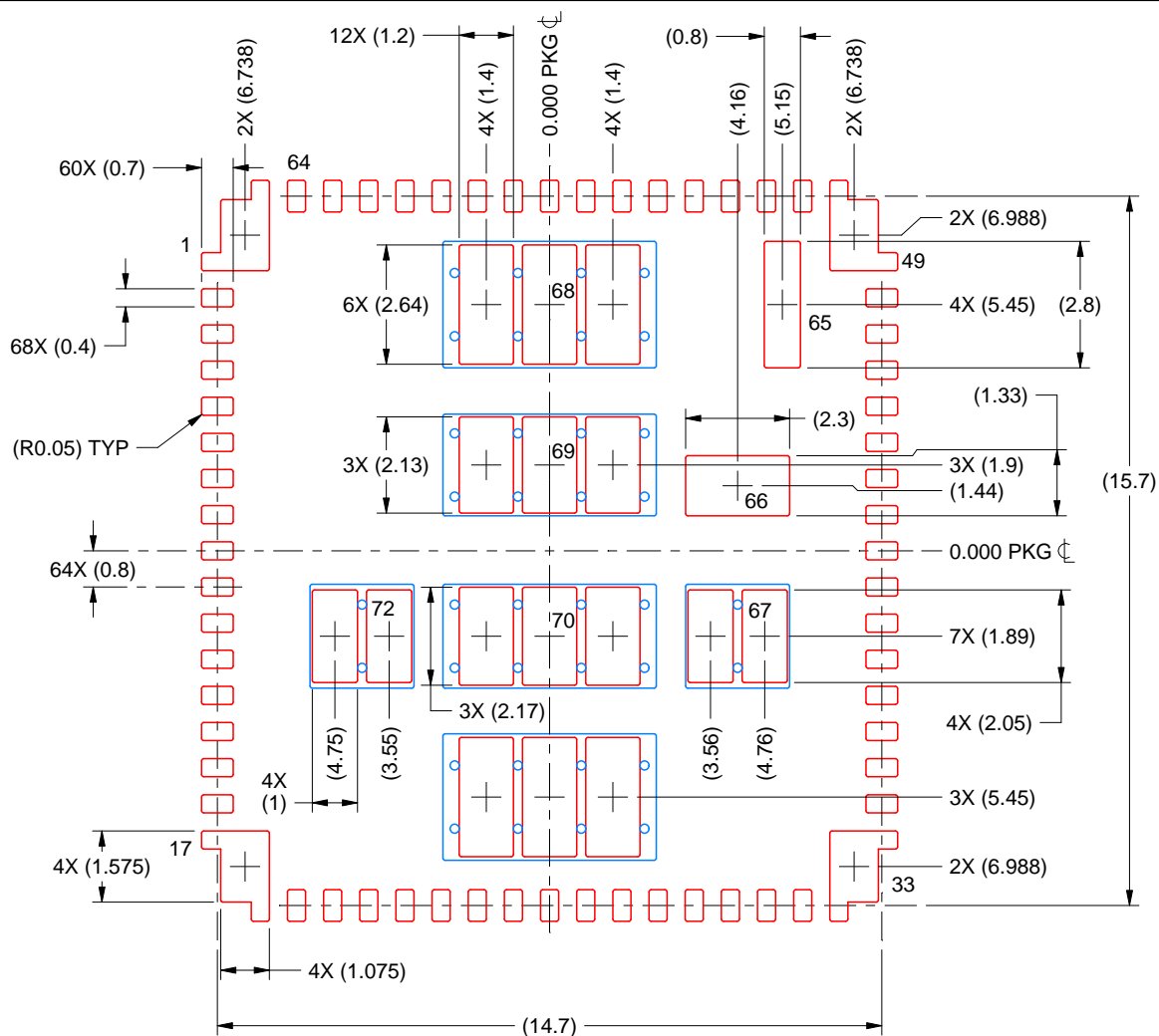
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE STENCIL DESIGN

RLG0072A

B4QFN - 5.9 mm max height

EXTREMELY THICK QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 67 & 72: 78%
PADS 68 & 71: 73%
PADS 69 & 70: 74%
SCALE: 6X

4226426/A 12/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025