

LP8728D-Q1 Quad-Output Step-Down DC-DC Converter

1 Features

- LP8728D-Q1 is an Automotive Grade Product that is AECQ-100 Grade 1 Qualified
- Four High Efficiency Step-Down DC-DC Converters:
 - 93% Peak Efficiency ($V_{IN} = 5\text{ V}$, $V_{OUT} = 3.3\text{ V}$)
 - Max Output Current 1 A
 - Forced PWM Operation
 - Soft-Start Control
 - $V_{OUT1} = 3.3\text{ V}$
 - $V_{OUT2} = 1.25\text{ V}$
 - $V_{OUT3} = 1.8\text{ V}$ or 2.65 V (pin selectable)
 - $V_{OUT4} = 1.8\text{ V}$
- Separate Enable Inputs for each Converter Control
- Separate Power Good Outputs for each Converter
- Output Overcurrent and Input Overvoltage Protection
- Overtemperature Protection
- Undervoltage Lockout (UVLO)

2 Applications

- FPGA, DSP Core Power
- Processor Power for Mobile Devices
- Peripheral I/O Power
- Automotive Safety Cameras
- Automotive Infotainment

3 Description

The LP8728D-Q1 is a quad-output Power Management Unit (PMU), optimized for low-power FPGAs, microprocessors, and DSPs for automotive applications. This device integrates four highly efficient step-down DC-DC converters into one package. Each converter has high current capability and separate controls which allows flexibility to use the device in multiple applications. All the converters operate above the AM band with a fixed 3.2-MHz switching frequency. The high-side switch turn-on time of each converter is phase shifted to minimize input current spikes.

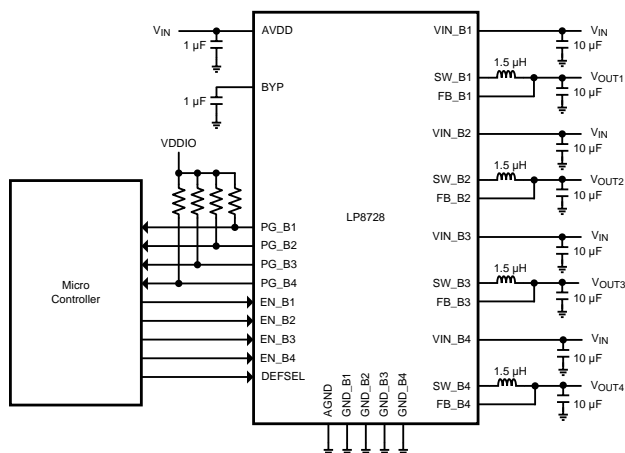
Protection features include output short-circuit protection, switch current limits, input overvoltage protection, input undervoltage lockout, and thermal shutdown functions. During start-up, the device controls the output slew rate to minimize output voltage overshoot and the input inrush current.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP8728D-Q1	WQFN (28)	5.00 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Efficiency

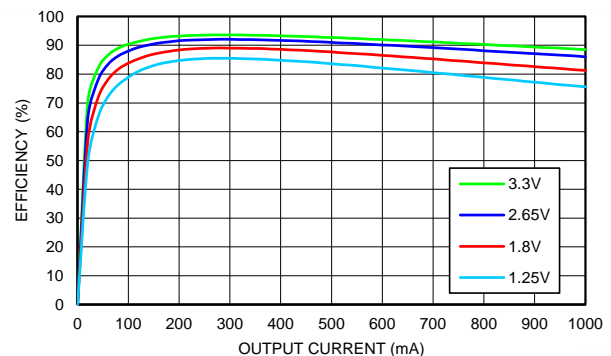


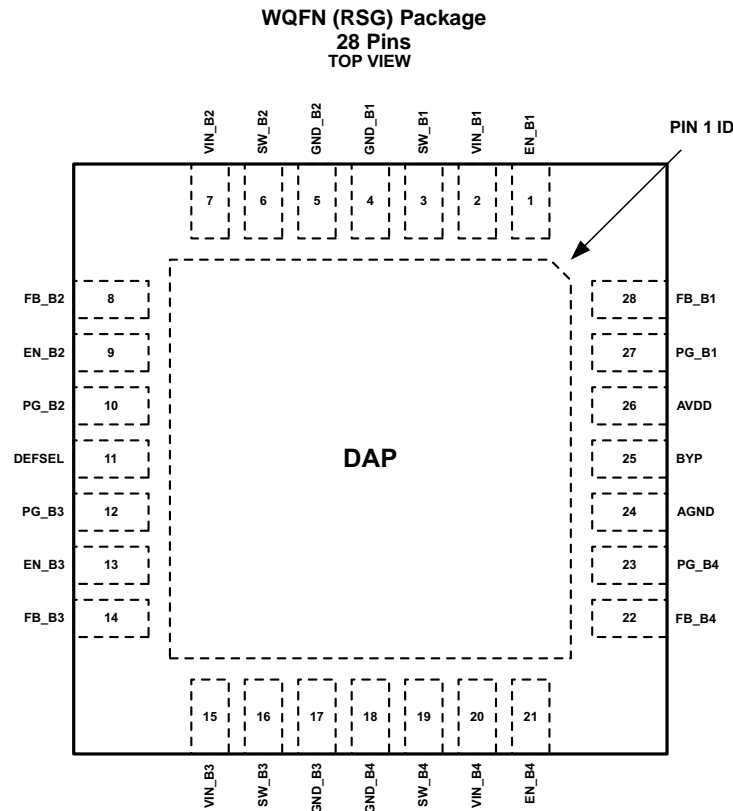
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4 Revision History

DATE	REVISION	NOTES
February 2015	*	Initial release.

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NUMBER	NAME		
1	EN_B1	D/I	Enable Buck 1
2	VIN_B1	P	Positive power supply input for Buck 1
3	SW_B1	P	Switch node for Buck 1
4	GND_B1	G	Power ground for Buck 1
5	GND_B2	G	Power ground for Buck 2
6	SW_B2	P	Switch node for Buck 2
7	VIN_B2	P	Positive power supply input for Buck 2
8	FB_B2	A	Feedback pin for Buck 2. Referenced against AGND.
9	EN_B2	D/I	Enable Buck 2
10	PG_B2	D/O	Open-drain Power Good output for Buck 2
11	DEFSEL	D/I	Buck 3 output voltage selection pin
12	PG_B3	D/O	Open-drain Power Good output for Buck 3
13	EN_B3	D/I	Enable Buck 3
14	FB_B3	A	Feedback pin for Buck 3. Referenced against AGND.
15	VIN_B3	P	Positive power supply input for Buck 3
16	SW_B3	P	Switch node for Buck 3
17	GND_B3	G	Power ground for Buck 3
18	GND_B4	G	Power ground for Buck 4
19	SW_B4	P	Switch node for Buck 4

(1) A: Analog Pin, G: Ground Pin, P: Power Pin, O: Output Pin, D/I: Digital Input, D/O: Digital Output.

Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NUMBER	NAME		
20	VIN_B4	P	Positive power supply input for Buck 4
21	EN_B4	D/I	Enable Buck 4
22	FB_B4	A	Feedback pin for Buck 4. Referenced against AGND.
23	PG_B4	D/O	Open-drain Power Good output for Buck 4
24	AGND	G	Analog ground
25	BYP	A	Internal 1.8-V supply voltage capacitor pin. A ceramic low-ESR 1- μ F capacitor should be connected from this pin to AGND. The BYP voltage is generated internally, do not supply or load this pin externally.
26	AVDD	P	Analog positive power supply pin (V_{IN} level)
27	PG_B1	D/O	Open-drain Power Good output for Buck 1
28	FB_B1	A	Feedback pin for Buck 1. Referenced against AGND.
DAP	Die Attachment Pad		Exposed die attachment pad should be connected to GND plane with thermal vias to improve the thermal performance of the system.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{IN}	Voltage on power pins (AVDD, VIN_Bx)	-0.3	6	V
V _{FB}	Voltage on feedback pins (FB_Bx)	-0.3	6	V
V _{SW}	Voltage on buck converter switch pins (SW_Bx)	(GND_Bx - 0.2 V) to (VIN_Bx + 0.2 V) with 6 V max		V
V _{DIG}	Voltage on digital pins (PG_Bx, EN_Bx, DEFSEL)	(AGND - 0.2V) to (AVDD + 0.2 V) with 6 V max		V
V _{BYP}	Voltage on BYP pin	-0.3	2	V
T _{J(MAX)}	Maximum operating junction temperature ⁽²⁾		150	°C
	Maximum lead temperature (Soldering)	See ⁽³⁾		
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typical) and disengages at T_J = 130°C (typical).
- (3) For detailed soldering specifications and information, please refer to Texas Instruments Application Note *Leadless Leadframe Package (LLP) SNOA401*.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000
		Charged-device model (CDM), per AEC Q100-011	±750

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage on AVDD, VIN_B1, VIN_B2, VIN_B3 and VIN_B4 pins	4.5	5	5.5	V
T _A	Operating ambient temperature ⁽²⁾	-40		125	°C
C _{OUT}	Effective output capacitance during operation. Min value over T _A -40°C to 125°C.	5	10	12	μF
C _{IN}	Effective input capacitance during operation. 4.5 V ≤ V _{IN_Bx} ≤ 5.5 V. Min value over T _A -40°C to 125°C.	2.5	10		μF
L	Effective inductance during operation Min value over T _A -40°C to 125°C.	0.47	1.5	2	μF

- (1) All voltage values are with respect to network ground terminal.
- (2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A(max)}) is dependent on the maximum operating junction temperature (T_{J(max)}), the maximum power dissipation of the device in the application (P_{D(max)}), and the junction-to-ambient thermal resistance of the part/package in the application (R_{θJA}), as given by the following equation: T_{A(max)} = T_{J(max)} - (R_{θJA} × P_{D(max)})

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LP8728-Q1	UNIT
		WQFN (RSG)	
		28 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽²⁾	37.7	°C/W
R _{θJctop}	Junction-to-case (top) thermal resistance	24.5	
R _{θJB}	Junction-to-board thermal resistance	10.8	
Ψ _{JT}	Junction-to-top characterization parameter	0.3	
Ψ _{JB}	Junction-to-board characterization parameter	10.8	
R _{θJcbot}	Junction-to-case (bottom) thermal resistance	2.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) Calculated using 4-layer standard JEDEC thermal test board with 5 thermal vias between the die attach pad in the first copper layer and second copper layer.

6.5 Electrical Characteristics⁽¹⁾⁽²⁾

Unless otherwise noted, V_{IN} = 5 V, typical values apply for T_A = 25°C, and minimum/maximum limits apply over junction temperature range, T_J = –40°C to 125°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{SHDN}	Shutdown supply current into power connections	EN_Bx = 0 V		1	6	μA
I _{OP}	Operating current	All buck-converters active, I _{OUT} = 0 mA		20		mA
LOGIC INPUTS (EN_Bx, DEFSEL)						
V _{IL}	Input low level				0.4	V
V _{IH}	Input high level		1.6			V
R _{PD_DI}	EN_Bx and DEFSEL internal pulldown resistance		300	520	820	kΩ
T _{H_MIN}	Minimum EN_Bx high time			1		ms
T _{L_MIN}	Minimum EN_Bx low time			10		μs
LOGIC OUTPUTS (PG_Bx)						
V _{OL}	Output low level	I _{SINK} = 3 mA			0.4	V
R _{PU}	Recommended pullup resistor			10		kΩ
BUCK CONVERTERS						
V _{OUT1}	Output voltage for Buck 1	Fixed voltage		3.3		V
V _{OUT2}	Output voltage for Buck 2	Fixed voltage		1.25		V
V _{OUT3}	Output voltage for Buck 3	DEFSEL = 1		2.65		V
		DEFSEL = 0		1.8		
V _{OUT4}	Output voltage for Buck 4	Fixed voltage		1.8		V
V _{FB_Bx}	Output voltage accuracy		–3%		3%	
ΔV _{OUT}	Line regulation	4.5 V ≤ V _{IN_Bx} ≤ 5.5 V, I _{LOAD} = 10 mA		3		mV
	Load regulation	V _{IN} = 5 V, 100 mA ≤ I _{LOAD} ≤ 900 mA		3		mV
I _{OUT}	Output current	DC load T _A = 25°C			1000	mA
f _{SW}	Switching frequency		3.03	3.2	3.37	MHz
GBW	Gain bandwidth			300		kHz
I _{LIMITP}	High-side switch current limit		1200	1500	1800	mA
I _{LIMITN}	Low-side switch current limit	Reverse current		500		mA
R _{DSONP}	Pin-pin resistance for PFET	I _{OUT} = 200 mA		210	300	mΩ
R _{DSONN}	Pin-pin resistance for NFET	I _{OUT} = 200 mA		140	240	mΩ

(1) All voltage values are with respect to network ground terminal.

(2) Minimum (Min) and Maximum (Max) limits are specified by design, test, or statistical analysis. Typical (Typ) numbers are not verified, but do represent the most likely norm. Unless otherwise specified, conditions for Typ specifications are: V_{IN} = 5 V and T_J = 25°C.

Electrical Characteristics⁽¹⁾⁽²⁾ (continued)

Unless otherwise noted, $V_{IN} = 5\text{ V}$, typical values apply for $T_A = 25^\circ\text{C}$, and minimum/maximum limits apply over junction temperature range, $T_J = -40^\circ\text{C}$ to 125°C .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LK_SW}	Switch pin leakage current	$V_{OUT} = 1.8\text{V}$			1	μA
R_{PD_FB}	Pulldown resistor from FB_Bx pin to GND	Only active when converter disabled. All limits apply for $T_A = 25^\circ\text{C}$	40	70	100	Ω
K_{RAMP}	Slew rate control	DEFSEL from 0 to 1		10		$\text{mV}/\mu\text{s}$
T_{START}	Start-up time	Time from first EN_Bx high to start of switching		420		μs
K_{START}	Soft-start VOUT slew rate			18		$\text{mV}/\mu\text{s}$
VOLTAGE MONITORING						
V_{PG}	Power good threshold voltage	Power good threshold for voltage rising	93.5%	96%	98%	
		Power good threshold for voltage falling	91%	93%	95%	
V_{OVP}	Input overvoltage protection trigger point	Voltage monitored on AVDD Pin, voltage rising	5.5	5.7	5.9	V
		Hysteresis		80		mV
V_{UVLO}	Input undervoltage lockout (UVLO) threshold.	Voltage monitored on AVDD Pin, voltage falling		2.7		V
		Hysteresis		80		mV
THERMAL SHUTDOWN AND MONITORING						
TSD	Thermal shutdown	Threshold, temperature rising		150		$^\circ\text{C}$
		Hysteresis		20		

6.6 System Characteristics⁽¹⁾⁽²⁾⁽³⁾

Typical values apply for $T_A = 25^\circ\text{C}$. Unless otherwise noted, $V_{IN} = 5\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_{OUT}	Load transient response	I_{OUT} 10% max load \rightarrow 90% max load, 1- μs load step		70		mV
		I_{OUT} 90% max load \rightarrow 10% max load, 1- μs load step		70		mV
	Line transient response	V_{IN_Bx} stepping 4.5 V \leftrightarrow 5.5 V, $t_{RISE} = t_{FALL} = 10\ \mu\text{s}$, $I_{OUT} = 400\ \text{mA}$		20		mV
V_{RIPPLE}	Output voltage ripple	C_{OUT} ESR = 10 m Ω , $I_{OUT} = 200\ \text{mA}$		10		mV_{PP}
η	Efficiency	$V_{OUT} = 3.3\ \text{V}$, $I_{OUT} = 300\ \text{mA}$		94%		
		$V_{OUT} = 2.65\ \text{V}$, $I_{OUT} = 300\ \text{mA}$		92%		
		$V_{OUT} = 1.8\ \text{V}$, $I_{OUT} = 300\ \text{mA}$		89%		
		$V_{OUT} = 1.25\ \text{V}$, $I_{OUT} = 300\ \text{mA}$		85%		

- (1) All voltage values are with respect to network ground terminal.
- (2) Minimum (Min) and Maximum (Max) limits are specified by design, test, or statistical analysis. Typical (Typ) numbers are not verified, but do represent the most likely norm. Unless otherwise specified, conditions for Typ specifications are: $V_{IN} = 5\text{ V}$ and $T_J = 25^\circ\text{C}$.
- (3) System Characteristics are highly dependent on external components and PCB layout. System Characteristics are verified using inductor type: TOKO MDT2520-CN1R5M, input and output capacitor type: MuRata GRM21BR71A106KE51L.

6.7 Typical Characteristics

Unless otherwise noted, $V_{IN} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, inductor type: TOKO MDT2520-CN1R5M, input and output capacitor type: MuRata GRM21BR71A106KE51L.

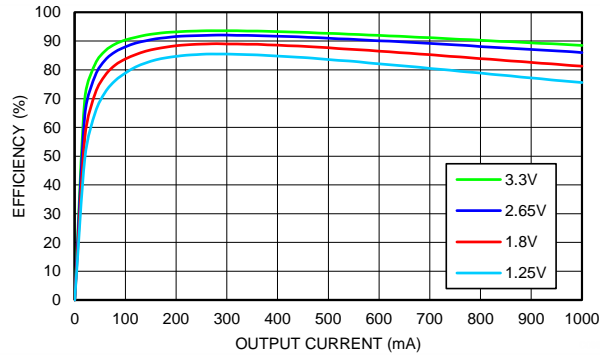


Figure 1. Efficiency vs Output Current

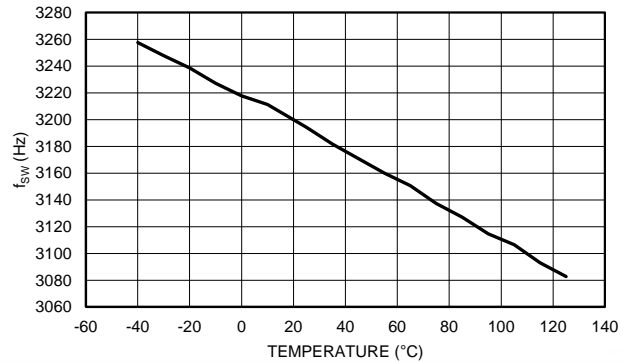


Figure 2. Switching Frequency vs Temperature

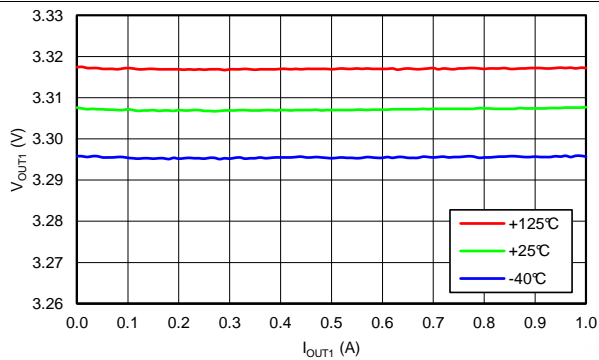


Figure 3. Buck1 Load Regulation

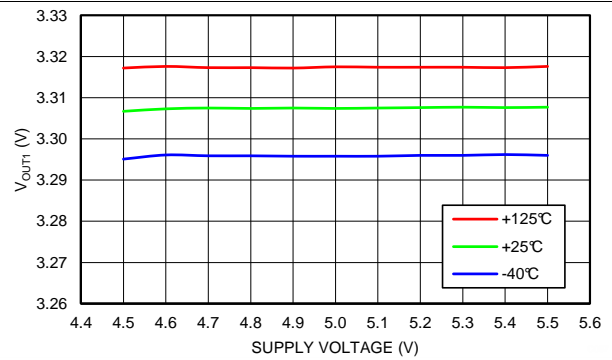


Figure 4. Buck1 Line Regulation

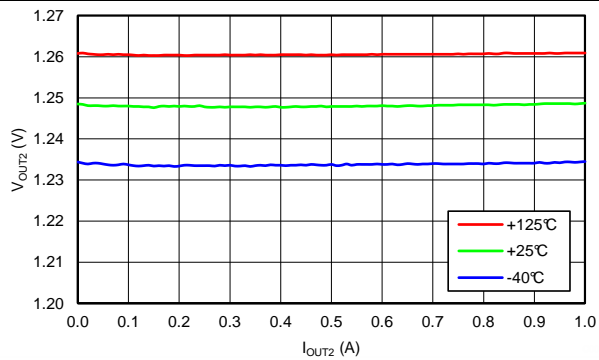


Figure 5. Buck2 Load Regulation

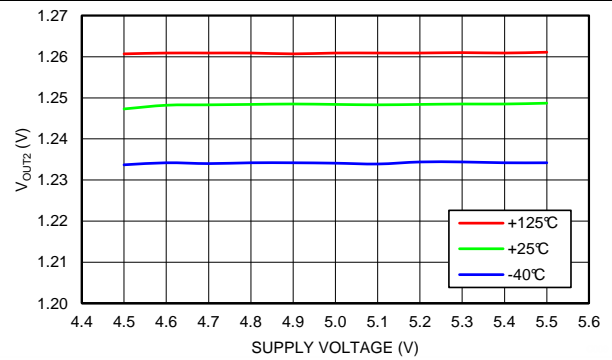


Figure 6. Buck2 Line Regulation

Typical Characteristics (continued)

Unless otherwise noted, $V_{IN} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, inductor type: TOKO MDT2520-CN1R5M, input and output capacitor type: MuRata GRM21BR71A106KE51L.

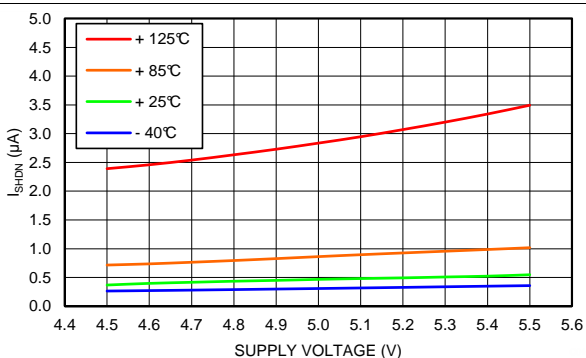


Figure 7. Shutdown Current Consumption

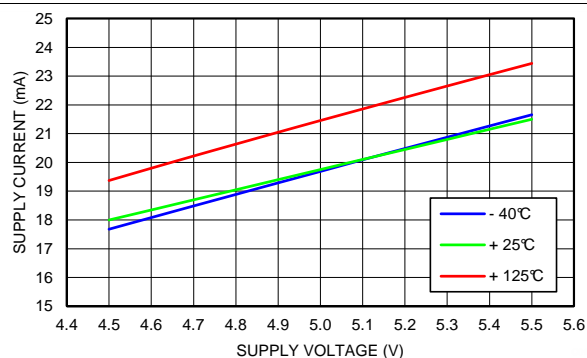


Figure 8. Active Mode Current Consumption (All Bucks Active)

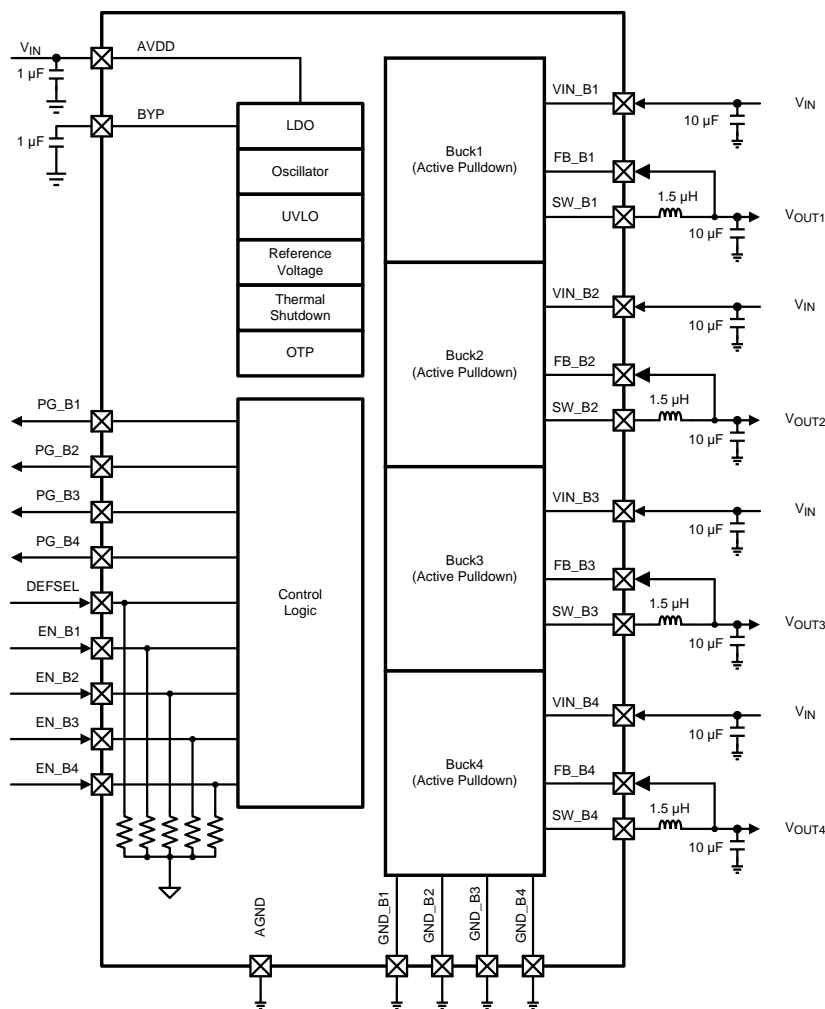
7 Detailed Description

7.1 Overview

The LP8728D-Q1 has four integrated high-efficiency buck converters. Each buck converter has individual enable input and power good output pins. When the first enable pin is pulled high there is a 420- μ s start-up delay when the device wakes up from the shutdown mode and all internal reference blocks are started up. Once reference blocks have settled, the corresponding buck converter turns on. Buck cores utilize the soft-start feature to limit the inrush current during start-up. Once a buck output reaches 96% (typical) of the desired output voltage, the power-good pin is pulled high (see Figure 9). When at least one buck core is active, the remaining buck converters will start up without any start-up delay.

If the output voltage drops below 93% (typical) of desired voltage due to, for example, an overload condition, the corresponding power-good pin is pulled low. The power-good signal is always held low for at least 50 ms. When the enable pin is pulled low, the corresponding buck converter's power good signals are set low, and the buck converter is instantly shut down. An output capacitor is then discharged through an internal 70- Ω (typical) pulldown resistor. The pulldown resistor is connected between buck feedback pin and ground and is only active when the enable pin is set low. When all enable signals are pulled low, the LP8728D-Q1 enters a low current shutdown mode.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Buck Information

The buck converters are operated in a forced PWM mode. Even with light load a minimum switching pulse is generated with every switching cycle. Each buck converter's high-side switch turn-on time is phase shifted to minimize the input current ripple (see Figure 20).

7.3.1.1 Features

The following features are supported for all converters:

- Synchronous rectification
- Current mode feedback loop with PI compensator
- Forced PWM operation
- Soft start
- Power-good output
- Overvoltage comparator

In addition to the aforementioned features, Buck3 output voltage can be selected with the DEFSEL pin. If the DEFSEL pin is pulled low, V_{OUT3} is set to 1.8 V. If DEFSEL is pulled high, V_{OUT3} is set to 2.65 V.

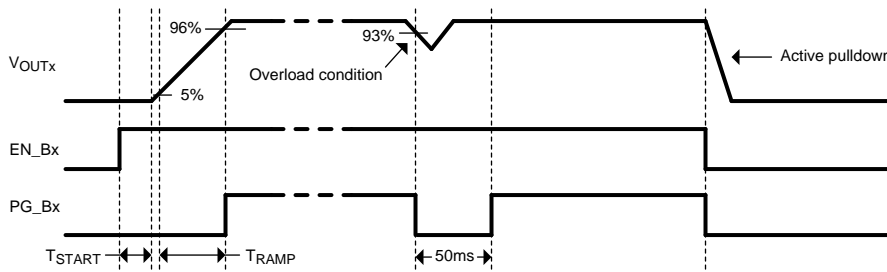


Figure 9. Buck Converter Start-up And Shutdown

7.3.2 Thermal Shutdown (TSD)

Thermal shutdown function shuts down all buck regulators if the device's junction temperature T_J rises above 150°C (typ.). All power-good signals are pulled low 5 ms before the buck regulators are shut down. Once T_J falls below 130°C (typical), the LP8728 will automatically start up the buck regulators. There is a 2-second safety delay included in the restart function. Buck regulators are not restarted until 2 seconds have elapsed after T_J falls below 130°C (typical). To minimize the inrush current during restarting, regulators are started in a Buck1 → Buck2 → Buck3 → Buck4 sequence. A 500- μ s delay is included between each buck start-up.

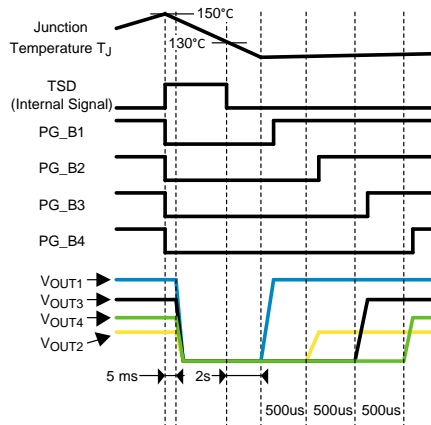


Figure 10. TSD Timing Diagram

Feature Description (continued)

7.3.3 Undervoltage Lockout (UVLO)

If input voltage drops below 2.7 V (typ.) the PG_Bx pins are pulled low and the buck converters are shut down. (Figure 11). The PG_Bx pins are always held low for at least 50 ms. The buck converters are restarted once the input voltage rises above UVLO level.

If a UVLO condition has lasted less than 50 ms, the PG_Bx pins are released high once 50 ms has elapsed and corresponding output voltage has settled. If an overvoltage condition has lasted more than 50 ms, the PG_Bx pins are released high once corresponding output voltage has settled.

Regulators are always restarted in a Buck1 → Buck2 → Buck3 → Buck4 sequence. A 500-μs delay is included between each buck start-up.

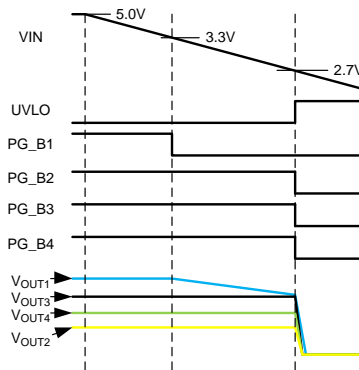


Figure 11. UVLO Operation

7.3.4 Overvoltage Protection (OVP)

Overvoltage protection protects the device in case of an overvoltage condition. If input voltage exceeds 5.7 V (typical), all PG_Bx pins are pulled low. the PG_Bx pins are always held low for at least 50 ms. Once the PG_Bx pins are pulled low, the system has 5 ms time to power down. After an overvoltage condition has lasted for 5 ms, all buck converters are shut down. The buck converters are restarted once input voltage falls below 5.62 V (typical). The buck converters are started in a Buck1 → Buck2 → Buck3 → Buck4 sequence. A 500-μs delay is included between each buck start-up.

If an overvoltage condition lasted more than 5 ms, but less than 50 ms, the PG_Bx pins are released high once 50 ms has elapsed and the corresponding output voltage has settled (Figure 12).

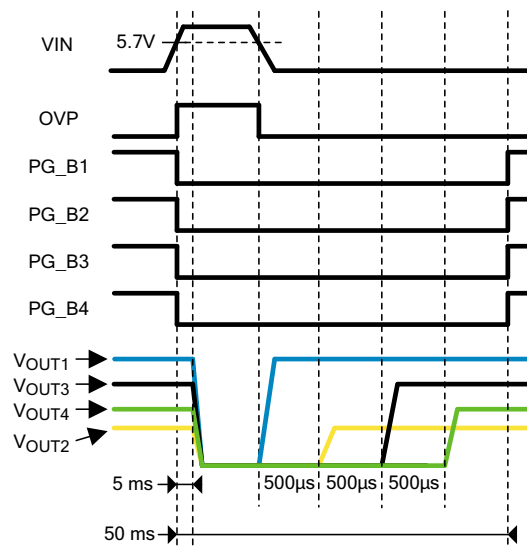


Figure 12. OVP Duration Less Than 50 ms

Feature Description (continued)

If an overvoltage condition has lasted more than 50 ms, the power-good signals are released high once the corresponding output voltage has settled. Regulators are started in a buck1 → buck2 → buck3 → buck4 sequence. A 500- μ s delay is included between each buck start-up (Figure 13). If an overvoltage condition has lasted less than 5 ms, the buck converters are not shut down. Even in this case the PG_Bx pins are held low for 50 ms.

NOTE

Since the regulators are allowed to operate for 5 ms during overvoltage condition it is the system designer's responsibility to verify that input voltage doesn't exceed limits stated in [Absolute Maximum Ratings](#). Exceeding these limits may cause permanent damage to the device.

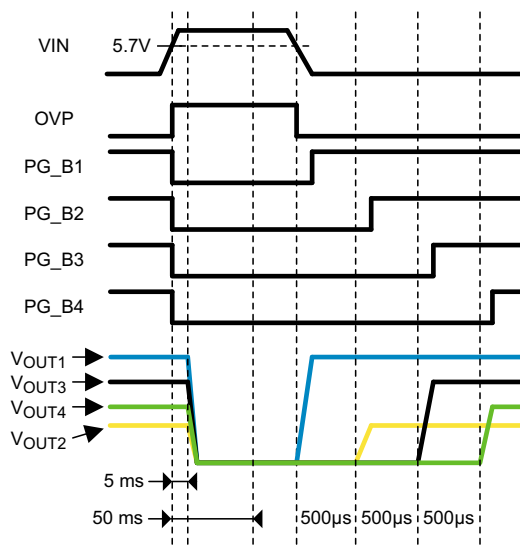


Figure 13. OVP Duration More Than 50 ms

7.4 Device Functional Modes

7.4.1 Shutdown Mode

When all EN_Bx inputs are low, the device is in a Shutdown mode. This is a low-power mode when all buck-regulators and all internal blocks are disabled.

7.4.2 Active Mode

When the first enable pin is pulled high there is a 420- μ s start-up delay when the device wakes up from the Shutdown; mode and all internal reference blocks are started up. Once the reference blocks have settled, the corresponding buck converter turns on. Buck cores utilize the soft-start feature to limit the inrush current during start-up. Once a buck output reaches 96% (typical) of the desired output voltage, the power-good pin is pulled high. When at least one buck converter is active device is in a Active mode. When device is in Active mode, the remaining buck converters will start up without any start-up delay when EN_Bx pin is pulled high. When EN_Bx pin is set low the corresponding buck converter will shut down. When all EN_Bx pins are set low the device shuts down all internal reference blocks and enters Shutdown mode.

If output voltage of a buck regulator falls below 93% (typical) of desired voltage due to, for example, an overload condition, the corresponding power good pin is pulled low. Once the output voltage rises back above 96% (typical) of desired voltage power good pin is set back high. Power good signal is held low for at least 50 ms.

Device Functional Modes (continued)

If OVP, or TSD fault occurs during normal operation, all power good pins are pulled low. Once fault condition has lasted for 5 ms all buck converters are shut down. In case of UVLO fault buck regulators are instantly shut down. Once fault condition has ended buck converters are restarted in a Buck1 → Buck2 → Buck3 → Buck4 power-up sequence. A 500- μ s delay is included between each buck start-up. In case of TSD fault there is a 2-second safety delay before power-up sequence.

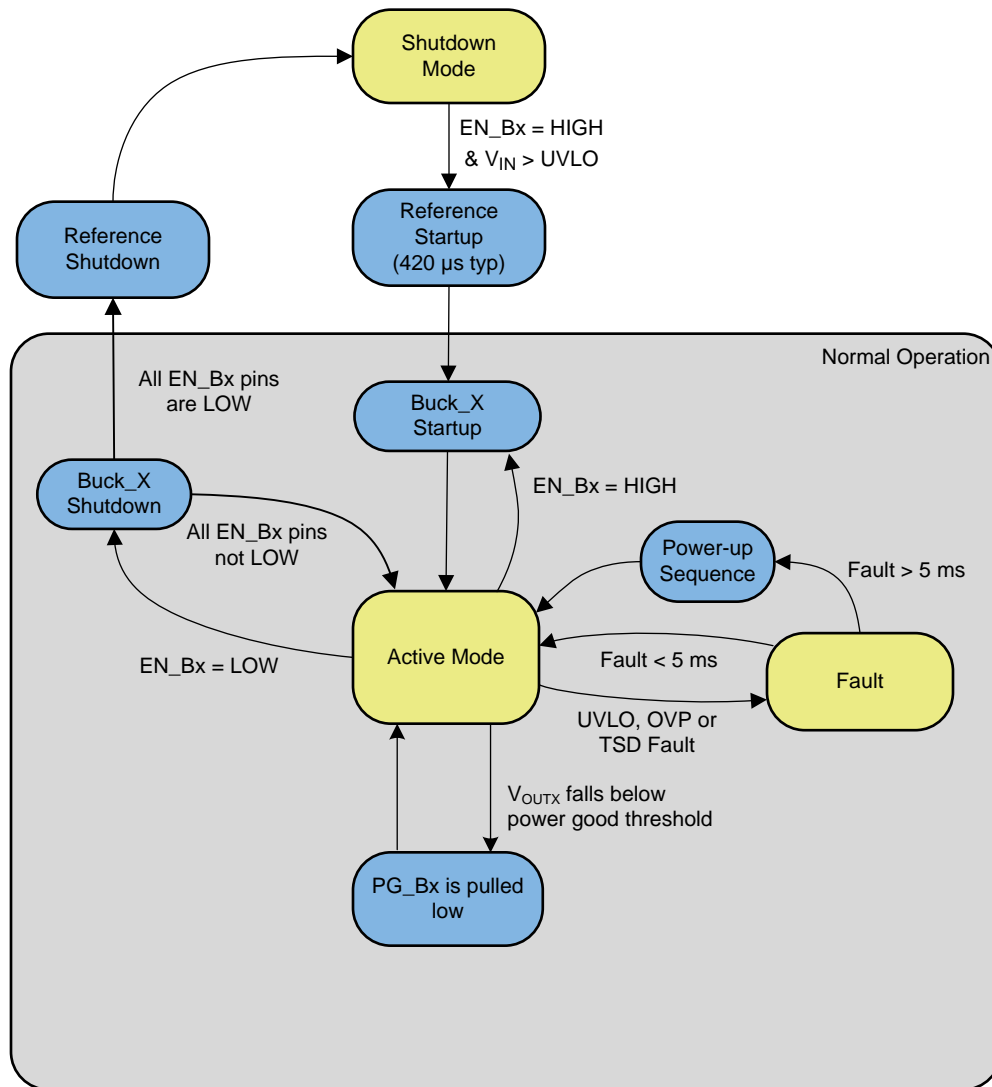


Figure 14. Device Functional Modes

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP8728D-Q1 is a quad-output Power Management Unit (PMU), optimized for low-power FPGAs, microprocessors, and DSPs.

8.2 Typical Application

Figure 15 shows an example of a typical application. A microcontroller controls each buck converter with separate enable signals. All four power good signals are connected to a microcontroller with dedicated pullup resistors. If only one master power good signal is required all power good signals can be connected in parallel and pulled up with a single pullup resistor. V_{OUT3} output voltage can be selected with a DEFSEL input. If V_{OUT3} output voltage control is not required during operation, output voltage can be selected by connecting DEFSEL pin to VDDIO or to GND.

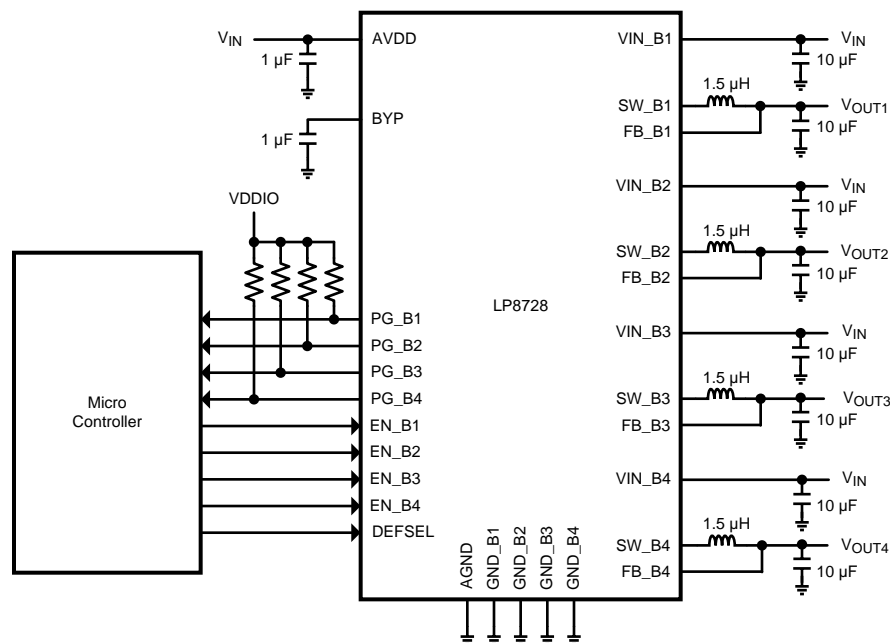


Figure 15. LP8728D-Q1 Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range (V_{IN})	4.5 V to 5.5 V
Buck converter output current	1 A maximum
Buck converter input capacitance	10 μ F, 6.3 V
Buck converter output capacitance	10 μ F, 6.3 V
Buck converter inductor	1.5 μ H, 1.5 A
AVDD pin bypass capacitor	1 μ F, 6.3 V
BYP pin bypass capacitor	1 μ F, 6.3 V

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor

The four converters operate with 1.5- μ H inductors. The inductor has to be selected based on the DC resistance and saturation current. The DC resistance of the inductor directly effects the efficiency of the converter. Therefore, an inductor with the lowest possible DC resistance should be selected for good efficiency. The inductor should have a saturation current rating equal or higher than the high-side switch current limit (1500 mA). To minimize radiated noise shielded inductor should be used. The inductor should be placed as close to the LP8728D-Q1 as possible, and the trace from the inductor to the buck converter switch pin needs to be wide enough to withstand the high switching currents.

8.2.2.2 Input and Output Capacitors

Because buck converters have a discontinuous input current, a low equivalent series resistance (ESR) input capacitor is required for the best input-voltage filtering and to minimize interference with other circuits caused by high input voltage spikes. Each DC-DC converter requires a 10- μ F ceramic input capacitor on its input pin VIN_Bx. The input capacitor capacitance can be increased without any limit for better input voltage filtering. Voltage rating of the capacitors should be at least 10V. A small 100-nF capacitor can be used in parallel to minimize high-frequency interferences. Input capacitors should be placed as close to the VIN_Bx pins as possible. Routing from input capacitor to VIN_Bx pins should be done on top layer without using any vias.

An output capacitor with a typical value of 10 μ F is recommended for each converter. Ceramic capacitors with low ESR value have lowest output voltage ripple and are recommended.

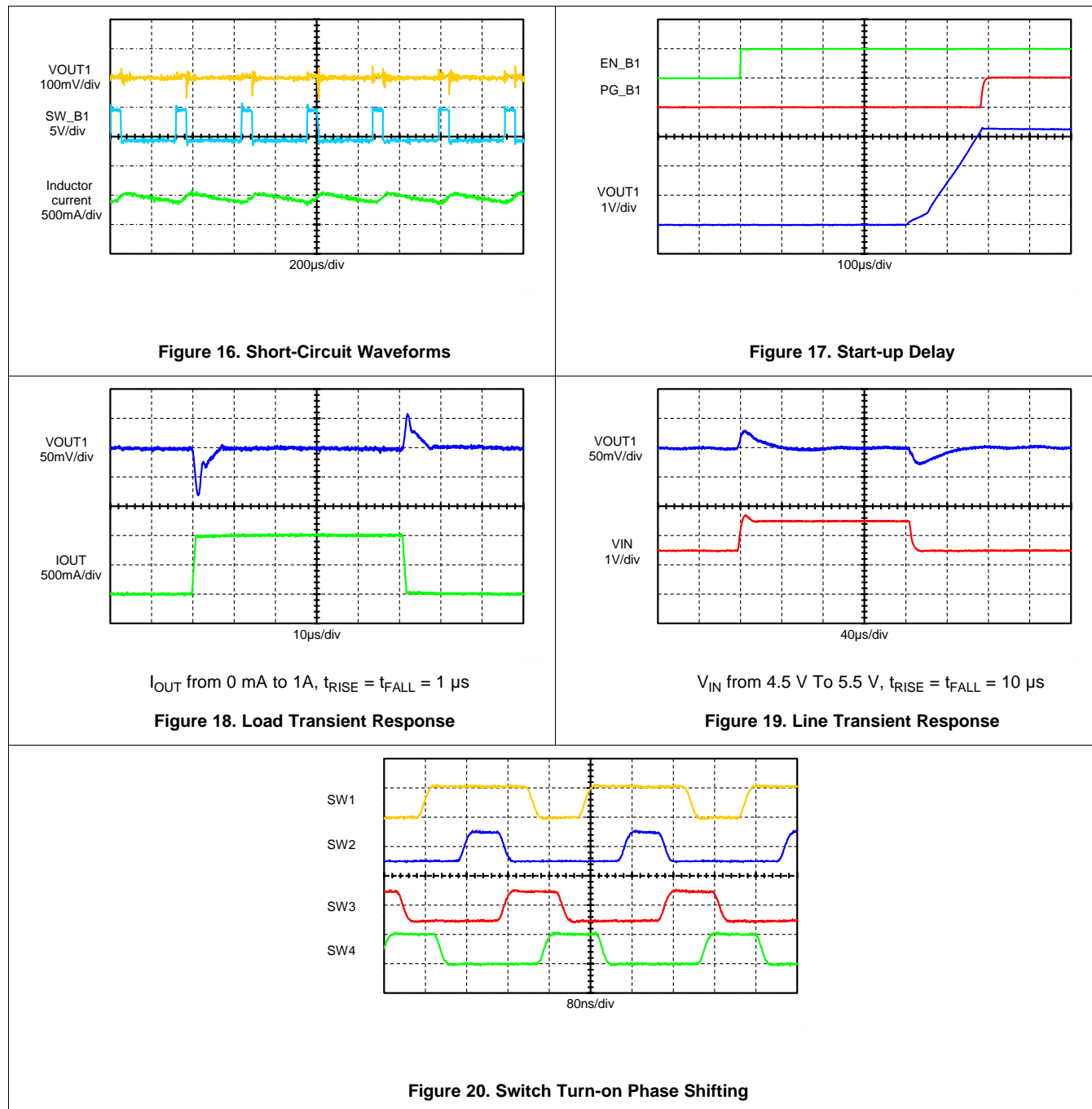
Some ceramic capacitors, especially those in small packages, exhibit a strong capacitance reduction with the increased applied DC voltage (DC bias effect). The capacitance value can fall below half of the nominal capacitance. This needs to be taken into consideration and, if necessary, use a capacitor with higher value or higher voltage rating.

Table 1. Recommended External Components

COMPONENT	DESCRIPTION	VALUE	TYPE	EXAMPLE
$C_{IN_B1,2,3,4}$	Buck regulator input capacitor	10 μ F	Ceramic, 10 V, X7R	MuRata, GRM21BR71A106KE51L
$C_{OUT_B1,2,3,4}$	Buck regulator output capacitor	10 μ F	Ceramic, 10 V, X7R	MuRata, GRM21BR71A106KE51L
C_{AVDD}	AVDD pin input capacitor	1 μ F	Ceramic, 10 V, X7R	MuRata, GRM188R71A105KA61D
C_{BYP}	Internal LDO bypass capacitor	1 μ F	Ceramic, 10 V, X7R	MuRata, GRM188R71A105KA61D
$L_{SW1,2,3,4}$	Buck regulator inductor	1.5 μ H	$I_{SAT} > 1.5$ A, DCR < 100 m Ω	TOKO MDT2520-CN1R5M

8.2.3 Application Performance Plots

Unless otherwise noted, $V_{IN} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, inductor type: TOKO MDT2520-CN1R5M, input and output capacitor type: MuRata GRM21BR71A106KE51L.



9 Power Supply Recommendations

The LP8728D-Q1 is designed to operate from an input voltage supply range between 4.5 V and 5.5 V. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

- AVDD and BYP pins must be bypassed to ground. 1- μ F ceramic capacitor is recommended. Place the capacitors close to the AVDD, BYP, and AGND pins.
- AGND pin must be tied to the PCB ground plane. Use multiple vias to minimize the inductance.
- AVDD pin must be connected to PCB VIN plane. Use multiple vias to minimize the inductance.
- Place the buck converter input capacitors as close to the buck input voltage and buck ground pins as possible.
- Place the buck converter output capacitors and inductors so that the buck converter switching loops can be routed on top layer. Try to minimize the area of the switching loops.
- Keep the trace width from switch pin to inductor wide enough to withstand the switching currents. Avoid any excess copper on the switch node to minimize parasitic switch node capacitance.
- Connect the exposed thermal pad to ground plane with multiple thermal vias.
- Avoid routing digital signals directly under the switching loops to avoid interferences.

10.2 Layout Example

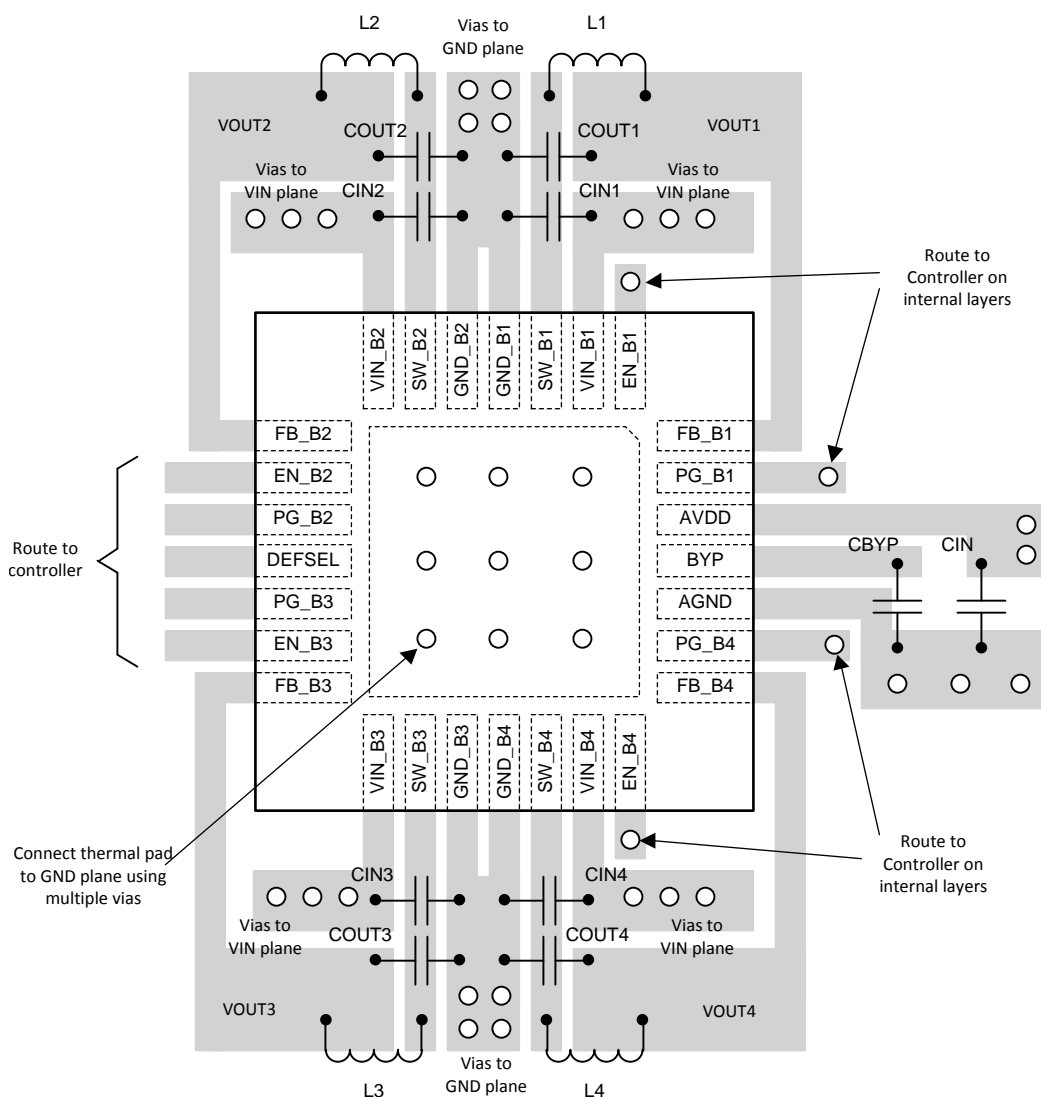


Figure 21. LP8728D-Q1 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Related Documentation

For related documentation see the following:

Texas Instruments Application Note 1187 *Leadless Leadframe Package (LLP)* ([SNOA401](#)).

See *Using the LP8728EVM Evaluation Module* ([SNVU231](#)) for more information about LP8728 evaluation module.

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP8728QSQX-D/NOPB	Active	Production	WQFN (RSG) 28	4500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	8728Q-D
LP8728QSQX-D/NOPB.A	Active	Production	WQFN (RSG) 28	4500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	8728Q-D
LP8728QSQX-D/NOPB.B	Active	Production	WQFN (RSG) 28	4500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	8728Q-D

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8728QSQX-D/NOPB	WQFN	RSG	28	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



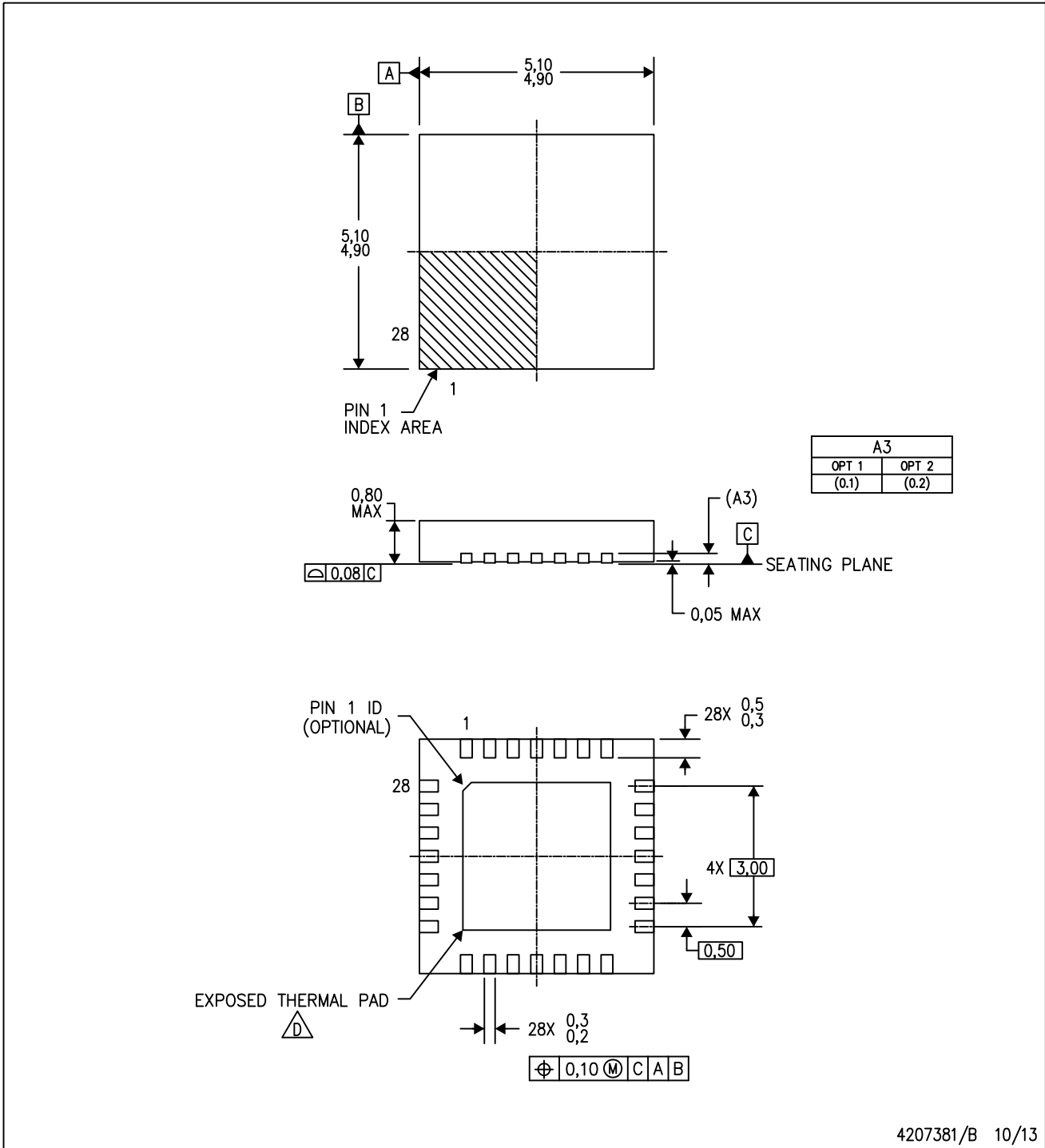
*All dimensions are nominal


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8728QSQX-D/NOPB	WQFN	RSG	28	4500	367.0	367.0	35.0

MECHANICAL DATA

RSG (S-PWQFN-N28)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.

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