MSP430FR247x Mixed-Signal Microcontrollers

1 Features

- Embedded microcontroller
  - 16-bit RISC architecture
  - Clock supports frequencies up to 16 MHz
  - Wide supply voltage range from 3.6 V down to 1.8 V (minimum supply voltage is restricted by SVS levels, see the SVS specifications)
- Optimized ultra-low-power modes
  - Active mode: 135 µA/MHz (typical)
  - Standby: LPM3.5, real-time clock (RTC) counter with 32768-Hz crystal: 660 nA (typical)
  - Shutdown (LPM4.5): 37 nA without SVS
- Low-power ferroelectric RAM (FRAM)
  - Up to 64KB of nonvolatile memory
  - Built-in error correction code (ECC)
  - Configurable write protection
  - Unified memory of program, constants, and storage
  - 10^{15} write cycle endurance
  - Radiation resistant and nonmagnetic
- Intelligent digital peripherals
  - Four 16-bit timers with three capture/compare registers each (Timer_A3)
  - One 16-bit timer with seven capture/compare registers (Timer_B7)
  - One 16-bit counter-only RTC
  - 16-bit cyclic redundancy check (CRC)
- Enhanced serial communications with support for pin remap feature
  - Two eUSCI_A supports UART, IrDA, and SPI
  - Two eUSCI_B supports SPI and I^2C
- High-performance analog
  - One 12-bit analog-to-digital converter (ADC) with up to 12 channels
    - Internal shared reference (1.5, 2.0, or 2.5 V)
    - Sample-and-hold 200 ksps
  - One enhanced comparator (eCOMP)
    - Integrated 6-bit DAC as reference voltage
    - Programmable hysteresis
    - Configurable high-power and low-power modes
- Clock system (CS)
  - On-chip 32-kHz RC oscillator (REFO) with 1 µA support
  - On-chip 16-MHz digitally controlled oscillator (DCO) with frequency-locked loop (FLL)
    - ±1% accuracy with on-chip reference at room temperature
  - On-chip very low-frequency 10-kHz oscillator (VLO)
  - On-chip high-frequency modulation oscillator (MODOSC)
  - External 32-kHz crystal oscillator (LFXT)
  - Programmable MCLK prescalar of 1 to 128
  - SMCLK derived from MCLK with programmable prescalar of 1, 2, 4, or 8
- General input/output and pin functionality
  - 43 I/Os on LQFP-48 package
  - 43 interrupt pins on all GPIOs can wake MCU from low-power modes
- Development tools and software
  - Development tools
    - Target development board MSP-TS430PT48A
    - LaunchPad™ development kit LP-MSP430FR2476
- Family members (also see Device Comparison)
  - MSP430FR2476: 64KB of program FRAM, 512B of information FRAM, 8KB of RAM
  - MSP430FR2475: 32KB of program FRAM, 512B of information FRAM, 6KB of RAM
- Package options
  - 48-pin: LQFP (PT)
  - 40-pin: VQFN (RHA)
  - 32-pin: VQFN (RHB)

2 Applications

- Small form factor industrial sensors
- Low-power medical, health, and fitness
- Battery packs
- EPOS
- Appliances
- Thermostats
- Electric toothbrushes
- PC accessories

3 Description

MSP430FR247x microcontrollers (MCUs) are part of the MSP430™ MCU value line portfolio of ultra-low-power low-cost devices for sensing and measurement applications. MSP430FR247x MCUs integrate a 12-bit SAR ADC and one comparator. The MSP430FR247x MCUs support an extended temperature range from –40°C up to 105°C, so higher temperature industrial applications can benefit from the devices' FRAM data-logging capabilities.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

MSP430FR247x MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get your design started quickly. Development kits include the MSP-TS430PT48 48-pin target development board. TI also provides free MSP430Ware™ software, which is available as a component of Code Composer Studio™ IDE desktop and cloud versions withinTI Resource Explorer. MSP430 MCUs are also supported by extensive online collateral, such as our housekeeping example series, MSP Academy training, and online support through the TI E2E™ support forums.

The MSP430 ultra-low-power (ULP) FRAM microcontroller platform combines uniquely embedded FRAM and a holistic ultra-low-power system architecture, allowing system designers to increase performance while lowering energy consumption. FRAM technology combines the low-energy fast writes, flexibility, and endurance of RAM with the nonvolatile behavior of flash.

The TI MSP430 family of low-power microcontrollers consists of devices with different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The MCU features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the MCU to wake up from low-power modes to active mode in less than 10 µs (typical).

For complete module descriptions, see the MSP430FR4xx and MSP430FR2xx Family User's Guide.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE(2)
MSP430FR2476TPT	LQFP (48)	7 mm × 7 mm
MSP430FR2475TPT	LQFP (48)	7 mm × 7 mm
MSP430FR2476TRHA	VQFN (40)	6 mm × 6 mm
MSP430FR2475TRHA	VQFN (40)	6 mm × 6 mm
MSP430FR2476TRHB	VQFN (32)	5 mm × 5 mm
MSP430FR2475TRHB	VQFN (32)	5 mm × 5 mm

(1) For the most current part, package, and ordering information, see the *Package Option Addendum* in Section 12, or see the TI website at www.ti.com.
(2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in Section 12.

CAUTION

System-level ESD protection must be applied in compliance with the device-level ESD specification to prevent electrical overstress or disturbing of data or code memory. See MSP430 System-Level ESD Considerations for more information.

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4 Functional Block Diagram

Figure 4-1 shows the functional block diagram.

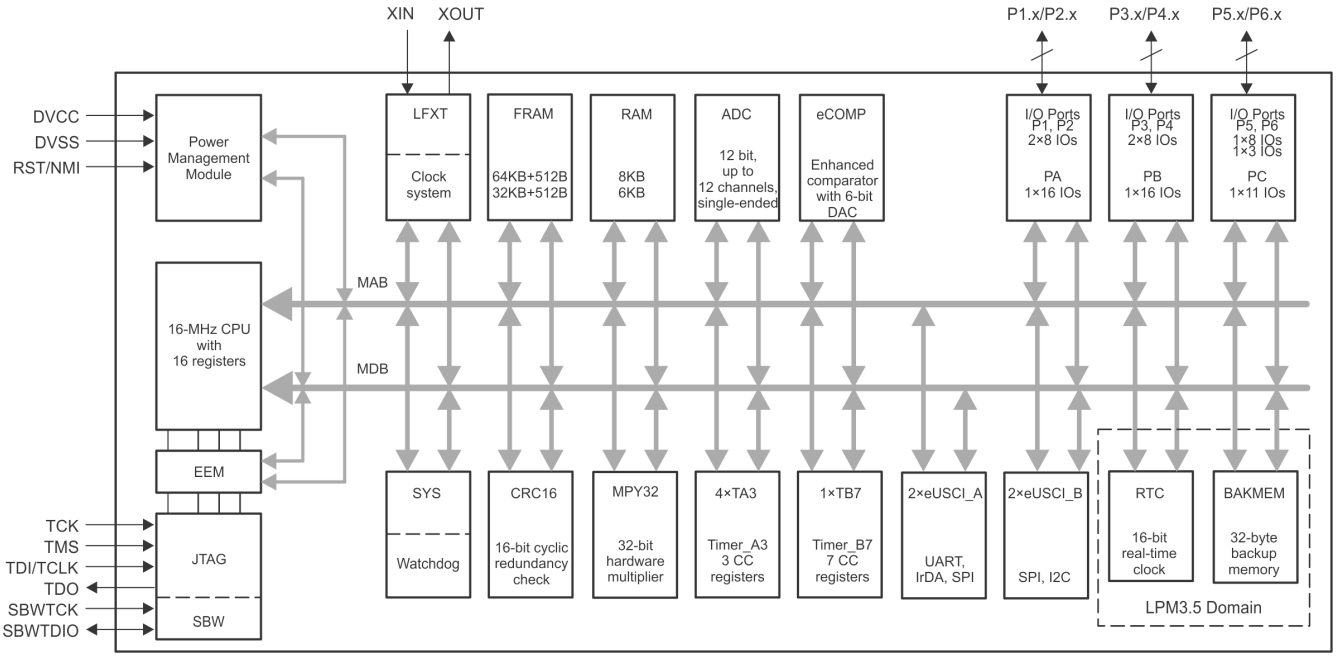

Figure 4-1. Functional Block Diagram

- The MCU has one main power pair of DVCC and DVSS that supplies digital and analog modules. Recommended bypass and decoupling capacitors are 4.7 µF to 10 µF and 0.1 µF, respectively, with ±5% accuracy.
- All GPIOs feature the pin interrupt function and can wake the MCU from all LPMs.
- In LPM3.5, the RTC module can be functional while the rest of the peripherals are off.

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from revision B to revision C

Changes from December 11, 2019 to September 14, 2021	Page
• Updated the numbering format for tables, figures, and cross references throughout the document	1
• Corrected the RAM size for the MSP430FR2475 throughout the document (changed from 4KB to 6KB)	1
• Added links to online collateral in Section 3 *Description*	1
• Corrected the pin numbers for the Veref+ and Veref- signals in Table 7-2, *Signal Descriptions*	15
• Corrected the TAxRMP, USCIA0RMP, USCIB0RMP, and USCIB1RMP bit names in the notes for Table 7-2, *Signal Descriptions*	15
• Corrected the USCIA0RMP and USCIBxRMP bit names in Section 9.10.7, *Enhanced Universal Serial Communication Interface (eUSCI_A0, eUSCI_B0)*	54
• Corrected the TAxRMP bit name in the notes for Table 9-16, *TA2 and TA3 Pin Configurations of Remap Functionality*	55
• Added an inverter to the Schmitt-trigger enable in Figure 9-4, *Port Input/Output With Schmitt Trigger*	64
• Corrected the value of the P5SEL.x column for P5.3 and P5.4 in Table 9-27, *Port P5 (P5.0 to P5.7) Pin Functions*	69
• Added the SYSCFG3 register to Table 9-35, *SYS Registers (Base Address: 0140h)*	74

Changes from revision A to revision B

Changes from April 26, 2019 to December 10, 2019	Page
• Updated Section 1, *Features*	1
• Changed the note that begins "Supply voltage changes faster than 0.2 V/µs can trigger a BOR reset..." in Section 8.3, *Recommended Operating Conditions*	20
• Added the note that begins "TI recommends that power to the DVCC pin must not exceed the limits..." in Section 8.3, *Recommended Operating Conditions*	20
• Changed the note that begins "A capacitor tolerance of ±20% or better is required..." in Section 8.3, *Recommended Operating Conditions*	20
• Added the note "See *MSP430 32-kHz Crystal Oscillators* for details on crystal section, layout, and testing" to Section 8.12.3.1, *XT1 Crystal Oscillator (Low Frequency)*	27
• Changed the note that begins "Requires external capacitors at both terminals..." in Section 8.12.3.1, *XT1 Crystal Oscillator (Low Frequency)*	27
• Added the $t_{TA,cap}$ parameter in Section 8.12.6.1, *Timer_A*	34
• Added the $t_{TB,cap}$ parameter in Section 8.12.6.2, *Timer_B*	34
• Corrected the test conditions for the R_I parameter in Section 8.12.8.1, *ADC, Power Supply and Input Range Conditions*	40
• Removed ADCDIV from the equations for $t_{CONVERT}$ because ADCCLK is after division in Section 8.12.8.2, *ADC, Timing Parameters*	40
• Added the note that begins "$t_{Sample} = \ln(2^{n+1}) \times \tau$ ..." in Section 8.12.8.2, *ADC, Timing Parameters*	40
• Changed CRC covered end address to 0x1AF7 in table note (1) in Table 9-30 , *Device Descriptors*	71

Changes from initial release to revision A

Changes from March 12, 2019 to April 25, 2019	Page
• Changed document status to Production Data	1
• Added memory sizes for MSP430FR2673 and MSP430FR2672 in Figure 4-1, *Functional Block Diagram*	3
• Updated Section 8.7 *Low-Power Mode (LPM3, LPM4) Supply Currents (Into V_{CC}) Excluding External Current* with production values	22
• Updated Section 8.12.3.2 *DCO FLL, Frequency* with production values	28

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6 Device Comparison

Table 6-1 summarizes the features of the available family members.

Table 6-1. Device Comparison

DEVICE(1) (2)	PROGRAM FRAM + INFORMATION FRAM (KB)	SRAM (KB)	TA0, TA1, TA2, TA3	TB0	eUSCI_A0 eUSCI_A1	eUSCI_B0 eUSCI_B1	12-BIT ADC CHANNELS	eCOMP	GPIOs	PACKAGE
MSP430FR2476TPT	64 + 0.5	8	4, 3 × CCR(3)	1, 7 × CCR(4)	2	2	12	1	43	48 LQFP (PT)
MSP430FR2475TPT	32 + 0.5	6	4, 3 × CCR(3)	1, 7 × CCR(4)	2	2	12	1	43	48 LQFP (PT)
MSP430FR2476TRHA	64 + 0.5	8	4, 3 × CCR(3)	1, 7 × CCR(4)	2	2	10	1	35	40 VQFN (RHA)
MSP430FR2475TRHA	32 + 0.5	6	4, 3 × CCR(3)	1, 7 × CCR(4)	2	2	10	1	35	40 VQFN (RHA)
MSP430FR2476TRHB	64 + 0.5	8	4, 3 × CCR(3)	1, 7 × CCR(5)	2	2	8	1	27	32 VQFN (RHB)
MSP430FR2475TRHB	32 + 0.5	6	4, 3 × CCR (3)	1, 7 × CCR(5)	2	2	8	1	27	32 VQFN (RHB)

(1) For the most current package and ordering information, see the *Package Option Addendum* in Section 12, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.
(3) A CCR register is a configurable register that provides internal and external capture or compare inputs, or internal and external PWM outputs. TA0 and TA1 are externally connected on CCR1, CCR2. TA2 and TA3 are externally connected on CCR0 to CCR2.
(4) A CCR register is a configurable register that provides internal and external capture or compare inputs, or internal and external PWM outputs. TB0 is externally connected on CCR0 to CCR6.
(5) A CCR register is a configurable register that provides internal capture only, CCR0 to CCR6 registers can only be used for period timing and interrupt generation, NO PWM outputs functionality.

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6.1 Related Products

For information about other devices in this family of products or related products, see the following links.

Products for microcontrollers

Our diverse portfolio of 16- and 32-bit microcontrollers (MCUs) with real-time control capabilities and high-precision analog integration are optimized for industrial and automotive applications. Backed by decades of expertise and innovative hardware and software solutions, our MCUs can meet the needs of any design and budget.

Products for MSP430 microcontrollers

Our 16-bit MSP430™ microcontrollers (MCUs) provide affordable solutions for all applications. Our leadership in integrated precision analog enables designers to enhance system performance and lower system costs. Designers can find a cost-effective MCU within the broad MSP430 portfolio of over 2000 devices for virtually any need. Get started quickly and reduce time to market with our simplified tools, software, and best-in-class support.

Reference designs for MSP430FR2476

Find reference designs leveraging the best in TI technology – from analog and power management to embedded processors

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7 Terminal Configuration and Functions

7.1 Pin Diagrams

Figure 7-1 shows the pinout of the 48-pin PT package.

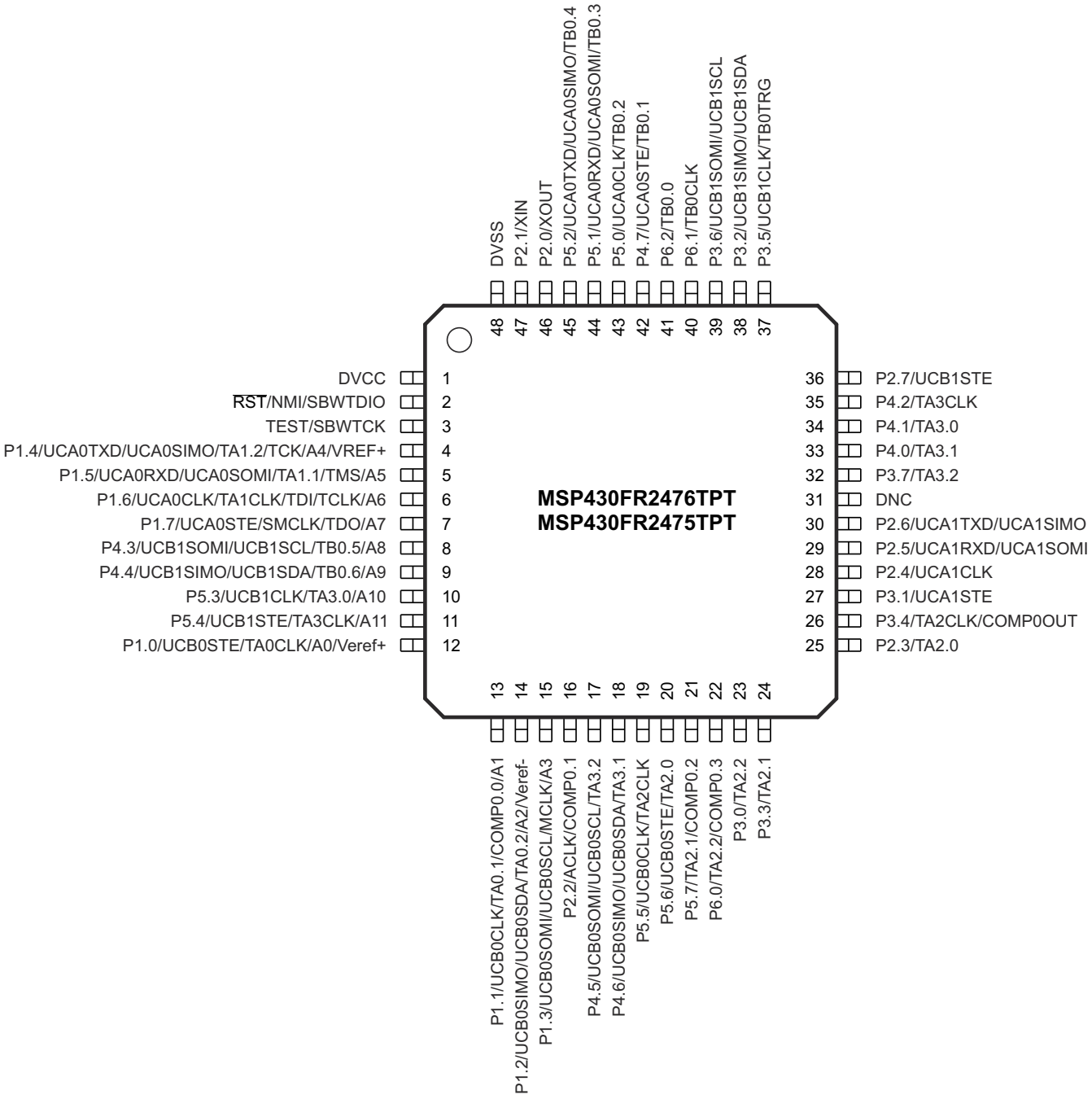

Figure 7-1. 48-Pin PT Package (Top View)

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Figure 7-2 shows the pinout of the 40-pin RHA package.

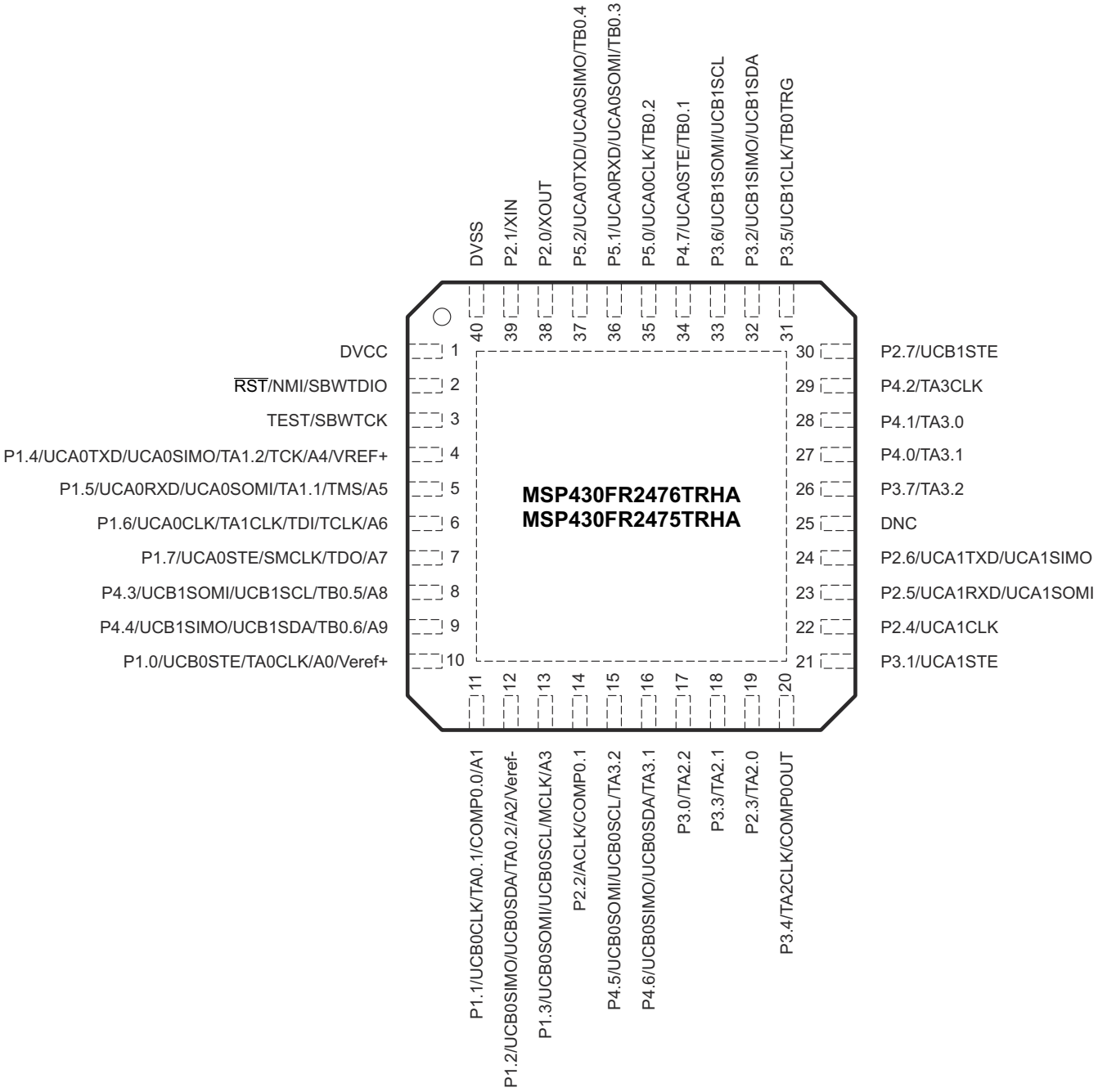

Figure 7-2. 40-Pin RHA Package (Top View)

Figure 7-3 shows the pinout of the 32-pin RHB package.

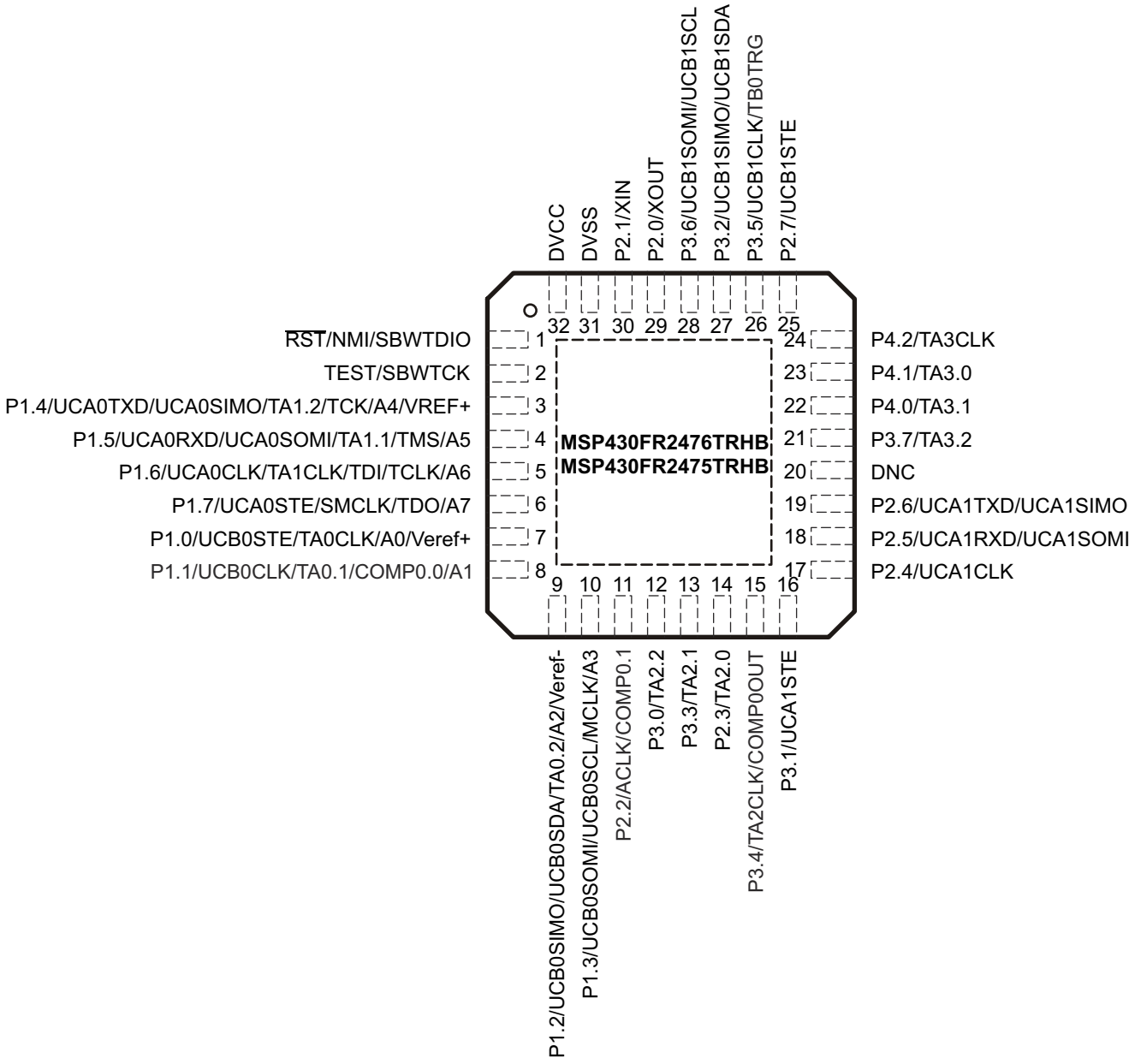

Figure 7-3. 32-Pin RHB Package (Top View)

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7.2 Pin Attributes

Table 7-1 lists the attributes of all pins.

Table 7-1. Pin Attributes

PIN NUMBER			SIGNAL NAME[1] [2]	SIGNAL TYPE[3]	BUFFER TYPE[4]	POWER SOURCE[5]	RESET STATE AFTER BOR[6]
PT	RHA	RHB					
1	1	32	DVCC	P	Power	DVCC	N/A
2	2	1	$\overline{\text{RST}}$ (RD)	I	LVCMOS	DVCC	PU
			NMI	I	LVCMOS	DVCC	–
			SBWTDIO	I/O	LVCMOS	DVCC	–
3	3	2	TEST (RD)	I	LVCMOS	DVCC	PD
			SBWTCK	I	LVCMOS	DVCC	–
4	4	3	P1.4 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA0TXD	O	LVCMOS	DVCC	–
			UCA0SIMO	I/O	LVCMOS	DVCC	–
			TA1.2	I/O	LVCMOS	DVCC	–
			TCK	I	LVCMOS	DVCC	–
			A4	I	Analog	DVCC	–
			VREF+	O	Power	DVCC	–
5	5	4	P1.5 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA0RXD	I	LVCMOS	DVCC	–
			UCA0SOMI	I/O	LVCMOS	DVCC	–
			TA1.1	I/O	LVCMOS	DVCC	–
			TMS	I	LVCMOS	DVCC	–
			A5	I	Analog	DVCC	–
6	6	5	P1.6 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA0CLK	I/O	LVCMOS	DVCC	–
			TA1CLK	I	LVCMOS	DVCC	–
			TDI	I	LVCMOS	DVCC	–
			TCLK	I	LVCMOS	DVCC	–
			A6	I	Analog	DVCC	–
7	7	6	P1.7 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA0STE	I/O	LVCMOS	DVCC	–
			SMCLK	O	LVCMOS	DVCC	–
			TDO	O	LVCMOS	DVCC	–
			A7	I	Analog	DVCC	–
8	8	–	P4.3 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB1SOMI	I/O	LVCMOS	DVCC	–
			UCB1SCL	I/O	LVCMOS	DVCC	–
			TB0.5	I/O	LVCMOS	DVCC	–
			A8	I	Analog	DVCC	–
9	9	–	P4.4 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB1SIMO	I/O	LVCMOS	DVCC	–
			UCB1SDA	I/O	LVCMOS	DVCC	–
			TB0.6	I/O	LVCMOS	DVCC	–
			A9	I	Analog	DVCC	–

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Table 7-1. Pin Attributes (continued)

PIN NUMBER			SIGNAL NAME[1] [2]	SIGNAL TYPE[3]	BUFFER TYPE[4]	POWER SOURCE[5]	RESET STATE AFTER BOR[6]
PT	RHA	RHB					
10	–	–	P5.3 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB1CLK	I/O	LVCMOS	DVCC	–
			TA3.0	I/O	LVCMOS	DVCC	–
			A10	I	Analog	DVCC	–
11	–	–	P5.4 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB1STE	I/O	LVCMOS	DVCC	–
			TA3CLK	I/O	LVCMOS	DVCC	–
			A11	I	Analog	DVCC	–
12	10	7	P1.0 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0STE	I/O	LVCMOS	DVCC	–
			TA0CLK	I	LVCMOS	DVCC	–
			A0	I	Analog	DVCC	–
			Veref+	I	Power	DVCC	–
13	11	8	P1.1 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0CLK	I/O	LVCMOS	DVCC	–
			TA0.1	I/O	LVCMOS	DVCC	–
			A1	I	Analog	DVCC	–
			COMP0.0	I	Analog	DVCC	–
14	12	9	P1.2 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0SIMO	I/O	LVCMOS	DVCC	–
			UCB0SDA	I/O	LVCMOS	DVCC	–
			TA0.2	I/O	LVCMOS	DVCC	–
			A2	I	Analog	DVCC	–
			Veref-	I	Power	DVCC	–
15	13	10	P1.3 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0SOMI	I/O	LVCMOS	DVCC	–
			UCB0SCL	I/O	LVCMOS	DVCC	–
			MCLK	O	LVCMOS	DVCC	–
			A3	I	Analog	DVCC	–
16	14	11	P2.2 (RD)	I/O	LVCMOS	DVCC	OFF
			ACLK	O	LVCMOS	DVCC	–
			COMP0.1	I	Analog	DVCC	–
17	15	–	P4.5 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0SOMI	I/O	LVCMOS	DVCC	–
			UCB0SCL	I/O	LVCMOS	DVCC	–
			TA3.2	I/O	LVCMOS	DVCC	–
18	16	–	P4.6 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0SIMO	I/O	LVCMOS	DVCC	–
			UCB0SDA	I/O	LVCMOS	DVCC	–
			TA3.1	I/O	LVCMOS	DVCC	–
19	–	–	P5.5 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0CLK	I/O	LVCMOS	DVCC	–
			TA2CLK	I/O	LVCMOS	DVCC	–

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Table 7-1. Pin Attributes (continued)

PIN NUMBER			SIGNAL NAME[1] [2]	SIGNAL TYPE[3]	BUFFER TYPE[4]	POWER SOURCE[5]	RESET STATE AFTER BOR[6]
PT	RHA	RHB					
20	–	–	P5.6 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0STE	I/O	LVCMOS	DVCC	–
			TA2.0	I/O	LVCMOS	DVCC	–
21	–	–	P5.7 (RD)	I/O	LVCMOS	DVCC	OFF
			TA2.1	I/O	LVCMOS	DVCC	–
			COMP0.2	I	Analog	DVCC	–
22	–	–	P6.0 (RD)	I/O	LVCMOS	DVCC	OFF
			TA2.2	I/O	LVCMOS	DVCC	–
			COMP0.3	I	Analog	DVCC	–
23	17	12	P3.0 (RD)	I/O	LVCMOS	DVCC	OFF
			TA2.2	I/O	LVCMOS	DVCC	–
24	18	13	P3.3 (RD)	I/O	LVCMOS	DVCC	OFF
			TA2.1	I/O	LVCMOS	DVCC	–
25	19	14	P2.3 (RD)	I/O	LVCMOS	DVCC	OFF
			TA2.0	I/O	LVCMOS	DVCC	–
26	20	15	P3.4 (RD)	I/O	LVCMOS	DVCC	OFF
			TA2CLK	I/O	LVCMOS	DVCC	–
			COMP0OUT	O	LVCMOS	DVCC	–
27	21	16	P3.1 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA1STE	I/O	LVCMOS	DVCC	–
28	22	17	P2.4 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA1CLK	I/O	LVCMOS	DVCC	–
29	23	18	P2.5 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA1RXD	I	LVCMOS	DVCC	–
			UCA1SOMI	I/O	LVCMOS	DVCC	–
30	24	19	P2.6 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA1TXD	O	LVCMOS	DVCC	–
			UCA1SIMO	I/O	LVCMOS	DVCC	–
31	25	20	DNC[7]	–	–	–	–
32	26	21	P3.7 (RD)	I/O	LVCMOS	DVCC	OFF
			TA3.2	I/O	LVCMOS	DVCC	–
33	27	22	P4.0 (RD)	I/O	LVCMOS	DVCC	OFF
			TA3.1	I/O	LVCMOS	DVCC	–
34	28	23	P4.1 (RD)	I/O	LVCMOS	DVCC	OFF
			TA3.0	I/O	LVCMOS	DVCC	–
35	29	24	P4.2 (RD)	I/O	LVCMOS	DVCC	OFF
			TA3CLK	I/O	LVCMOS	DVCC	–
36	30	25	P2.7 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB1STE	I/O	LVCMOS	DVCC	–
37	31	26	P3.5 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB1CLK	I/O	LVCMOS	DVCC	–
			TB0TRG	I	LVCMOS	DVCC	–

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Table 7-1. Pin Attributes (continued)

PIN NUMBER			SIGNAL NAME[1] [2]	SIGNAL TYPE[3]	BUFFER TYPE[4]	POWER SOURCE[5]	RESET STATE AFTER BOR[6]
PT	RHA	RHB					
38	32	27	P3.2 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB1SIMO	I/O	LVCMOS	DVCC	–
			UCB1SDA	I/O	LVCMOS	DVCC	–
39	33	28	P3.6(RD)	I/O	LVCMOS	DVCC	OFF
			UCB1SOMI	I/O	LVCMOS	DVCC	–
			UCB1SCL	I/O	LVCMOS	DVCC	–
40	–	–	P6.1 (RD)	I/O	LVCMOS	DVCC	OFF
			TB0CLK	I/O	LVCMOS	DVCC	–
41	–	–	P6.2 (RD)	I/O	LVCMOS	DVCC	OFF
			TB0.0	I/O	LVCMOS	DVCC	–
42	34	–	P4.7 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA0STE	I/O	LVCMOS	DVCC	–
			TB0.1	I/O	LVCMOS	DVCC	–
43	35	–	P5.0 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA0CLK	I/O	LVCMOS	DVCC	–
			TB0.2	I	LVCMOS	DVCC	–
44	36	–	P5.1 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA0RXD	I	LVCMOS	DVCC	–
			UCA0SOMI	I/O	LVCMOS	DVCC	–
			TB0.3	I/O	LVCMOS	DVCC	–
45	37	–	P5.2 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA0TXD	O	LVCMOS	DVCC	–
			UCA0SIMO	I/O	LVCMOS	DVCC	–
			TB0.4	I/O	LVCMOS	DVCC	–
46	38	29	P2.0 (RD)	I/O	LVCMOS	DVCC	OFF
			XOUT	O	LVCMOS	DVCC	–
47	39	30	P2.1 (RD)	I/O	LVCMOS	DVCC	OFF
			XIN	I	LVCMOS	DVCC	–
48	40	31	DVSS	P	Power	DVCC	N/A

(1) Signals names with (RD) denote the reset default pin name.
(2) To determine the pin mux encodings for each pin, see Section 9.11.
(3) Signal types: I = input, O = output, I/O = input or output
(4) Buffer types: LVCMOS, Analog, or Power (see Table 7-3)
(5) The power source shown in this table is the I/O power source, which may differ from the module power source.
(6) Reset States:
OFF = High impedance with Schmitt trigger and pullup or pulldown (if available) disabled
PU = Pullup is enabled
PD = Pulldown is enabled
N/A = Not applicable
(7) DNC = do not connect

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7.3 Signal Descriptions

Table 7-2 describes the signals for all device variants and package options.

Table 7-2. Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NUMBER			PIN TYPE[1]	DESCRIPTION
		PT	RHA	RHB		
ADC	A0	12	10	7	I	Analog input A0
	A1	13	11	8	I	Analog input A1
	A2	14	12	9	I	Analog input A2
	A3	15	13	10	I	Analog input A3
	A4	4	4	3	I	Analog input A4
	A5	5	5	4	I	Analog input A5
	A6	6	6	5	I	Analog input A6
	A7	7	7	6	I	Analog input A7
	A8	8	8	–	I	Analog input A8
	A9	9	9	–	I	Analog input A9
	A10	10	–	–	I	Analog input A10
	A11	11	–	–	I	Analog input A11
	Veref+	12	10	7	I	ADC positive reference
	Veref-	14	12	9	I	ADC negative reference
eCOMP0	COMP0.0	13	11	8	I	Enhanced comparator input channel C0
	COMP0.1	16	14	11	I	Enhanced comparator input channel C1
	COMP0.2	21	–	–	I	Enhanced comparator input channel C2
	COMP0.3	22	–	–	I	Enhanced comparator input channel C3
	COMP0OUT	26	20	15	O	Enhanced comparator output channel COUT
Clock	ACLK	16	14	11	I/O	ACLK output
	MCLK	15	13	10	O	MCLK output
	SMCLK	7	7	6	O	SMCLK output
	XIN	47	39	30	I	Input terminal for crystal oscillator
	XOUT	46	38	29	O	Output terminal for crystal oscillator
Debug	SBWTCK	3	3	2	I	Spy-Bi-Wire input clock
	SBWTDIO	2	2	1	I/O	Spy-Bi-Wire data input/output
	TCK	4	4	3	I	Test clock
	TCLK	6	6	5	I	Test clock input
	TDI	6	6	5	I	Test data input
	TDO	7	7	6	O	Test data output
	TEST	3	3	2	I	Test Mode pin – selected digital I/O on JTAG pins
	TMS	5	5	4	I	Test mode select
GPIO, Port 1	P1.0	12	10	7	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P1.1	13	11	8	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P1.2	14	12	9	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P1.3	15	13	10	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P1.4	4	4	3	I/O	General-purpose I/O with port interrupt and wake from LPMx.5 [2]
	P1.5	5	5	4	I/O	General-purpose I/O with port interrupt and wake from LPMx.5[2]
	P1.6	6	6	5	I/O	General-purpose I/O with port interrupt and wake from LPMx.5[2]
	P1.7	7	7	6	I/O	General-purpose I/O with port interrupt and wake from LPMx.5[2]

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Table 7-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NUMBER			PIN TYPE[1]	DESCRIPTION
		PT	RHA	RHB		
GPIO, Port 2	P2.0	46	38	29	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P2.1	47	39	30	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P2.2	16	14	11	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P2.3	25	19	14	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P2.4	28	22	17	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P2.5	29	23	18	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P2.6	30	24	19	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P2.7	36	30	25	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
GPIO, Port 3	P3.0	23	17	12	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P3.1	27	21	16	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P3.2	38	32	27	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P3.3	24	18	13	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P3.4	26	20	15	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P3.5	37	31	26	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P3.6	39	33	28	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P3.7	32	26	21	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
GPIO, Port 4	P4.0	33	27	22	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P4.1	34	28	23	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P4.2	35	29	24	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P4.3	8	8	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P4.4	9	9	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P4.5	17	15	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P4.6	18	16	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P4.7	42	34	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
GPIO, Port 5	P5.0	43	35	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P5.1	44	36	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P5.2	45	37	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P5.3	10	–	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P5.4	11	–	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P5.5	19	–	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P5.6	20	–	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P5.7	21	–	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
GPIO, Port 6	P6.0	22	–	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P6.1	40	–	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P6.2	41	–	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
I^2C	UCB0SCL[3]	15	13	10	I/O	eUSCI_B0 I^2C clock
	UCB0SDA[3]	14	12	9	I/O	eUSCI_B0 I^2C data
	UCB0SCL[4]	17	15	–	I/O	eUSCI_B0 I^2C clock
	UCB0SDA[4]	18	16	–	I/O	eUSCI_B0 I^2C data
	UCB1SCL[3]	39	33	28	I/O	eUSCI_B1 I^2C clock
	UCB1SDA[3]	38	32	27	I/O	eUSCI_B1 I^2C data
	UCB1SCL[4]	8	8	–	I/O	eUSCI_B1 I^2C clock
	UCB1SDA[4]	9	9	–	I/O	eUSCI_B1 I^2C data

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Table 7-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NUMBER			PIN TYPE[1]	DESCRIPTION
		PT	RHA	RHB		
Power	DVCC	1	1	32	P	Power supply
	DVSS	48	40	31	P	Power ground
	VREF+	4	4	3	P	Output of positive reference voltage with ground as reference
SPI	UCA0STE[3]	7	7	6	I/O	eUSCI_A0 SPI slave transmit enable
	UCA0CLK[3]	6	6	5	I/O	eUSCI_A0 SPI clock input/output
	UCA0SOMI[3]	5	5	4	I/O	eUSCI_A0 SPI slave out/master in
	UCA0SIMO[3]	4	4	3	I/O	eUSCI_A0 SPI slave in/master out
	UCA0STE[4]	42	34	–	I/O	eUSCI_A0 SPI slave transmit enable
	UCA0CLK[4]	43	35	–	I/O	eUSCI_A0 SPI clock input/output
	UCA0SOMI[4]	44	36	–	I/O	eUSCI_A0 SPI slave out/master in
	UCA0SIMO[4]	45	37	–	I/O	eUSCI_A0 SPI slave in/master out
	UCA1STE	27	21	16	I/O	eUSCI_A1 SPI slave transmit enable
	UCA1CLK	28	22	17	I/O	eUSCI_A1 SPI clock input/output
	UCA1SOMI	29	23	18	I/O	eUSCI_A1 SPI slave out/master in
	UCA1SIMO	30	24	19	I/O	eUSCI_A1 SPI slave in/master out
	UCB0STE[3]	12	10	7	I/O	eUSCI_B0 slave transmit enable
	UCB0CLK[3]	13	11	8	I/O	eUSCI_B0 clock input/output
	UCB0SOMI[3]	15	13	10	I/O	eUSCI_B0 SPI slave out/master in
	UCB0SIMO[3]	14	12	9	I/O	eUSCI_B0 SPI slave in/master out
	UCB0STE[4]	20	–	–	I/O	eUSCI_B0 slave transmit enable
	UCB0CLK[4]	19	–	–	I/O	eUSCI_B0 clock input/output
	UCB0SOMI[4]	17	–	–	I/O	eUSCI_B0 SPI slave out/master in
	UCB0SIMO[4]	18	–	–	I/O	eUSCI_B0 SPI slave in/master out
	UCB1STE[3]	36	30	25	I/O	eUSCI_B1 slave transmit enable
	UCB1CLK[3]	37	31	26	I/O	eUSCI_B1 clock input/output
	UCB1SOMI[3]	39	33	28	I/O	eUSCI_B1 SPI slave out/master in
	UCB1SIMO[3]	38	32	27	I/O	eUSCI_B1 SPI slave in/master out
	UCB1STE[4]	11	–	–	I/O	eUSCI_B1 slave transmit enable
	UCB1CLK[4]	10	–	–	I/O	eUSCI_B1 clock input/output
	UCB1SOMI[4]	8	–	–	I/O	eUSCI_B1 SPI slave out/master in
	UCB1SIMO[4]	9	–	–	I/O	eUSCI_B1 SPI slave in/master out
System	NMI	2	2	1	I	Nonmaskable interrupt input
	$\overline{\text{RST}}$	2	2	1	I	Active-low reset input

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Table 7-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NUMBER			PIN TYPE[1]	DESCRIPTION
		PT	RHA	RHB		
Timer_A	TA0.1	13	11	8	I/O	Timer TA0 CCR1 capture: CCI1A input, compare: Out1 outputs
	TA0.2	14	12	9	I/O	Timer TA0 CCR2 capture: CCI2A input, compare: Out2 outputs
	TA0CLK	12	10	7	I	Timer clock input TACLK for TA0
	TA1.1	5	5	4	I/O	Timer TA1 CCR1 capture: CCI1A input, compare: Out1 outputs
	TA1.2	4	4	3	I/O	Timer TA1 CCR2 capture: CCI2A input, compare: Out2 outputs
	TA1CLK	6	6	5	I	Timer clock input TACLK for TA1
	TA2.0[5]	25	19	14	I/O	Timer TA2 CCR0 capture: CCI0A input, compare: Out0 outputs
	TA2.1[5]	24	18	13	I/O	Timer TA2 CCR1 capture: CCI1A input, compare: Out1 outputs
	TA2.2[5]	23	17	12	I/O	Timer TA2 CCR2 capture: CCI2A input, compare: Out2 outputs
	TA2CLK[5]	26	20	15	I	Timer clock input TACLK for TA2
	TA2.0[6]	20	–	–	I/O	Timer TA2 CCR0 capture: CCI0A input, compare: Out0 outputs
	TA2.1[6]	21	–	–	I/O	Timer TA2 CCR1 capture: CCI1A input, compare: Out1 outputs
	TA2.2[6]	22	–	–	I/O	Timer TA2 CCR2 capture: CCI2A input, compare: Out2 outputs
	TA2CLK[6]	19	–	–	I	Timer clock input TACLK for TA2
	TA3.0[5]	34	28	23	I/O	Timer TA3 CCR0 capture: CCI0A input, compare: Out0 outputs
	TA3.1[5]	33	27	22	I/O	Timer TA3 CCR1 capture: CCI1A input, compare: Out1 outputs
	TA3.2[5]	32	26	21	I/O	Timer TA3 CCR2 capture: CCI2A input, compare: Out2 outputs
	TA3CLK[5]	35	29	24	I	Timer clock input TACLK for TA3
	TA3.0[6]	10	–	–	I/O	Timer TA3 CCR0 capture: CCI0A input, compare: Out0 outputs
	TA3.1[6]	18	16	–	I/O	Timer TA3 CCR1 capture: CCI1A input, compare: Out1 outputs
	TA3.2[6]	17	15	–	I/O	Timer TA3 CCR2 capture: CCI2A input, compare: Out2 outputs
	TA3CLK[6]	11	–	–	I	Timer clock input TACLK for TA3
Timer_B	TB0.0	41	–	–	I/O	Timer TB0 CCR0 capture: CCI0A input, compare: Out0 outputs
	TB0.1	42	34	–	I/O	Timer TB0 CCR1 capture: CCI1A input, compare: Out1 outputs
	TB0.2	43	35	–	I/O	Timer TB0 CCR2 capture: CCI2A input, compare: Out2 outputs
	TB0.3	44	36	–	I/O	Timer TB0 CCR3 capture: CCI3A input, compare: Out3 outputs
	TB0.4	45	37	–	I/O	Timer TB0 CCR4 capture: CCI4A input, compare: Out4 outputs
	TB0.5	8	8	–	I/O	Timer TB0 CCR5 capture: CCI5A input, compare: Out5 outputs
	TB0.6	9	9	–	I/O	Timer TB0 CCR6 capture: CCI6A input, compare: Out6 outputs
	TB0CLK	40	–	–	I	Timer clock input TBCLK for TB0
	TB0TRG	37	31	26		Timer TB0 external trigger input for TB0OUTH
UART	UCA0RXD	5	5	4	I	eUSCI_A0 UART receive data
	UCA0TXD	4	4	3	O	eUSCI_A0 UART transmit data
	UCA0RXD[3]	44	36	–	I	eUSCI_A0 UART receive data
	UCA0TXD[3]	45	37	–	O	eUSCI_A0 UART transmit data
	UCA1RXD[4]	29	23	18	I	eUSCI_A1 UART receive data
	UCA1TXD[4]	30	24	19	O	eUSCI_A1 UART transmit data
DNC	Do not connect	31	25	20	–	Do not connect
VQFN pad	VQFN thermal pad	–	PAD	PAD	–	VQFN package exposed thermal pad. TI recommends connecting to V_{SS}

(1) Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power
(2) Because this pin is multiplexed with the JTAG function, TI recommends disabling the pin interrupt function while in JTAG debug to prevent collisions.

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(3) This is the default functionality that can be remapped by the USCIBxRMP or USCIA0RMP bit of the SYSCFG2 or SYCFG3 register. Only one selected port is valid at any time.
(4) This is the remapped functionality controlled by the USCIBxRMP or USCIA0RMP bit of the SYSCFG2 or SYCFG3 register. Only one selected port is valid at any time.
(5) This is the default functionality that can be remapped by the TAxRMP bit of the SYSCFG3 register. Only one selected port is valid at any time.
(6) This is the remapped functionality controlled by the TAxRMP bit of the SYSCFG3 register. Only one selected port is valid at any time.

7.4 Pin Multiplexing

Pin multiplexing for this MCU is controlled by both register settings and operating modes (for example, if the MCU is in test mode). For details of the settings for each pin and diagrams of the multiplexed ports, see Section 9.11.

7.5 Buffer Types

Table 7-3 defines the pin buffer types that are listed in Table 7-1

Table 7-3. Buffer Types

BUFFER TYPE (STANDARD)	NOMINAL VOLTAGE	HYSTERESIS	PU OR PD	NOMINAL PU OR PD STRENGTH (µA)	OUTPUT DRIVE STRENGTH (mA)	OTHER CHARACTERISTICS
LVCMOS	3.0 V	Y(1)	Programmable	See Section 8.12.4	See Section 8.12.4	
Analog	3.0 V	N	N/A	N/A	N/A	See analog modules in Section 8 for details.
Power (DVCC)	3.0 V	N	N/A	N/A	N/A	SVS enables hysteresis on DVCC.
Power (AVCC)	3.0 V	N	N/A	N/A	N/A	

(1) Only for input pins.

7.6 Connection of Unused Pins

Table 7-4 lists the correct termination of unused pins.

Table 7-4. Connection of Unused Pins

PIN(1)	POTENTIAL	COMMENT
Px.0 to Px.7	Open	Switched to port function, output direction (PxDIR.n = 1)
$\overline{\text{RST}}$/NMI	DV_{CC}	47-kΩ pullup or internal pullup selected with 10-nF (or 1.1-nF) pulldown(2)
TEST	Open	This pin always has an internal pulldown enabled.

(1) Any unused pin with a secondary function that is shared with general-purpose I/O should follow the Px.0 to Px.7 unused pin connection guidelines.
(2) The pulldown capacitor should not exceed 1.1 nF when using MCUs with Spy-Bi-Wire interface in Spy-Bi-Wire mode with TI tools like FET interfaces or GANG programmers.

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Voltage applied at DVCC pin to V_{SS}	–0.3	4.1	V
Voltage applied to any other pin(2)	–0.3	V_{CC} + 0.3 (4.1 V Max)	V
Diode current at any device pin		±2	mA
Junction temperature, T_J		115	°C
Storage temperature, T_{stg} (3)	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

8.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage applied at DVCC pin(1) (3) (2)		1.8(4)		3.6	V
V_{SS}	Supply voltage applied at DVSS pin			0		V
T_A	Operating free-air temperature		–40		105	°C
T_J	Operating junction temperature		–40		115	°C
C_{DVCC}	Recommended capacitor at DVCC(5)		4.7	10		µF
f_{SYSTEM}	Processor frequency (MCLK frequency)(4) (6)	No FRAM wait states (NWAITSx = 0)	0		8	MHz
		With FRAM wait states (NWAITSx = 1)(7)	0		16(8)	
f_{ACLK}	ACLK frequency				40	kHz
f_{SMCLK}	SMCLK frequency				16(8)	MHz

(1) Supply voltage changes faster than 0.2 V/µs can trigger a BOR reset even within the recommended supply voltage range. Following the data sheet recommendation for capacitor C_{DVCC} limits the slopes accordingly.
(2) TI recommends that power to the DVCC pin must not exceed the limits specified in *Recommended Operating Conditions*. Exceeding the specified limits can cause malfunction of the device including erroneous writes to RAM and FRAM.
(3) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
(4) The minimum supply voltage is defined by the SVS levels. Refer to the SVS threshold parameters in Section 8.12.1.1.
(5) A capacitor tolerance of ±20% or better is required. A low-ESR ceramic capacitor of 100 nF (minimum) should be placed as close as possible (within a few millimeters) to the respective pin pair.
(6) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.
(7) Wait states only occur on actual FRAM accesses (that is, on FRAM cache misses). RAM and peripheral accesses are always executed without wait states.
(8) If clock sources such as HF crystals or the DCO with frequencies >16 MHz are used, the clock must be divided in the clock system to comply with this operating condition.

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8.4 Active Mode Supply Current Into V_{CC} Excluding External Current

See (1)

PARAMETER	EXECUTION MEMORY	TEST CONDITION	FREQUENCY ($f_{MCLK} = f_{SMCLK}$)						UNIT
			1 MHz 0 WAIT STATES (NWAITSx = 0)		8 MHz 0 WAIT STATES (NWAITSx = 0)		16 MHz 1 WAIT STATE (NWAITSx = 1)		
			TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM, FRAM}$(0%)	FRAM 0% cache hit ratio	3 V, 25°C	567		3208		3472		µA
		3 V, 85°C	578		3226		3471		
		3 V, 105°C	593		3249		3496	3750	
$I_{AM, FRAM}$(75%)	FRAM 75% cache hit ratio	3 V, 25°C	324		1272		2022		µA
		3 V, 85°C	340		1304		2065		
		3 V, 105°C	354		1321		2085		
$I_{AM, FRAM}$(100%)	FRAM 100% cache hit ratio	3 V, 25°C	241		604		1016		µA
		3 V, 85°C	255		624		1041		
		3 V, 105°C	270		641		1060	1150	
$I_{AM, RAM}$ (2)	RAM	3 V, 25°C	268		821		1446		µA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current. Characterized with program executing typical data processing.
f_{ACLK} = 32768 Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ at specified frequency
Program and data entirely reside in FRAM. All execution is from FRAM.
(2) Program and data reside entirely in RAM. All execution is from RAM. No access to FRAM.

8.5 Active Mode Supply Current Per MHz

V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
$dI_{AM,FRAM}/df$	Active mode current consumption per MHz, execution from FRAM, no wait states	[I_{AM} (75% cache hit rate) at 8 MHz – I_{AM} (75% cache hit rate) at 1 MHz) / 7 MHz	135	µA/MHz

8.6 Low-Power Mode LPM0 Supply Currents Into V_{CC} Excluding External Current

V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)(1) (2)

PARAMETER	V_{CC}	FREQUENCY (f_{SMCLK})						UNIT
		1 MHz		8 MHz		16 MHz		
		TYP	MAX	TYP	MAX	TYP	MAX	
I_{LPM0}	2 V	204		312		437		µA
	3 V	215		325		450		

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Current for watchdog timer clocked by SMCLK included.
f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} at specified frequency.

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8.7 Low-Power Mode (LPM3, LPM4) Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

PARAMETER		V_{CC}	–40°C		25°C		85°C		105°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3,XT1}$	Low-power mode 3, 12.5-pF crystal, includes SVS(2) (3) (4)	3 V	1.2		1.48		7.82		17.12	46	µA
		2 V	1.17		1.46		7.75		16.99		
$I_{LPM3, REFO}$	Low-power mode 3, RTC, excludes SVS(10)	3 V	1.87		2.20		8.53		17.76		µA
		2 V	1.85		2.18		8.47		17.65		
$I_{LPM3,VLO}$	Low-power mode 3, VLO, excludes SVS(5)	3 V	0.92		1.20		7.54		16.83	45.8	µA
		2 V	0.90		1.17		7.47		16.70		
$I_{LPM3, RTC}$	Low-power mode 3, RTC, excludes SVS(9)	3 V	0.99		1.27		7.6		16.9		µA
		2 V	0.97		1.24		7.53		16.77		
$I_{LPM4, SVS}$	Low-power mode 4, includes SVS(6)	3 V	0.65		0.90		7.19		16.41		µA
		2 V	0.64		0.89		7.13		16.30		
I_{LPM4}	Low-power mode 4, excludes SVS(6)	3 V	0.50		0.74		7.02		16.24		µA
		2 V	0.49		0.73		6.96		16.13		
$I_{LPM4,VLO}$	Low-power mode 4, RTC is soured from VLO, excludes SVS(7)	3 V	0.59		0.83		7.12		16.35		µA
		2 V	0.58		0.82		7.06		16.24		
$I_{LPM4,XT1}$	Low-power mode 4, RTC is soured from XT1, excludes SVS(8)	3 V	0.92		1.2		7.54		16.84		µA
		2 V	0.90		1.18		7.47		16.70		

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Not applicable for MCUs with HF crystal oscillator only.
(3) Characterized with a Seiko Crystal SC-32S MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5-pF load.
(4) Low-power mode 3, 12.5-pF crystal, includes SVS test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(5) Low-power mode 3, VLO, excludes SVS test conditions:
Current for watchdog timer clocked by VLO included. RTC disabled. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3)
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz
(6) Low-power mode 4, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4), CPU and all clocks are disabled, WDT and RTC disabled
(7) Low-power mode 4, VLO, excludes SVS test conditions:
Current for RTC clocked by VLO included. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4)
f_{XT1} = 0 Hz, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(8) Low-power mode 4, XT1, excludes SVS test conditions:
Current for RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4)
f_{XT1} = 32768 Hz, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(9) RTC periodically wakes up every second with external 32768-Hz input as source.
(10) RTC periodically wakes up every second with internal REFO 32768-Hz input as source.

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8.8 Low-Power Mode LPMx.5 Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	–40°C		25°C		85°C		105°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3.5, XT1}$	Low-power mode 3.5, 12.5-pF crystal, includes SVS(1) (2) (3) (also see Figure 8-3)	3 V	0.60		0.66		0.96		1.41	2.95	µA
		2 V	0.58		0.65		0.92		1.33		
$I_{LPM4.5, SVS}$	Low-power mode 4.5, includes SVS(4)	3 V	0.24		0.26		0.40		0.61	1.10	µA
		2 V	0.23		0.25		0.37		0.56		
$I_{LPM4.5}$	Low-power mode 4.5, excludes SVS(5)	3 V	0.029		0.041		0.161		0.361	0.80	µA
		2 V	0.027		0.037		0.137		0.31		

(1) Not applicable for MCUs with HF crystal oscillator only.
(2) Characterized with a Seiko Crystal SC-32S MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5-pF load.
(3) Low-power mode 3.5, 12.5-pF crystal, includes SVS test conditions:
Current for RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 32768 Hz, f_{ACLK} = 0, f_{MCLK} = f_{SMCLK} = 0 MHz
(4) Low-power mode 4.5, includes SVS test conditions:
Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5)
f_{XT1} = 0 Hz, f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz
(5) Low-power mode 4.5, excludes SVS test conditions:
Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5)
f_{XT1} = 0 Hz, f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz

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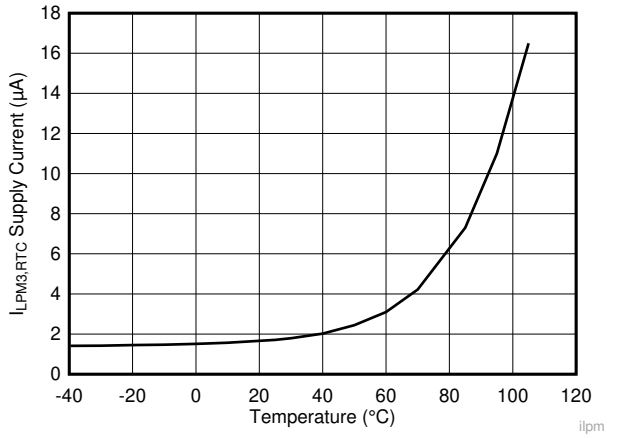
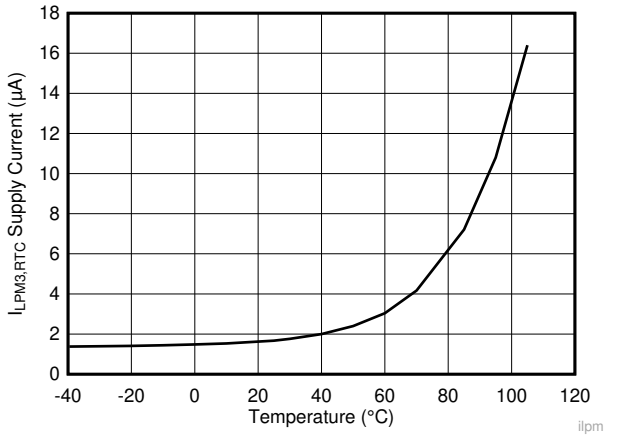
8.9 Typical Characteristics – Low-Power Mode Supply Currents



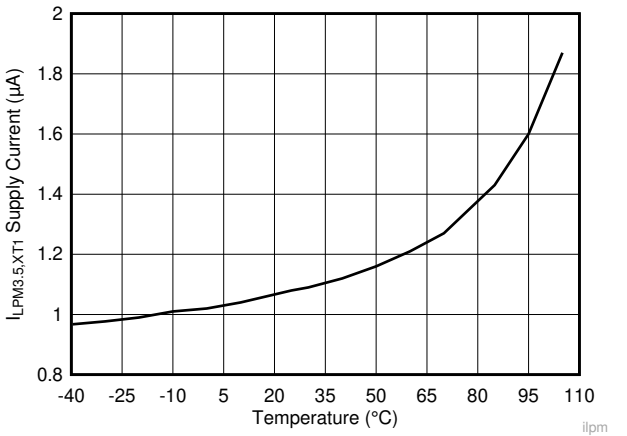
V_{CC} = 3 V RTC enabled SVS disabled

Figure 8-1. LPM3 Supply Current vs Temperature



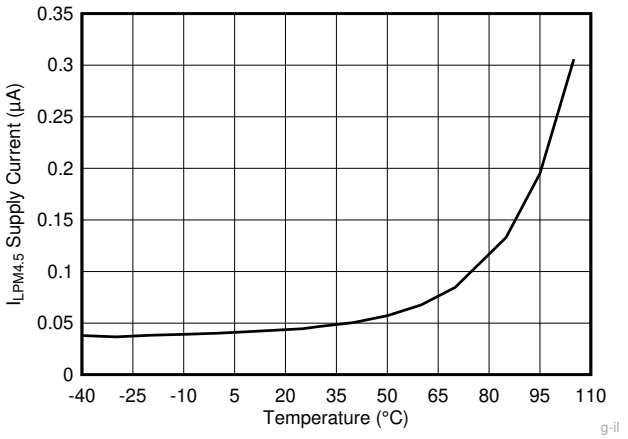
V_{CC} = 2 V RTC enabled SVS disabled

Figure 8-2. LPM3 Supply Current vs Temperature



V_{CC} = 3 V XT1 enabled SVS enabled

Figure 8-3. LPM3.5 Supply Current vs Temperature



V_{CC} = 3 V SVS disabled

Figure 8-4. LPM4.5 Supply Current vs Temperature

8.10 Current Consumption Per Module

MODULE	TEST CONDITIONS	REFERENCE CLOCK	MIN	TYP	MAX	UNIT
Timer_A		Module input clock		5		µA/MHz
eUSCI_A	UART mode	Module input clock		7		µA/MHz
eUSCI_A	SPI mode	Module input clock		5		µA/MHz
eUSCI_B	SPI mode	Module input clock		5		µA/MHz
eUSCI_B	I^2C mode, 100 kbaud	Module input clock		5		µA/MHz
RTC		32 kHz		85		nA
CRC	From start to end of operation	MCLK		8.5		µA/MHz

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8.11 Thermal Resistance Characteristics

THERMAL METRIC[1]			VALUE[2]	UNIT
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air	LQFP 48 pin (PT)	62.4	°C/W
		VQFN 40 pin (RHA)	31.0	
		VQFN 32 pin (RHB)	30.8	
$R\theta_{JC}$	Junction-to-case (top) thermal resistance	LQFP 48 pin (PT)	22.1	°C/W
		VQFN 40 pin (RHA)	22.3	
		VQFN 32 pin (RHB)	20.8	
$R\theta_{JB}$	Junction-to-board thermal resistance	LQFP 48 pin (PT)	26.3	°C/W
		VQFN 40 pin (RHA)	12.3	
		VQFN 32 pin (RHB)	11.6	

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC ($R\theta_{JC}$) value, which is based on a JEDEC-defined 1S0P system) and will change based on environment and application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

8.12 Timing and Switching Characteristics

8.12.1 Power Supply Sequencing

8.12.1.1 PMM, SVS and BOR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BOR, safe}$	Safe BOR power-down level[1]		0.1			V
$t_{BOR, safe}$	Safe BOR reset delay[2]		10			ms
$I_{SVSH,AM}$	SVS_H current consumption, active mode	V_{CC} = 3.6 V			1.5	µA
$I_{SVSH,LPM}$	SVS_H current consumption, low-power modes	V_{CC} = 3.6 V		240		nA
V_{SVSH-}	SVS_H power-down level[4]		1.71	1.80	1.87	V
V_{SVSH+}	SVS_H power-up level[4]		1.76	1.88	1.99	V
V_{SVSH_hys}	SVS_H hysteresis			100		mV
$t_{PD,SVSH, AM}$	SVS_H propagation delay, active mode				10	µs
$t_{PD,SVSH, LPM}$	SVS_H propagation delay, low-power modes				100	µs

(1) A safe BOR can be correctly generated only if DVCC drops below this voltage before it rises.
(2) When an BOR occurs, a safe BOR can be correctly generated only if DVCC is kept low longer than this period before it reaches V_{SVSH+}.
(3) This is a characterized result with external 1-mA load to ground from –40°C to 85°C.
(4) For additional information, see the Dynamic Voltage Scaling Power Solution for MSP430 Devices With Single-Channel LDO Reference Design.

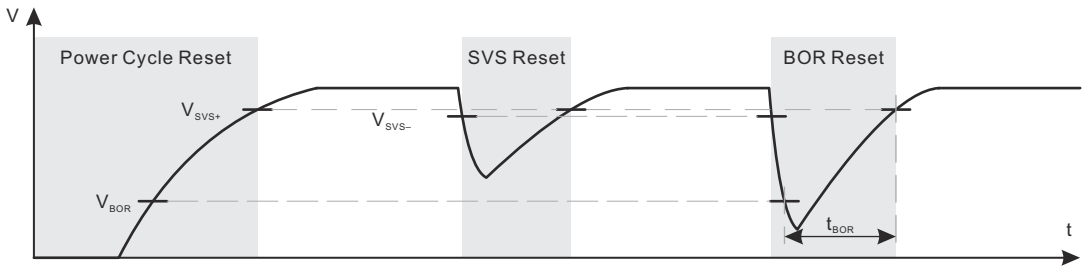

Figure 8-5. Power Cycle, SVS, and BOR Reset Conditions

8.12.2 Reset Timing

8.12.2.1 Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{WAKE-UP\ FRAM}$	Additional wake-up time to activate the FRAM in AM if previously disabled by the FRAM controller or from a LPM if immediate activation is selected for wakeup(1)		3 V		10		µs
$t_{WAKE-UP\ LPM0}$	Wake-up time from LPM0 to active mode (1)		3 V			200 + 2.5 / f_{DCO}	ns
$t_{WAKE-UP\ LPM3}$	Wake-up time from LPM3 to active mode (2)		3 V		10		µs
$t_{WAKE-UP\ LPM4}$	Wake-up time from LPM4 to active mode		3 V		10		µs
$t_{WAKE-UP\ LPM3.5}$	Wake-up time from LPM3.5 to active mode (2)		3 V		350		µs
$t_{WAKE-UP\ LPM4.5}$	Wake-up time from LPM4.5 to active mode (2)	SVSHE = 1	3 V		350		µs
		SVSHE = 0			1		ms
$t_{WAKE-UP-RESET}$	Wake-up time from $\overline{RST}$ or BOR event to active mode (2)		3 V		1		ms
t_{RESET}	Pulse duration required at $\overline{RST}$/NMI pin to accept a reset		3 V	2			µs

(1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) to the first externally observable MCLK clock edge.
(2) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.

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8.12.3 Clock Specifications

8.12.3.1 XT1 Crystal Oscillator (Low Frequency)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{XT1, LF}$	XT1 oscillator crystal, low frequency	LFXTBYPASS = 0			32768		Hz
$DC_{XT1, LF}$	XT1 oscillator LF duty cycle	Measured at MCLK, f_{LFXT} = 32768 Hz		30%		70%	
$f_{XT1,SW}$	XT1 oscillator logic-level square-wave input frequency	LFXTBYPASS = 1 (3) (4)			32.768		kHz
$DC_{XT1, SW}$	LFXT oscillator logic-level square-wave input duty cycle	LFXTBYPASS = 1		40%		60%	
OA_{LFXT}	Oscillation allowance for LF crystals (5)	LFXTBYPASS = 0, LFXTDRIVE = {3}, f_{LFXT} = 32768 Hz, $C_{L,eff}$ = 12.5 pF			200		kΩ
$C_{L,eff}$	Integrated effective load capacitance(6)	See (7)			1		pF
$t_{START,LFXT}$	Start-up time (9)	f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {3}, T_A = 25°C, $C_{L,eff}$ = 12.5 pF			1000		ms
$f_{Fault,LFXT}$	Oscillator fault frequency (10)	XTS = 0(8)		0		3500	Hz

(1) To improve EMI on the LFXT oscillator, observe the following guidelines:
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) See the *MSP430 32-kHz Crystal Oscillators* application note for details on crystal section, layout, and testing.

(3) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger inputs section of this data sheet. Duty cycle requirements are defined by $DC_{LFXT, SW}$.

(4) Maximum frequency of operation of the entire device cannot be exceeded.

(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF
- For LFXTDRIVE = {1}, 6 pF ≤ $C_{L,eff}$ ≤ 9 pF
- For LFXTDRIVE = {2}, 6 pF ≤ $C_{L,eff}$ ≤ 10 pF
- For LFXTDRIVE = {3}, 6 pF ≤ $C_{L,eff}$ ≤ 12 pF

(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).

(7) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 3.7 pF, 6 pF, 9 pF, and 12.5 pF. Maximum shunt capacitance of 1.6 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.

(8) Measured with logic-level input frequency but also applies to operation with crystals.

(9) Includes start-up counter of 1024 clock cycles.

(10) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag. A static condition or stuck at fault condition sets the flag.

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8.12.3.2 DCO FLL, Frequency

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{DCO, FLL}$	FLL lock frequency, 16 MHz, 25°C	Measured at MCLK, Internal trimmed REFO as reference	3 V	–1.0%		1.0%	
	FLL lock frequency, 16 MHz, –40°C to 105°C		3 V	–3.0%		3.0%	
	FLL lock frequency, 16 MHz, –40°C to 105°C	Measured at MCLK, XT1 crystal as reference	3 V	–0.5%		0.5%	
f_{DUTY}	Duty cycle	Measured at MCLK, XT1 crystal as reference	3 V	40%	50%	60%	
$Jitter_{cc}$	Cycle-to-cycle jitter, 16 MHz		3 V		0.25%		
$Jitter_{long}$	Long term jitter, 16 MHz		3 V		0.022%		
$t_{FLL, lock}$	FLL lock time, 16MHz		3 V		200		ms

8.12.3.3 DCO Frequency

over recommended operating free-air temperature (unless otherwise noted) (see Figure 8-6)

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
$f_{DCO, 16MHz}$	DCO frequency, 16 MHz	DCORSEL = 101b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0	3 V	8.5	MHz
		DCORSEL = 101b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511		13.9	
		DCORSEL = 101b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0		20	
		DCORSEL = 101b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511		32.7	
$f_{DCO, 12MHz}$	DCO frequency, 12 MHz	DCORSEL = 100b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0	3 V	6.4	MHz
		DCORSEL = 100b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511		10.5	
		DCORSEL = 100b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0		15.4	
		DCORSEL = 100b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511		24.8	
$f_{DCO, 8MHz}$	DCO frequency, 8 MHz	DCORSEL = 011b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0	3 V	4.3	MHz
		DCORSEL = 011b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511		7.1	
		DCORSEL = 011b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0		10.4	
		DCORSEL = 011b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511		16.9	
$f_{DCO, 4MHz}$	DCO frequency, 4 MHz	DCORSEL = 010b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0	3 V	2.1	MHz
		DCORSEL = 010b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511		3.5	
		DCORSEL = 010b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0		5.2	
		DCORSEL = 010b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511		8.5	

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8.12.3.3 DCO Frequency (continued)

over recommended operating free-air temperature (unless otherwise noted) (see Figure 8-6)

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
$f_{DCO, 2MHz}$	DCO frequency, 2 MHz	DCORSEL = 001b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0	3 V	1.1	MHz
		DCORSEL = 001b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511		1.8	
		DCORSEL = 001b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0		2.6	
		DCORSEL = 001b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511		4.3	
$f_{DCO, 1MHz}$	DCO frequency, 1 MHz	DCORSEL = 000b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0	3 V	0.5	MHz
		DCORSEL = 000b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511		0.9	
		DCORSEL = 000b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0		1.3	
		DCORSEL = 000b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511		2.2	

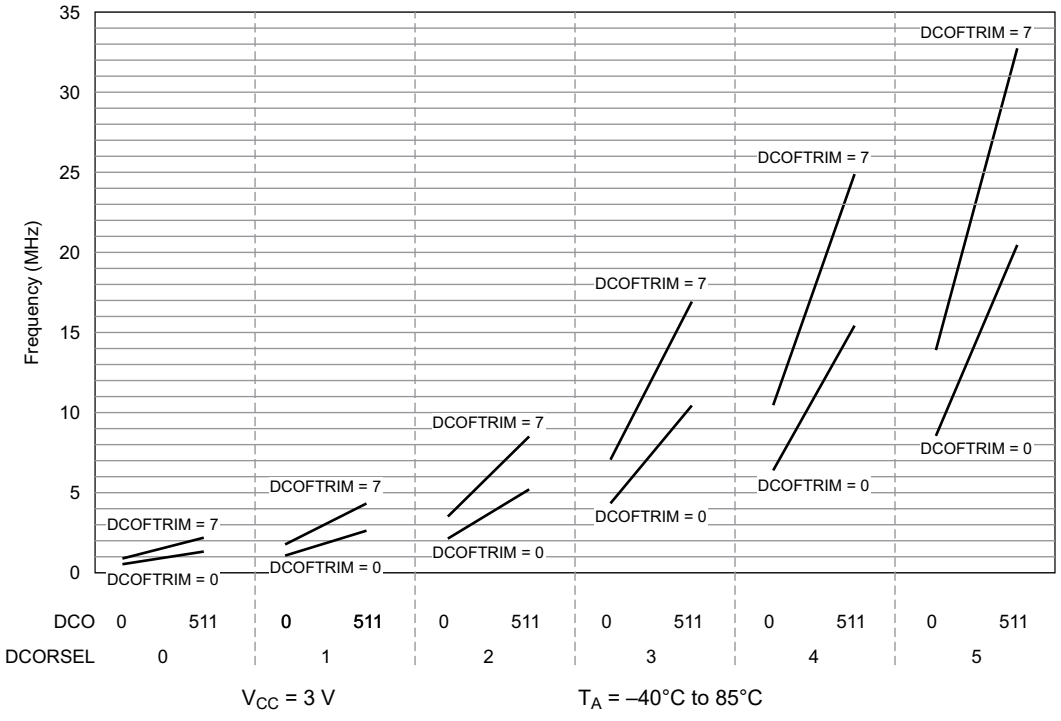

Figure 8-6. Typical DCO Frequency

8.12.3.4 REFO

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REFO}	REFO oscillator current consumption	T_A = 25°C	3 V		1		µA
f_{REFO}	REFO calibrated frequency	Measured at MCLK	3 V		32768		Hz
	REFO absolute calibrated tolerance	–40°C to 105°C	1.8 V to 3.6 V	–3.5%		+3.5%	
df_{REFO}/d_T	REFO frequency temperature drift	Measured at MCLK(1)	3 V		0.01		%/°C
df_{REFO}/d_{VCC}	REFO frequency supply voltage drift	Measured at MCLK at 25°C(2)	1.8 V to 3.6 V		1		%/V
f_{DC}	REFO duty cycle	Measured at MCLK	1.8 V to 3.6 V	40%	50%	60%	
t_{START}	REFO start-up time	40% to 60% duty cycle			50		µs

(1) Calculated using the box method: (MAX(–40°C to 105°C) – MIN(–40°C to 105°C)) / MIN(–40°C to 105°C) / (105°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

8.12.3.5 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
f_{VLO}	VLO frequency	Measured at MCLK	3 V	10	kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at MCLK(1)	3 V	0.5	%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at MCLK(2)	1.8 V to 3.6 V	4	%/V
$f_{VLO,DC}$	Duty cycle	Measured at MCLK	3 V	50%	

(1) Calculated using the box method: (MAX(–40°C to 105°C) – MIN(–40°C to 105°C)) / MIN(–40°C to 105°C) / (105°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Note

The VLO clock frequency is reduced by 15% (typical) when the device switches from active mode to LPM3 or LPM4, because the reference changes. This lower frequency is not a violation of the VLO specifications (see Section 8.12.3.5).

8.12.3.6 Module Oscillator (MODOSC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{MODOSC}	MODOSC frequency		3 V	3.0	3.8	4.6	MHz
f_{MODOSC}/dT	MODOSC frequency temperature drift		3 V		0.102		%/°C
f_{MODOSC}/dV_{CC}	MODOSC frequency supply voltage drift		1.8 V to 3.6 V		1.17		%/V
$f_{MODOSC,DC}$	Duty cycle		3 V	40%	50%	60%	

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8.12.4 Digital I/Os

8.12.4.1 Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		2 V	0.90		1.50	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage		2 V	0.50		1.10	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} – V_{IT-}$)		2 V	0.3		0.8	V
			3 V	0.4		1.2	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
$C_{I,dig}$	Input capacitance, digital only port pins	$V_{IN} = V_{SS}$ or V_{CC}			3		pF
$C_{I,ana}$	Input capacitance, port pins with shared analog functions	$V_{IN} = V_{SS}$ or V_{CC}			5		pF
$I_{lkg(Px.y)}$	High-impedance leakage current of GPIO Pins	See (1) (2)	2 V, 3 V	–20		20	nA
$t_{(int)}$	External interrupt timing (external trigger pulse duration to set interrupt flag)(3)	Ports with interrupt capability (see block diagram and terminal function descriptions)	2 V, 3 V	50			ns

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.
(3) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

8.12.4.2 Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –3 mA(1)	2 V	1.4		2.0	V
		$I_{(OHmax)}$ = –5 mA(1)	3 V	2.4		3.0	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 3 mA(1)	2 V	0.0		0.60	V
		$I_{(OHmax)}$ = 5 mA(1)	3 V	0.0		0.60	
f_{Port_CLK}	Clock output frequency	C_L = 20 pF(2)	2 V	16			MHz
			3 V	16			
$t_{rise,dig}$	Port output rise time, digital only port pins	C_L = 20 pF	2 V		10		ns
			3 V		7		
$t_{fall,dig}$	Port output fall time, digital only port pins	C_L = 20 pF	2 V		10		ns
			3 V		5		

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The port can output frequencies at least up to the specified limit and might support higher frequencies.

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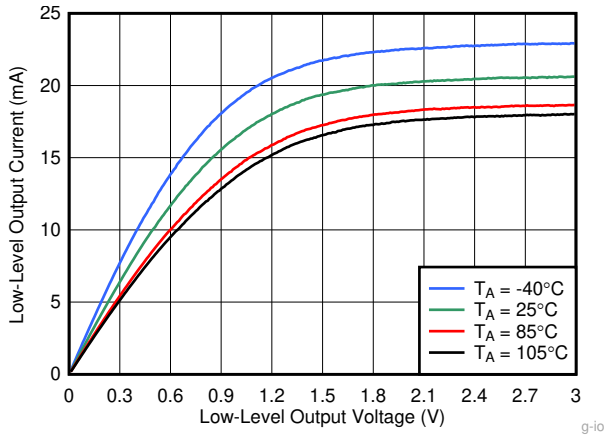
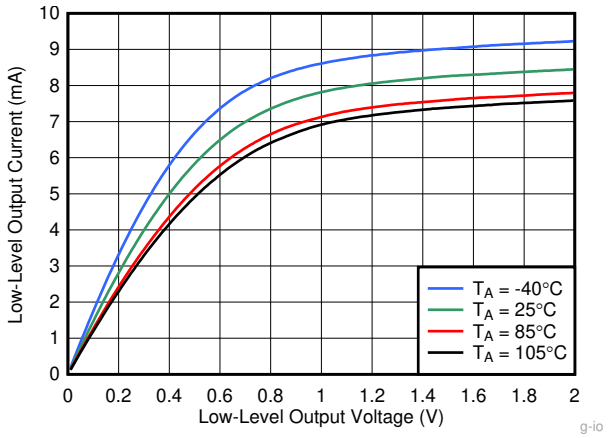
8.12.4.3 Typical Characteristics – Outputs at 3 V and 2 V



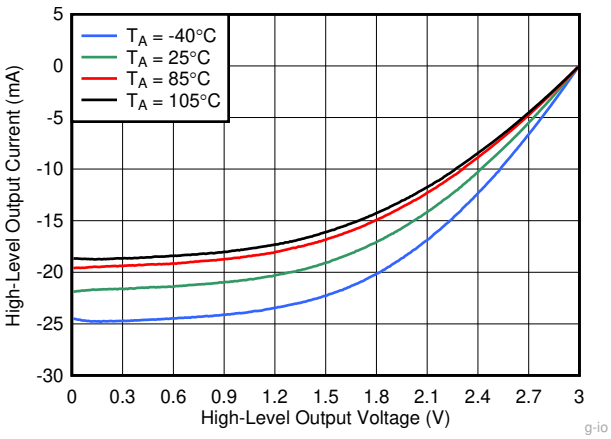
DVCC = 3 V

Figure 8-7. Typical Low-Level Output Current vs Low-Level Output Voltage



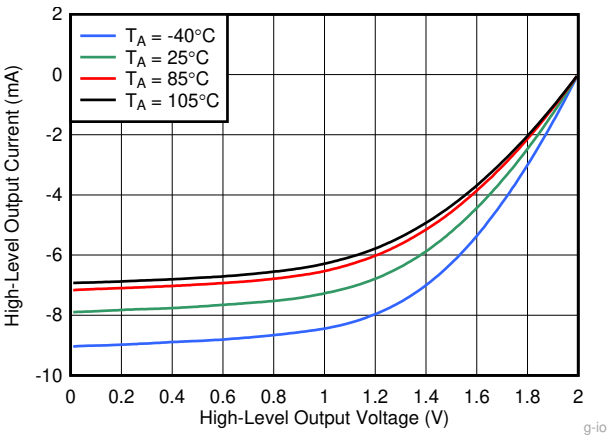
DVCC = 2 V

Figure 8-8. Typical Low-Level Output Current vs Low-Level Output Voltage



DVCC = 3 V

Figure 8-9. Typical High-Level Output Current vs High-Level Output Voltage



DVCC = 2 V

Figure 8-10. Typical High-Level Output Current vs High-Level Output Voltage

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8.12.5 Internal Shared Reference

8.12.5.1 Internal Reference Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{SENSOR}	Temperature sensor voltage	T_J = 30°C	2.0 V, 3.0 V		788		mV
TC_{SENSOR}	Temperature sensor coefficient	T_J = 30°C			2.5		mV/°C
$V_{eCOMP, LP}$	Low-power threshold for eCOMP	T_J = 30°C	2.0 V, 3.0 V		1.20		V
$V_{REF+, 1.2V Output}$	Positive built-in reference output at VREF+ pin with 1-mA load current to ground	EXTREFEN = 1 with 1-mA load current	2.0 V, 3.0 V	1.16	1.20	1.24	V
$TC_{REF+, 1.2V}$	Temperature coefficient of VREF+ = 1.2 V built-in reference	EXTREFEN = 1 with 1-mA load current	3.0 V		30		µV/°C
The following parameters are for the 1.5-V, 2.0-V, and 2.5-V internal reference only and cannot be output to the VREF+ pin.							
$V_{REF+, 1.5V, 2.0V, 2.5V}$	Positive built-in reference voltage as internal reference	REFVSEL = {2} for 2.5 V, INTREFEN = 1	3.0 V		2.5	±1.5%	V
		REFVSEL = {1} for 2.0 V, INTREFEN = 1	2.5 V		2.0	±1.5%	
		REFVSEL = {0} for 1.5 V, INTREFEN = 1	2.0 V		1.5	±1.8%	
Noise	RMS noise at VREF (3)	From 0.1 Hz to 10 Hz, REFVSEL = {0}			30	130	µV
$DV_{CC(min)}$	DVCC minimum voltage, Positive built-in reference active	REFVSEL = {0} for 1.5 V		1.8			V
		REFVSEL = {1} for 2.0 V		2.2			
		REFVSEL = {2} for 2.5 V		2.7			
I_{REF+}	Operating supply current into DVCC terminal(1)	INTREFEN = 1	3 V		19	26	µA
$I_{REF+_ADC_BUF}$	Operating supply current into AVCC terminal(1)	ADC ON, REFVSEL = {0, 1, 2}	3 V		247	400	µA
$I_{O(VREF+)}$	VREF (1.5 V, 2.0 V, 2.5 V) maximum load current, VREF+ terminal	REFVSEL = {0, 1, 2}, AVCC = AVCC(min) for each reference level, INTREFEN = 1	3 V	-1000		+10	µA
ΔVout/ ΔIo (VREF+)	Load-current regulation, VREF+ terminal	REFVSEL = {0, 1, 2}, $I_{O(VREF+)}$ = +10 µA or -1000 µA AVCC = AVCC(min) for each reference level, INTREFEN = 1	3 V			1500	µV/mA
$C_{VREF+/-}$	Capacitance at VREF+ and VREF- terminals	INTREFEN = 1	3 V	0		100	pF
TC_{REF+}	Temperature coefficient of built-in reference	REFVSEL = {0, 1, 2}, INTREFEN = 1, T_A = –40°C to 105°C(4)	3 V		24	50	ppm/K
PSRR_DC	Power supply rejection ratio (DC)	AV_{CC} = $AV_{CC\ (min)}$ to $AV_{CC(max)}$, T_A = 25°C, REFVSEL = {0, 1, 2}, INTREFEN = 1	3 V		100	420	µV/V
PSRR_AC	Power supply rejection ratio (AC)	ΔAV_{CC}= 0.1 V at 1 kHz	3 V		3.0		mV/V
t_{SETTLE}	Settling time of reference voltage(2)	AV_{CC} = $AV_{CC\ (min)}$ to $AV_{CC(max)}$, REFVSEL = {0, 1, 2}, INTREFEN = 0 → 1	3 V		75	100	µs

(1) The internal reference current is supplied through the AVCC terminal.
(2) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.
(3) The internal reference noise affects ADC performance when the ADC uses the internal reference.
(4) Calculated using the box method: (MAX(–40°C to 105°C) – MIN(–40°C to 105°C)) / MIN(–40°C to 105°C) / (105°C – (–40°C))

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8.12.6 Timer_A and Timer_B

8.12.6.1 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK, ACLK External: TACLK Duty cycle = 50% ±10%	2 V, 3 V		16	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, minimum pulse duration required for capture	2 V, 3 V	20		ns

8.12.6.2 Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TB}	Timer_B input clock frequency	Internal: SMCLK, ACLK External: TBCLK Duty cycle = 50% ±10%	2 V, 3 V		16	MHz
$t_{TB,cap}$	Timer_B capture timing	All capture inputs, minimum pulse duration required for capture	2 V, 3 V	20		ns

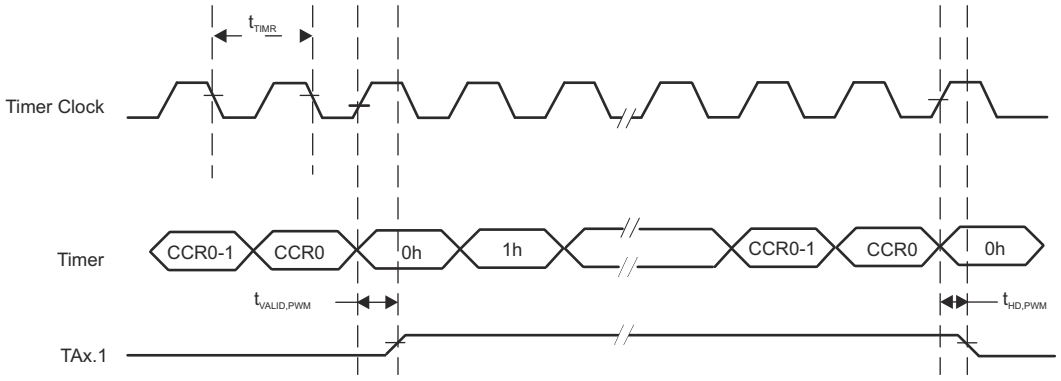

Figure 8-11. Timer PWM Mode

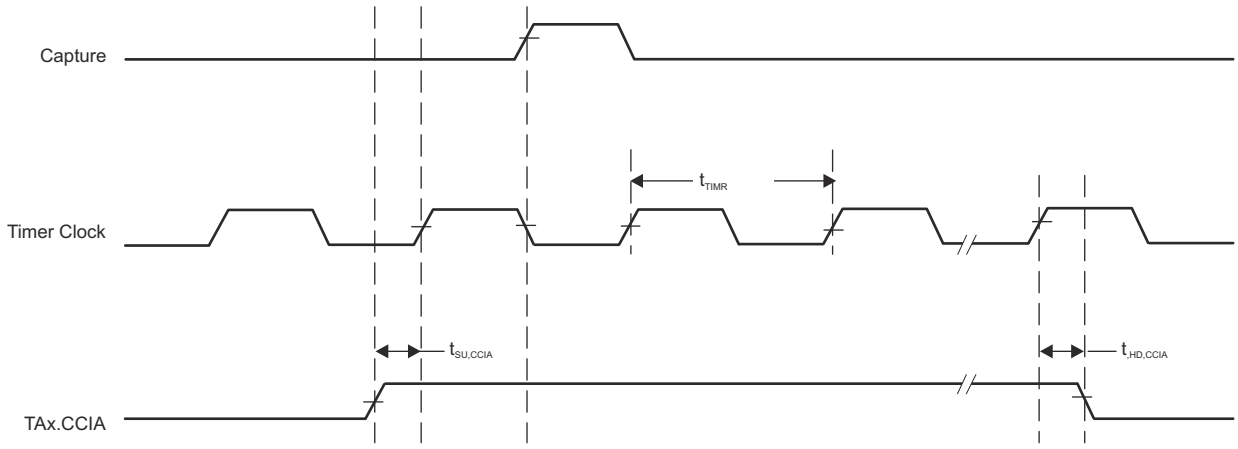

Figure 8-12. Timer Capture Mode

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8.12.7 eUSCI

8.12.7.1 eUSCI (UART Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK, MODCLK External: UCLK Duty cycle = 50% ±10%	2 V, 3 V		16	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in Mbaud)		2 V, 3 V		5	MHz

8.12.7.2 eUSCI (UART Mode) Timing Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
t_t	UART receive deglitch time (1)	UCGLITx = 0	2 V, 3 V	12	ns
		UCGLITx = 1		40	
		UCGLITx = 2		68	
		UCGLITx = 3		110	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

8.12.7.3 eUSCI (SPI Master Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK, MODCLK Duty cycle = 50% ±10%		8	MHz

8.12.7.4 eUSCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock	UCSTEM = 0, UCMODEx = 01 or 10		1		UCxCLK cycles
		UCSTEM = 1, UCMODEx = 01 or 10				
$t_{STE,LAG}$	STE lag time, last clock to STE inactive	UCSTEM = 0, UCMODEx = 01 or 10		1		UCxCLK cycles
		UCSTEM = 1, UCMODEx = 01 or 10				
$t_{SU,MI}$	SOMI input data setup time		2 V	58		ns
			3 V	40		
$t_{HD,MI}$	SOMI input data hold time		2 V	0		ns
			3 V	0		
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF	2 V		20	ns
			3 V		20	
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF	2 V	-3		ns
			3 V	-3		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$.
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 8-13 and Figure 8-14.

(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. Refer to the timing diagrams in Figure 8-13 and Figure 8-14.

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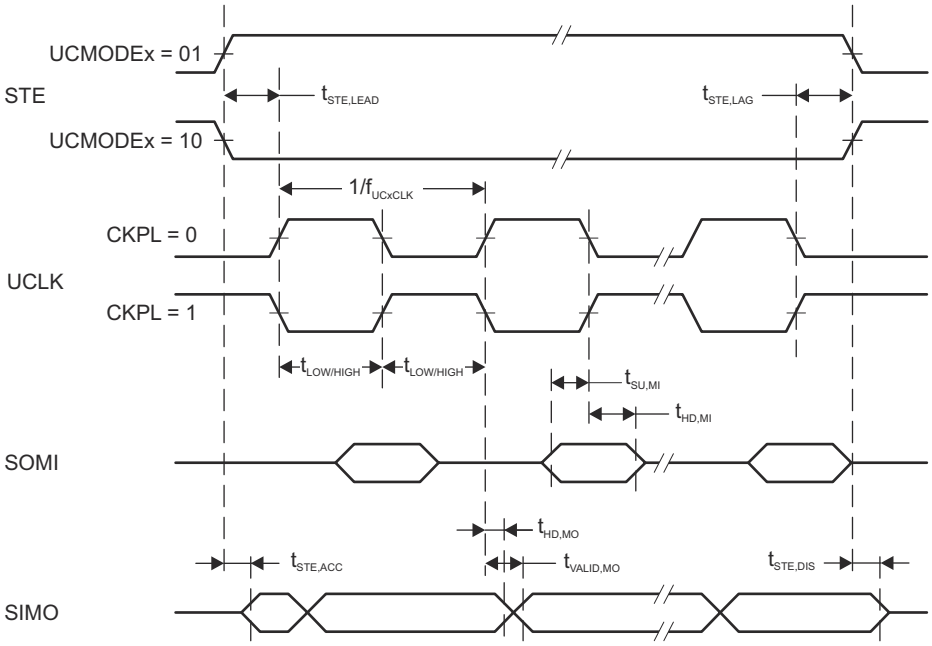

Figure 8-13. SPI Master Mode, CKPH = 0

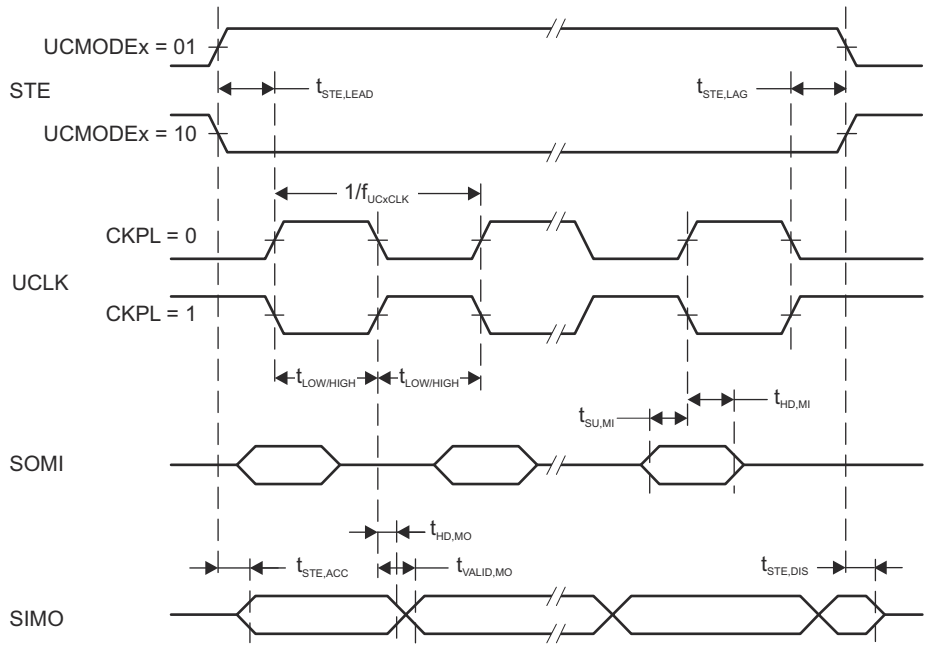

Figure 8-14. SPI Master Mode, CKPH = 1

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8.12.7.5 eUSCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock		2 V	55		ns
			3 V	45		
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive		2 V	20		ns
			3 V	20		
$t_{STE,ACC}$	STE access time, STE active to SOMI data out		2 V		65	ns
			3 V		40	
$t_{STE,DIS}$	STE disable time, STE inactive to SOMI high impedance		2 V		40	ns
			3 V		35	
$t_{SU,SI}$	SIMO input data setup time		2 V	15		ns
			3 V	6		
$t_{HD,SI}$	SIMO input data hold time		2 V	12		ns
			3 V	12		
$t_{VALID,SO}$	SOMI output data valid time[2]	UCLK edge to SOMI valid, C_L = 20 pF	2 V		71	ns
			3 V		42	
$t_{HD,SO}$	SOMI output data hold time [3]	C_L = 20 pF	2 V	5		ns
			3 V	5		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$.
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.

(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 8-15 and Figure 8-16.

(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. Refer to the timing diagrams in Figure 8-15 and Figure 8-16.

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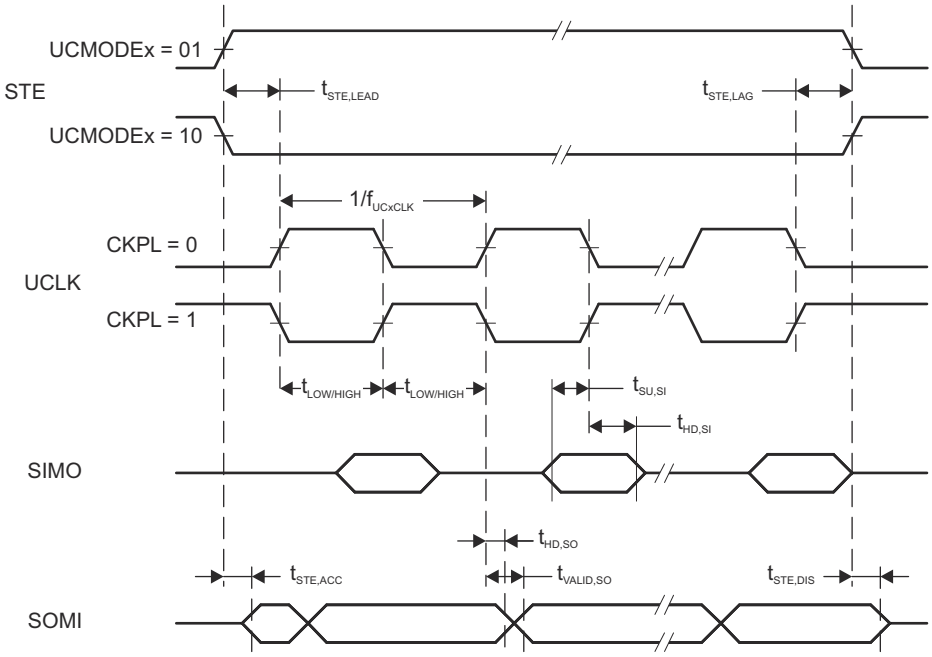

Figure 8-15. SPI Slave Mode, CKPH = 0

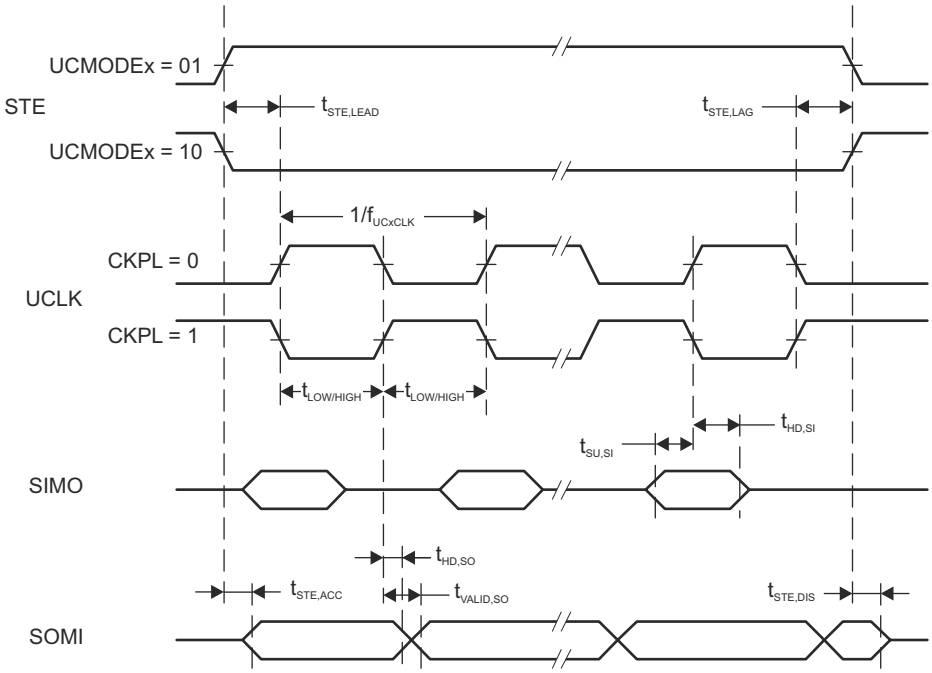

Figure 8-16. SPI Slave Mode, CKPH = 1

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8.12.7.6 eUSCI (I^2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 8-17)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK, MODCLK External: UCLK Duty cycle = 50% ±10%				16	MHz
f_{SCL}	SCL clock frequency		2 V, 3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100 kHz	2 V, 3 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100 kHz	2 V, 3 V	4.7			µs
		f_{SCL} > 100 kHz		0.6			
$t_{HD,DAT}$	Data hold time		2 V, 3 V	0			ns
$t_{SU,DAT}$	Data setup time		2 V, 3 V	250			ns
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100 kHz	2 V, 3 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
t_{SP}	Pulse duration of spikes suppressed by input filter	UCGLITx = 0	2 V, 3 V	50		600	ns
		UCGLITx = 1		25		300	
		UCGLITx = 2		12.5		150	
		UCGLITx = 3		6.3		75	
$t_{TIMEOUT}$	Clock low time-out	UCCLTOx = 1	2 V, 3 V		27		ms
		UCCLTOx = 2			30		
		UCCLTOx = 3			33		

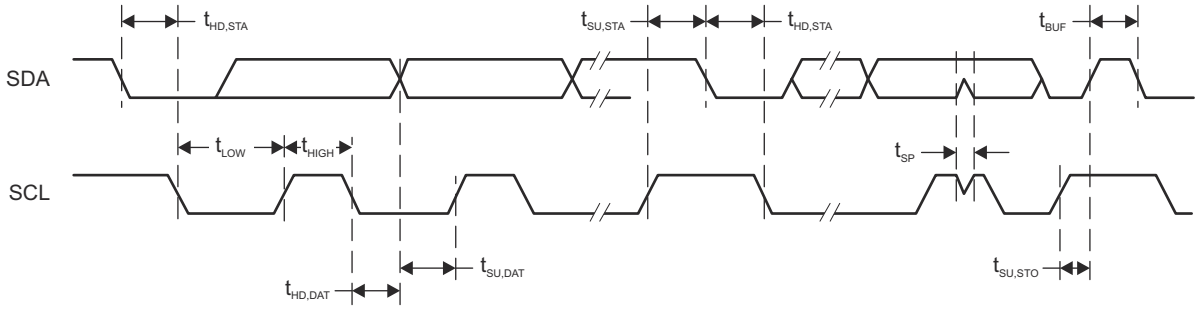

Figure 8-17. I^2C Mode Timing

8.12.8 ADC

8.12.8.1 ADC, Power Supply and Input Range Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
DV_{CC}	ADC supply voltage			2.0		3.6	V
$V_{(Ax)}$	Analog input voltage range	All ADC pins		0		DV_{CC}	V
I_{ADC}	Operating supply current into DVCC terminal, reference current not included, repeat-single-channel mode	f_{ADCCLK} = 5 MHz, ADCON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADCDIV = 0, ADCCONSEQx = 10b	2.0 V		220		µA
			3.0 V		277		
C_I	Input capacitance	Only one terminal Ax can be selected at one time from the pad to the ADC capacitor array, including wiring and pad	2.2 V		4.5	5.5	pF
R_I	Input MUX ON resistance	DV_{CC} = 2 V, 0 V ≤ V_{Ax} ≤ DV_{CC}				2	kΩ

8.12.8.2 ADC, Timing Parameters

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{ADCCLK}		For specified performance of ADC linearity parameters, 10-bit mode	2.4 V to 3.6 V		6		MHz
		For specified performance of ADC linearity parameters, 12-bit mode	2.4 V to 3.6 V		4.4		
$t_{CONVERT}$	Conversion time	External f_{ADCCLK} from ACLK, MCLK, or SMCLK, ADCSSEL ≠ 0	2.4 V to 3.6 V		(2)		µs
t_{ADCON}	Turn-on settling time of the ADC	The error in a conversion started after t_{ADCON} is less than ±0.5 LSB, Reference and input signal already settled				100	ns
t_{Sample}	Sampling time	R_S = 1000 Ω, R_I = 20000 Ω, C_I = 5.5 pF, C_{EXT} = 8 pF, Approximately 7.62 Tau (t) are required for an error of less than ±0.5 LSB, 10-bit mode.(3)	2.4 V to 3.6 V	0.52			µs
		R_S = 1000 Ω, R_I = 40000 Ω, C_I = 5.5 pF, C_{EXT} = 8 pF, Approximately 9.01 Tau (t) are required for an error of less than ±0.5 LSB, 12-bit mode.(3)	2.4 V to 3.6 V	0.61			

(1) $12 \times 1/f_{ADCCLK}$
(2) $(n + 2) \times 1/f_{ADCCLK}$, n = ADC resolution (8, 10, 12)
(3) $t_{Sample} = \ln(2^{n+1}) \times \tau$, where n = ADC resolution, $\tau = (R_I + R_S) \times C_I$

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8.12.8.3 ADC, Linearity Parameters

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error (12-bit mode)	Veref+ reference	2.4 V to 3.6 V	–2.5		2.5	LSB
	Integral linearity error (10-bit mode)	Veref+ reference	2.4 V to 3.6 V	–2		2	
E_D	Differential linearity error (12-bit mode)	Veref+ reference	2.4 V to 3.6 V	–1		1.5	LSB
	Differential linearity error (10-bit mode)	Veref+ reference	2.4 V to 3.6 V	–1		1.5	
E_O	Offset error (12-bit mode)	Veref+ reference, TLV calibration data can be used to improve the parameter(2)	2.4 V to 3.6 V	-4.0		4.0	mV
	Offset error (10-bit mode)	Veref+ reference, TLV calibration data can be used to improve the parameter(2)	2.4 V to 3.6 V	-4.0		4.0	
E_G	Gain error (12-bit mode)	Veref+ as reference, TLV calibration data can be used to improve the parameter(2)	2.4 V to 3.6 V	-9.0		9.0	LSB
	Gain error (10-bit mode)	Veref+ as reference, TLV calibration data can be used to improve the parameter(2)	2.4 V to 3.6 V	-3.0		3.0	LSB
E_T	Total unadjusted error (12-bit mode)	Veref+ as reference, TLV calibration data can be used to improve the parameter(2)	2.4 V to 3.6 V	–5.0		5.0	LSB
	Total unadjusted error (10-bit mode)	Veref+ as reference, TLV calibration data can be used to improve the parameter(2)	2.4 V to 3.6 V	–2.0		2.0	LSB

(1) The typical equivalent impedance of the sensor is 700 kΩ. The sample time required includes the sensor on time, $t_{SENSOR(on)}$.
(2) For details, see the device descriptor in the *MP430FR4xx and MP430FR2xx Family User's Guide*, and see *Designing With the MP430FR4xx and MP430FR2xx ADC* application note for details on optimizing ADC performance for your application with the choice of internal or external reference.

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8.12.9 Enhanced Comparator (eCOMP)

8.12.9.1 eCOMP0 Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.0		3.6	V
V_{IC}	Common mode input range		0		VCC	V
V_{HYS}	DC input hysteresis	CPEN = 1, CPHSEL= 00		0		mV
		CPEN = 1, CPHSEL= 01		10		
		CPEN = 1, CPHSEL= 10		20		
		CPEN = 1, CPHSEL= 11		30		
V_{OFFSET}	Input offset voltage	CPEN = 1, CPMSEL = 0	–30		+30	mV
		CPEN = 1, CPMSEL = 1	–40		+40	
I_{COMP}	Quiescent current draw from V_{CC}, only comparator	V_{IC} = V_{CC}/2, CPEN = 1, CPMSEL = 0		24	35	µA
		V_{IC} = V_{CC}/2, CPEN = 1, CPMSEL = 1		1.6	5	
C_{IN}	Input channel capacitance(1)			1		pF
R_{IN}	Input channel series resistance	On (switch closed)		10	20	kΩ
		Off (switch open)	50			MΩ
t_{PD}	Propagation delay, response time	CPMSEL = 0, CPFLT = 0, Overdrive = 20 mV			1	µs
		CPMSEL = 1, CPFLT = 0, Overdrive = 20 mV		3.2		
t_{EN_CP}	Comparator enable time	CPEN = 0→1, CPMSEL = 0, V+ and V- from pads, Overdrive = 20 mV		10.91		µs
		CPEN = 0→1, CPMSEL = 1, V+ and V- from pads, Overdrive = 20 mV		36.78		
$t_{EN_CP_DAC}$	Comparator with reference DAC enable time	CPEN = 0→1, CPDACEN = 0→1, CPMSEL = 0, CPDACREFS = 1, CPDACBUF1 = 0F, Overdrive = 20 mV		11		µs
		CPEN = 0→1, CPDACEN = 0→1, CPMSEL = 1, Overdrive = 20 mV, CPDACREFS = 1, CPDACBUF1 = 0F		36.82		
t_{FDLY}	Propagation delay with analog filter active	CPMSEL = 0, CPFLTDY = 00, Overdrive = 20 mV, CPFLT = 1		0.7		µs
		CPMSEL = 0, CPFLTDY = 01, Overdrive = 20 mV, CPFLT = 1		1.1		
		CPMSEL = 0, CPFLTDY = 10, Overdrive = 20 mV, CPFLT = 1		1.9		
		CPMSEL = 0, CPFLTDY = 11, Overdrive = 20 mV, CPFLT = 1		3.4		
INL	Integral nonlinearity		–0.5		0.5	LSB
DNL	Differential nonlinearity		–0.5		0.5	LSB

(1) See Figure 8-18 for eCOMP C_{IN} model.

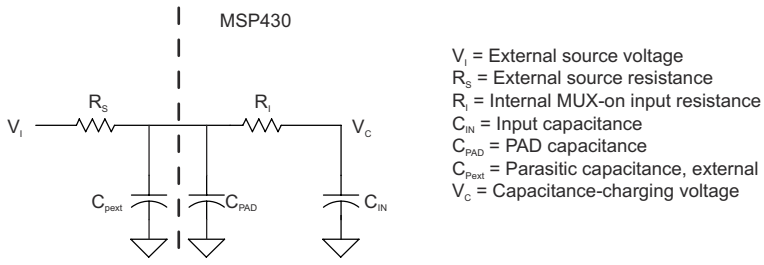

Figure 8-18. eCOMP Input Circuit

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8.12.10 FRAM

8.12.10.1 FRAM Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Read and write endurance		10^{15}			cycles
$t_{Retention}$	Data retention duration	T_J = 25°C	100			years
		T_J = 70°C	40			
		T_J = 95°C	10			
		T_J = 115°C	10			
I_{WRITE}	Current to write into FRAM			I_{READ} (1)		nA
I_{ERASE}	Erase current			N/A(2)		nA
t_{WRITE}	Write time			t_{READ} (3)		ns
t_{READ}	Read time	NWAITSx = 0		1 / f_{SYSTEM} (4)		ns
		NWAITSx = 1		2 / f_{SYSTEM} (4)		

(1) Writing to FRAM does not require a setup sequence or additional power when compared to reading from FRAM. The FRAM read current I_{READ} is included in the active mode current consumption parameter $I_{AM,FRAM}$.
(2) FRAM does not require a special erase sequence.
(3) Writing into FRAM is as fast as reading.
(4) The maximum read (and write) speed is specified by f_{SYSTEM} using the appropriate wait state settings (NWAITSx).

8.12.11 Debug and Emulation

8.12.11.1 JTAG, 4-Wire and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	2.2 V, 3.0 V	0		8	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2.2 V, 3.0 V	0.04		15	µs
$t_{SBW, En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge)(1)	2.2 V, 3.0 V			100	µs
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time		15		100	µs
f_{TCK}	TCK input frequency, 4-wire JTAG(2)	2.2 V	0		10	MHz
		3.0 V	0		10	MHz
$R_{internal}$	Internal pulldown resistance on TEST	2.2 V, 3.0 V	20	35	50	kΩ
f_{TCLK}	TCLK/MCLK frequency during JTAG access, no FRAM access (limited by f_{SYSTEM})				16	MHz
$t_{TCLK,Low/High}$	TCLK low or high clock pulse duration, no FRAM access				25	ns
$f_{TCLK,FRAM}$	TCLK/MCLK frequency during JTAG access, including FRAM access (limited by f_{SYSTEM} with no FRAM wait states)				4	MHz
$t_{TCLK,FRAM,Low/High}$	TCLK low or high clock pulse duration, including FRAM accesses				100	ns

(1) Tools that access the Spy-Bi-Wire and BSL interfaces must wait for the $t_{SBW,En}$ time after the first transition of the TEST/SBWTCK pin (low to high), before the second transition of the pin (high to low) during the entry sequence.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

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9 Detailed Description

9.1 Overview

The MSP430FR247x is an ultra-low-power MCU. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in, for example, portable measurement applications. The MCU features five 16-bit timers, four eUSCIs that support UART, SPI, and I^2C, a hardware multiplier, an RTC module, and a high-performance 12-bit ADC, an enhanced comparator with built in 6-bit DAC for internal voltage reference .

9.2 CPU

The MSP430™ CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter (PC), stack pointer (SP), status register (SR), and constant generator (CG), respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be handled with all instructions.

9.3 Operating Modes

The MSP430 has one active mode and several software-selectable low-power modes of operation (see Table 9-1). An interrupt event can wake the MCU from low-power mode LPM0, LPM3 or LPM4, service the request, and restore the MCU back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

Note

XT1CLK and VLOCLK can be active during LPM4 mode if requested by low-frequency peripherals, such as RTC and WDT.

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Table 9-1. Operating Modes

MODE		AM	LPM0	LPM3	LPM4	LPM3.5	LPM4.5
		ACTIVE MODE (FRAM ON)	CPU OFF	STANDBY	OFF	ONLY RTC	SHUTDOWN
Maximum system clock		16 MHz	16 MHz	40 kHz	0	40 kHz	0
Power consumption at 25°C, 3 V		135 µA/MHz	40 µA/MHz	1.48 µA with RTC counter only in LFXT	0.74 µA without SVS	0.66 µA with RTC counter only in LFXT	41 nA without SVS
Wake-up time		N/A	Instant	10 µs	10 µs	350 µs	350 µs
Wake-up events		N/A	All	All	I/O	RTC or I/O	I/O
Power	Regulator	Full regulation	Full regulation	Partial power down	Partial power down	Partial power down	Power down
	SVS	On	On	Optional	Optional	Optional	Optional
	Brownout	On	On	On	On	On	On
Clock[2]	MCLK	Active	Off	Off	Off	Off	Off
	SMCLK	Optional	Optional	Off	Off	Off	Off
	FLL	Optional	Optional	Off	Off	Off	Off
	DCO	Optional	Optional	Off	Off	Off	Off
	MODCLK	Optional	Optional	Off	Off	Off	Off
	REFO	Optional	Optional	Optional	Off	Off	Off
	ACLK	Optional	Optional	Optional	Off	Off	Off
	XT1CLK	Optional	Optional	Optional	Off	Optional	Off
	VLOCLK	Optional	Optional	Optional	Off	Optional	Off
Core	CPU	On	Off	Off	Off	Off	Off
	FRAM	On	On	Off	Off	Off	Off
	RAM	On	On	On	On	Off	Off
	Backup memory[1]	On	On	On	On	On	Off
Peripherals	Timer0_A3	Optional	Optional	Optional	Off	Off	Off
	Timer1_A3	Optional	Optional	Optional	Off	Off	Off
	Timer2_A3	Optional	Optional	Optional	Off	Off	Off
	Timer3_A3	Optional	Optional	Optional	Off	Off	Off
	Timer0_B7	Optional	Optional	Optional	Off	Off	Off
	WDT	Optional	Optional	Optional	Off	Off	Off
	eUSCI_A0	Optional	Optional	Optional	Off	Off	Off
	eUSCI_A1	Optional	Optional	Optional	Off	Off	Off
	eUSCI_B0	Optional	Optional	Optional	Off	Off	Off
	eUSCI_B1	Optional	Optional	Optional	Off	Off	Off
	CRC	Optional	Optional	Off	Off	Off	Off
	ADC	Optional	Optional	Optional	Off	Off	Off
	RTC	Optional	Optional	Optional	Off	Optional	Off
I/O	GPIO	On	Optional	State held	State held	State held	State held

(1) Backup memory contains 32 bytes of register space in peripheral memory. See Table 9-32 and Table 9-54 for its memory allocation.
(2) The status shown for LPM4 applies to internal clocks only.

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9.4 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see Table 9-2). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 9-2. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power up, Brownout, Supply supervisor External reset $\overline{RST}$ Watchdog time-out, key violation FRAM uncorrectable bit error detection Software POR, BOR FLL unlock error	SVSHIFG PMMRSTIFG WDTIFG PMMPORIFG, PMMBORIFG SYSRSTIV FLLUNLOCKIFG	Reset	FFFEh	63, Highest
System NMI Vacant memory access JTAG mailbox FRAM access time error FRAM bit error detection	VMAIFG JMBINIFG, JMBOUTIFG CBDIFG, UBDIFG	Nonmaskable	FFFCh	62
User NMI External NMI Oscillator fault	NMIIFG OFIFG	Nonmaskable	FFFAh	61
Timer0_A3	TA0CCR0 CCIFG0	Maskable	FFF8h	60
Timer0_A3	TA0CCR1 CCIFG1, TA0CCR2 CCIFG2, TA0IFG (TA0IV)	Maskable	FFF6h	59
Timer1_A3	TA1CCR0 CCIFG0	Maskable	FFF4h	58
Timer1_A3	TA1CCR1 CCIFG1, TA1CCR2 CCIFG2, TA1IFG (TA1IV)	Maskable	FFF2h	57
Time2_A3	TA2CCR0 CCIFG0	Maskable	FFF0h	56
Timer2_A3	TA2CCR1 CCIFG1, TA2CCR2 CCIFG2, TA2IFG (TA2IV)	Maskable	FFEEh	55
Timer3_A3	TA3CCR0 CCIFG0	Maskable	FFECh	54
Timer3_A3	TA3CCR1 CCIFG1, TA3CCR2 CCIFG2, TA3IFG (TA3IV)	Maskable	FFEAh	53
Timer0_B7	TB0CCR0 CCIFG0	Maskable	FFE8h	52
Timer0_B7	TB0CCR1 CCIFG1, TB0CCR2 CCIFG2, TB0CCR3 CCIFG3, TB0CCR4 CCIFG4, TB0CCR5 CCIFG5, TB0CCR6 CCIFG6, TB0IFG (TB0IV)	Maskable	FFE6h	51
RTC	RTCIFG	Maskable	FFE4h	50
Watchdog timer interval mode	WDTIFG	Maskable	FFE2h	49
eUSCI_A0 receive or transmit	UCTXCPTIFG, UCSTTIFG, UCRXIFG, UCTXIFG (UART mode) UCRXIFG, UCTXIFG (SPI mode) (UCA0IV)	Maskable	FFE0h	48
eUSCI_A1 receive or transmit	UCTXCPTIFG, UCSTTIFG, UCRXIFG, UCTXIFG (UART mode) UCRXIFG, UCTXIFG (SPI mode) (UCA0IV)	Maskable	FFDEh	47
eUSCI_B0 receive or transmit	UCB0RXIFG, UCB0TXIFG (SPI mode) UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I^2C mode) (UCB0IV)	Maskable	FFDCh	46

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Table 9-2. Interrupt Sources, Flags, and Vectors (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
eUSCI_B1 receive or transmit	UCB1RXIFG, UCB1TXIFG (SPI mode) UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I^2C mode) (UCB0IV)	Maskable	FFDAh	45
ADC	ADCIFG0, ADCINIFG, ADCLOIFG, ADCHIIFG, ADCTOVIFG, ADCOVIFG (ADCIV)	Maskable	FFD8h	44
P1	P1IFG.0 to P1IFG.7 (P1IV)	Maskable	FFD6h	43
P2	P2IFG.0 to P2IFG.7 (P2IV)	Maskable	FFD4h	42
P3	P3IFG.0 to P2IFG.7 (P3IV)	Maskable	FFD2h	41
P4	P4IFG.0 to P4IFG.7 (P4IV)	Maskable	FFD0h	40
P5	P5IFG.0 to P5IFG.7 (P5IV)	Maskable	FFCEh	39
P6	P6IFG.0 to P6IFG.2 (P6IV)	Maskable	FFCCh	38
eCOMP0	CPIIFG, CPIFG (CP0IV)	Maskable	FFCAh	37, Lowest
Reserved	Reserved	Maskable	FFC6h–FF88h	

Table 9-3. Signatures

SIGNATURE	WORD ADDRESS
BSL I2C Address(1)	0FFA0h
BSL Config	0FF8Ah
BSL Config Signature	0FF88h
BSL Signature2	0FF86h
BSL Signature1	0FF84h
JTAG Signature2	0FF82h
JTAG Signature1	0FF80h

(1) 7-bit address BSL I^2C interface

9.5 Bootloader (BSL)

The BSL lets users program the FRAM or RAM using either the UART serial interface or the I^2C interface. Access to the MCU memory through the BSL is protected by an user-defined password. Use of the BSL requires four pins (see Table 9-4 and Table 9-5). The BSL entry requires a specific entry sequence on the $\overline{\text{RST}}$/NMI/SBWTDIO and TEST/SBWTCK pins. This device can support the blank device detection automatically to invoke the BSL with bypass this special entry sequence for saving time and on board programmable. For the complete description of the feature of the BSL, see the *MSP430™ FRAM Devices Bootloader (BSL) User's Guide*.

Table 9-4. UART BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}$/NMI/SBWTDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P1.4	Data transmit
P1.5	Data receive
VCC	Power supply
VSS	Ground supply

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Table 9-5. I²C BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}$/NMI/SBWTDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P1.2	Data transmit and receive
P1.3	Clock
VCC	Power supply
VSS	Ground supply

9.6 JTAG Standard Interface

The MSP low-power microcontrollers support the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin enables the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. Table 9-6 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For details on using the JTAG interface, see *MSP430 Programming With the JTAG Interface User's Guide*.

Table 9-6. JTAG Pin Requirements and Function

DEVICE SIGNAL	DIRECTION	JTAG FUNCTION
P1.4/.../TCK	IN	JTAG clock input
P1.5/.../TMS	IN	JTAG state control
P1.6/.../TDI/TCLK	IN	JTAG data input, TCLK input
P1.7/.../TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
$\overline{\text{RST}}$/NMI/SBWTDIO	IN	External reset
DVCC	–	Power supply
DVSS	–	Ground supply

9.7 Spy-Bi-Wire Interface (SBW)

The MSP low-power microcontrollers support the 2-wire SBW interface. SBW can be used to interface with MSP development tools and device programmers. Table 9-7 lists the SBW interface pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For details on using the SBW interface, see the *MSP430 Programming With the JTAG Interface User's Guide*.

Table 9-7. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	SBW FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
$\overline{\text{RST}}$/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input and output
DVCC	–	Power supply
DVSS	–	Ground supply

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9.8 FRAM

The FRAM can be programmed using the JTAG port, SBW, the BSL, or in-system by the CPU. Features of the FRAM include:

- Byte and word access capability
- Programmable wait state generation
- Error correction coding (ECC)

9.9 Memory Protection

The device features memory protection for user access authority and write protection, including options to:

- Secure the whole memory map to prevent unauthorized access from JTAG port or BSL, by writing JTAG and BSL signatures using the JTAG port, SBW, the BSL, or in-system by the CPU.
- Enable write protection to prevent unwanted write operation to FRAM contents by setting the control bits in the System Configuration 0 register. For detailed information, see the SYS chapter in the *MP430FR4xx and MP430FR2xx Family User's Guide*.

9.10 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. All peripherals can be handled by using all instructions in the memory map. For complete module description, see the *MP430FR4xx and MP430FR2xx Family User's Guide*.

9.10.1 Power-Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes supply voltage supervisor (SVS) and brownout protection. The brownout reset circuit (BOR) is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a user-selectable safe level. SVS circuitry is available on the primary supply.

The device contains two on-chip reference: 1.5 V for internal reference and 1.2 V for external reference.

The 1.5-V reference is internally connected to ADC channel 13. DVCC is internally connected to ADC channel 15. When DVCC is set as the reference voltage for ADC conversion, the DVCC can be easily represent as Equation 1 by using ADC sampling 1.5-V reference without any external components support.

$$DVCC = (1023 \times 1.5\ V) \div 1.5\text{-V reference ADC result} \quad (1)$$

A 1.2-V reference voltage can be buffered, when EXTREFEN = 1 on PMMCTL2 register, and it can be output to P1.4/../A1/VREF+ , meanwhile the ADC channel 1 can also be selected to monitor this voltage. For more detailed information, see the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

9.10.2 Clock System (CS) and Clock Distribution

The clock system includes a 32-kHz crystal oscillator (XT1), an internal very-low-power low-frequency oscillator (VLO), an integrated 32-kHz RC oscillator (REFO), an integrated internal digitally controlled oscillator (DCO) that may use frequency-locked loop (FLL) locking with internal or external 32-kHz reference clock, and an on-chip asynchronous high-speed clock (MODOSC). The clock system is designed for cost-effective designs with minimal external components. A fail-safe mechanism is included for XT1. The clock system module offers the following clock signals.

- Main Clock (MCLK): The system clock used by the CPU and all relevant peripherals accessed by the bus. All clock sources except MODOSC can be selected as the source with a predivider of 1, 2, 4, 8, 16, 32, 64, or 128.
- Sub-Main Clock (SMCLK): The subsystem clock used by the peripheral modules. SMCLK derives from the MCLK with a predivider of 1, 2, 4, or 8. This means SMCLK is always equal to or less than MCLK.
- Auxiliary Clock (ACLK): This clock is derived from the external XT1 clock, internal VLO or internal REFO clock up to 40 kHz.

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All peripherals may have one or several clock sources depending on specific functionality. Table 9-8 lists the clock distribution used in this device.

Table 9-8. Clock Distribution

	CLOCK SOURCE SELECT BITS	MCLK	SMCLK	ACLK	MODCLK	XT1CLK	VLOCLK	EXTERNAL PIN
Frequency range		DC to 16 MHz	DC to 16 MHz	DC to 40 kHz	5 MHz ±10%	DC to 40 kHz	10 kHz ±50%	–
CPU	N/A	Default	–	–	–	–	–	–
FRAM	N/A	Default	–	–	–	–	–	–
RAM	N/A	Default	–	–	–	–	–	–
CRC	N/A	Default	–	–	–	–	–	–
MPY32	N/A	Default	–	–	–	–	–	–
I/O	N/A	Default	–	–	–	–	–	–
TA0	TASSEL	–	10b	01b	–	–	11b	00b (TA0CLK pin)
TA1	TASSEL	–	10b	01b	–	–	–	00b (TA1CLK pin)
TA2	TASSEL	–	10b	01b	–	–	11b	00b (TA2CLK pin)
TA3	TASSEL	–	10b	01b	–	–	–	00b (TA3CLK pin)
TB0	TBSSEL	–	10b	01b	–	–	–	00b (TB0CLK pin)
eUSCI_A0	UCSSEL	–	10b or 11b	01b	–	–	–	00b (UCA0CLK pin)
eUSCI_A1	UCSSEL	–	10b or 11b	01b	–	–	–	00b (UCA1CLK pin)
eUSCI_B0	UCSSEL	–	10b or 11b	01b	–	–	–	00b (UCB0CLK pin)
eUSCI_B1	UCSSEL	–	10b or 11b	01b	–	–	–	00b (UCB1CLK pin)
WDT	WDTSSEL	–	00b	01b	–	–	10b	–
ADC	ADCSSEL	–	10b or 11b	01b	00b	–	–	–
RTC	RTCSS	–	01b(1)	01b(1)	–	10b	11b	–

(1) Controlled by the RTCCKSEL bit in the SYSCFG2 register.

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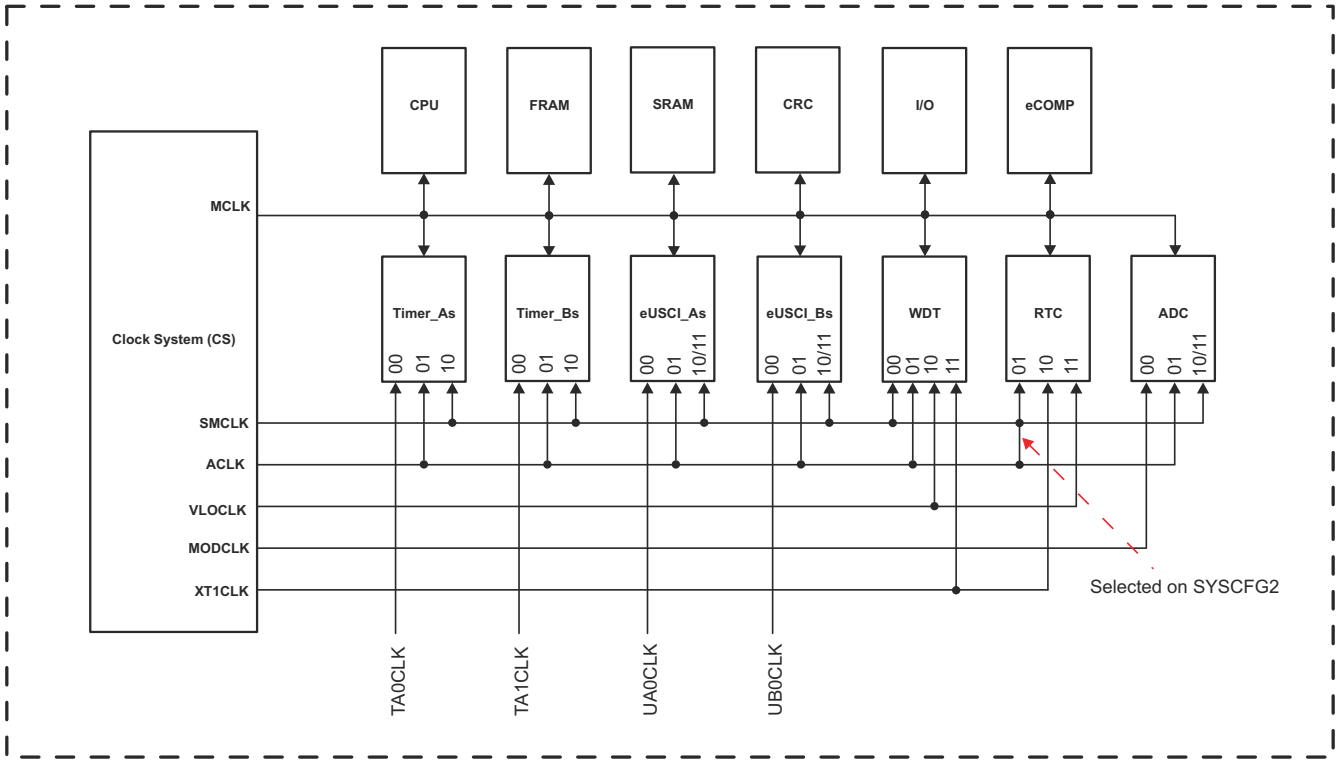

Figure 9-1. Clock Distribution Block Diagram

9.10.3 General-Purpose Input/Output Port (I/O)

Up to 43 I/O ports are implemented.

- P1, P3, P4, and P5 implement 8 bits each. P2 implements 6 bits excluding the I/Os multiplexed with XIN and XOUT. P6 implements 3 bits.
- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPMx.5 wake-up input capability are available for all GPIOs (up to 43)
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise as a pair.

Note

Configuration of digital I/Os after BOR reset

To prevent any cross currents during start-up of the device, all port pins are high-impedance with Schmitt triggers and module functions disabled. To enable the I/O functions after a BOR reset, the ports must be configured first and then the LOCKLPM5 bit must be cleared. For details, see the *Configuration After Reset* section in the Digital I/O chapter of the MP430FR4xx and MP430FR2xx Family User's Guide.

9.10.4 Watchdog Timer (WDT)

The primary function of the WDT module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals. Table 9-9 lists the system clocks that can be used to source the WDT.

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Table 9-9. WDT Clocks

WDTSSEL	NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE)
00	SMCLK
01	ACLK
10	VLOCLK
11	Reserved

9.10.5 System (SYS) Module

The SYS module handles many of the system functions within the device. These features include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors). The SYS module also includes a data exchange mechanism through SBW called a JTAG mailbox mail box that can be used in the application. Table 9-10 summarizes the interrupts that are managed by the SYS module.

Table 9-10. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	015Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		RSTIFG $\overline{\text{RST}}$/NMI (BOR)	04h	
		PMMSWBOR software BOR (BOR)	06h	
		LPMx.5 wakeup (BOR)	08h	
		Security violation (BOR)	0Ah	
		Reserved	0Ch	
		SVSHIFG SVSH event (BOR)	0Eh	
		Reserved	10h	
		Reserved	12h	
		PMMSWPOR software POR (POR)	14h	
		WDTIFG watchdog time-out (PUC)	16h	
		WDTPW password violation (PUC)	18h	
		FRCTLPW password violation (PUC)	1Ah	
		Uncorrectable FRAM bit error detection	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMMPW PMM password violation (PUC)	20h	
		FLL unlock (PUC)	24h	
		Reserved	22h, 26h to 3Eh	Lowest

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Table 9-10. System Module Interrupt Vector Registers (continued)

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSSNIV, System NMI	015Ch	No interrupt pending	00h	
		SVS low-power reset entry	02h	Highest
		Uncorrectable FRAM bit error detection	04h	
		Reserved	06h	
		Reserved	08h	
		Reserved	0Ah	
		Reserved	0Ch	
		Reserved	0Eh	
		Reserved	10h	
		VMAIFG vacant memory access	12h	
		JMBINIFG JTAG mailbox input	14h	
		JMBOUTIFG JTAG mailbox output	16h	
		Correctable FRAM bit error detection	18h	
		Reserved	1Ah to 1Eh	Lowest
SYSUNIV, User NMI	015Ah	No interrupt pending	00h	
		NMIIFG NMI pin or SVS_H event	02h	Highest
		OFIFG oscillator fault	04h	
		Reserved	06h to 1Eh	Lowest

9.10.6 Cyclic Redundancy Check (CRC)

The 16-bit cyclic redundancy check (CRC) module produces a signature based on a sequence of data values and can be used for data checking purposes. The CRC generation polynomial is compliant with CRC-16-CCITT standard of $x^{16} + x^{12} + x^5 + 1$.

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9.10.7 Enhanced Universal Serial Communication Interface (eUSCI_A0, eUSCI_B0)

The eUSCI modules are used for serial data communications. The eUSCI_A module supports either UART or SPI communications. The eUSCI_B module supports either SPI or I^2C communications. Additionally, eUSCI_A supports automatic baud-rate detection and IrDA. The eUSCI_A and eUSCI_B are connected either from P1 port or P2 port, it can be selected from the USCIA0RMP or USCIBxRMP bits of SYSCFG2 and SYSCFG3. Table 9-11 lists the pin configurations that are required for each eUSCI mode.

Table 9-11. eUSCI Pin Configurations

eUSCI_A0	**PIN (PxSEL Selection)**	**UART**	**SPI**
	P1.4(1)	TXD	SIMO
	P1.5(1)	RXD	SOMI
	P1.6(1)	–	SCLK
	P1.7(1)	–	STE
	PIN (PxSEL Selection)	**UART**	**SPI**
	P5.2(2)	TXD	SIMO
	P5.1(2)	RXD	SOMI
	P5.0(2)	–	SCLK
	P4.7(2)	–	STE
eUSCI_A1	**PIN (PxSEL Selection)**	**UART**	**SPI**
	P2.6	TXD	SIMO
	P2.5	RXD	SOMI
	P2.4	–	SCLK
	P3.1	–	STE
eUSCI_B0	**PIN (PxSEL Selection)**	**I^2C**	**SPI**
	P1.0(1)	–	STE
	P1.1(1)	–	SCLK
	P1.2(1)	SDA	SIMO
	P1.3(1)	SCL	SOMI
	PIN (PxSEL Selection)	**I^2C**	**SPI**
	P5.6(2)	–	STE
	P5.5(2)	–	SCLK
	P4.6(2)	SDA	SIMO
	P4.5(2)	SCL	SOMI
eUSCI_B1	**PIN (PxSEL Selection)**	**I^2C**	**SPI**
	P2.7(1)	–	STE
	P3.5(1)	–	SCLK
	P3.2(1)	SDA	SIMO
	P3.6(1)	SCL	SOMI
	PIN (PxSEL Selection)	**I^2C**	**SPI**
	P5.4(2)	–	STE
	P5.3(2)	–	SCLK
	P4.4(2)	SDA	SIMO
	P4.3(2)	SCL	SOMI

(1) This is the default functionality that can be remapped by the USCIBxRMP or USCIA0RMP bit of the SYSCFG2 or SYCFG3 register. Only one selected port is valid at any time.
(2) This is the remapped functionality controlled by the USCIBxRMP or USCIA0RMP bit of the SYSCFG2 or SYCFG3 register. Only one selected port is valid at any time.

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9.10.8 Timers (TA0, TA1, TA2, TA3 and TB0)

The TA0, TA1, TA2 and TA3 modules are 16-bit timers and counters with three capture/compare registers each. Each timer supports multiple captures or compares, PWM outputs, and interval timing (see Table 9-12 and Table 9-13). Each timer has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. The CCR0 registers on both TA0 and TA2 are not externally connected and can only be used for hardware period timing and interrupt generation. In Up mode, they can be used to set the overflow value of the counter.

Table 9-12. Timer0_A0 Signal Connections

PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
P1.0	TA0CLK	TACLK	Timer	N/A	
	ACLK (internal)	ACLK			
	SMCLK (internal)	SMCLK			
	VLO (internal)	INCLK			
	ACLK (internal)	CCI0A	CCR0	TA0	Not used
	VLO (internal)	CCI0B			Timer1_A1 CCI0B input
	DVSS	GND			
	DVCC	V_{CC}			
P1.1	TA0.1	CCI1A	CCR1	TA1	TA0.1
	RTC (internal)	CCI1B			Timer1_A1 CCI1B input
	DVSS	GND			
	DVCC	V_{CC}			
P1.2	TA0.2	CCI2A	CCR2	TA2	TA0.2
	N/A	CCI2B			Timer1_A1 INCLK Timer1_A1 CCI2B input, IR carrier input
	DVSS	GND			
	DVCC	V_{CC}			

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Table 9-13. Timer0_A1 Signal Connections

PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
P1.6	TA1CLK	TACLK	Timer	N/A	
	ACLK (internal)	ACLK			
	SMCLK (internal)	SMCLK			
	Timer0_A3 CCR2B output (internal)	INCLK			
	N/A	CCI0A	CCR0	TA0	Not used
	Timer0_A3 CCR0B output (internal)	CCI0B			Not used
	DVSS	GND			
	DVCC	V_{CC}			
P1.5	TA1.1	CCI1A	CCR1	TA1	TA1.1
	Timer0_A3 CCR1B output (internal)	CCI1B			To ADC trigger
	DVSS	GND			
	DVCC	V_{CC}			
P1.4	TA1.2	CCI2A	CCR2	TA2	TA1.2
	Timer0_A3 CCR2B output (internal)	CCI2B			IR coding input
	DVSS	GND			
	DVCC	V_{CC}			

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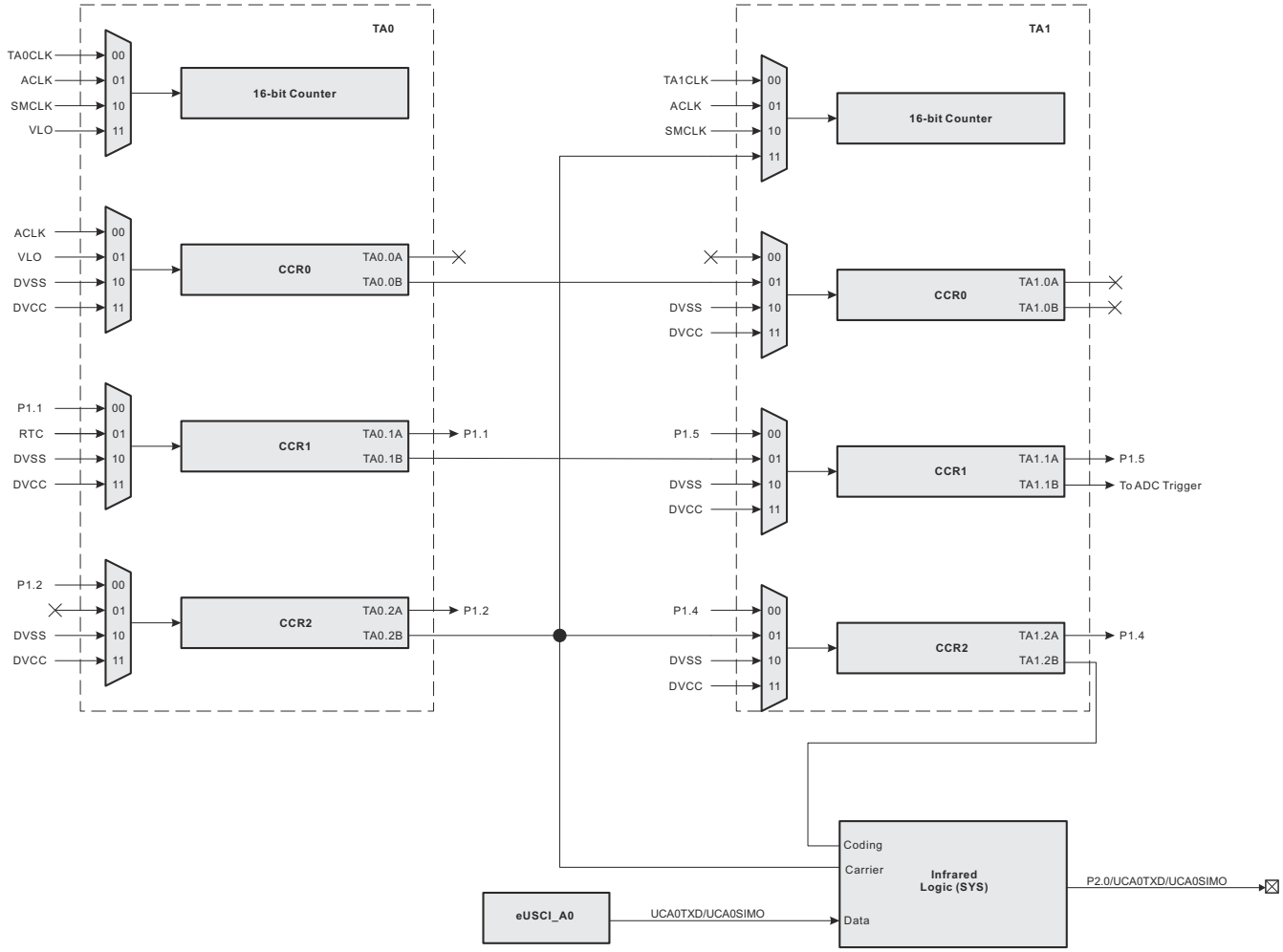

Figure 9-2. TA0 and TA1 Signal Connections

Table 9-14. Timer2_A3 and Timer3_A3 Signal Connections

PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
P3.4	TA2CLK	TACLK	Timer	N/A	
	ACLK (internal)	ACLK			
	SMCLK (internal)	SMCLK			
	VLO (internal)	INCLK			
P2.3	TA2.0	CCI0A	CCR0	TA0	TA2.0
	VLO (internal)	CCI0B			Timer3_A3 CCI0B input
	DVSS	GND			
	DVCC	V_{CC}			
P3.3	TA2.1	CCI1A	CCR1	TA1	TA2.1
	RTC (internal)	CCI1B			Timer3_A3 CCI1B input
	DVSS	GND			
	DVCC	V_{CC}			
P3.0	TA2.2	CCI2A	CCR2	TA2	TA2.2
	N/A	CCI2B			Timer3_A3 CCI2B input
	DVSS	GND			
	DVCC	V_{CC}			
P4.2	TA3CLK	TACLK	Timer	N/A	
	ACLK (internal)	ACLK			
	SMCLK (internal)	SMCLK			
	Timer2_A3 CCR2B output (internal)	INCLK			
P4.1	TA3.0	CCI0A	CCR0	TA0	TA3.0
	Timer2_A3 CCR0B output (internal)	CCI0B			Timer3_B0 CCI0B input
	DVSS	GND			
	DVCC	V_{CC}			
P4.0	TA3.1	CCI1A	CCR1	TA1	TA3.1
	Timer2_A3 CCR1B output (internal)	CCI1B			Timer3_B0 CCI1B input
	DVSS	GND			
	DVCC	V_{CC}			
P3.7	TA3.2	CCI2A	CCR2	TA2	TA3.2
	Timer2_A3 CCR2B output (internal)	CCI2B			Timer3_B0 CCI2B input
	DVSS	GND			
	DVCC	V_{CC}			

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Table 9-15. Timer0_B7 Signal Connections

PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
P6.1	TB0CLK	TBCLK	Timer	N/A	
	ACLK (internal)	ACLK			
	SMCLK (internal)	SMCLK			
	N/A	INCLK			
P6.2	TB0.0	CCI0A	CCR0	TB0	TB0.0
	Timer3_A3 CCI0B input (internal)	CCI0B			
	DVSS	GND			
	DVCC	V_{CC}			
P4.7	TB0.1	CCI1A	CCR1	TB1	TB0.1
	Timer3_A3 CCI1B input (internal)	CCI1B			
	DVSS	GND			
	DVCC	V_{CC}			
P5.0	TB0.2	CCI2A	CCR2	TB2	TB0.2
	Timer3_A3 CCI2B input (internal)	CCI2B			
	DVSS	GND			
	DVCC	V_{CC}			
P5.1	TB0.3	CCI1A	CCR3	TB3	TB0.3
	N/A	CCI1B			
	DVSS	GND			
	DVCC	V_{CC}			
P5.2	TB0.4	CCI1A	CCR4	TB4	TB0.4
	N/A	CCI1B			
	DVSS	GND			
	DVCC	V_{CC}			
P4.3	TB0.5	CCI1A	CCR5	TB5	TB0.5
	N/A	CCI1B			
	DVSS	GND			
	DVCC	V_{CC}			
P4.4	TB0.6	CCI1A	CCR6	TB6	TB0.6
	N/A	CCI1B			
	DVSS	GND			
	DVCC	V_{CC}			

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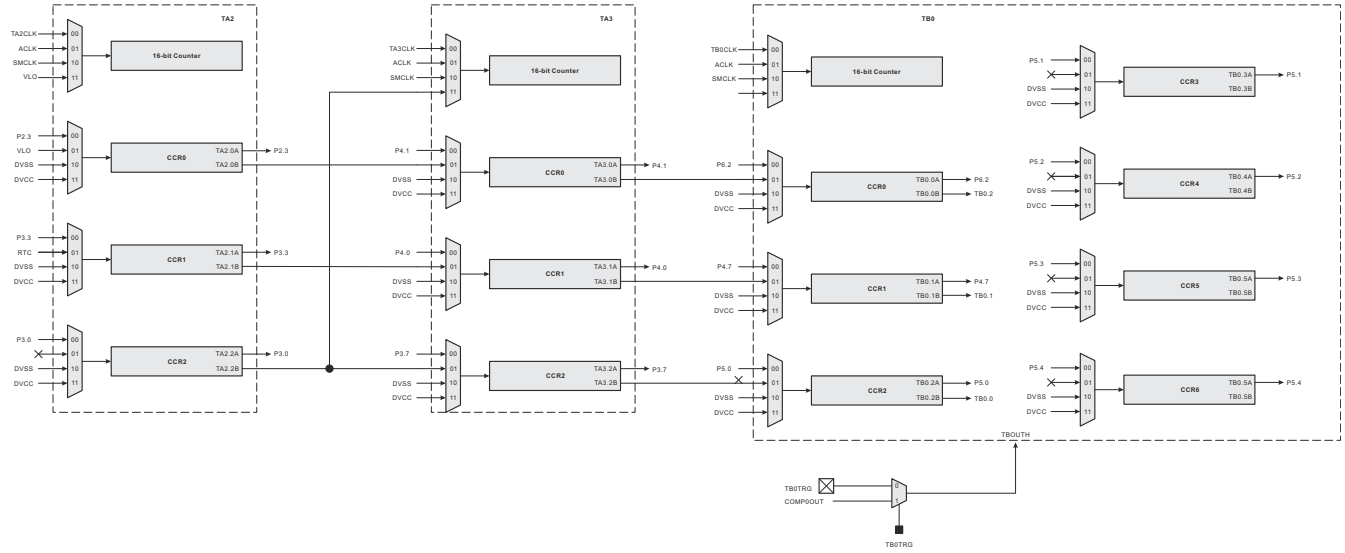

Figure 9-3. TA2, TA3 and TB0 Signal Connections

Table 9-16. TA2 and TA3 Pin Configurations of Remap Functionality

	PIN (PxSEL Selection)	DEVICE INPUT/OUTPUT SIGNAL
TA2	P3.4(1)	TA2CLK
	P2.3(1)	TA2.0
	P3.3(1)	TA2.1
	P3.0(1)	TA2.2
	PIN (PxSEL Selection)	**DEVICE INPUT/OUTPUT SIGNAL**
	P5.5(2)	TA2CLK
	P5.6(2)	TA2.0
	P5.7(2)	TA2.1
	P6.0(2)	TA2.2
TA3	**PIN (PxSEL Selection)**	**DEVICE INPUT/OUTPUT SIGNAL**
	P4.2(1)	TA3CLK
	P4.1(1)	TA3.0
	P4.0(1)	TA3.1
	P3.7(1)	TA3.2
	PIN (PxSEL Selection)	**DEVICE INPUT/OUTPUT SIGNAL**
	P5.4(2)	TA3CLK
	P5.3(2)	TA3.0
	P4.6(2)	TA3.1
	P4.5(2)	TA3.2

(1) This is the default functionality that can be remapped by the TAxRMP bit of the SYSCFG3 register. Only one selected port is valid at any time.
(2) This is the remapped functionality controlled by the TAxRMP bit of the SYSCFG3 register. Only one selected port is valid at any time.

The interconnection of Timer0_A3 and Timer1_A3 can be used to modulate the eUSCI_A pin of UCA0TXD/UCA0SIMO in either ASK or FSK mode, with which a user can easily acquire a modulated infrared command for directly driving an external IR diode. The IR functions are fully controlled by SYS configuration register 1 including IREN (enable), IRPSEL (polarity select), IRMSEL (mode select), IRDSSEL (data select), and IRDATA

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(data) bits. For more information, see the SYS chapter in the *MP430FR4xx and MP430FR2xx Family User's Guide*.

The Timer_B module feature the function to put Timer_B all outputs into a high impedance state when the selected source is triggered. The source can be selected from external pin or internal of the device, it is controlled by TBxTRG in SYS. For more information, see the SYS chapter in the *MP430FR4xx and MP430FR2xx Family User's Guide*.

Table 9-17 lists the Timer_B high-impedance trigger source selections.

Table 9-17. TB0OUTH Selection

TB0TRGSEL	TB0OUTH TRIGGER SOURCE SELECTION	Timer_B PAD OUTPUT HIGH IMPEDANCE
TB0TRGSEL = 0	eCOMP0 output (internal)	P6.2, P4.7, P5.0, P5.1, P5.2, P4.3, P4.4
TB0TRGSEL= 1	P3.5	

9.10.9 Hardware Multiplier (MPY)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The MPY module supports signed multiplication, unsigned multiplication, signed multiply-and-accumulate, and unsigned multiply-and-accumulate operations.

9.10.10 Backup Memory (BAKMEM)

The BAKMEM supports data retention during LPM3.5. This device provides up to 32 bytes that are retained during LPM3.5.

9.10.11 Real-Time Clock (RTC)

The RTC is a 16-bit modulo counter that is functional in AM, LPM0, LPM3, and LPM3.5. This module may periodically wake up the CPU from LPM0, LPM3 and LPM3.5 based on timing from a low-power clock source such as the XT1 and VLO clocks. RTC also can be sourced from ACLK controlled by RTCCKSEL in SYSCFG2. In AM, RTC can be driven by SMCLK to generate high-frequency timing events and interrupts. The RTC overflow events trigger:

- Timer0_B3 CCI1B
- ADC conversion trigger when ADCSHSx bits are set as 01b

Table 9-18. RTC Clock Source

RTCSS	CLOCK SOURCE
00	Reserved
01	SMCLK, or ACLK is selected(1)
10	XT1CLK
11	VLOCLK

(1) Controlled by RTCCLK bit of SYSCFG2 register.

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9.10.12 12-Bit Analog-to-Digital Converter (ADC)

The 12-bit ADC module supports fast 12-bit analog-to-digital conversions with single-ended input. The module implements a 12-bit SAR core, sample select control, reference generator and a conversion result buffer. A window comparator with a lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

The ADC supports 12 external inputs and four internal inputs (see Table 9-19).

Table 9-19. ADC Channel Connections

ADCINCHx	ADC CHANNELS	EXTERNAL PIN OUTPUT
0	A0/Veref+	P1.0
1	A1/	P1.1
2	A2/Veref-	P1.2
3	A3	P1.3
4	A4(1)	P1.4
5	A5	P1.5
6	A6	P1.6
7	A7	P1.7
8	A8	P4.3
9	A9	P4.4
10	A10	P5.3
11	A11	P5.4
12	On-chip temperature sensor	N/A
13	Internal shared reference voltage (1.5, 2.0, or 2.5-V)	N/A
14	DVSS	N/A
15	DVCC	N/A

(1) When A4 is used, the PMM 1.2-V reference voltage can be output to this pin by setting the PMM control register. The 1.2-V voltage can be measured by channel A4.

The analog-to-digital conversion can be started by software or a hardware trigger. Table 9-20 shows the trigger sources that are available.

Table 9-20. ADC Trigger Signal Connections

ADCSHSx		TRIGGER SOURCE
BINARY	DECIMAL	
00	0	ADCSC bit (software trigger)
01	1	RTC event
10	2	TA1.1B
11	3	eCOMP0 COUT

9.10.13 eCOMP0

This device features one enhanced comparator. The enhanced comparator is an analog voltage comparator with a built-in 6-bit DAC as an internal voltage reference. The integrated 6-bit DAC can be set to 64 steps for the comparator reference voltage. This module has 4-level programmable hysteresis and configurable power modes: high-power and low-power modes.

The eCOMP0 supports a propagation delay up to 1 µs in high-power mode. In low-power mode, eCOMP0 supports 3.2-µs delay with 1.5-µA leakage at room temperature, which can be an ideal wake-up source in LPM3 for a voltage monitor.

eCOMP0 contains a programmable 6-bit DAC that can use the internal shared reference (1.5 V, 2.0 V, or 2.5 V) for a high-precision comparison threshold. In addition to the internal shared reference, a low-power 1.2-V

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reference is fixed at channel 2 of both the inverting and noninverting paths and allows the DAC to be turned off to reduce power consumption.

The eCOMP0 supports external inputs and internal inputs (see Table 9-21) and outputs (see Table 9-22)

Table 9-21. eCOMP0 Input Channel Connections

CPPSEL OR CPNSEL	eCOMP0 CHANNELS
000	P1.1/.../COMP0.0
001	P2.2/.../COMP0.1
010	Low-power 1.2-V reference
011	P5.7/.../COMP0.2
100	P6.0/.../COMP0.3
101	N/A
110	eCOMP0 6-bit DAC

Table 9-22. eCOMP0 Output Channel Connections

ECOMP0 OUT	EXTERNAL PINOUT, MODULE
1	P3.4
2	TB0 (TB0OUTH), TB1 (TB1OUTH), ADC trigger

9.10.14 Embedded Emulation Module (EEM)

The EEM supports real-time in-system debugging. The EEM on these devices has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level
- EEM version: S

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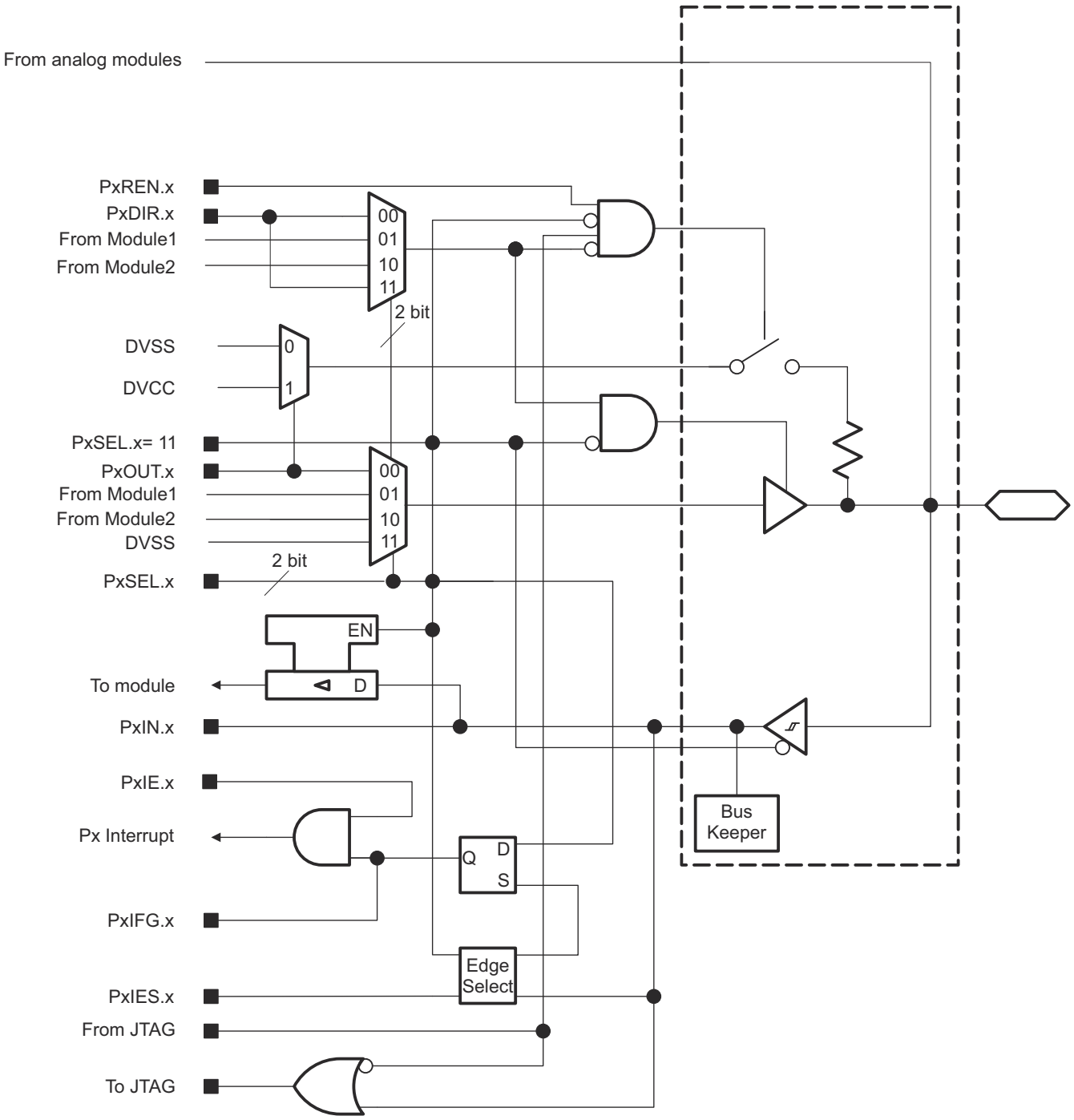
9.11 Input/Output Diagrams

Figure 9-4 shows the overall port diagram.



NOTE: For details on the specific analog modules, digital function modules, interrupts, and JTAG, see the Port Pin Functions table.

Figure 9-4. Port Input/Output With Schmitt Trigger

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9.11.1 Port P1 (P1.0 to P1.7) Input/Output With Schmitt Trigger

Table 9-23 summarizes the selection of the pin functions.

Table 9-23. Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)		
			P1DIR.x	P1SELx	JTAG
P1.0/UCB0STE/TA0CLK/A0/Veref+	0	P1.0 (I/O)	I: 0; O: 1	00	0
		UCB0STE	X	01	0
		TA0CLK	0	10	0
		A0,Veref+	X	11	N/A
P1.1/UCB0CLK/TA0.1/COMP0.0/A1	1	P1.1 (I/O)	I: 0; O: 1	00	0
		UCB0CLK	X	01	0
		TA0.CCI1A	0	10	0
		TA0.1	1		
		A1, COMP0.0	X	11	N/A
P1.2/UCB0SIMO/UCB0SDA/TA0.2/A2/Veref-	2	P1.2 (I/O)	I: 0; O: 1	00	0
		UCB0SIMO/UCB0SDA	X	01	0
		TA0.CCI2A	0	10	0
		TA0.2	1		
		A2, Veref-	X	11	N/A
P1.3/UCB0SOMI/UCB0SCL/MCLK/A3	3	P1.3 (I/O)	I: 0; O: 1	00	0
		UCB0SOMI/UCB0SCL	X	01	0
		MCLK	1	10	0
		A3	X	11	N/A
P1.4/UCA0TXD/UCA0SIMO/TA1.2/TCK/A4/VREF+	4	P1.4 (I/O)	I: 0; O: 1	00	Disabled
		UCA0TXD/UCA0SIMO	X	01	Disabled
		TA1.CCI2A	0	10	Disabled
		TA1.2	1		
		A4, VREF+	X	11	Disabled
		JTAG TCK	X	X	TCK
P1.5/UCA0RXD/UCA0SOMI/TA1.1/TMS/A5	5	P1.5 (I/O)	I: 0; O: 1	00	Disabled
		UCA0RXD/UCA0SOMI	X	01	Disabled
		TA1.CCI1A	0	10	Disabled
		TA1.1	1		
		A5	X	11	Disabled
		JTAG TMS	X	X	TMS
P1.6/UCA0CLK/TA1CLK/TDI/TCLK/A6	6	P1.6 (I/O)	I: 0; O: 1	00	Disabled
		UCA0CLK	X	01	Disabled
		TA1CLK	0	10	Disabled
		A6	X	11	Disabled
		JTAG TDI/TCLK	X	X	TDI/TCLK
P1.7/UCA0STE/SMCLK/TDO/A7	7	P1.7 (I/O)	I: 0; O: 1	00	Disabled
		UCA0STE	X	01	Disabled
		SMCLK	1	10	Disabled
		A7	X	11	Disabled
		JTAG TDO	X	X	TDO

(1) X = don't care

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9.11.2 Port P2 (P2.0 to P2.7) Input/Output With Schmitt Trigger

Table 9-24 summarizes the selection of the pin functions.

Table 9-24. Port P2 (P2.0 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)	
			P2DIR.x	P2SELx
P2.0/XOUT	0	P2.0 (I/O)	I: 0; O: 1	00
		XOUT	X	01
P2.1/XIN	1	P2.1 (I/O)	I: 0; O: 1	00
		XIN	X	01
P2.2/ACLK/COMP0.1	2	P2.2 (I/O)	I: 0; O: 1	00
		ACLK	1	10
		COMP0.1	X	11
P2.3/TA2.0	3	P2.3 (I/O)	I: 0; O: 1	00
		TA2.CCI0A	0	01
		TA2.0	1	
P2.4/UCA1CLK	4	P2.4 (I/O)	I: 0; O: 1	00
		UCA1CLK	X	01
P2.5/UCA1RXD/UCA1SOMI	5	P2.5 (I/O)	I: 0; O: 1	00
		UCA1RXD/UCA1SOMI	X	01
P2.6/UCA1TXD/UCA1SIMO	6	P2.6 (I/O)	I: 0; O: 1	00
		UCA1TXD/UCA1SIMO	X	01
P2.7/UCB1STE	7	P2.7 (I/O)	I: 0; O: 1	0
		UCB1STE	X	01

(1) X = don't care

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9.11.3 Port P3 (P3.0 to P3.7) Input/Output With Schmitt Trigger

Table 9-25 summarizes the selection of the pin functions.

Table 9-25. Port P3 (P3.0 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)	
			P3DIR.x	P3SEL.x
P3.0/TA2.2	0	filter9	I: 0; O: 1	00
		TA2.CCI2A	0	01
		TA2.2	1	
P3.1/UCA1STE	1	P3.1 (I/O)	I: 0; O: 1	00
		UCA1STE	X	01
P3.2/UCB1SIMO/UCB1SDA	2	P3.2 (I/O)	I: 0; O: 1	00
		UCB1SIMO/UCB1SDA	X	01
P3.3/TA2.1	3	P3.3 (I/O)	I: 0; O: 1	00
		TA2.CCI1A	0	01
		TA2.1	1	
P3.4/TA2CLK/COMP0OUT	4	P3.4 (I/O)	I: 0; O: 1	00
		TA2CLK	0	01
		COMP0OUT	1	10
P3.5/UCB1CLK/TB0TRG	5	P3.5 (I/O)	I: 0; O: 1	00
		UCB1CLK	X	01
		TB0TRG	0	10
P3.6/UCB1SOMI/UCB1SCL	6	P3.6 (I/O)	I: 0; O: 1	00
		UCB1SOMI/UCB1SCL	X	01
P3.7/TA3.2	7	P3.7 (I/O)	I: 0; O: 1	00
		TA3.CCI2A	0	01
		TA3.2	1	

(1) X = don't care

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9.11.4 Port P4 (P4.0 to P4.7) Input/Output With Schmitt Trigger

Table 9-26 summarizes the selection of the pin functions.

Table 9-26. Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)	
			P4DIR.x	P4SEL.x
P4.0/TA3.1	0	P4.0 (I/O)	I: 0; O: 1	00
		TA3.CCI1A	0	01
		TA3.1	1	
P4.1/TA3.0	1	P4.1 (I/O)	I: 0; O: 1	00
		TA3.CCI0A	0	01
		TA3.0	1	
P4.2/TA3CLK	2	P4.2 (I/O)	I: 0; O: 1	00
		TA3CLK	0	01
P4.3/UCB1SOMI/UCB1SCL/TB0.5/A8	3	P4.3 (I/O)	I: 0; O: 1	00
		UCB1SOMI/UCB1SCL	X	01
		TB0.CCI5A	0	10
		TB0.5	1	
		A8	X	11
P4.4/UCB1SIMO/UCB1SDA/TB0.6/A9	4	P3.4 (I/O)	I: 0; O: 1	00
		UCB1SIMO/UCB1SDA	X	01
		TB0.CCI6A	0	10
		TB0.6	1	
		A9	X	11
P4.5/UCB0SOMI/UCB0SCL/TA3.2	5	P4.5 (I/O)	I: 0; O: 1	00
		UCB0SOMI/UCB0SCL	X	01
		TA3.CCI2A	0	10
		TA3.2	1	
P4.6/UCB0SIMO/UCB0SDA/TA3.1	6	P4.6 (I/O)	I: 0; O: 1	00
		UCB0SIMO/UCB0SDA	X	01
		TA3.CCI1A	0	10
		TA3.1	1	
P4.7/UCA0STE/TB0.1	7	P4.7 (I/O)	I: 0; O: 1	00
		UCA0STE	X	01
		TB0.CCI1A	0	10
		TB0.1	1	

(1) X = don't care

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9.11.5 Port P5 (P5.0 to P5.7) Input/Output With Schmitt Trigger

Table 9-27 summarizes the selection of the pin functions.

Table 9-27. Port P5 (P5.0 to P5.7) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)	
			P5DIR.x	P5SEL.x
P5.0/UCA0CLK/TB0.2	0	P5.0 (I/O)	I: 0; O: 1	00
		UCA0CLK	X	01
		TB0.CCI2A	0	10
		TB0.2	1	
P5.1/UCA0RXD/UCA0SOMI/TB0.3	1	P5.1 (I/O)	I: 0; O: 1	00
		UCA0RXD/UCA0SOMI	X	01
		TB0.CCI3A	0	10
		TB0.3	1	
P5.2/UCA0TXD/UCA0SIMO/TB0.4	2	P5.2 (I/O)	I: 0; O: 1	00
		UCA0TXD/UCA0SIMO	X	01
		TB0.CCI4A	0	10
		TB0.4	1	
P5.3/UCB1CLK/TA3.0/A10	3	P5.3 (I/O)	I: 0; O: 1	00
		UCB1CLK	X	01
		TA3.CCI0A	0	10
		TA3.0	1	
		A10	X	11
P5.4/UCB1STE/TA3CLK/A11	4	P5.4 (I/O)	I: 0; O: 1	00
		UCB1STE	X	01
		TA3CLK	0	10
		A11	X	11
P5.5/UCB0CLK/TA2CLK	5	P5.5 (I/O)	I: 0; O: 1	00
		UCB0CLK	X	01
		TA2CLK	0	10
P5.6/UCB0STE/TA2.0	6	P5.6 (I/O)	I: 0; O: 1	00
		UCB0STE	X	01
		TA2.CCI0A	0	10
		TA2.0	1	
P5.7/TA2.1/COMP0.2	7	P5.7 (I/O)	I: 0; O: 1	00
		TA2.CCI1A	0	01
		TA2.1	1	
		COMP0.2	X	11

(1) X = don't care

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9.11.6 Port P6 (P6.0 to P6.2) Input/Output With Schmitt Trigger

Table 9-28 summarizes the selection of the pin functions.

Table 9-28. Port P6 (P6.0 to P6.2) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)	
			P6DIR.x	P6SEL.x
P6.0/TA2.2/COMP0.3	0	P6.0 (I/O)	I: 0; O: 1	00
		TA2.CCI2A	0	01
		TA2.2	1	
		COMP0.3	X	11
P6.1/TB0CLK	1	P6.1 (I/O)	I: 0; O: 1	00
		TB0CLK	0	01
P6.2/TB0.0	2	P6.2 (I/O)	I: 0; O: 1	00
		TB0.CCI0A	0	01
		TB0.0	1	

(1) X = don't care

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9.12 Device Descriptors

Table 9-29 lists the Device IDs. Table 9-30 lists the contents of the device descriptor tag-length-value (TLV) structure.

Table 9-29. Device IDs

DEVICE	DEVICE ID	
	1A05h	1A04h
MSP430FR2476	83h	2Ah
MSP430FR2475	83h	2Bh

Table 9-30. Device Descriptors

DESCRIPTION		ADDRESS	VALUE
Information block	Info length	1A00h	06h
	CRC length	1A01h	06h
	CRC value(1)	1A02h	Per unit
		1A03h	Per unit
	Device ID	1A04h	See Table 9-29
		1A05h	
	Hardware revision	1A06h	Per unit
	Firmware revision	1A07h	Per unit
Die record	Die record tag	1A08h	08h
	Die record length	1A09h	0Ah
	Lot wafer ID	1A0Ah	Per unit
		1A0Bh	Per unit
		1A0Ch	Per unit
		1A0Dh	Per unit
	Die X position	1A0Eh	Per unit
		1A0Fh	Per unit
	Die Y position	1A10h	Per unit
		1A11h	Per unit
	Test result	1A12h	Per unit
		1A13h	Per unit

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Table 9-30. Device Descriptors (continued)

DESCRIPTION		ADDRESS	VALUE
ADC calibration	ADC calibration tag	1A14h	11h
	ADC calibration length	1A15h	10h
	ADC gain factor(3)	1A16h	Per unit
		1A17h	Per unit
	ADC offset(4)	1A18h	Per unit
		1A19h	Per unit
	ADC internal shared 1.5-V reference, temperature sensor 30°C	1A1Ah	Per unit
		1A1Bh	Per unit
	ADC internal shared 1.5-V reference, temperature sensor 105°C	1A1Ch	Per unit
		1A1Dh	Per unit
	ADC internal shared 2.0-V reference, temperature sensor 30°C	1A1Eh	Per unit
		1A1Fh	Per unit
	ADC internal shared 2.0-V reference, temperature sensor 105°C	1A20h	Per unit
		1A21h	Per unit
	ADC internal shared 2.5-V reference, temperature sensor 30°C	1A22h	Per unit
		1A23h	Per unit
	ADC internal shared 2.5-V reference, temperature sensor 105°C	1A24h	Per unit
		1A25h	Per unit
Reference and DCO calibration	Internal shared reference Calibration tag	1A26h	12h
	Internal shared reference Calibration length	1A27h	0Ah
	Internal shared 1.5-V reference factor	1A28h	Per unit
		1A29h	Per unit
	Internal shared 2.0-V reference factor	1A2Ah	Per unit
		1A2Bh	Per unit
	Internal shared 2.5-V reference factor	1A2Ch	Per unit
		1A2Dh	Per unit
	DCO tap settings for 16 MHz, temperature 30°C	1A2Eh	Per unit
		1A2Fh	Per unit
	DCO tap settings for 24 MHz, temperature 30°C (2)	1A30h	Per unit
		1A31h	Per unit

(1) CRC value covers the checksum from 0x1A04h to 0x1AF7h by applying CRC-CCITT-16 polynomial of $x^{16} + x^{12} + x^5 + 1$.
(2) This value can be directly loaded into the DCO bits in the CSCTL0 register to get an accurate 24-MHz frequency at room temperature, especially when MCU exits from LPM3 and below. TI also suggests to use a predivider to decrease the frequency if the temperature drift might result an overshoot faster than 24 MHz.
(3) ADC gain: the gain correction factor is measured at 2.4 V and room temperature using ADCSREFx = 0x7, an external reference without internal buffer. $V_{R+} = V_{eref+}$, $V_{R-} = V_{eref-}$. Other settings can result in different factors.
(4) ADC offset: the offset correction factor is measured at 2.4 V and room temperature using ADCSREFx = 0x7, an external reference without internal buffer. $V_{R+} = V_{eref+}$, $V_{R-} = V_{eref-}$. Other settings can result in different factors

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9.13 Memory

9.13.1 Memory Organization

Table 9-31 summarizes the memory organization of the devices.

Table 9-31. Memory Organization

	ACCESS	MSP430FR2476	MSP430FR2475
Bootloader (BSL2) memory (ROM)	Read only	1KB FFFFFh to FFC00h	1KB FFFFFh to FFC00h
Memory (FRAM) Main: interrupt vectors and signatures Main: code memory	Read/Write (Optional Write Protect)(1)	64KB FFFFh to FF80h 17FFFh to 8000h	32KB FFFFh to FF80h FFFFh to 8000h
RAM	Read/Write	8KB 3FFFh to 2000h	6KB 37FFh to 2000h
Information memory (FRAM)	Read/Write (Optional Write Protect)(2)	512 bytes 19FFh to 1800h	512 bytes 19FFh to 1800h
Bootloader (BSL1) memory (ROM)	Read only	2KB 17FFh to 1000h	2KB 17FFh to 1000h
Peripherals	Read/Write	4KB 0FFFh to 0020h	4KB 0FFFh to 0020h
Tiny RAM	Read/Write	26 bytes 001Fh to 0006h	26 bytes 001Fh to 0006h
Reserved(3)	Read only	6 bytes 0005h to 0000h	6 bytes 0005h to 0000h

(1) The Program FRAM can be write protected by setting PFWP bit in SYSCFG0 register. See the SYS chapter in the *MP430FR4xx and MP430FR2xx Family User's Guide* for more details
(2) The Information FRAM can be write protected by setting DFWP bit in SYSCFG0 register. See the SYS chapter in the *MP430FR4xx and MP430FR2xx Family User's Guide* for more details
(3) Read as: D032h at 00h (Opcode: BIS.W LPM4, SR), 00F0h at 02h (Opcode: BIS.W LPM4, SR), 3FFFh at 04h (Opcode: JMP$)

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9.13.2 Peripheral File Map

Table 9-32 lists the available peripherals and the register base address for each.

Table 9-32. Peripherals Summary

MODULE NAME	BASE ADDRESS	SIZE
Special Functions (see Table 9-33)	0100h	0010h
PMM (see Table 9-34)	0120h	0020h
SYS (see Table 9-35)	0140h	0040h
CS (see Table 9-36)	0180h	0020h
FRAM (see Table 9-37)	01A0h	0010h
CRC (see Table 9-38)	01C0h	0008h
WDT (see Table 9-39)	01CCh	0002h
Port P1, P2 (see Table 9-40)	0200h	0020h
Port P3, P4 (see Table 9-41)	0220h	0020h
Port P5, P6 (see Table 9-42)	0240h	0020h
RTC (see Table 9-43)	0300h	0010h
Timer0_A3 (see Table 9-44)	0380h	0030h
Timer1_A3 (see Table 9-45)	03C0h	0030h
Timer2_A3 (see Table 9-46)	0400h	0030h
Timer3_A3 (see Table 9-47)	0440h	0030h
Timer0_B7 (see Table 9-48)	0480h	0030h
MPY32 (see Table 9-49)	04C0h	0030h
eUSCI_A0 (see Table 9-50)	0500h	0020h
eUSCI_A1 (see Table 9-51)	0520h	0020h
eUSCI_B0 (see Table 9-52)	0540h	0030h
eUSCI_B1 (see Table 9-53)	0580h	0030h
Backup Memory (see Table 9-54)	0660h	0020h
ADC (see Table 9-55)	0700h	0040h
eCOMP0 (see Table 9-56)	08E0h	0020h

Table 9-33. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

Table 9-34. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
PMM control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
PMM control 2	PMMCTL2	04h
PMM interrupt flags	PMMIFG	0Ah
PM5 control 0	PM5CTL0	10h

Table 9-35. SYS Registers (Base Address: 0140h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
System control	SYSCTL	00h
Bootloader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h

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Table 9-35. SYS Registers (Base Address: 0140h) (continued)

REGISTER DESCRIPTION	ACRONYM	OFFSET
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
Bus error vector generator	SYSBERRIV	18h
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh
System configuration 0	SYSCFG0	20h
System configuration 1	SYSCFG1	22h
System configuration 2	SYSCFG2	24h
System configuration 3	SYSCFG3	26h

Table 9-36. CS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
CS control 0	CSCTL0	00h
CS control 1	CSCTL1	02h
CS control 2	CSCTL2	04h
CS control 3	CSCTL3	06h
CS control 4	CSCTL4	08h
CS control 5	CSCTL5	0Ah
CS control 6	CSCTL6	0Ch
CS control 7	CSCTL7	0Eh
CS control 8	CSCTL8	10h

Table 9-37. FRAM Registers (Base Address: 01A0h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
FRAM control 0	FRCTL0	00h
General control 0	GCCTL0	04h
General control 1	GCCTL1	06h

Table 9-38. CRC Registers (Base Address: 01C0h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
CRC data input	CRC16DI	00h
CRC data input reverse byte	CRCDIRB	02h
CRC initialization and result	CRCINIRES	04h
CRC result reverse byte	CRCRESR	06h

Table 9-39. WDT Registers (Base Address: 01CCh)

REGISTER DESCRIPTION	ACRONYM	OFFSET
Watchdog timer control	WDTCTL	00h

Table 9-40. Port P1, P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 pulling enable	P1REN	06h

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Table 9-40. Port P1, P2 Registers (Base Address: 0200h) (continued)

REGISTER DESCRIPTION	ACRONYM	OFFSET
Port P1 selection 0	P1SEL0	0Ah
Port P1 selection 1	P1SEL1	0Ch
Port P1 interrupt vector word	P1IV	0Eh
Port P1 complement selection	P1SELC	16h
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 pulling enable	P2REN	07h
Port P2 selection 0	P2SEL0	0Bh
Port P2 selection 1	P2SEL1	0Dh
Port P2 interrupt vector word	P2IV	1Eh
Port P2 complement selection	P2SELC	17h
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

Table 9-41. Port P3, P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 pulling enable	P3REN	06h
Port P3 selection 0	P3SEL0	0Ah
Port P3 selection 1	P3SEL1	0Ch
Port P3 interrupt vector word	P3IV	0Eh
Port P3 complement selection	P3SELC	16h
Port P3 interrupt edge select	P3IES	18h
Port P3 interrupt enable	P3IE	1Ah
Port P3 interrupt flag	P3IFG	1Ch
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 pulling enable	P4REN	07h
Port P4 selection 0	P4SEL0	0Bh
Port P4 selection 1	P4SEL1	0Dh
Port P4 interrupt vector word	P4IV	1Eh
Port P4 complement selection	P4SELC	17h
Port P4 interrupt edge select	P4IES	19h
Port P4 interrupt enable	P4IE	1Bh
Port P4 interrupt flag	P4IFG	1Dh

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Table 9-42. Port P5, P6 Registers (Base Address: 0240h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 pulling enable	P5REN	06h
Port P5 selection 0	P5SEL0	0Ah
Port P5 selection 1	P5SEL1	0Ch
Port P5 interrupt vector word	P5IV	0Eh
Port P5 complement selection	P5SELC	16h
Port P5 interrupt edge select	P5IES	18h
Port P5 interrupt enable	P5IE	1Ah
Port P5 interrupt flag	P5IFG	1Ch
Port P6 input	P6IN	01h
Port P6 output	P6OUT	03h
Port P6 direction	P6DIR	05h
Port P6 pulling enable	P6REN	07h
Port P6 selection 0	P6SEL0	0Bh
Port P6 selection 1	P6SEL1	0Dh
Port P6 interrupt vector word	P6IV	1Eh
Port P6 complement selection	P6SELC	17h
Port P6 interrupt edge select	P6IES	19h
Port P6 interrupt enable	P6IE	1Bh
Port P6 interrupt flag	P6IFG	1Dh

Table 9-43. RTC Registers (Base Address: 0300h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
RTC control	RTCCTL	00h
RTC interrupt vector	RTCIV	04h
RTC modulo	RTCMOD	08h
RTC counter	RTCCNT	0Ch

Table 9-44. Timer0_A3 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
TA0 counter	TA0R	10h
Capture/compare 0	TA0CCR0	12h
Capture/compare 1	TA0CCR1	14h
Capture/compare 2	TA0CCR2	16h
TA0 expansion 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

Table 9-45. Timer1_A3 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h

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Table 9-45. Timer1_A3 Registers (Base Address: 03C0h) (continued)

REGISTER DESCRIPTION	ACRONYM	OFFSET
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter	TA1R	10h
Capture/compare 0	TA1CCR0	12h
Capture/compare 1	TA1CCR1	14h
Capture/compare 2	TA1CCR2	16h
TA1 expansion 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

Table 9-46. Timer2_A3 Registers (Base Address: 0400h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
TA2 control	TA2CTL	00h
Capture/compare control 0	TA2CCTL0	02h
Capture/compare control 1	TA2CCTL1	04h
Capture/compare control 2	TA2CCTL2	06h
TA2 counter	TA2R	10h
Capture/compare 0	TA2CCR0	12h
Capture/compare 1	TA2CCR1	14h
Capture/compare 2	TA2CCR2	16h
TA2 expansion 0	TA2EX0	20h
TA2 interrupt vector	TA2IV	2Eh

Table 9-47. Timer3_A3 Registers (Base Address: 0440h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
TA3 control	TA3CTL	00h
Capture/compare control 0	TA3CCTL0	02h
Capture/compare control 1	TA3CCTL1	04h
Capture/compare control 2	TA3CCTL2	06h
TA3 counter	TA3R	10h
Capture/compare 0	TA3CCR0	12h
Capture/compare 1	TA3CCR1	14h
Capture/compare 2	TA3CCR2	16h
TA3 expansion 0	TA3EX0	20h
TA3 interrupt vector	TA3IV	2Eh

Table 9-48. Timer0_B7 Registers (Base Address: 0480h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
Capture/compare control 3	TB0CCTL3	08h
Capture/compare control 4	TB0CCTL4	0Ah
Capture/compare control 5	TB0CCTL5	0Ch
Capture/compare control 6	TB0CCTL6	0Eh
TB0 counter	TB0R	10h
Capture/compare 0	TB0CCR0	12h

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Table 9-48. Timer0_B7 Registers (Base Address: 0480h) (continued)

REGISTER DESCRIPTION	ACRONYM	OFFSET
Capture/compare 1	TB0CCR1	14h
Capture/compare 2	TB0CCR2	16h
Capture/compare 3	TB0CCR3	18h
Capture/compare 4	TB0CCR4	1Ah
Capture/compare 5	TB0CCR5	1Ch
Capture/compare 6	TB0CCR6	1Eh
TB0 expansion 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

Table 9-49. MPY32 Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP6	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 × 16 sum extension	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control 0	MPY32CTL0	2Ch

Table 9-50. eUSCI_A0 Registers (Base Address: 0500h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
eUSCI_A control word 0	UCA0CTLW0	00h
eUSCI_A control word 1	UCA0CTLW1	02h
eUSCI_A control rate 0	UCA0BR0	06h
eUSCI_A control rate 1	UCA0BR1	07h
eUSCI_A modulation control	UCA0MCTLW	08h
eUSCI_A status	UCA0STAT	0Ah
eUSCI_A receive buffer	UCA0RXBUF	0Ch
eUSCI_A transmit buffer	UCA0TXBUF	0Eh
eUSCI_A LIN control	UCA0ABCTL	10h

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Table 9-50. eUSCI_A0 Registers (Base Address: 0500h) (continued)

REGISTER DESCRIPTION	ACRONYM	OFFSET
eUSCI_A IrDA transmit control	IUCA0IRTCTL	12h
eUSCI_A IrDA receive control	IUCA0IRRCTL	13h
eUSCI_A interrupt enable	UCA0IE	1Ah
eUSCI_A interrupt flags	UCA0IFG	1Ch
eUSCI_A interrupt vector word	UCA0IV	1Eh

Table 9-51. eUSCI_A1 Registers (Base Address: 0520h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
eUSCI_A control word 0	UCA1CTLW0	00h
eUSCI_A control word 1	UCA1CTLW1	02h
eUSCI_A control rate 0	UCA1BR0	06h
eUSCI_A control rate 1	UCA1BR1	07h
eUSCI_A modulation control	UCA1MCTLW	08h
eUSCI_A status	UCA1STAT	0Ah
eUSCI_A receive buffer	UCA1RXBUF	0Ch
eUSCI_A transmit buffer	UCA1TXBUF	0Eh
eUSCI_A LIN control	UCA1ABCTL	10h
eUSCI_A IrDA transmit control	IUCA1IRTCTL	12h
eUSCI_A IrDA receive control	IUCA1IRRCTL	13h
eUSCI_A interrupt enable	UCA1IE	1Ah
eUSCI_A interrupt flags	UCA1IFG	1Ch
eUSCI_A interrupt vector word	UCA1IV	1Eh

Table 9-52. eUSCI_B0 Registers (Base Address: 0540h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
eUSCI_B control word 0	UCB0CTLW0	00h
eUSCI_B control word 1	UCB0CTLW1	02h
eUSCI_B bit rate 0	UCB0BR0	06h
eUSCI_B bit rate 1	UCB0BR1	07h
eUSCI_B status word	UCB0STATW	08h
eUSCI_B byte counter threshold	UCB0TBCNT	0Ah
eUSCI_B receive buffer	UCB0RXBUF	0Ch
eUSCI_B transmit buffer	UCB0TXBUF	0Eh
eUSCI_B I2C own address 0	UCB0I2COA0	14h
eUSCI_B I2C own address 1	UCB0I2COA1	16h
eUSCI_B I2C own address 2	UCB0I2COA2	18h
eUSCI_B I2C own address 3	UCB0I2COA3	1Ah
eUSCI_B receive address	UCB0ADDRX	1Ch
eUSCI_B address mask	UCB0ADDMASK	1Eh
eUSCI_B I2C slave address	UCB0I2CSA	20h
eUSCI_B interrupt enable	UCB0IE	2Ah
eUSCI_B interrupt flags	UCB0IFG	2Ch
eUSCI_B interrupt vector word	UCB0IV	2Eh

Table 9-53. eUSCI_B1 Registers (Base Address: 0580h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
eUSCI_B control word 0	UCB1CTLW0	00h

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Table 9-53. eUSCI_B1 Registers (Base Address: 0580h) (continued)

REGISTER DESCRIPTION	ACRONYM	OFFSET
eUSCI_B control word 1	UCB1CTLW1	02h
eUSCI_B bit rate 0	UCB1BR0	06h
eUSCI_B bit rate 1	UCB1BR1	07h
eUSCI_B status word	UCB1STATW	08h
eUSCI_B byte counter threshold	UCB1TBCNT	0Ah
eUSCI_B receive buffer	UCB1RXBUF	0Ch
eUSCI_B transmit buffer	UCB1TXBUF	0Eh
eUSCI_B I2C own address 0	UCB1I2COA0	14h
eUSCI_B I2C own address 1	UCB1I2COA1	16h
eUSCI_B I2C own address 2	UCB1I2COA2	18h
eUSCI_B I2C own address 3	UCB1I2COA3	1Ah
eUSCI_B receive address	UCB1ADDRX	1Ch
eUSCI_B address mask	UCB1ADDMASK	1Eh
eUSCI_B I2C slave address	UCB1I2CSA	20h
eUSCI_B interrupt enable	UCB1IE	2Ah
eUSCI_B interrupt flags	UCB1IFG	2Ch
eUSCI_B interrupt vector word	UCB1IV	2Eh

Table 9-54. Backup Memory Registers (Base Address: 0660h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
Backup memory 0	BAKMEM0	00h
Backup memory 1	BAKMEM1	02h
Backup memory 2	BAKMEM2	04h
Backup memory 3	BAKMEM3	06h
Backup memory 4	BAKMEM4	08h
Backup memory 5	BAKMEM5	0Ah
Backup memory 6	BAKMEM6	0Ch
Backup memory 7	BAKMEM7	0Eh
Backup memory 8	BAKMEM8	10h
Backup memory 9	BAKMEM9	12h
Backup memory 10	BAKMEM10	14h
Backup memory 11	BAKMEM11	16h
Backup memory 12	BAKMEM12	18h
Backup memory 13	BAKMEM13	1Ah
Backup memory 14	BAKMEM14	1Ch
Backup memory 15	BAKMEM15	1Eh

Table 9-55. ADC Registers (Base Address: 0700h)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC control 0	ADCCTL0	00h
ADC control 1	ADCCTL1	02h
ADC control 2	ADCCTL2	04h
ADC window comparator low threshold	ADCLO	06h
ADC window comparator high threshold	ADCHI	08h
ADC memory control 0	ADCMCTL0	0Ah
ADC conversion memory	ADCMEM0	12h

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Table 9-55. ADC Registers (Base Address: 0700h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC interrupt enable	ADCIE	1Ah
ADC interrupt flags	ADCIFG	1Ch
ADC interrupt vector word	ADCIV	1Eh

Table 9-56. eCOMP Registers (Base Address: 08E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Comparator control 0	CP0CTL0	00h
Comparator control 1	CP0CTL1	02h
Comparator interrupt	CP0INT	06h
Comparator interrupt vector	CP0IV	08h
Comparator built-in DAC control	CP0DACCTL	10h

9.14 Identification

9.14.1 Revision Identification

The device revision information is included as part of the top-side marking on the device package. The device-specific errata sheet describes these markings.

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the Hardware Revision entries in Section 9.12.

9.14.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings.

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the Device ID entries in Section 9.12.

9.14.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in MSP430 Programming With the JTAG Interface.

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10 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP430 devices. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

10.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 10-µF plus a 100-nF low-ESR ceramic decoupling capacitor to the DVCC and DVSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, TI recommends separated grounds with a single-point connection for better noise isolation from digital-to-analog circuits on the board and to achieve high analog accuracy.

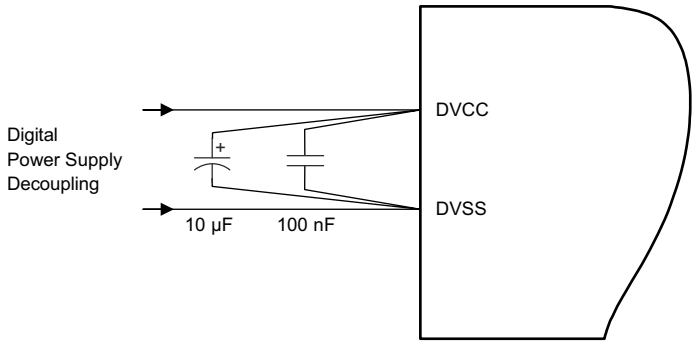

Figure 10-1. Power Supply Decoupling

10.1.2 External Oscillator

This device supports only a low-frequency crystal (32 kHz) on the XIN and XOUT pins. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the XIN input pin that meet the specifications of the respective oscillator if the appropriate XT1BYPASS mode is selected. In this case, the associated XOUT pin can be used for other purposes. If the XIN and XOUT pins are not used, they must be terminated according to Section 7.6.

Figure 10-2 shows a typical connection diagram.

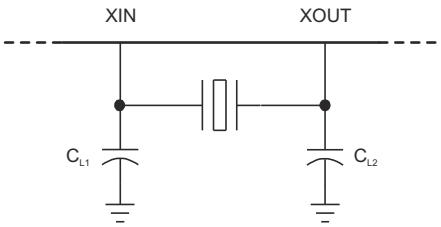

Figure 10-2. Typical Crystal Connection

See MSP430 32-kHz Crystal Oscillators for more information on selecting, testing, and designing a crystal oscillator with the MSP430 devices.

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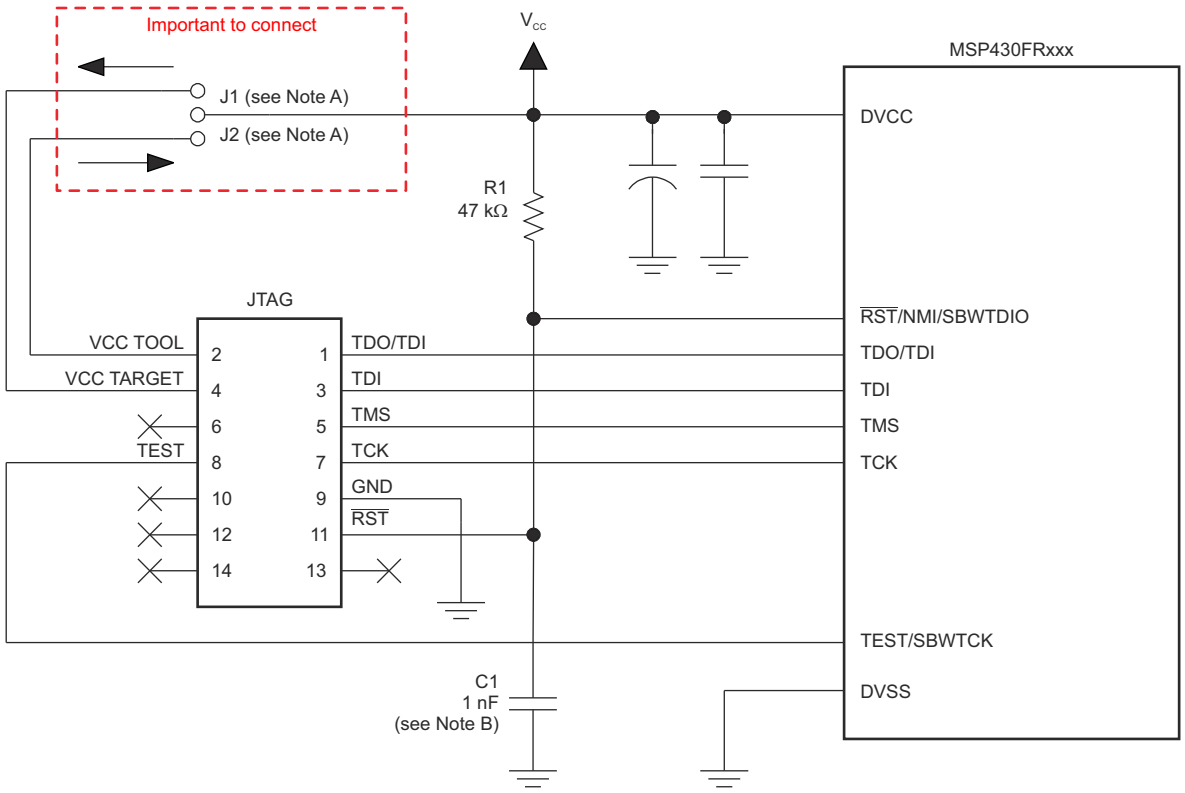
10.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. Figure 10-3 shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. Figure 10-4 shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply V_{CC} to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a V_{CC} sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The V_{CC} sense feature detects the local V_{CC} present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. Figure 10-3 and Figure 10-4 show a jumper block that supports both scenarios of supplying V_{CC} to the target board. If this flexibility is not required, the desired V_{CC} connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

For additional design information regarding the JTAG interface, see the MSP430 Hardware Tools User's Guide.



A. If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.

B. The upper limit for C1 is 1.1 nF when using current TI tools.

Figure 10-3. Signal Connections for 4-Wire JTAG Communication

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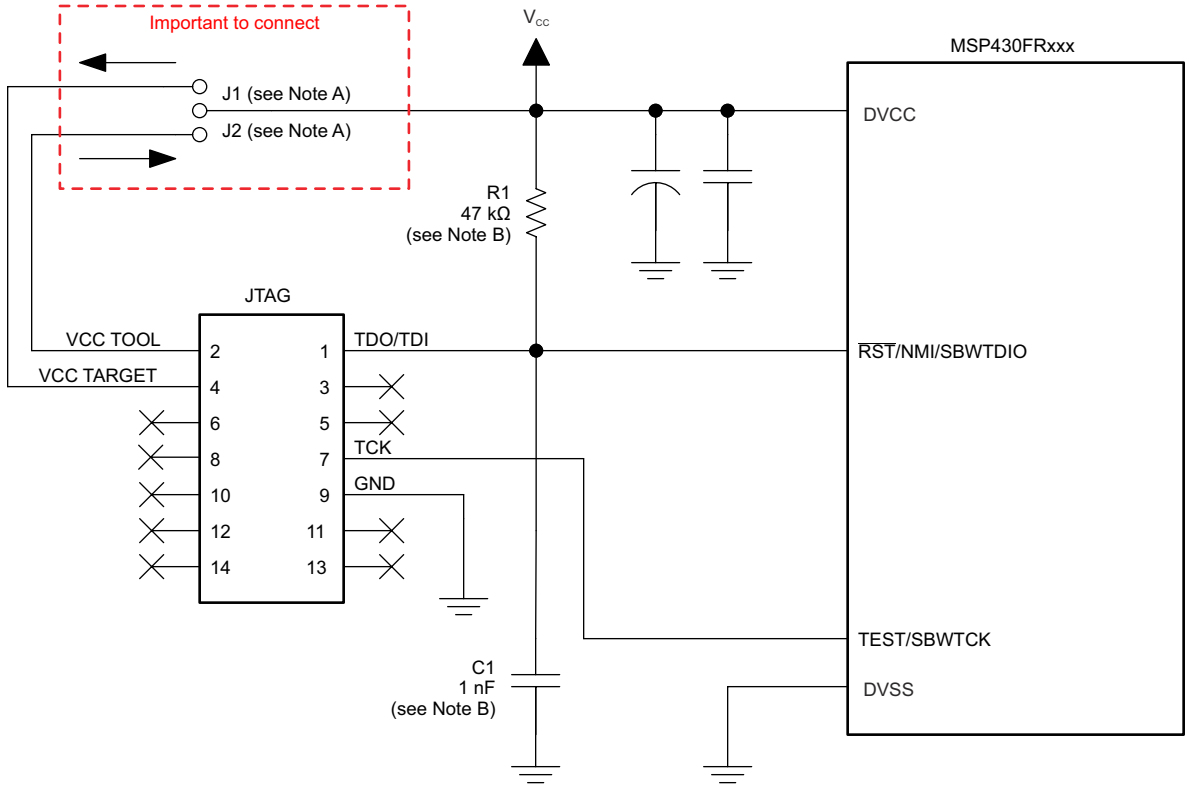

A. Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.

B. The device RST/NMI/SBWTDIO pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 1.1 nF when using current TI tools.

Figure 10-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)

10.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the Special Function Register (SFR), SFRRPCR.

In reset mode, the RST/NMI pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the RST/NMI pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The RST/NMI pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the RST/NMI pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-kΩ pullup resistor to the RST/NMI pin with a 10-nF pulldown capacitor. The pulldown capacitor should not exceed 1.1 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the MP430FR4xx and MP430FR2xx Family User's Guide for more information on the referenced control registers and bits.

10.1.5 Unused Pins

For details on the connection of unused pins, see Section 7.6.

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10.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See MSP430 32-kHz Crystal Oscillators for recommended layout guidelines.
- Proper bypass capacitors on DVCC and reference pins, if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See MSP430 System-Level ESD Considerations for guidelines.

10.1.7 Do's and Don'ts

During power up, power down, and device operation, DVCC must not exceed the limits specified in Section 8.1, *Absolute Maximum Ratings*. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

10.2 Peripheral- and Interface-Specific Design Information

10.2.1 ADC Peripheral

10.2.1.1 Partial Schematic

Figure 10-5 shows the recommended decoupling circuit when an external voltage reference is used.

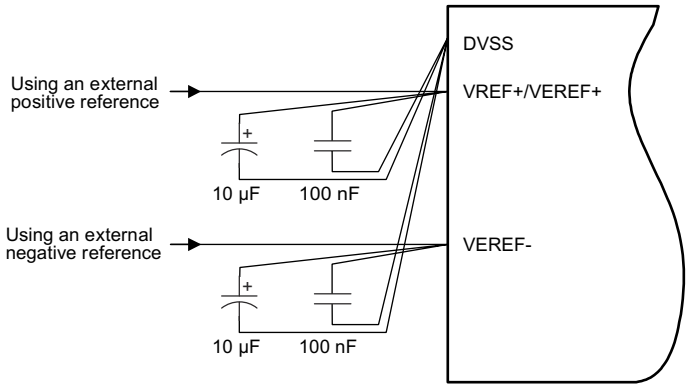

Figure 10-5. ADC Grounding and Noise Considerations

10.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate printed-circuit-board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in Section 10.1.1 combined with the connections shown in Figure 10-5 prevent this.

Quickly switching digital signals and noisy power supply lines can corrupt the conversion results, so keep the ADC input trace shielded from those digital and power supply lines. Putting the MCU in low-power mode during the ADC conversion improves the ADC performance in a noisy environment. If the device includes the analog power pair inputs (AVCC and AVSS), TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

Figure 10-5 shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as described in the sections *ADC Pin Enable* and *1.2-V Reference Settings* of the MSP430FR4xx and MSP430FR2xx Family User's Guide.

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters

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the device. In this case, the 10-µF capacitor buffers the reference pin and filters low-frequency ripple. A 100-nF bypass capacitor of filters high-frequency noise.

10.2.1.3 Layout Guidelines

Components that are shown in the partial schematic (see Figure 10-5) should be placed as close as possible to the respective device pins to avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

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11 Device and Documentation Support

11.1 Getting Started and Next Steps

For more information on the MSP low-power microcontrollers and the tools and libraries that are available to help with your development, visit the MSP430™ ultra-low-power sensing & measurement MCUs overview.

11.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

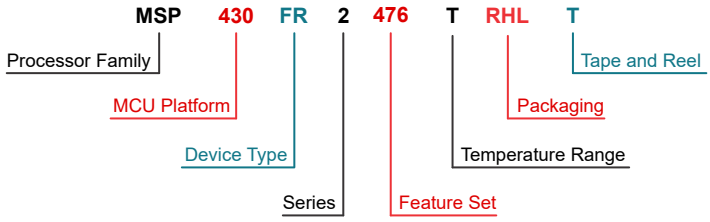
XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 11-1 provides a legend for reading the complete device name.



Processor Family	MSP = Mixed-signal processor XMS = Experimental silicon	
MCU Platform	430 = MSP430 16-bit low-power platform	
Device Type	**Memory type** FR = FRAM	
Series	2 = No LCD driver	
Feature Set	**First and second digits:** **ADC12 channels / eUSCIs / 16-bit timers** 47 = Up to 12 / 4 / 5	**Third digit:** **FRAM (KB) / SRAM (KB)** 6 = 64 / 8 5 = 32 / 6
Temperature Range	T = –40°C to 105°C	
Packaging	www.ti.com/packaging	
Distribution Format	T = Small reel R = Large reel No marking = Tube or tray	

Figure 11-1. Device Nomenclature

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11.3 Tools and Software

Table 11-1 lists the debug features supported by these microcontrollers. See the *Code Composer Studio™ IDE for MSP430™ MCUs User's Guide* for details on the available features.

Table 11-1. Hardware Features

MSP430 ARCHITECTURE	4-WIRE JTAG	2-WIRE JTAG	BREAK-POINTS (N)	RANGE BREAK-POINTS	CLOCK CONTROL	STATE SEQUENCER	TRACE BUFFER	LPMx.5 DEBUGGING SUPPORT	EEM VERSION
MSP430Xv2	Yes	Yes	3	Yes	Yes	No	No	No	S

Design Kits and Evaluation Modules

MSP430FR2476 LaunchPad™ development kit

The LP-MSP430FR2476 LaunchPad development kit is an easy-to-use evaluation module (EVM) based on the MSP430FR2476 value line sensing microcontroller (MCU). It contains everything needed to start developing on the ultra-low-power MSP430FR2x value line sensing MCU platform, including on-board debug probe for programming, debugging and energy measurements.

Target development board for MSP430FR2476 MCU

The MSP-TS430PT48A microcontroller development board is a standalone ZIF socket target board used to program and debug the MSP430 in-system through the JTAG interface or the Spy Bi-Wire (2-wire JTAG) protocol. This development board supports the MSP430FR2476 FRAM devices in a 48-pin QFP package (TI package code: PT).

Software

MSP430Ware™ Software

MSP430Ware software is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 design resources, MSP430Ware software also includes a high-level API called MSP430 Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware software is available as a component of CCS or as a stand-alone package.

MSP430FR267x, MSP430FR247x Code Examples

C code examples that configure each of the integrated peripherals for various application needs.

MSP Driver Library

The driver library's abstracted API keeps you above the bits and bytes of the MSP430 hardware by providing easy-to-use function calls. Thorough documentation is delivered through a helpful API guide, which includes details on each function call and the recognized parameters. Developers can use driver library functions to write complete projects with minimal overhead.

MSP EnergyTrace™ Technology

EnergyTrace technology for MSP430 microcontrollers is an energy-based code analysis tool that measures and displays the application's energy profile and helps to optimize it for ultra-low-power consumption.

ULP (Ultra-Low Power) Advisor

ULP Advisor™ software is a tool for guiding developers to write more efficient code to fully utilize the unique ultra-low power features of MSP and MSP432 microcontrollers. Aimed at both experienced and new microcontroller developers, ULP Advisor checks your code against a thorough ULP checklist to squeeze every last nano amp out of your application. At build time, ULP Advisor will provide notifications and remarks to highlight areas of your code that can be further optimized for lower power.

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FRAM Embedded Software Utilities for MSP Ultra-Low-Power Microcontrollers

The FRAM Utilities is designed to grow as a collection of embedded software utilities that leverage the ultra-low-power and virtually unlimited write endurance of FRAM. The utilities are available for MSP430FRxx FRAM microcontrollers and provide example code to help start application development. Included utilities include Compute Through Power Loss (CTPL). CTPL is utility API set that enables ease of use with LPMx.5 low-power modes and a powerful shutdown mode that allows an application to save and restore critical system components when a power loss is detected.

IEC60730 Software Package

The IEC60730 MSP430 software package helps you comply with IEC 60730-1:2010 (Automatic Electrical Controls for Household and Similar Use – Part 1: General Requirements) for up to Class B products, which includes home appliances, arc detectors, power converters, power tools, e-bikes, and many others. The IEC60730 MSP430 software package can be embedded in applications that run on MSP430 MCUs to help simplify the certification efforts of functional safety compliant consumer devices to IEC 60730-1:2010 Class B.

Fixed-Point Math Library for MSP

The MSP IQmath and Qmath Libraries are a collection of highly optimized and high-precision mathematical functions for C programmers to seamlessly port a floating-point algorithm into fixed-point code on MSP430 and MSP432 devices. These routines are typically used in computationally intensive real-time applications where optimal execution speed, high accuracy, and ultra-low energy are critical. By using the IQmath and Qmath libraries, it is possible to achieve execution speeds considerably faster and energy consumption considerably lower than equivalent code written using floating-point math.

Floating-Point Math Library for MSP430

Continuing to innovate in the low power and low cost microcontroller space, TI brings you MSPMATHLIB. Leveraging the intelligent peripherals of our devices, this floating point math library of scalar functions brings you up to 26x better performance. Mathlib is easy to integrate into your designs. This library is free and is integrated in both Code Composer Studio IDE and IAR Embedded Workbench IDE.

Development Tools

Code Composer Studio™ Integrated Development Environment for MSP Microcontrollers

Code Composer Studio integrated development environment (IDE) supports all MSP microcontroller devices. Code Composer Studio IDE comprises a suite of embedded software utilities used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features.

IAR Embedded Workbench® IDE

IAR Embedded Workbench IDE for MSP430 MCUs is a complete C/C++ compiler toolchain for building and debugging embedded applications based on MSP430 microcontrollers. The debugger can be used for source and disassembly code with support for complex code and data breakpoints. It also provides a hardware simulator that allows debugging without a physical target connected.

Uniflash Standalone Flash Tool

CCS Uniflash is a stand-alone tool used to program on-chip flash memory on TI MCUs. Uniflash has a GUI, command line, and scripting interface. Uniflash is a software tool available by TI Cloud Tools or desktop application download from the TI web page.

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MSP MCU Programmer and Debugger

The MSP-FET is a powerful emulation development tool – often called a debug probe – that lets users quickly begin application development on MSP low-power microcontrollers (MCU). Creating MCU software usually requires downloading the resulting binary program to the MSP device for validation and debugging. The MSP-FET provides a debug communication pathway between a host computer and the target MSP. Furthermore, the MSP-FET also provides a backchannel UART connection between the computer's USB interface and the MSP UART. This affords the MSP programmer a convenient method for communicating serially between the MSP and a terminal running on the computer.

MSP-GANG Production Programmer

The MSP Gang Programmer can program up to eight identical MSP430 or MSP432 flash or FRAM devices at the same time. The MSP Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that allow the user to fully customize the process. The MSP Gang Programmer is provided with an expansion board, called the Gang Splitter, that implements the interconnections between the MSP Gang Programmer and multiple target devices.

TIREX Resource Explorer (TIRex)

An online portal to examples, libraries, executables, and documentation for your device and development board. TIRex can be accessed directly in Code Composer Studio IDE or in TI Cloud Tools.

TI Cloud Tools

Start development immediately on dev.ti.com. Begin by using the Resource Explorer interface to quickly find all the files you need. Then, edit, build, and debug embedded applications in the cloud, using industry-leading Code Composer Studio Cloud IDE.

GCC - Compiler for MSP

MSP430 and MSP432 GCC open source packages are complete debugger and open source C/C++ compiler toolchains for building and debugging embedded applications based on MSP430 and MSP432 microcontrollers. These free GCC compilers support all MSP430 and MSP432 devices without code size limitations. In addition, these compilers can be used stand-alone from the command-line or within Code Composer Studio v6.0 or later. Get started today whether you are using a Windows®, Linux®, or macOS® environment.

11.4 Documentation Support

The following documents describe the MSP430FR247x microcontrollers. Copies of these documents are available on the Internet at www.ti.com.

Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (for example, MSP430FR2476). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

Errata

MSP430FR2476 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430FR2475 Device Erratasheet

Describes the known exceptions to the functional specifications.

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User's Guides

MSP430FR4xx and MSP430FR2xx Family User's Guide

Detailed description of all modules and peripherals available in this device family.

MSP430™ FRAM Devices Bootloader (BSL) User's Guide

The bootloader (BSL) on MSP430 microcontrollers (MCUs) lets users communicate with embedded memory in the MSP430 MCU during the prototyping phase, final production, and in service. Both the programmable memory (FRAM memory) and the data memory (RAM) can be modified as required.

MSP430™ Programming With the JTAG Interface

This document describes the functions that are required to erase, program, and verify the memory module of the MSP430 flash-based and FRAM-based microcontroller families using the JTAG communication port.

MSP430™ Hardware Tools User's Guide

This manual describes the hardware of the TI MSP-FET430 Flash Emulation Tool (FET). The FET is the program development tool for the MSP430 ultra-low-power microcontroller. Both available interface types, the parallel port interface and the USB interface, are described.

Application Reports

MSP430 32-kHz Crystal Oscillators

Selection of the right crystal, correct load circuit, and proper board layout are important for a stable crystal oscillator. This application report summarizes crystal oscillator function and explains the parameters to select the correct crystal for MSP430 ultra-low-power operation. In addition, hints and examples for correct board layout are given. The document also contains detailed information on the possible oscillator tests to ensure stable oscillator operation in mass production.

MSP430 System-Level ESD Considerations

System-level ESD has become increasingly demanding with silicon technology scaling towards lower voltages and the need for designing cost-effective and ultra-low-power components. This application report addresses ESD topics to help board designers and OEMs understand and design robust system-level designs.

11.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.6 Trademarks

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Windows® is a registered trademark of Microsoft Corporation.
Linux® is a registered trademark of Linus Torvalds.
macOS® is a registered trademark of Apple, Inc.
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11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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11.8 Export Control Notice

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11.9 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, see the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
M430FR2476TRHBRG4	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	FR2476
M430FR2476TRHBRG4.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	FR2476
MSP430FR2475TPT	Active	Production	LQFP (PT) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	430FR2475
MSP430FR2475TPT.A	Active	Production	LQFP (PT) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	430FR2475
MSP430FR2475TPTR	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	430FR2475
MSP430FR2475TPTR.A	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	430FR2475
MSP430FR2475TRHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	FR2475
MSP430FR2475TRHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	FR2475
MSP430FR2475TRHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	FR2475
MSP430FR2475TRHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	FR2475
MSP430FR2475TRHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	FR2475
MSP430FR2475TRHBR.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	FR2475
MSP430FR2475TRHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	FR2475
MSP430FR2475TRHBT.A	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	FR2475
MSP430FR2476TPT	Active	Production	LQFP (PT) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	430FR2476
MSP430FR2476TPT.A	Active	Production	LQFP (PT) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	430FR2476
MSP430FR2476TPTR	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	430FR2476
MSP430FR2476TPTR.A	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	430FR2476
MSP430FR2476TRHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	FR2476
MSP430FR2476TRHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	FR2476
MSP430FR2476TRHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	FR2476
MSP430FR2476TRHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	FR2476
MSP430FR2476TRHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	FR2476
MSP430FR2476TRHBR.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	FR2476
MSP430FR2476TRHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	FR2476
MSP430FR2476TRHBT.A	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	FR2476

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

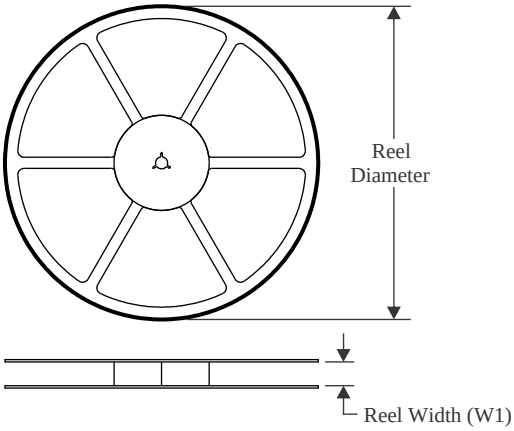
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

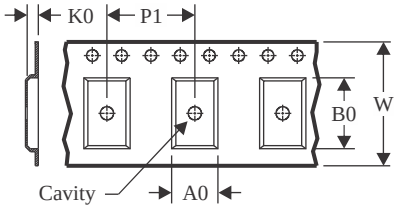
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

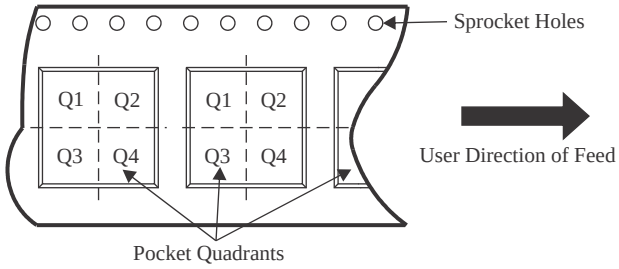


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

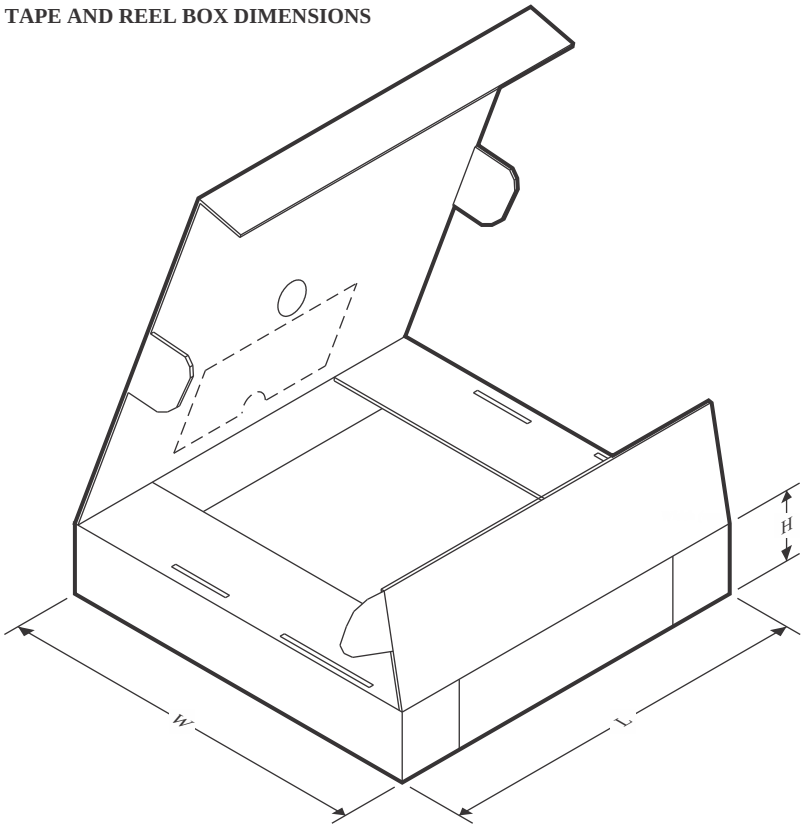
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
M430FR2476TRHBRG4	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430FR2475TPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
MSP430FR2475TPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
MSP430FR2475TRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR2475TRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR2475TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430FR2475TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430FR2476TPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
MSP430FR2476TPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
MSP430FR2476TRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR2476TRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR2476TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430FR2476TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

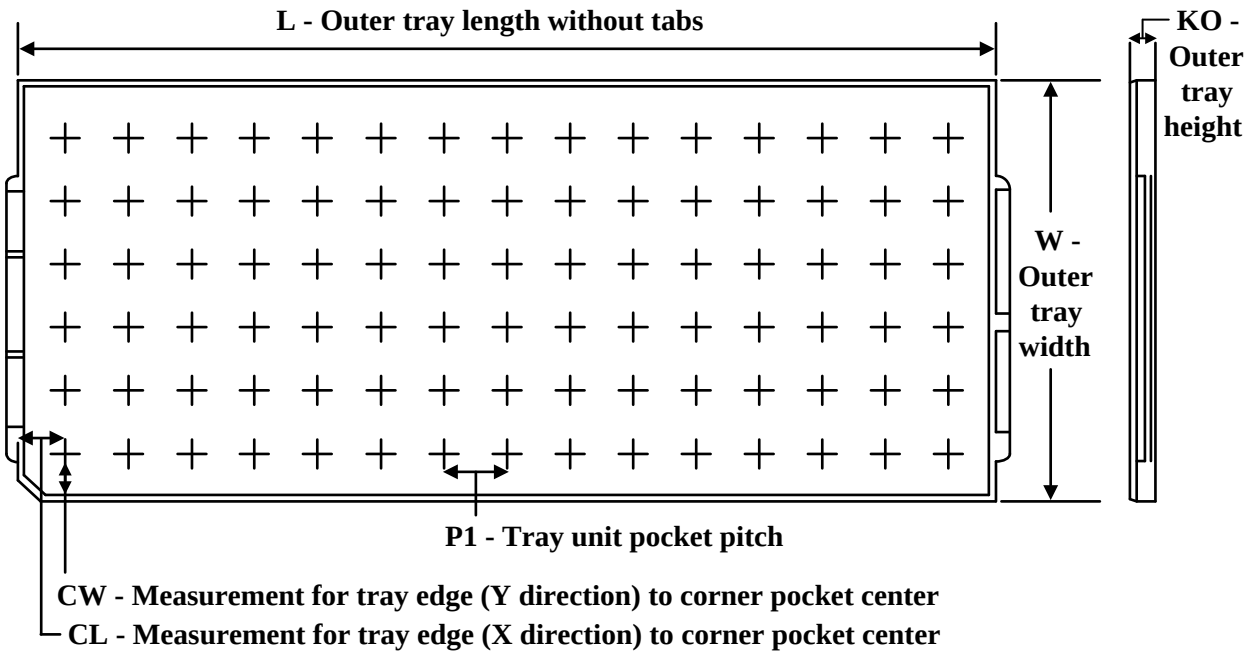
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
M430FR2476TRHBRG4	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430FR2475TPTR	LQFP	PT	48	1000	336.6	336.6	31.8
MSP430FR2475TPTR	LQFP	PT	48	1000	350.0	350.0	43.0
MSP430FR2475TRHAR	VQFN	RHA	40	2500	360.0	360.0	36.0
MSP430FR2475TRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430FR2475TRHBR	VQFN	RHB	32	3000	360.0	360.0	36.0
MSP430FR2475TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430FR2476TPTR	LQFP	PT	48	1000	350.0	350.0	43.0
MSP430FR2476TPTR	LQFP	PT	48	1000	336.6	336.6	31.8
MSP430FR2476TRHAR	VQFN	RHA	40	2500	360.0	360.0	36.0
MSP430FR2476TRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430FR2476TRHBR	VQFN	RHB	32	3000	360.0	360.0	36.0
MSP430FR2476TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
MSP430FR2475TPT	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430FR2475TPT	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430FR2475TPT.A	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430FR2475TPT.A	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430FR2476TPT	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430FR2476TPT	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430FR2476TPT.A	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430FR2476TPT.A	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

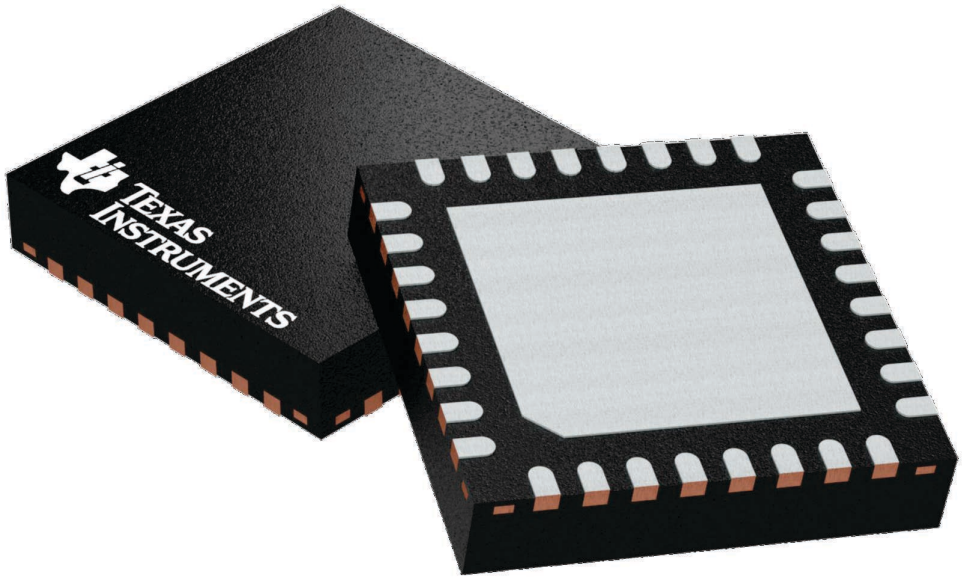
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

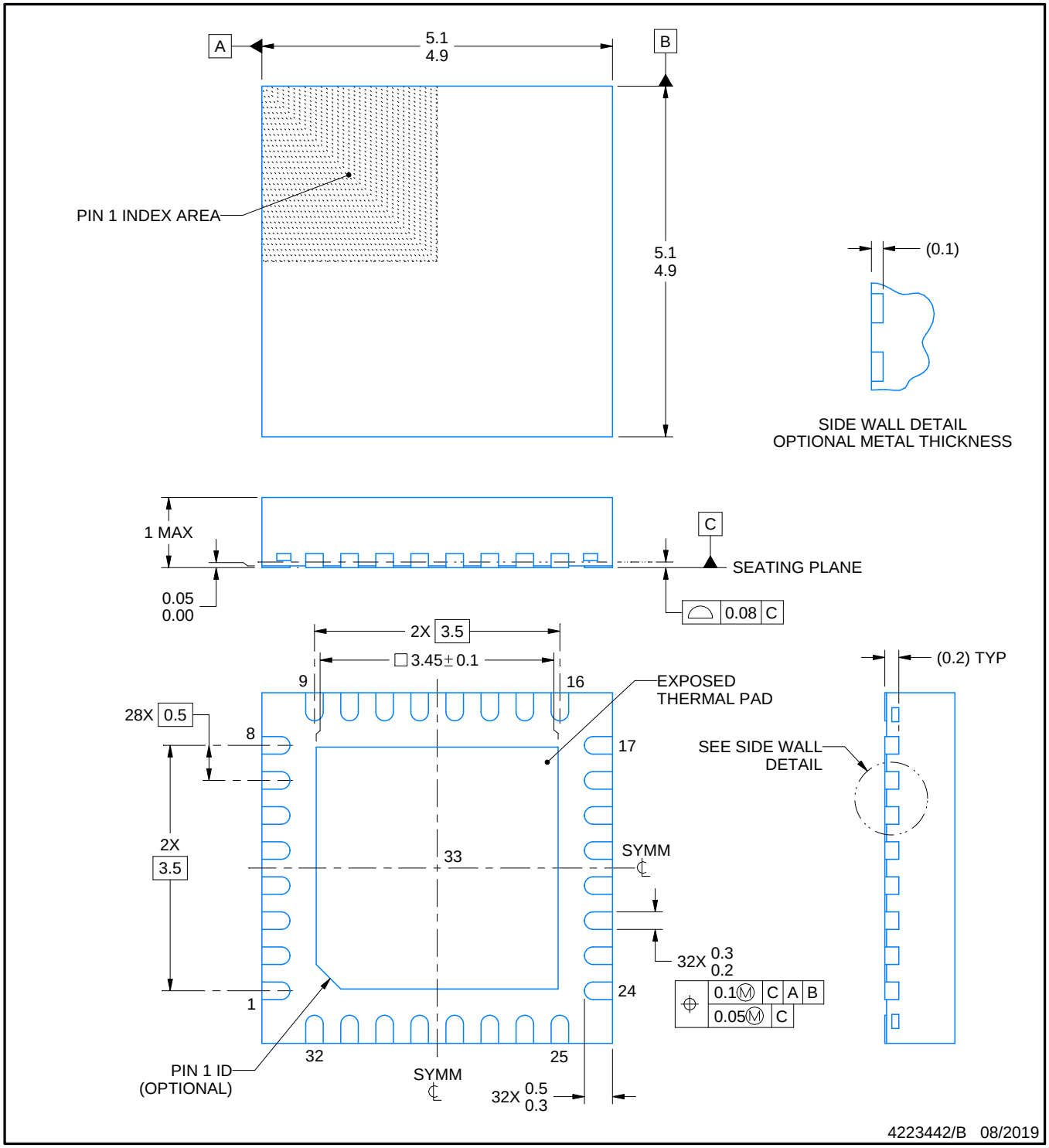
4224745/A

RHB0032E

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

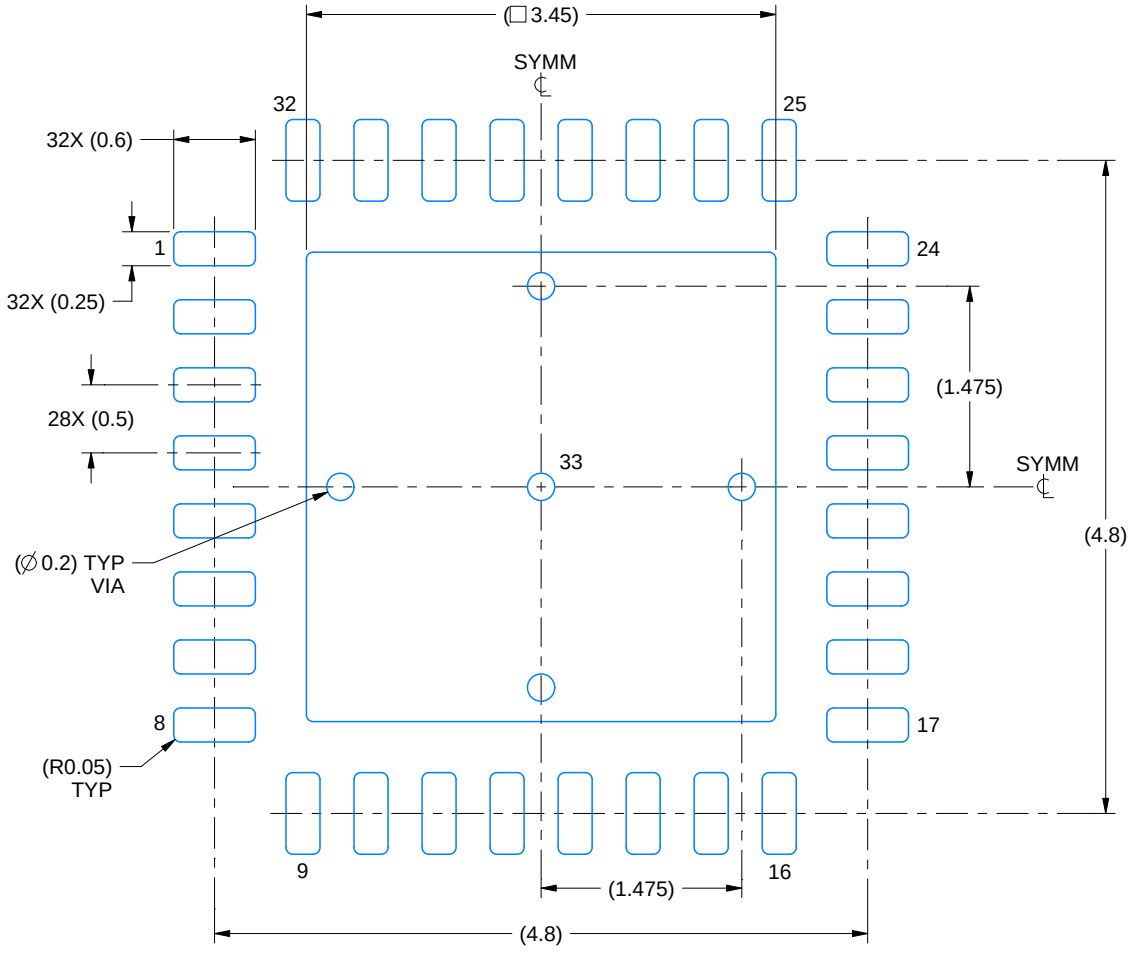
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

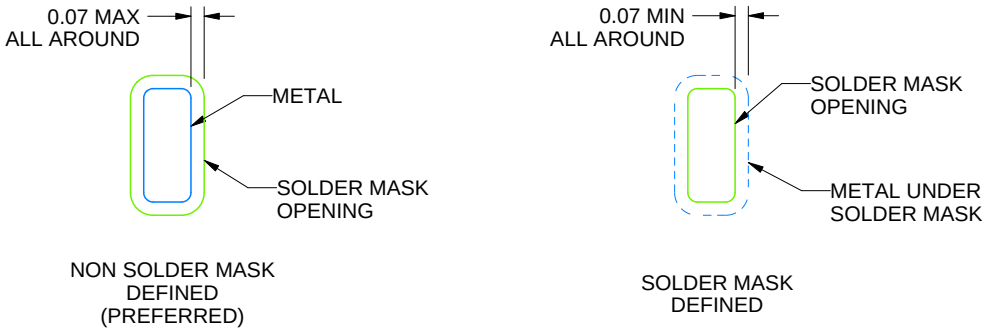
RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:18X

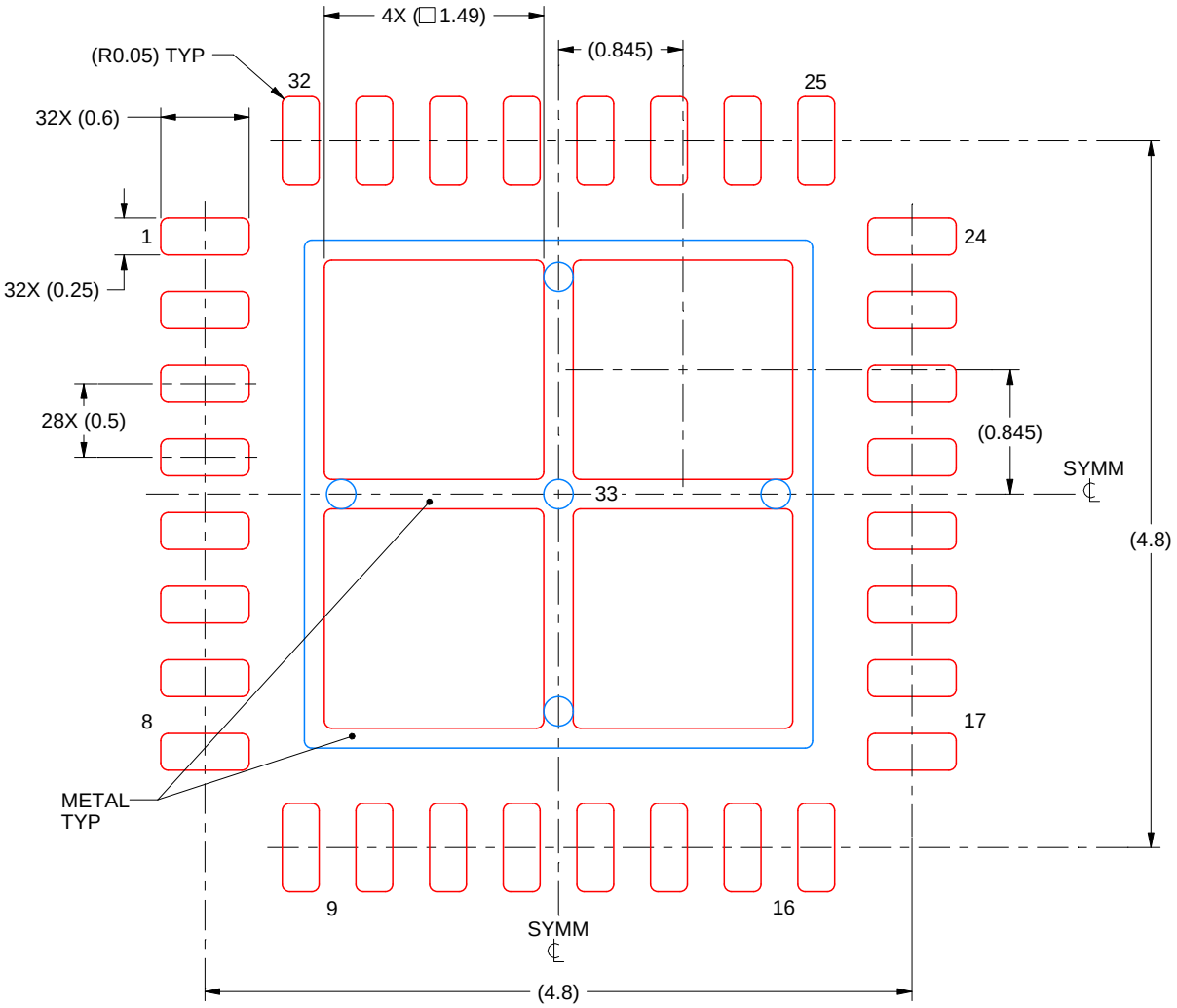


SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

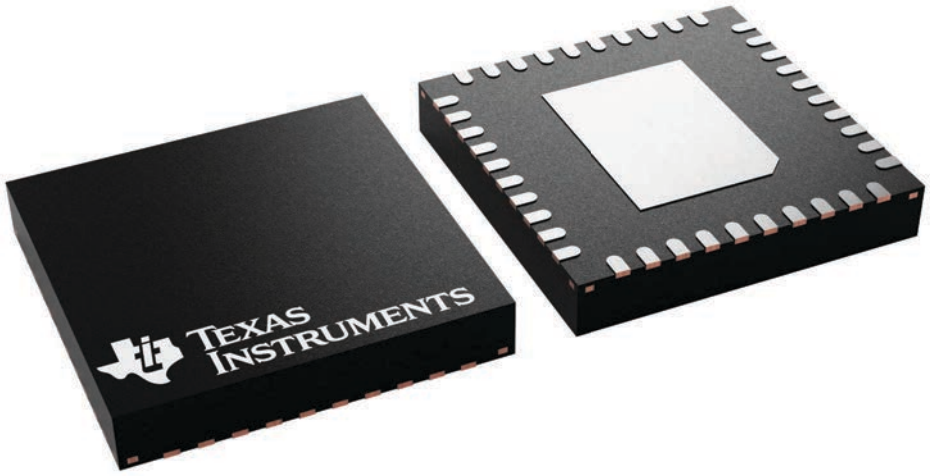
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



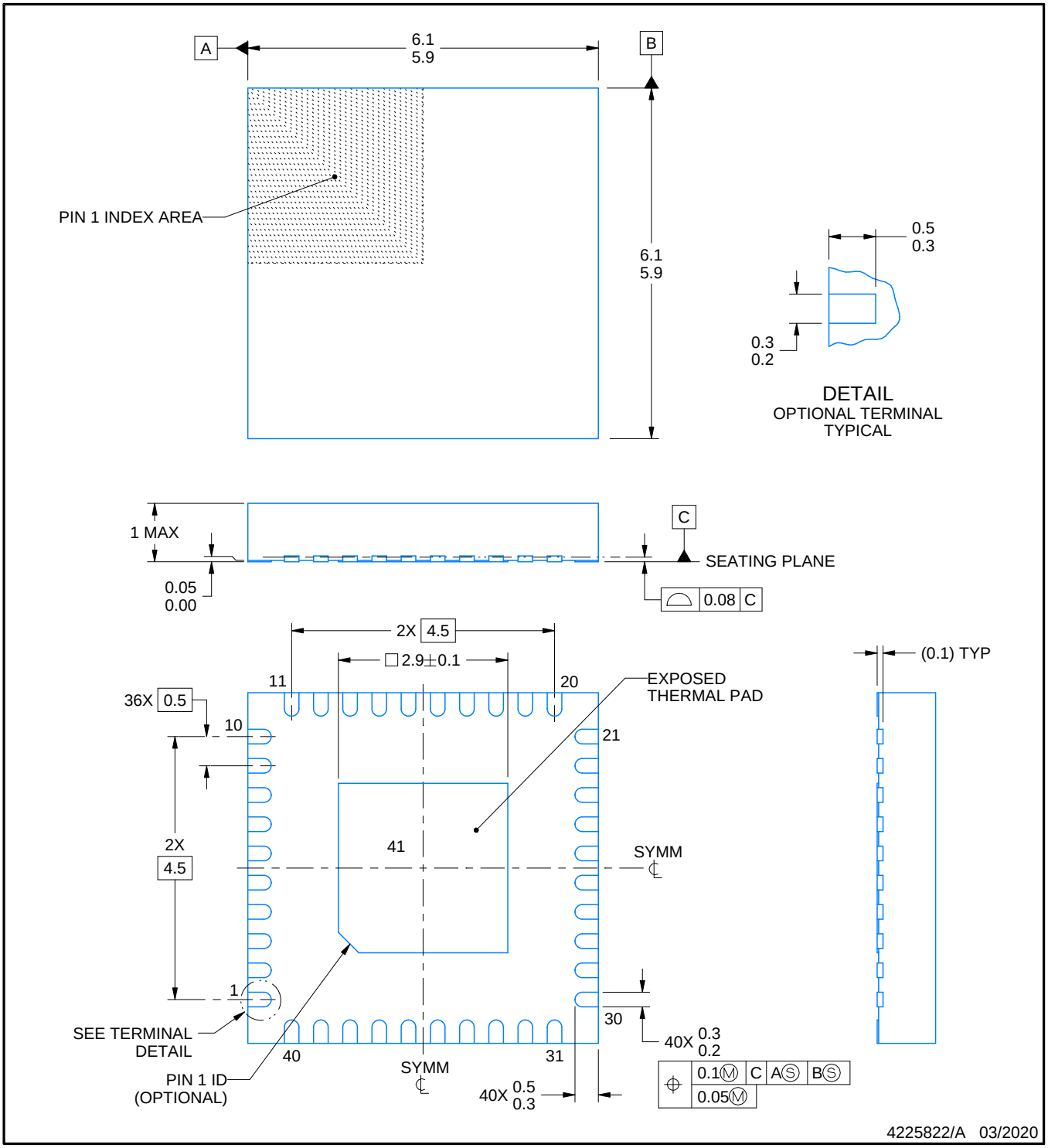
4225870/A

PACKAGE OUTLINE

RHA0040D

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

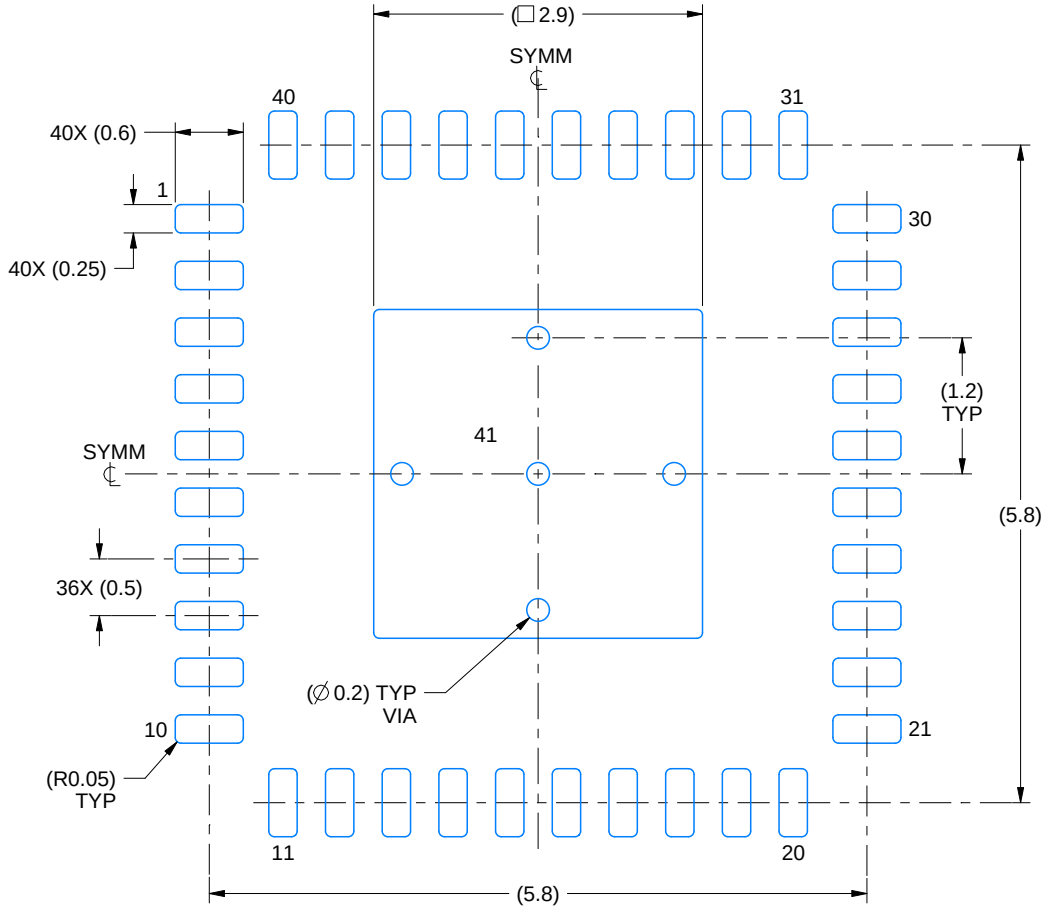
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

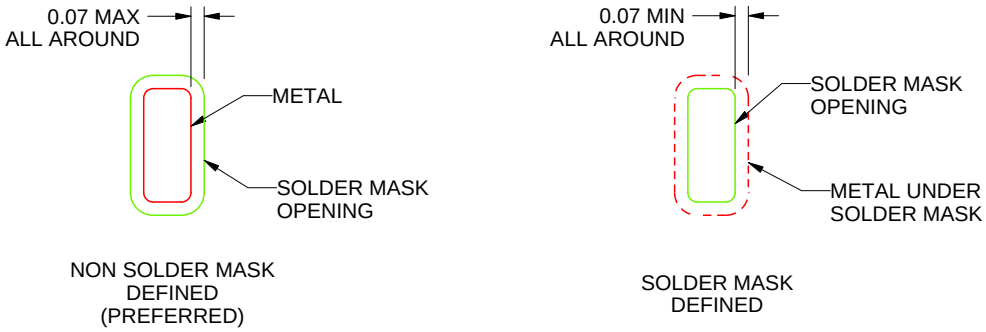
RHA0040D

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:15X

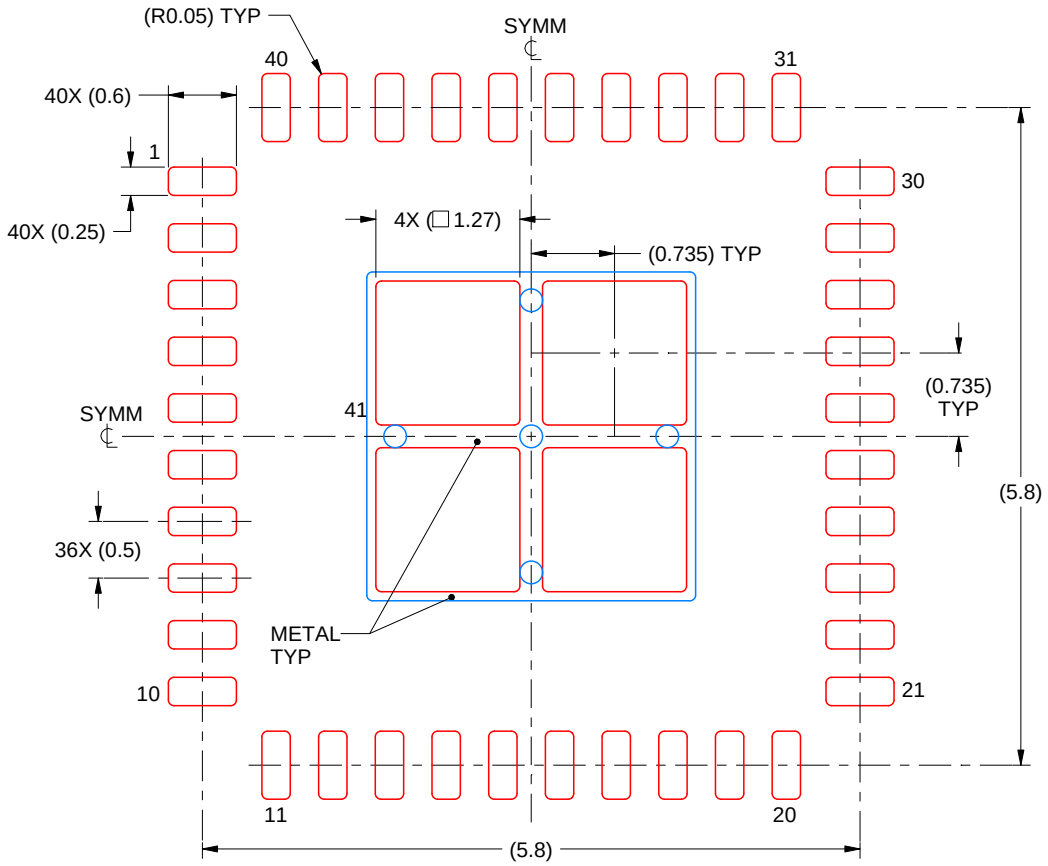


SOLDER MASK DETAILS

4225822/A 03/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
76.46% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4225822/A 03/2020

NOTES: (continued)

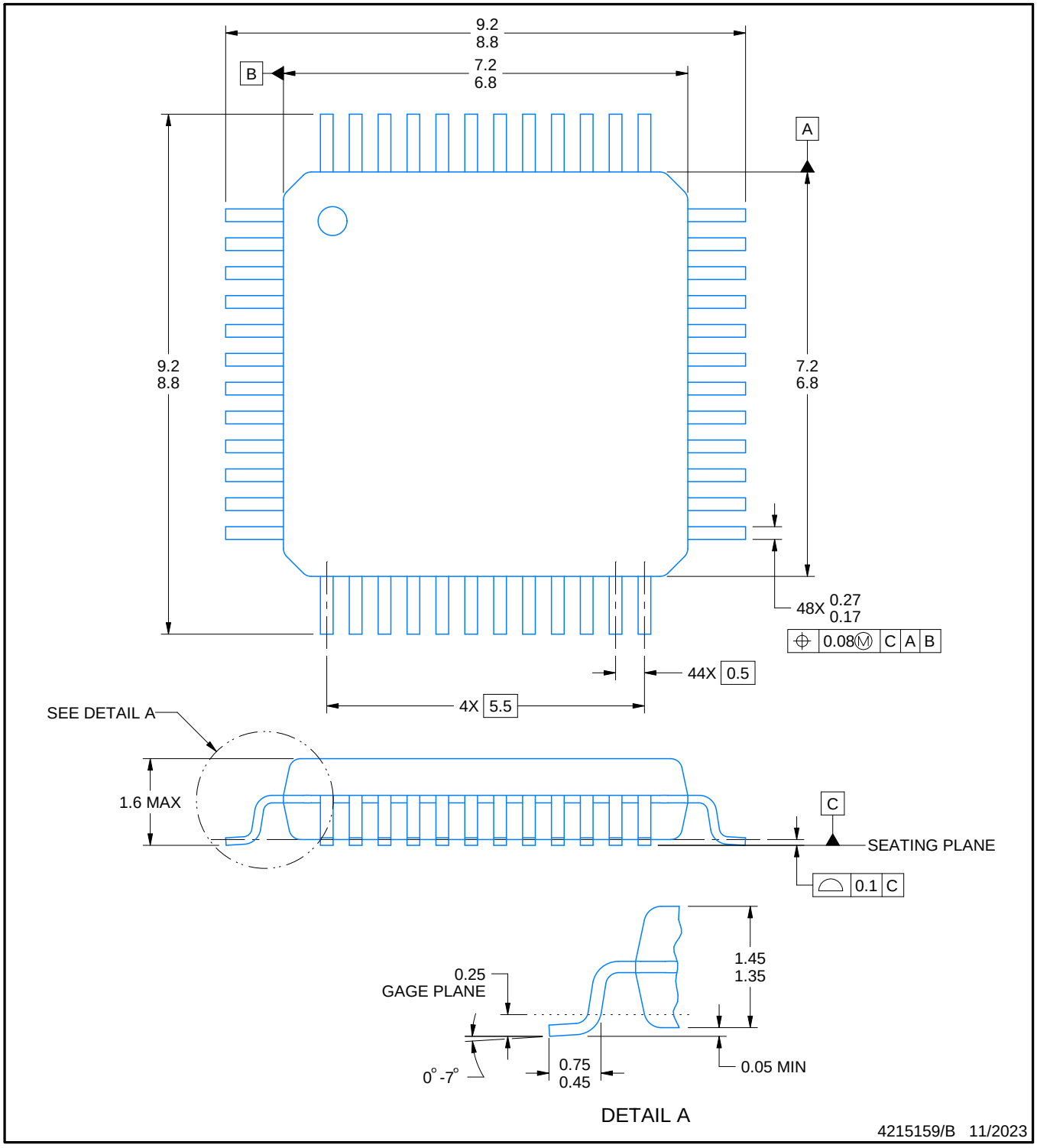
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PT0048A

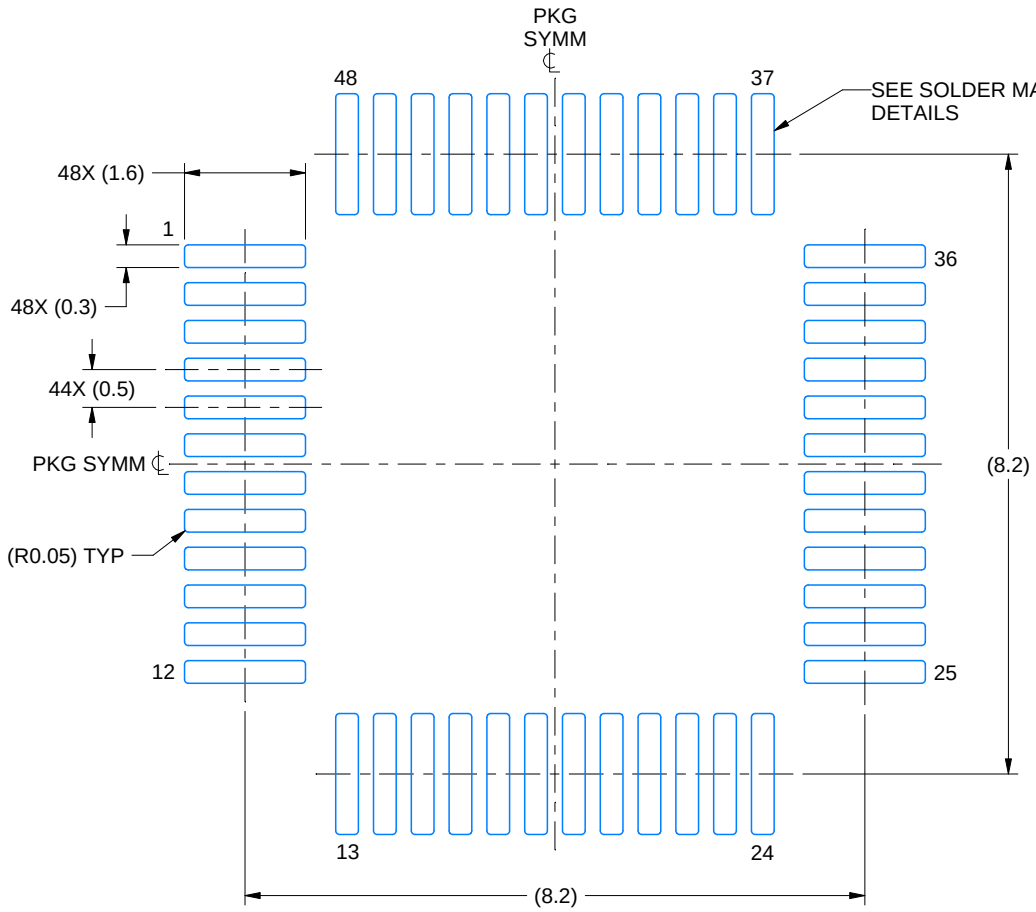
LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK

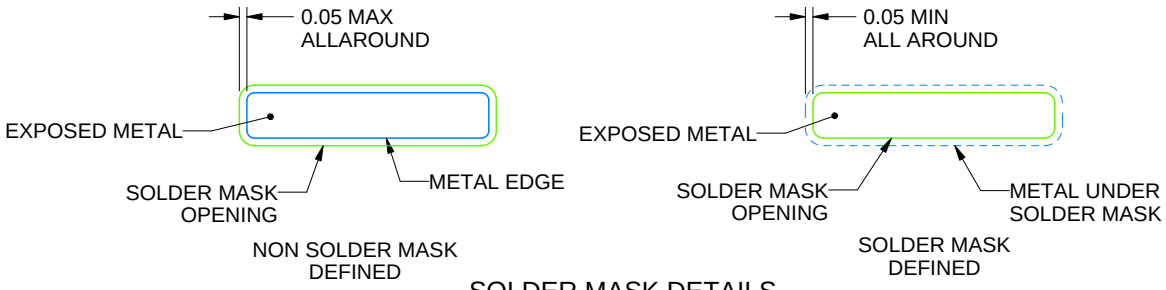


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000

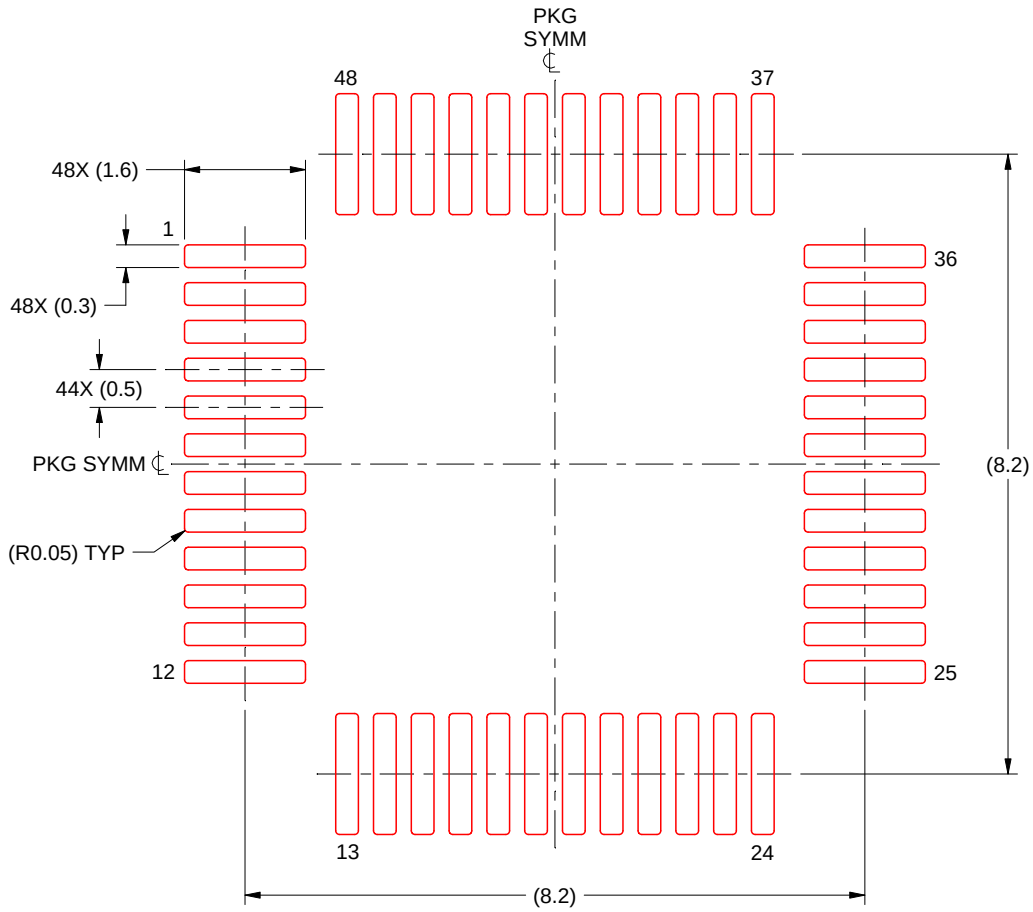


SOLDER MASK DETAILS

4215159/B 11/2023

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4215159/B 11/2023

NOTES: (continued)

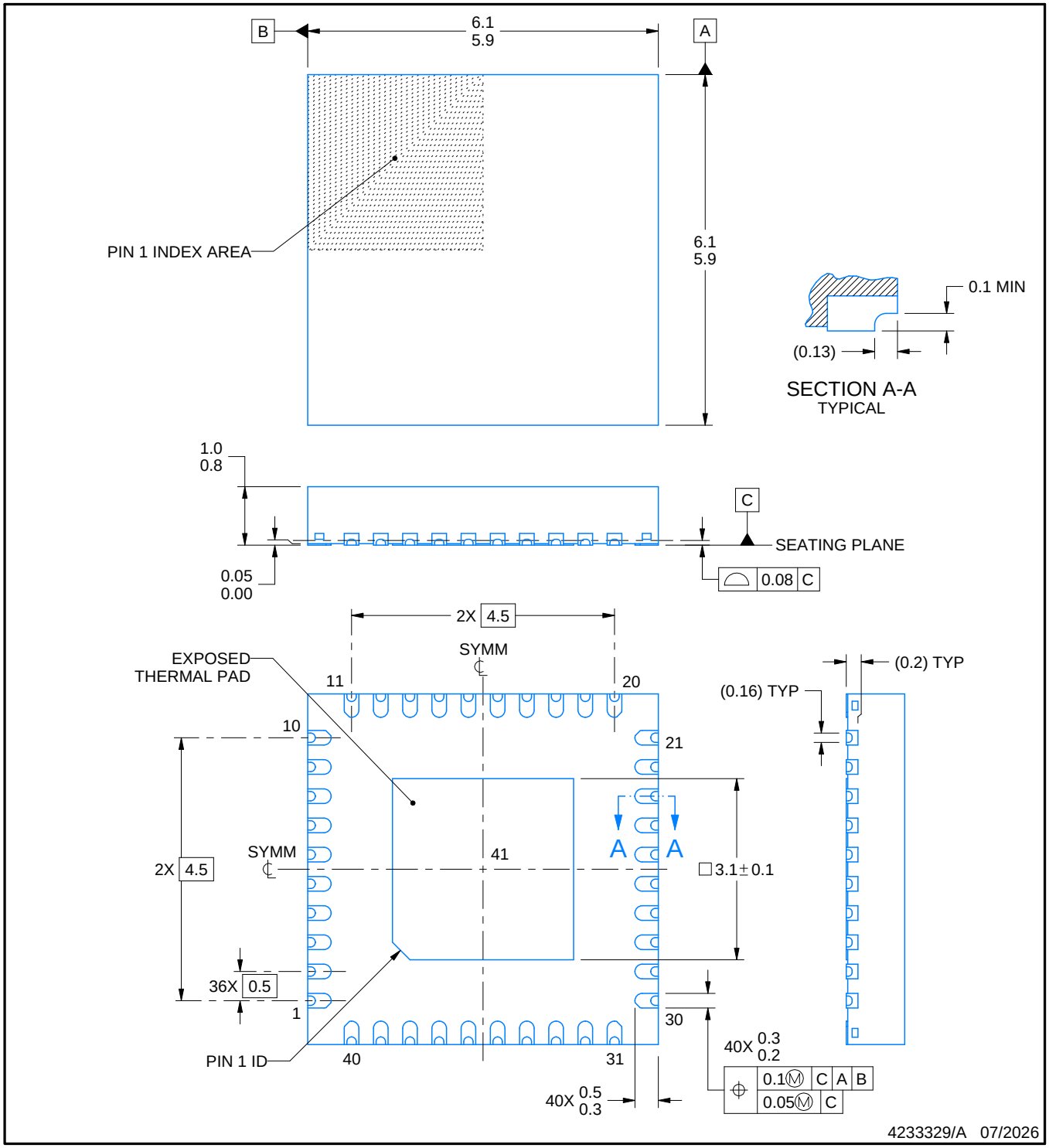
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

RHA0040Y

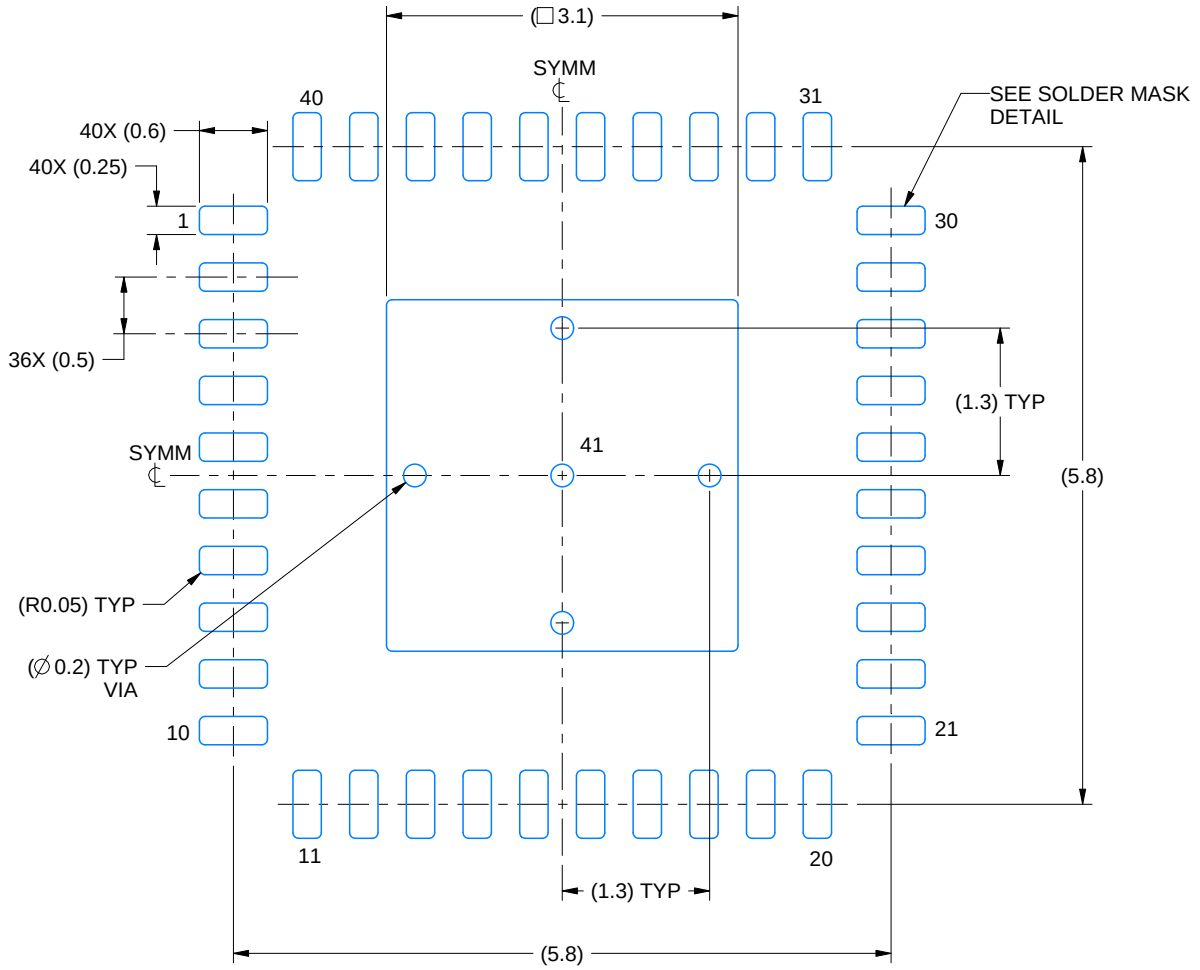
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

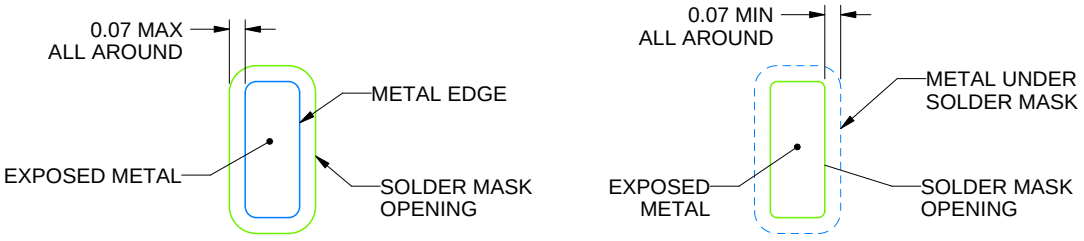


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4233329/A 07/2026

NOTES: (continued)

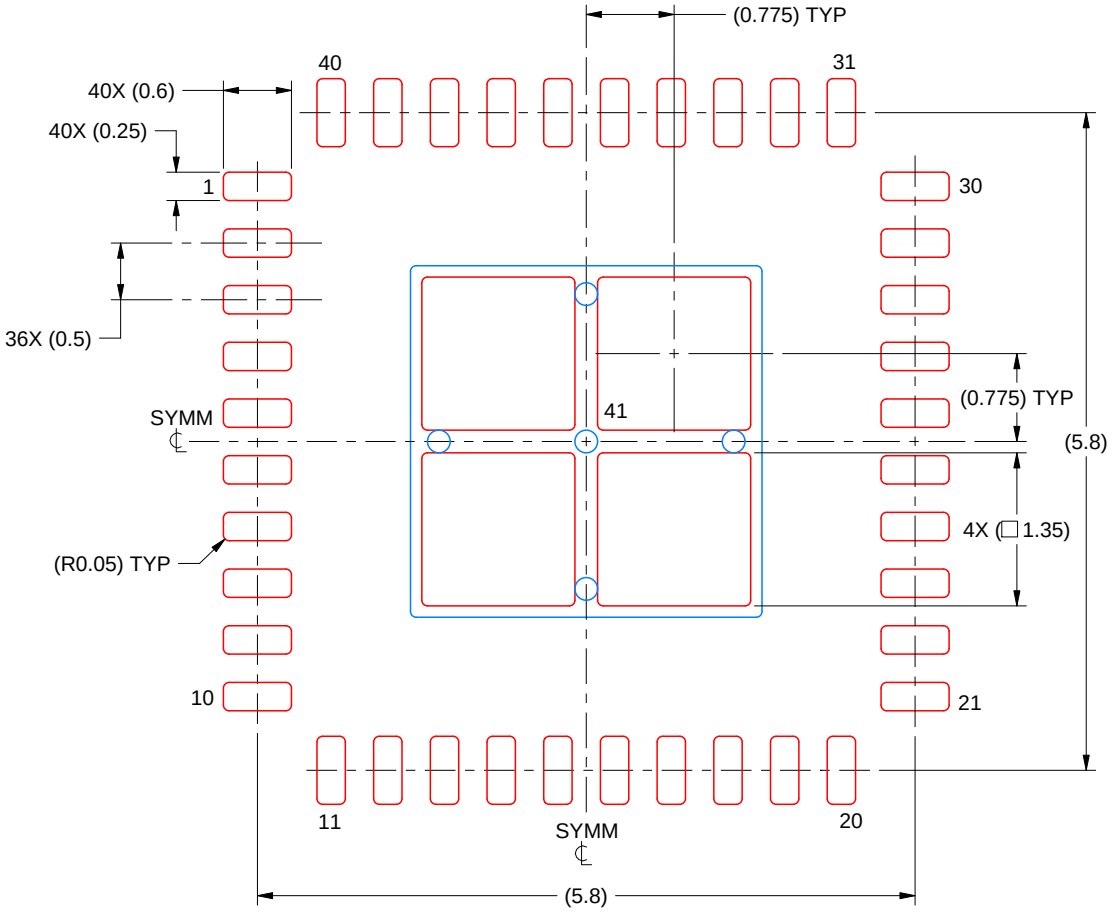
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHA0040Y

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 41
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4233329/A 07/2026

NOTES: (continued)

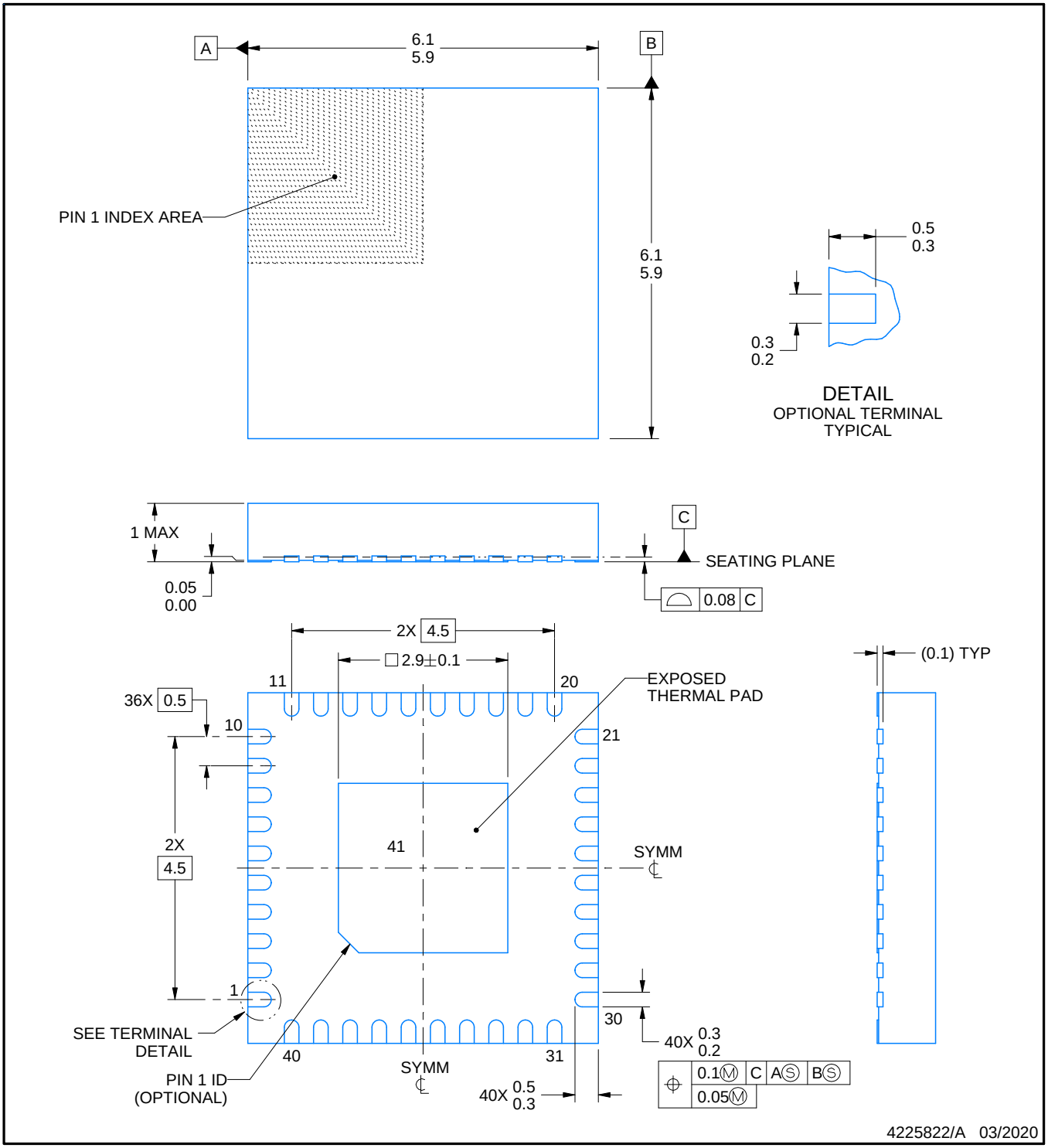
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RHA0040D

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

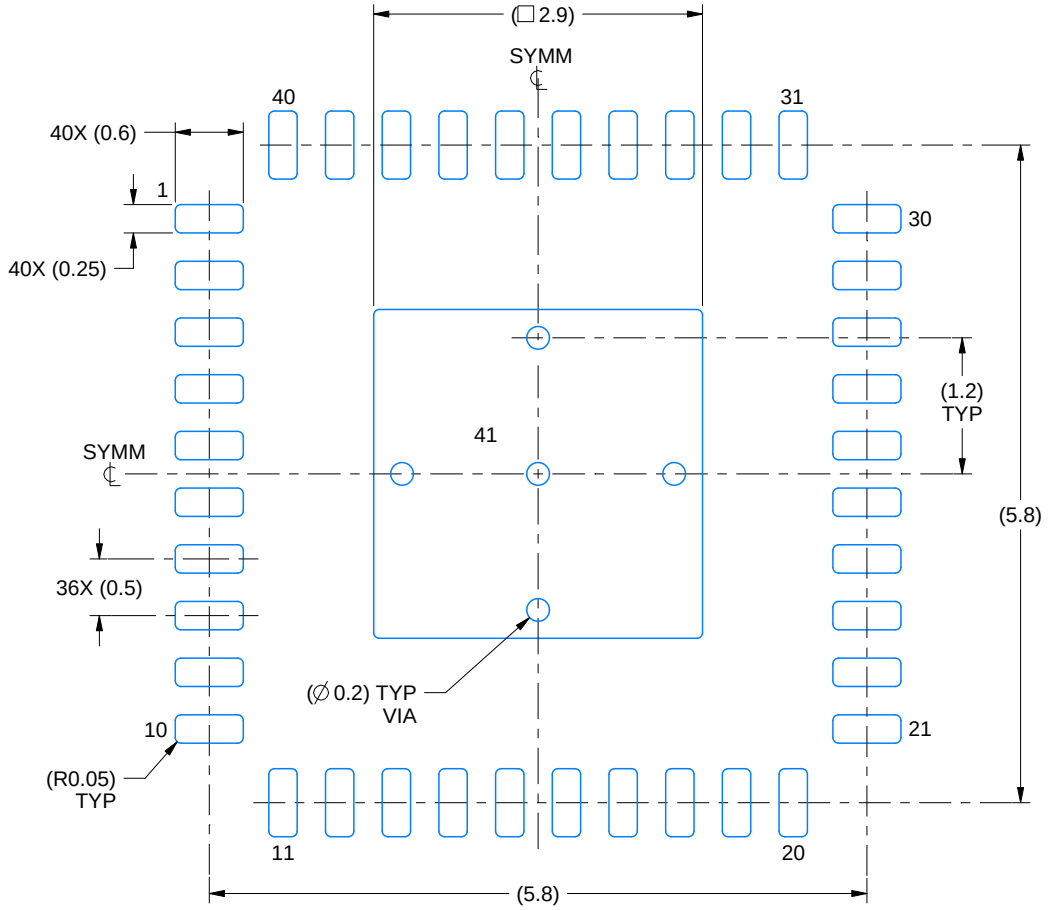
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

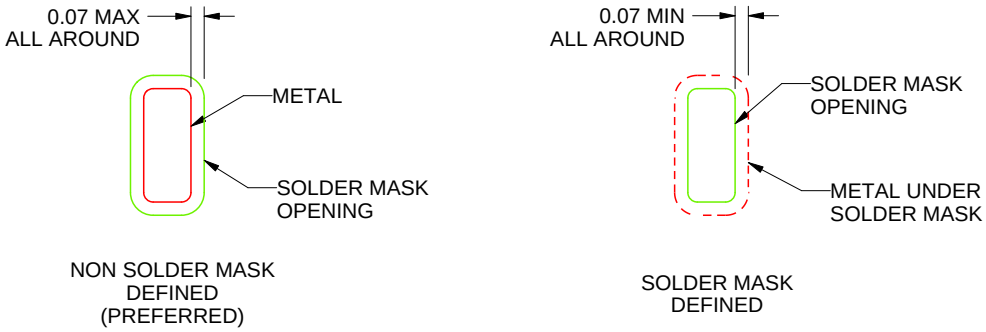
RHA0040D

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:15X

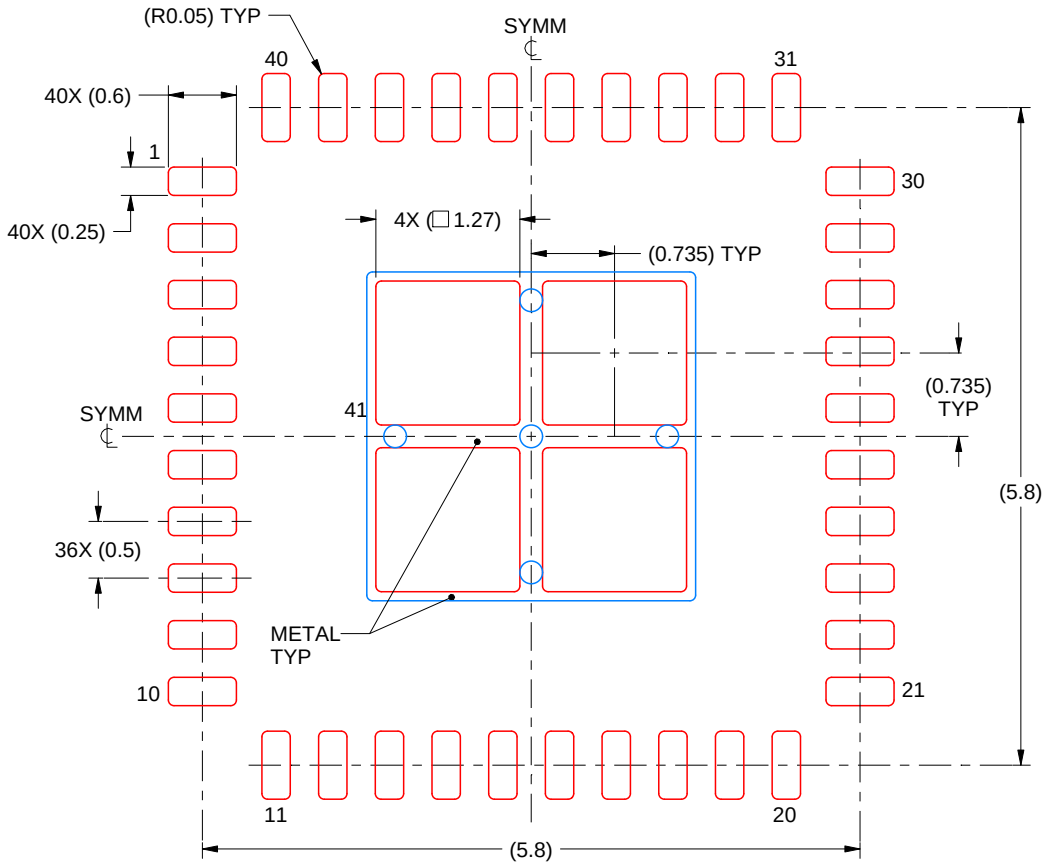


SOLDER MASK DETAILS

4225822/A 03/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
76.46% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4225822/A 03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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