11.3 Gbps Limiting Amplifier

Check for Samples: ONET1151P

FEATURES

- Up to 11.3 Gbps Operation
- Two-Wire Digital Interface
- Adjustable LOS Threshold
- Digitally Selectable Output Voltage
- Digitally Selectable Output De-Emphasis
- Adjustable Input Threshold Voltage
- Output Polarity Select
- Programmable LOS Masking Time
- Input Offset Cancellation
- CML Data Outputs with On-Chip 50-Ω Back-Termination to VCC
- Single +3.3-V Supply
- Low Power Consumption
- Output Disable
- Surface Mount Small Footprint 3 mm × 3 mm 16-Pin RoHS Compliant QFN Package
- Pin Compatible to the ONET8501PB

APPLICATIONS

- 10 Gigabit Ethernet Optical Receivers
- 2x/4x/8x and 10x Fibre Channel Optical Receivers
- SONET OC-192/SDH-64 Optical Receivers
- SFP+ and XFP Transceiver Modules
- Cable Driver and Receiver

DESCRIPTION

The ONET1151P is a high-speed, 3.3-V limiting amplifier for multiple fiber optic and copper cable applications with data rates up to 11.3 Gbps.

The device provides a two-wire serial interface which allows digital control of the output amplitude, output pre-emphasis, input threshold voltage (slice level) and the loss of signal assert level.

The ONET1151P provides a gain of about 33dB which ensures a fully differential output swing for input signals as low as 20 mV_{p-p}. The output amplitude can be adjusted between 350 mV_{p-p} and 850 mV_{p-p}. To compensate for frequency dependent loss of microstrips or striplines connected to the output of the device, programmable de-emphasis is included in the output stage. A settable loss of signal (LOS) detection with programmable output masking time and output disable are also provided.

The part, available in RoHS compliant small footprint 3 mm x 3 mm 16-pin QFN package, typically dissipates 132 mW with 550 mV_{p-p} output and is characterized for operation from −40°C to 100°C.

BLOCK DIAGRAM

A simplified block diagram of the ONET1151P is shown in Figure 1.

This compact, low power 11.3 Gbps limiting amplifier consists of a high-speed data path with offset cancellation block (DC feedback) combined with an analog settable input threshold adjust, a loss of signal detection block using 2 peak detectors, a two-wire interface with a control-logic block and a bandgap voltage reference and bias current generation block.

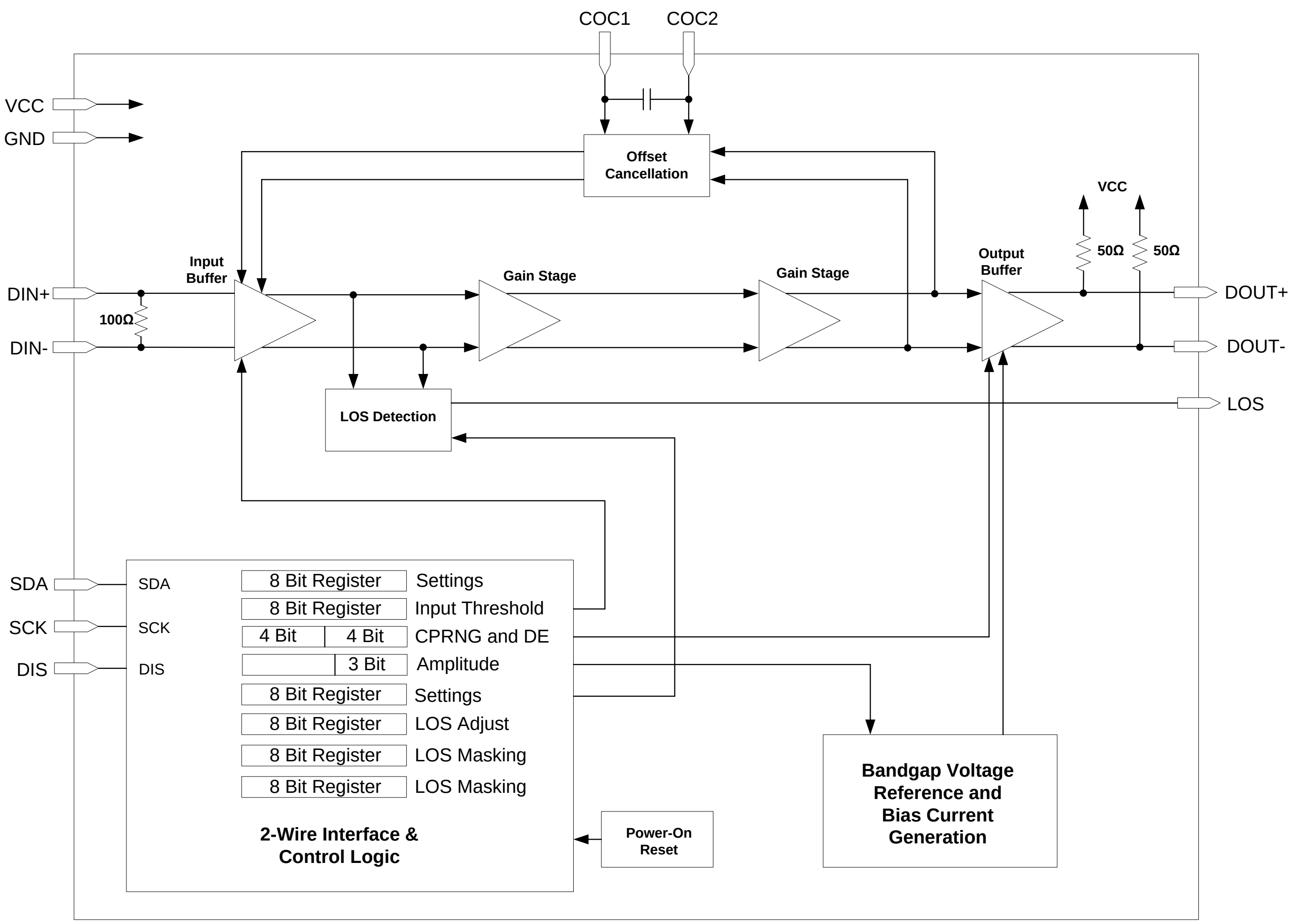

Figure 1. Simplified Block Diagram of the ONET1151P

PACKAGE

The ONET1151P is available in a small footprint 3 mm × 3 mm 16-pin RoHS compliant QFN package with a lead pitch of 0.5 mm. The pinout is shown in Figure 2.

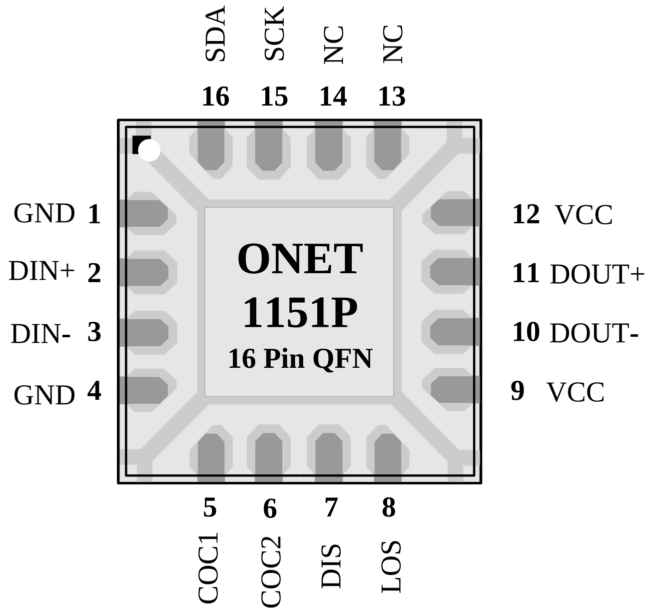

Figure 2. Pinout of ONET1151P in a 3mm x 3mm 16-Pin QFN Package (Top View)

Table 1. PIN DESCRIPTIONS

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	1, 4, EP	Supply	Circuit ground. Exposed die pad (EP) must be grounded.
DIN+	2	Analog-input	Non-inverted data input. Differentially 100 Ω terminated to DIN–.
DIN–	3	Analog-input	Inverted data input. Differentially 100 Ω terminated to DIN+.
COC1	5	Analog	Offset cancellation filter capacitor plus terminal. An external capacitor can be connected between this pin and COC2 to reduce the low frequency cutoff. To disable the offset cancellation loop, connect COC1 and COC2 together.
COC2	6	Analog	Offset cancellation filter capacitor minus terminal. An external capacitor can be connected between this pin and COC1 to reduce the low frequency cutoff. To disable the offset cancellation loop, connect COC1 and COC2 together.
DIS	7	Digital-input	Disables the output stage when set to a high level.
LOS	8	Open drain MOS	High level indicates that the input signal amplitude is below the programmed threshold level. Open drain output. Requires an external 10kΩ pull-up resistor to VCC for proper operation.
VCC	9, 12	Supply	3.3-V supply voltage.
DOUT–	10	CML-out	Inverted data output. On-chip 50 Ω back-terminated to VCC.
DOUT+	11	CML-out	Non-inverted data output. On-chip 50 Ω back-terminated to VCC.
NC	13, 14	No Connect	Do not connect
SCK	15	Digital-input	Serial interface clock input. Connect a pull-up resistor (10 kΩ typical) to VCC.
SDA	16	Digital-input	Serial interface data input. Connect a pull-up resistor (10 kΩ typical) to VCC.

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

PARAMETER		VALUE		UNIT
		MIN	MAX	
V_{CC}	Supply voltage[2]	–0.3	4	V
V_{DIN+}, $V_{DIN–}$	Voltage at DIN+, DIN– [2]	0.5	4	V
V_{LOS}, V_{COC1}, V_{COC2}, V_{DOUT+}, $V_{DOUT–}$, V_{DIS}, V_{SDA}, V_{SCK}	Voltage at LOS, COC1, COC2, DOUT+, DOUT-, DIS, SDA, SCK[2]	–0.3	4.0	V
$V_{DIN,\ DIFF}$	Differential voltage between DIN+ and DIN–		±2.5	V
I_{DIN+}, $I_{DIN–}$, I_{DOUT+}, $I_{DOUT–}$	Continuous current at inputs and outputs		25	mA
ESD	ESD rating at all pins		2	kV (HBM)
T_A	Characterized free-air operating temperature range	–40	100	°C
$T_{J,\ max}$	Maximum junction temperature		125	°C
T_{STG}	Storage temperature range	–65	150	°C
T_C	Case temperature	–40	110	°C
T_{LEAD}	Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage	T_A = –40°C to +100°C	2.9	3.3	3.63	V
		T_A = –30°C to +100°C	2.85	3.3	3.63	
T_A	Operating free-air temperature		–40		100	°C
	DIGITAL input high voltage		2.0			V
	DIGITAL input low voltage				0.8	V

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions with 50-Ω output load, 550 mV_{p-p} output voltage and BIAS bit (Register 7) set to 1, unless otherwise noted. Typical operating condition is at 3.3 V and T_A = 25°C

PARAMETER		TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage	T_A = –40°C to +100°C	2.9	3.3	3.63	V
		T_A = –30°C to +100°C	2.85	3.3	3.63	
I_{VCC}	Supply current	DIS = 0, CML currents included		40	52	mA
R_{IN}	Data input resistance	Differential		100		Ω
R_{OUT}	Data output resistance	Single-ended, referenced to V_{CC}		50		Ω
	LOS HIGH voltage	I_{SOURCE} = 50 µA with 10 kΩ pull-up to V_{CC}	2.3			V
	LOS LOW voltage	I_{SINK} = 10 mA with 10 kΩ pull-up to V_{CC}			0.4	V

AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions with 50-Ω output load, 550mVpp output voltage and BIAS bit (Register 7) set to 1, unless otherwise noted. Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C.

PARAMETER		TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
f3dB-H	-3dB bandwidth default settings		7.5	9.5		GHz
f3dB-L	Low frequency -3dB bandwidth	With 330 pF COC capacitor		10	45	kHz
$V_{IN,MIN}$	Data input sensitivity	PRBS31 pattern at 11.3 Gbps, BER < 10^{-12}		6	9	mV_{p-p}
		V_{OD-min} ≥ 0.95 * V_{OD} (output limited)		20	40	
SDD11	Differential input return gain	0.01 GHz < f < 5 GHz		–15		dB
		5 GHz < f < 12.1 GHz		–8		
SDD22	Differential output return gain	0.01 GHz < f < 5 GHz		–15		dB
		5 GHz < f < 12.1 GHz		–8		
SCD11	Differential to common mode conversion gain	0.01 GHz < f < 12.1 GHz		–15		dB
SCC22	Common mode output return gain	0.01 GHz < f < 5 GHz		–13		dB
		5 GHz < f < 12.1 GHz		–9		
A	Small signal gain		26	33		dB
V_{IN-MAX}	Data input overload	BIAS (Reg7 bit 0) set to 1	2000			mV_{p-p}
DJ	Deterministic jitter at 11.3 Gbps	V_{IN} = 15 mV_{p-p}, K28.5 pattern		3	8	ps_{p-p}
		V_{IN} = 30 mV_{p-p}, K28.5 pattern		3	10	
		V_{IN} = 2000 mV_{p-p}, K28.5 pattern		6	15	
RJ	Random jitter	V_{IN} = 30 mV_{p-p}		1		ps_{rms}
V_{OD}	Differential data output voltage	V_{IN} > 30 mV_{p-p}, DIS = 0, AMP[0..2] = 000		380		mV_{p-p}
		V_{IN} > 30 mV_{p-p}, DIS = 0, AMP[0..2] = 111		820		
		DIS = 1			5	mV_{rms}
V_{PREEM}	Output de-emphasis step size			1		dB
t_R	Output rise time	20% – 80%, V_{IN} > 30 mV_{p-p}		30	40	ps
t_F	Output fall time	20% – 80%, V_{IN} > 30 mV_{p-p}		30	40	ps
CMOV	AC common mode output voltage	PRBS31 pattern; AMP[0..2] = 010			7	mV_{rms}
V_{TH}	LOW LOS assert threshold range min.	K28.5 pattern at 11.3 Gbps, LOSRNG = 0		15		mV_{p-p}
	LOW LOS assert threshold range max.	K28.5 pattern at 11.3 Gbps, LOSRNG = 0		35		
V_{TH}	HIGH LOS assert threshold range min.	K28.5 pattern at 11.3 Gbps, LOSRNG = 1		35		mV_{p-p}
	HIGH LOS assert threshold range max.	K28.5 pattern at 11.3 Gbps, LOSRNG = 1		80		
	LOS threshold variation	Versus temperature at 11.3 Gbps		1.5		dB
		Versus supply voltage VCC at 11.3 Gbps		1		dB
		Versus data rate		1.5		dB
	LOS hysteresis (electrical)	K28.5 pattern at 11.3 Gbps	2	4	6.5	dB
T_{LOS_AST}	LOS assert time		2.5	10	80	µs
T_{LOS_DEA}	LOS deassert time		2.5	10	80	µs
	Maximum LOS output masking time		2000			µs
	LOS masking time step size			32		µs
T_{DIS}	Disable response time			20		ns

DETAILED DESCRIPTION

HIGH-SPEED DATA PATH

The high-speed data signal is applied to the data path by means of input signal pins DIN+ / DIN–. The data path consists of a 100-Ω differential termination resistor followed by an input buffer. A gain stage and an output buffer stage follow the input buffer, which together provide a gain of 33dB. The device can accept input amplitude levels from 6mV$_{p-p}$ up to 2000mV$_{p-p}$. The amplified data output signal is available at the output pins DOUT+ / DOUT– which include on-chip 2 × 50-Ω back-termination to VCC.

Offset cancellation compensates for internal offset voltages and thus ensures proper operation even for very small input data signals. The offset cancellation can be disabled so that the input threshold voltage can be adjusted to optimize the bit error rate or change the eye crossing to compensate for input signal pulse width distortion. The offset cancellation can be disabled by setting OCDIS = 1 (bit 1 of register 0). The input threshold level can be adjusted using register settings THADJ[0..7] (register 1). When register 1 is set to 0x00, the threshold adjustment circuitry is disabled to reduce the supply current. Setting register 1 to any other value will enable the circuitry and the supply current will increase by approximately 2 mA. The amount of adjustment that register 1 can provide is controlled by the CPRNG[1..0] bits (register 2). For details regarding input threshold adjust and range, see Table 12.

The low frequency cutoff is as low as 80 kHz with the built-in filter capacitor. For applications, which require even lower cutoff frequencies, an additional external filter capacitor may be connected to the COC1 and COC2 pins. A value of 330 pF results in a low frequency cutoff of 10 kHz.

The receiver can be optimized for various applications using the settings in register 7. To enable the settings, set the SEL bit (bit 7 of register 7) to 1. It is recommended that the BIAS bit (bit 0 of register 7) be set to 1, especially if the input voltage to the ONET1151P will exceed about 500 mV$_{p-p}$ differential. Setting BIAS to 1 adds 2 mA of bias current to the input stage, making it more robust for high input voltages. For input voltages lower than 500 mV$_{p-p}$, as typically would be supplied from a transimpedance amplifier (TIA), BIAS can be set to 0 to reduce the supply current. In addition, the RXOPT[1..0] bits (register 7) can be used to optimize the jitter based upon the TIA that is used. When RXOPT is set to 00, there is some input equalization set at the input to the limiting amplifier. This is a good general setting to use and for most applications it is recommended to set register 7 to 0x81. If the input voltage to the limiting amplifier does not exceed about 500 mV$_{p-p}$ differential, then the jitter may be reduced by setting register 7 to 0x85.

BANDGAP VOLTAGE AND BIAS GENERATION

The ONET1151P limiting amplifier is supplied by a single +3.3-V supply voltage connected to the VCC pins. This voltage is referred to ground (GND).

On-chip bandgap voltage circuitry generates a reference voltage, independent of supply voltage, from which all other internally required voltages and bias currents are derived.

HIGH-SPEED OUTPUT BUFFER

The output amplitude of the buffer can be varied from 350 mV$_{p-p}$ to 850 mV$_{p-p}$ using the register settings AMP[0..2] (register 3) via the serial interface. The default amplitude setting is AMP[0..2] = 010 which provides 550 mV$_{p-p}$ differential output voltage. To compensate for frequency dependant losses of transmission lines connected to the output, the ONET1151P has adjustable de-emphasis of the output stage. The de-emphasis can be set from 0 to 8dB in 1dB steps using register settings DEADJ[0..3] (register 2).

In addition, the polarity of the output pins can be inverted by setting the output polarity switch bit, POL (bit 4 of register 0) to 1.

LOSS OF SIGNAL DETECTION

The loss of signal detection is done by 2 separate level detectors to cover a wide dynamic range. The peak values of the input signal and the output signal of the gain stage are monitored by the peak detectors. The peak values are compared to a pre-defined loss of signal threshold voltage inside the loss of signal detection block. As a result of the comparison, the LOS signal, which indicates that the input signal amplitude is below the defined threshold level, is generated. The LOS assert level is settable through the serial interface. There are 2 LOS ranges settable with the LOSRNG bit (bit 2 register 0). By setting LOSRNG = 1, the high range of the LOS assert values are used (35 mV_{p-p} to 80 mV_{p-p}) and by setting LOSRNG = 0, the low range of the LOS assert values are used (15 mV_{p-p} to 35 mV_{p-p}).

There are 128 possible internal LOS settings (7bit) for each LOS range to adjust the LOS assert level. If the LOS register selection bit is set low, LOSSEL = 0 (bit 7 of register 11), then the default LOS assert level of approximately 25 mV_{p-p} is used. If the register selection bit is set high, LOSSEL = 1 (bit 7 of register 11), then the content of LOS[0..6] (register 11) is used to set the LOS assert level.

An LOS output masking time can be enabled on the raising and falling edges of the LOS output signal. The LOS rising edge masking time is enabled by setting LOSTMRENA = 1 (bit 7 of register 13) and the time programmed using LOSTMR[0..6] (register 13). The LOS falling edge masking time is enabled by setting LOSTMFENA = 1 (bit 7 of register 12) and the time programmed using LOSTMF[0..6] (register 12).This feature is used to mask a false input to the limiting amplifier after a loss of signal has occurred or when the input signal is re-applied. The masking time can be set from 10 µs to 2 ms.

2-WIRE INTERFACE AND CONTROL LOGIC

The ONET1151P uses a 2-wire serial interface for digital control. The two circuit inputs, SDA and SCK, are driven, respectively, by the serial data and serial clock from a microcontroller, for example. Both inputs include 100-kΩ pull-up resistors to VCC. For driving these inputs, an open drain output is recommended.

The 2-wire interface allows write access to the internal memory map to modify control registers and read access to read out control and status signals. The ONET1151P is a slave device only which means that it can not initiate a transmission itself; it always relies on the availability of the SCK signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The protocol for a data transmission is as follows:

1. START command
2. 7 bit slave address (1000100) followed by an eighth bit which is the data direction bit (R/W). A zero indicates a WRITE and a 1 indicates a READ.
3. 8-bit register address
4. 8-bit register data word
5. STOP command

Regarding timing, the ONET1151P is I^2C compatible. The typical timing is shown in Figure 3 and complete data transfer is shown in Figure 4. Parameters for Figure 3 are defined in Table 2.

Bus Idle: Both SDA and SCK lines remain HIGH.

Start Data Transfer: A change in the state of the SDA line, from HIGH to LOW, while the SCK line is HIGH, defines a START condition (S). Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from LOW to HIGH while the SCK line is HIGH defines a STOP condition (P). Each data transfer is terminated with a STOP condition; however, if the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

Data Transfer: Only one data byte can be transferred between a START and a STOP condition. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver doesn't acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

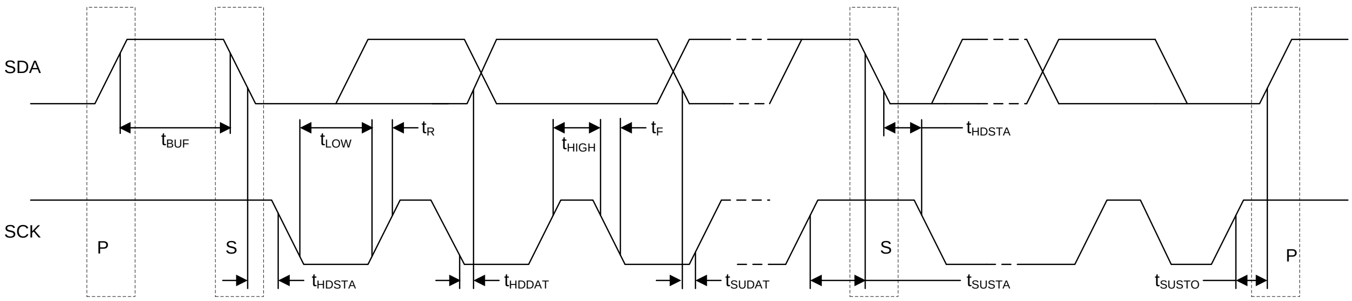

Figure 3. I^2C Timing Diagram

Table 2. Timing Diagram Definitions

Parameter	Symbol	Min	Max	Unit
SCK clock frequency	f_{SCK}		400	kHz
Bus free time between STOP and START conditions	t_{BUF}	1.3		µs
Hold time after repeated START condition. After this period, the first clock pulse is generated	t_{HDSTA}	0.6		µs
Low period of the SCK clock	t_{LOW}	1.3		µs
High period of the SCK clock	t_{HIGH}	0.6		µs
Setup time for a repeated START condition	t_{SUSTA}	0.6		µs
Data HOLD time	t_{HDDAT}	0		µs
Data setup time	t_{SUDAT}	100		ns
Rise time of both SDA and SCK signals	t_R		300	ns
Fall time of both SDA and SCK signals	t_F		300	ns
Setup time for STOP condition	t_{SUSTO}	0.6		µs

Write Sequence

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Register Address	A	Data Byte	A	P

Read Sequence

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	Wr	A	Register Address	A	S	Slave Address	Rd	A	Data Byte	N	P

Legend

S	Start Condition
Wr	Write Bit (bit value = 0)
Rd	Read Bit (bit value = 1)
A	Acknowledge
N	Not Acknowledge
P	Stop Condition

Figure 4. Data Transfer

REGISTER MAPPING

The register mapping for read/write register addresses 0 (0x00) through 13 (0x0D) are shown in Table 3 through Table 10. The register mapping for the read only register address 15 (0x0F) is shown in Table 11. Table 12 describes the circuit functionality based on the register settings.

Table 3. Register 0 (0x00) Mapping – Control Settings

Register Address 0 (0x00)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	CLKDIS	POL	DIS	LOSRNG	OCDIS	-

Table 4. Register 1 (0x01) Mapping – Input Threshold Adjust

Register Address 1 (0x01)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
THADJ7	THADJ6	THADJ5	THADJ4	THADJ3	THADJ2	THADJ1	THADJ0

Table 5. Register 2 (0x02) Mapping – Cross Point Range and De-emphasis Adjust

Register Address 2 (0x02)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	CPRNG1	CPRNG0	DEADJ3	DEADJ2	DEADJ1	DEADJ0

Table 6. Register 3 (0x03) Mapping – Output Amplitude Adjust

Register Address 3 (0x03)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	AMP2	AMP1	AMP0

Table 7. Register 7 (0x07) Mapping – Receiver Optimization

Register Address 7 (0x07)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SEL	-	-	-	RXOPT1	RXOPT0	-	BIAS

Table 8. Register 11 (0x0B) Mapping – LOS Assert Level

Register Address 11 (0x0B)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LOSSEL	LOSA6	LOSA5	LOSA4	LOSA3	LOSA2	LOSA1	LOSA0

Table 9. Register 12 (0x0C) Mapping – Falling Edge LOS Masking Register

Register Address 12 (0x0C)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LOSTMFENA	LOSTMF6	LOSTMF5	LOSTMF4	LOSTMF3	LOSTMF2	LOSTMF1	LOSTMF0

Table 10. Register 13 (0x0D) Mapping – Rising Edge LOS Masking Register

Register Address 13 (0x0D)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LOSTMRENA	LOSTMR6	LOSTMR5	LOSTMR4	LOSTMR3	LOSTMR2	LOSTMR1	LOSTMR0

Table 11. Register 15 (0x0F) Mapping – Selected LOS Level (Read Only)

Register Address 15 (0x0F)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
-	SELLOS6	SELLOS5	SELLOS4	SELLOS3	SELLOS2	SELLOS1	SELLOS0

Table 12. Register Functionality

Register	Bit	Symbol	Function
0	7	-	
	6	-	
	5	CLKDIS	**Disable I^2C clock**: 1 = clock disabled when DIS pin is high 0 = clock enabled
	4	POL	**Output polarity switch bit**: 1 = inverted polarity 0 = normal polarity
	3	DIS	**Output disable bit**: 1 = output disabled 0 = output enabled
	2	LOSRNG	**LOS range bit**: 1 = high LOS assert voltage range 0 = low LOS assert voltage range
	1	OCDIS	**Offset cancellation disable bit**: 1 = offset cancellation is disabled 0 = offset cancellation is enabled
	0	-	Reserved
1	7	THADJ7	**Input threshold adjustment setting**:
	6	THADJ6	Circuit disabled for 00000000 (0) – low supply current option
	5	THADJ5	Maximum positive shift for 00000001 (1)
	4	THADJ4	Minimum positive shift for 01111111 (127)
	3	THADJ3	Zero shift for 10000000 (128) – added supply current
	2	THADJ2	Minimum negative shift for 10000001 (129)
	1	THADJ1	Maximum negative shift for 11111111 (255)
	0	THADJ0	
2	7	-	
	6	-	
	5	CPRNG1	**Cross point range setting**: Minimum range for 00 Maximum range for 11
	4	CPRNG0	
	3	PEADJ3	**De-emphasis setting**:
	2	PEADJ2	0000 = 0dB 0100 = 3dB 1100 = 6dB
	1	PEADJ1	0001 = 1dB 0101 = 4dB 1101 = 7dB
	0	PEADJ0	0011= 2dB 0111 = 5dB 1111 = 8dB
3	7	-	
	6	-	
	5	-	
	4	-	
	3	-	
	2	AMP2	**Output amplitude adjustment**:
	1	AMP1	000 = 350 mV_{p-p}, 001 = 450 mV_{p-p}, 010 = 550 mV_{p-p} (default), 011 = 600 mV_{p-p}
	0	AMP0	100 = 650 mV_{p-p}, 101 = 700 mV_{p-p}, 110 = 750 mV_{p-p}, 111 = 850 mV_{p-p}

Table 12. Register Functionality (continued)

Register	Bit	Symbol	Function
7	7	SEL	**Receiver Optimization**: 1 = Content of register used to optimize the receiver 0 = Default receiver settings
	6	-	
	5	-	
	4	-	
	3	RXOPT1	00 = Some input equalization (recommended) 01 = Reduced input equalization
	2	RXOPT0	
	1	-	
	0	BIAS	**Bias current for input stage control bit**: 1 = Add 2 mA extra bias current to the input stage (recommended). 0 = Default
11	7	LOSSEL	**LOS assert level:**
	6	LOSA6	LOSSEL = 1
	5	LOSA5	Content of register bits 6 to 0 is used to select the LOS assert level
	4	LOSA4	Minimum LOS assert level for 0000000
	3	LOSA3	Maximum LOS assert level for 1111111
	2	LOSA2	LOSASEL = 0
	1	LOSA1	Default LOS assert level of 25 mV_{p-p} is used
	0	LOSA0	
12	7	LOSTMFENA	**Falling edge LOS mask enable and duration**:
	6	LOSTMF6	LOSTMFENA = 1 enables falling edge LOS masking
	5	LOSTMF5	LOSTMFENA = 0 disables falling edge LOS masking
	4	LOSTMF4	Mask time < 10 µs for 000000
	3	LOSTMF3	Mask time > 2 ms for 111111
	2	LOSTMF2	
	1	LOSTMF1	
	0	LOSTMF0	
13	7	LOSTMRENA	**Rising edge LOS mask enable and duration**:
	6	LOSTMR6	LOSTMRENA = 1 enables rising edge LOS masking
	5	LOSTMR5	LOSTMRENA = 0 disables rising edge LOS masking
	4	LOSTMR4	Mask time < 10 µs for 000000
	3	LOSTMR3	Mask time > 2 ms for 111111
	2	LOSTMR2	
	1	LOSTMR1	
	0	LOSTMR0	
15	-	-	**Selected LOS assert level (read only)**
	6	SELLOS6	
	5	SELLOS5	
	4	SELLOS4	
	3	SELLOS3	
	2	SELLOS2	
	1	SELLOS1	
	0	SELLOS0	

APPLICATION INFORMATION

Figure 5 shows a typical application circuit using the ONET1151P.

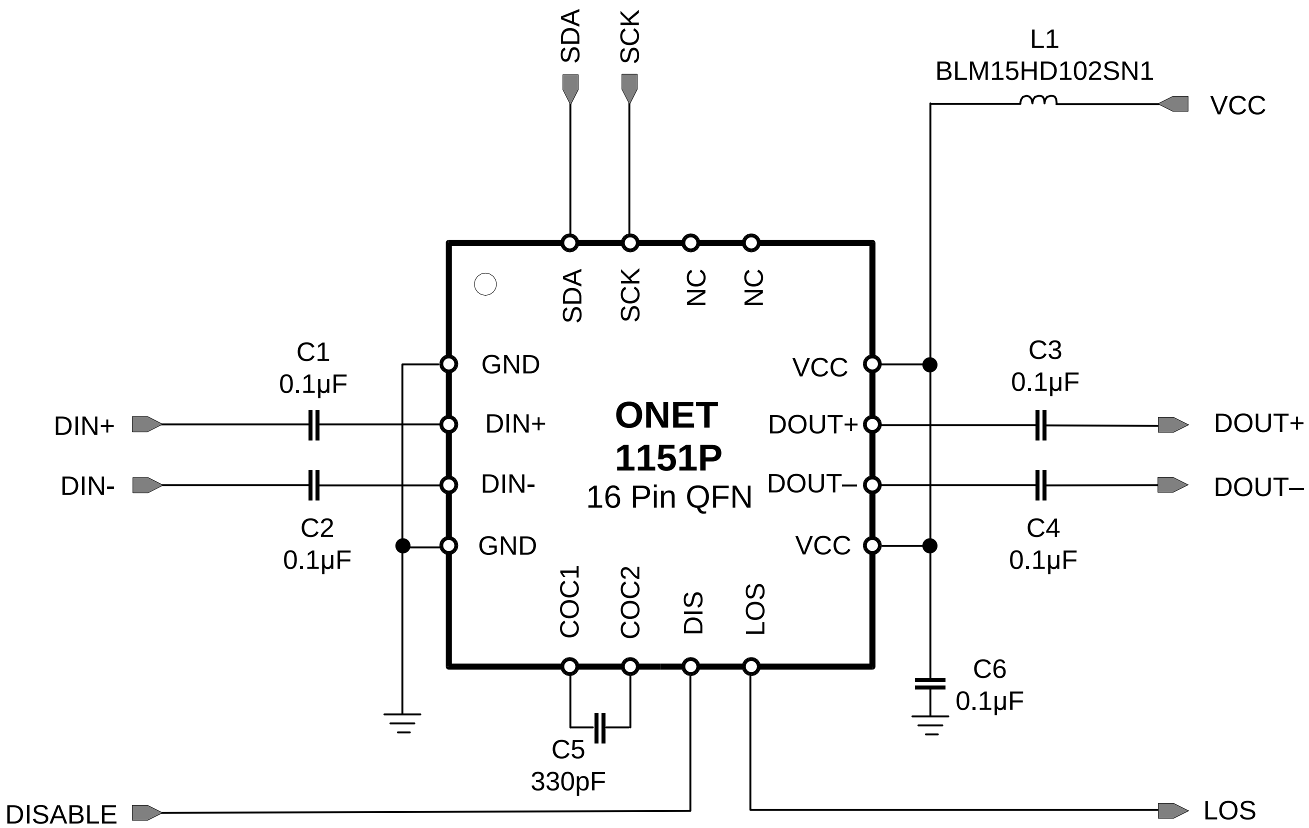

Figure 5. Typical Application Circuit

TYPICAL CHARACTERISTICS

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, and Register 7 set to 0x81 (unless otherwise noted).

FREQUENCY RESPONSE

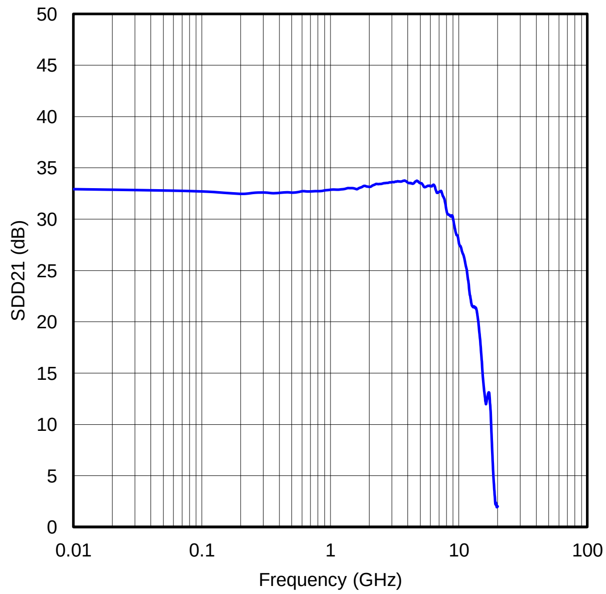

Figure 6.

TRANSFER FUNCTION

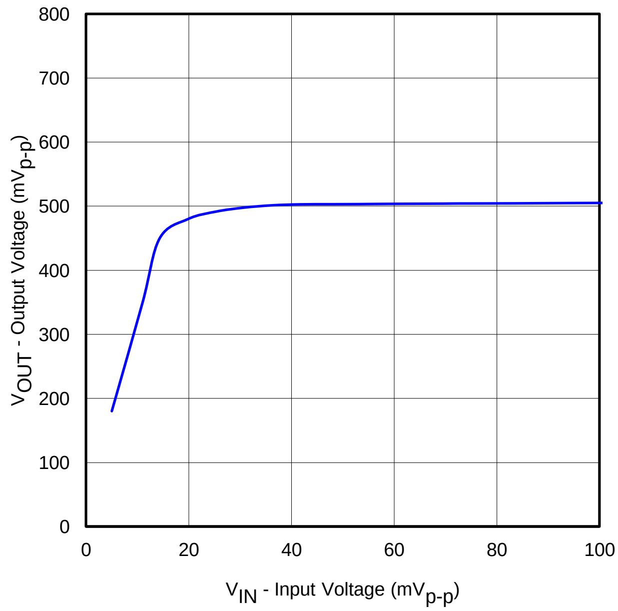

Figure 7.

DIFFERENTIAL INPUT RETURN GAIN vs FREQUENCY

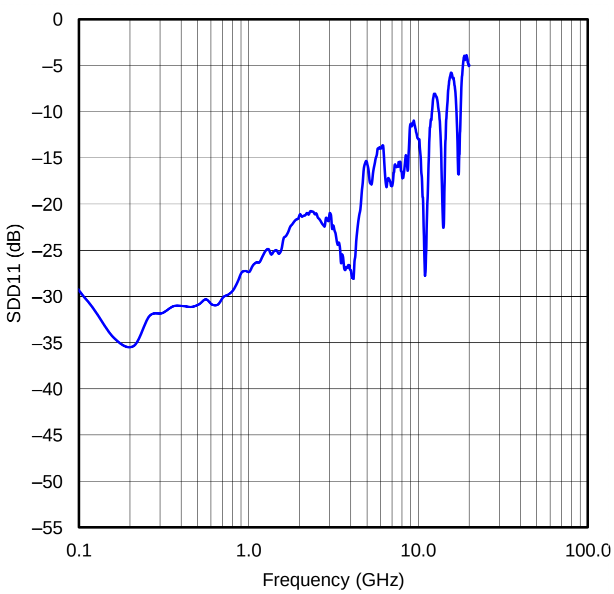

Figure 8.

DIFFERENTIAL OUTPUT RETURN GAIN vs FREQUENCY

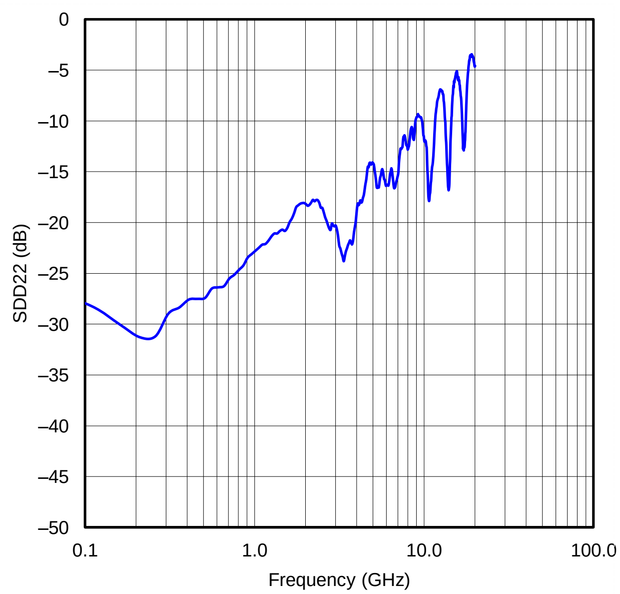

Figure 9.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, and Register 7 set to 0x81 (unless otherwise noted).

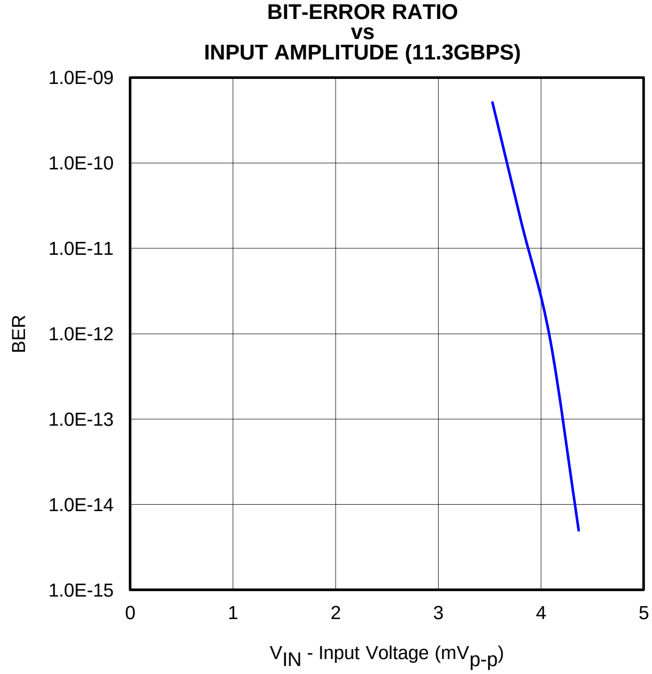

Figure 10.

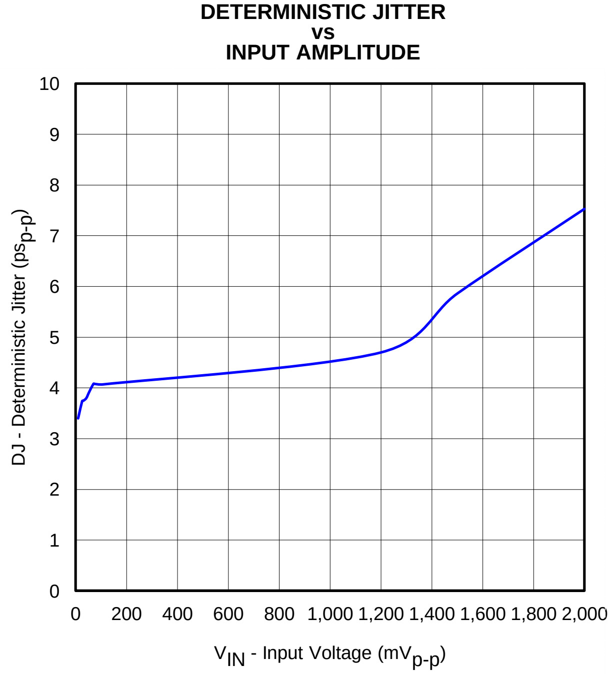

Figure 11.

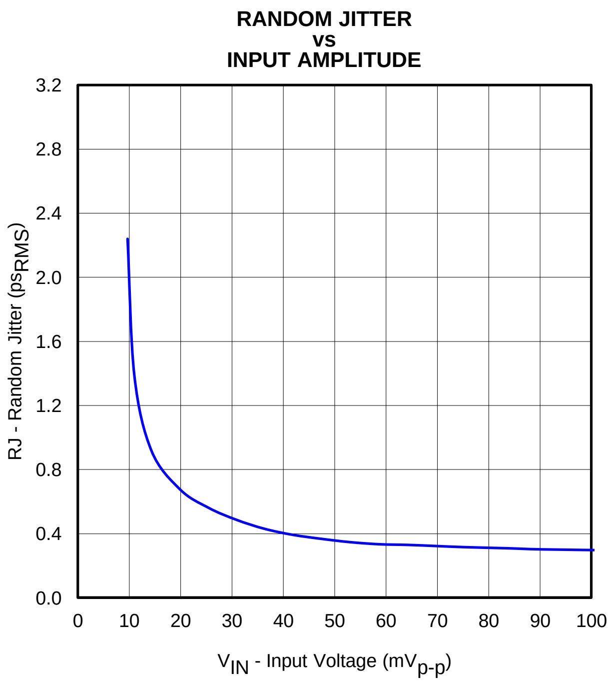

Figure 12.

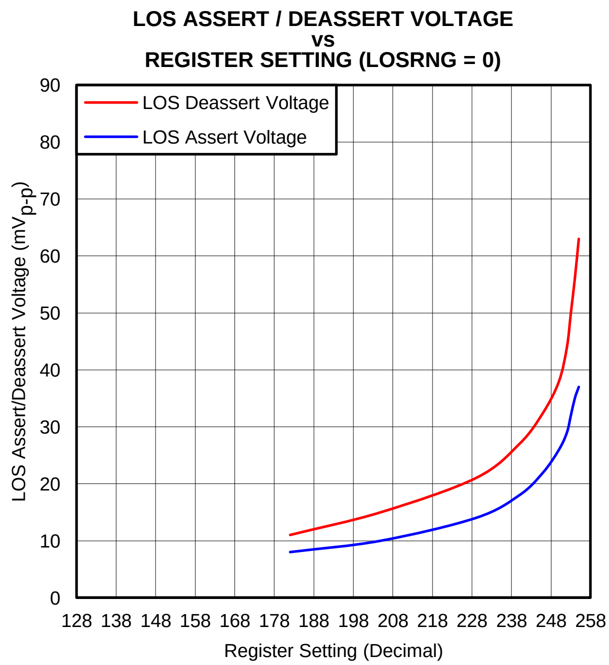

Figure 13.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, and Register 7 set to 0x81 (unless otherwise noted).

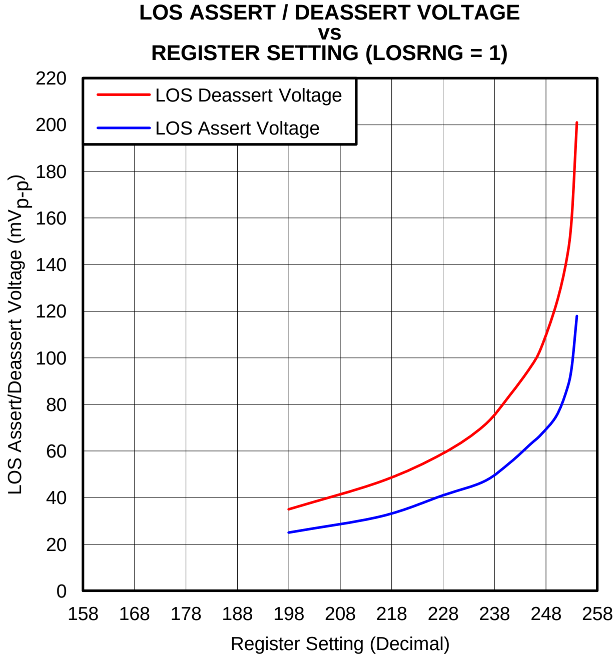

Figure 14.

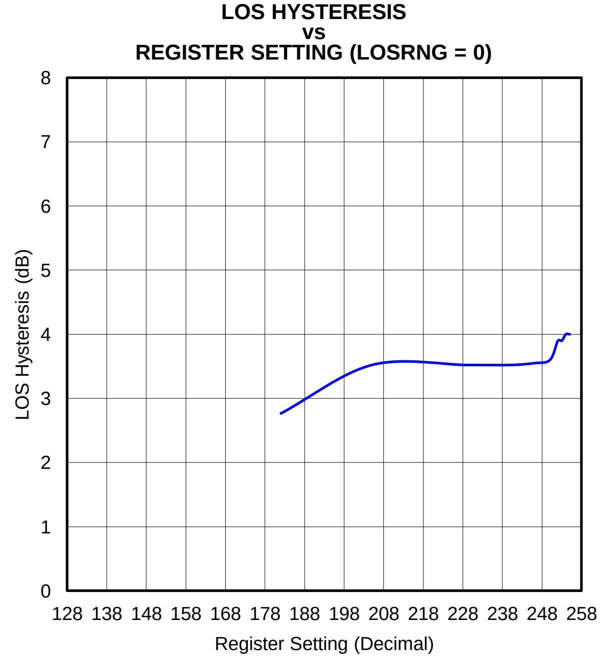

Figure 15.

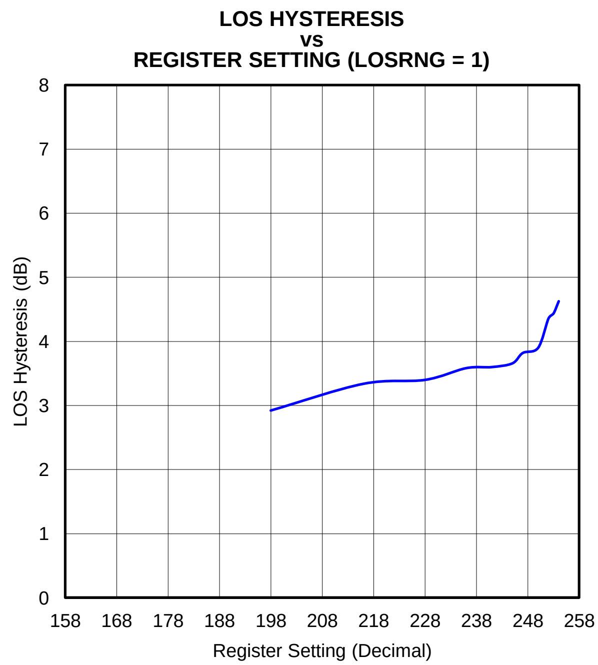

Figure 16.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, and Register 7 set to 0x81 (unless otherwise noted).

OUTPUT EYE-DIAGRAM AT 11.3 GBPS AND 20 mV_{p-p} INPUT VOLTAGE

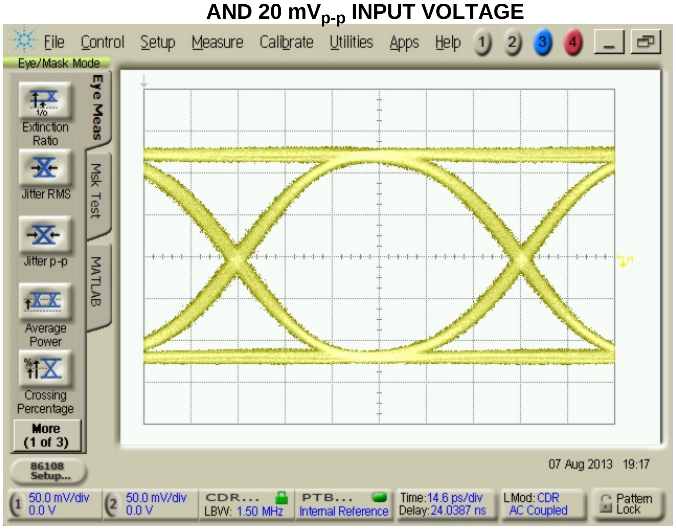

Figure 17.

OUTPUT EYE-DIAGRAM AT 11.3 GBPS AND MAXIMUM INPUT VOLTAGE (2000 mV_{p-p})

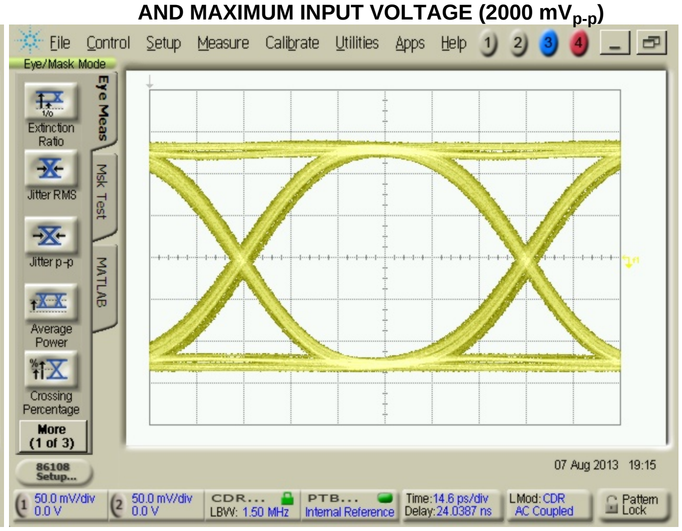

Figure 18.

OUTPUT EYE-DIAGRAM AT 10.3 GBPS AND 20 mV_{p-p} INPUT VOLTAGE (20 mV_{p-p})

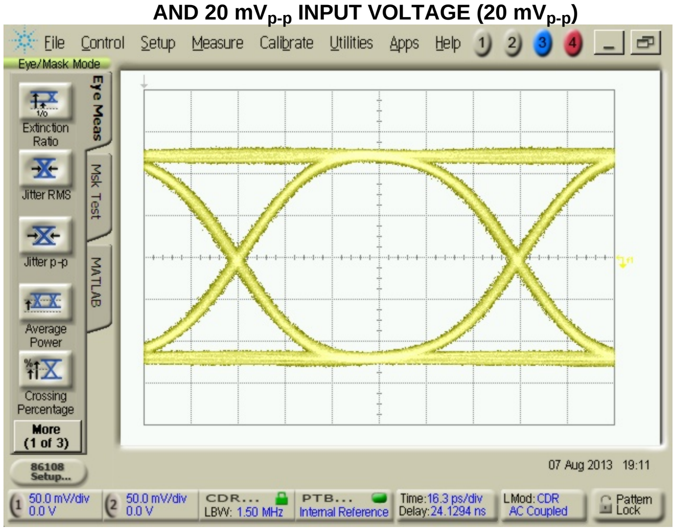

Figure 19.

OUTPUT EYE-DIAGRAM AT 10.3 GBPS AND MAXIMUM INPUT VOLTAGE (2000 mV_{p-p})

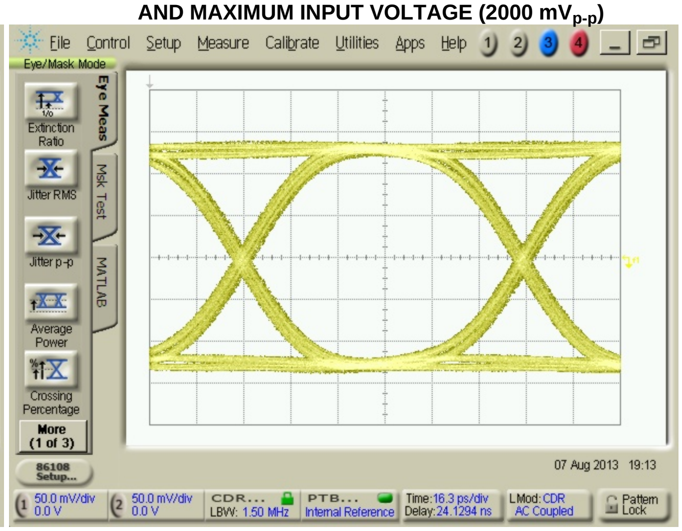

Figure 20.