
11.3-Gbps Limiting Amplifier

FEATURES

- Up to 11.3-Gbps Operation
- Loss-of-Signal Detection (LOS)
- Adjustable Output Voltage
- Low Power Consumption
- Input Offset Cancellation
- CML Data Outputs With On-Chip, 50- Ω Back-Termination to VCC
- Single 3.3 V Supply
- Surface-Mount, Small-Footprint, 3-mm \times 3-mm, 16-Pin QFN Package

APPLICATIONS

- 10 Gigabit Ethernet Optical Transmitters
- 8 \times and 10 \times Fibre Channel Optical Transmitters
- SONET OC-192/SDH-64 Optical Transmitters
- XFP and SFP+ Transceiver Modules
- XENPAK, XPAK, X2 and 300-Pin MSA Transponder Modules
- Cable Driver and Receiver

DESCRIPTION

The ONET1191P is a high-speed, 3.3-V limiting amplifier for copper-cable and fiber-optic applications with data rates up to 11.3 Gbps.

This device provides a gain of about 40 dB which ensures a fully differential output swing for input signals as low as 5 mV_{pp}. The output amplitude can be adjusted from 400 mV_{pp} to 700 mV_{pp}. Loss-of-signal detection and output disable are also provided.

The part is available in a small-footprint, 3-mm \times 3-mm, 16-pin QFN package, typically dissipates less than 110 mW, and is characterized for operation from -40°C to 85°C .

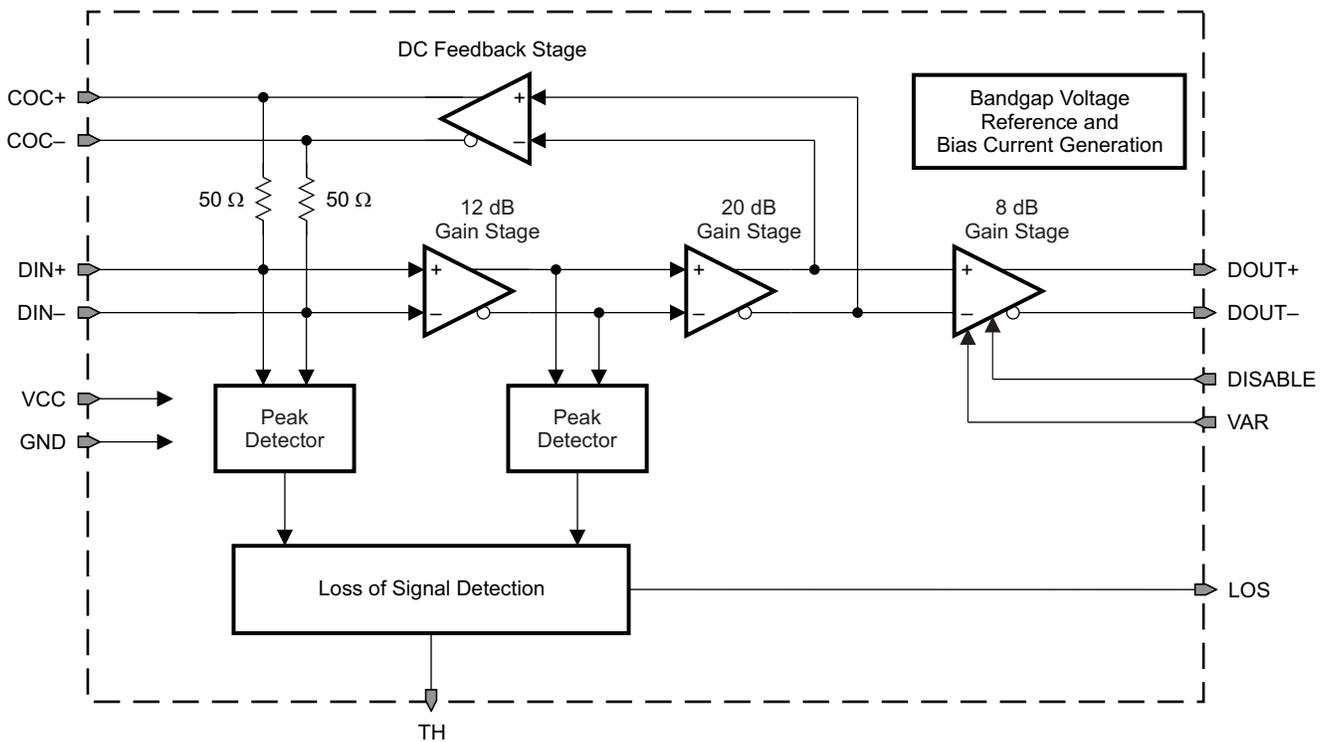


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BLOCK DIAGRAM

A simplified block diagram of the ONET1191P is shown in Figure 1.

This compact, low-power, 11.3-Gbps limiting amplifier consists of a high-speed data path with offset cancellation (dc feedback), a loss-of-signal detection block using two peak detectors, and a band-gap voltage reference and bias current generation block.



B0067-02

Figure 1. Simplified Block Diagram of the ONET1191P

HIGH-SPEED DATA PATH

The high-speed data signal is applied to the data path by means of the input signal pins, DIN+/DIN-. The data path consists of a 12-dB input gain stage with $2 \times 50\text{-}\Omega$ on-chip line-termination resistors, a second gain stage with 20 dB of gain, and a variable-gain output stage which provides another 8 dB of gain. The amplified data output signal is available at the output pins DOUT+/DOUT-, which include on-chip $2 \times 50\text{-}\Omega$ back-termination to VCC. The output amplitude can be adjusted between 400 mV_{pp} and 700 mV_{pp} by connecting an external resistor between the VAR pin and ground (GND).

A dc feedback stage compensates for internal offset voltages and thus ensures proper operation even for very small input data signals. This stage is driven by the output signal of the second gain stage. The signal is low-pass filtered, amplified, and fed back to the input of the first gain stage via the on-chip, $50\text{-}\Omega$ termination resistors. The required low-frequency cutoff is determined by an external $0.1\text{ }\mu\text{F}$ capacitor, which must be differentially connected to the COC+/COC- pins.

LOSS-OF-SIGNAL DETECTION

The peak values of the input signal and output signal of the first gain stage are monitored by two peak detectors. The peak values are compared to a predefined loss-of-signal threshold voltage inside the loss-of-signal detection block. As a result of the comparison, the LOS signal, which indicates that the input signal amplitude is below the defined threshold level, is generated.

The threshold voltage can be set within a certain range by means of an external resistor connected between the TH pin and ground.

BAND-GAP VOLTAGE AND BIAS GENERATION

The ONET1191P limiting amplifier is supplied by a single 3.3-V supply voltage connected to the VCC pins. This voltage is referred to ground (GND).

On-chip band-gap voltage circuitry generates a reference voltage, independent of supply voltage, from which all other internally required voltages and bias currents are derived.

PACKAGE

For the ONET1191P, a small-footprint, 3-mm × 3-mm, 16-pin QFN package, with a lead pitch of 0,5 mm, is used. The pinout is shown in [Figure 2](#).

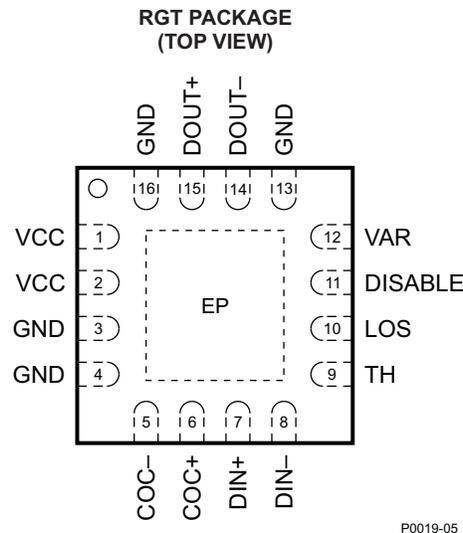


Figure 2. Pinout of ONET1191P in a 3-mm × 3-mm, 16-Pin QFN Package

TERMINAL FUNCTIONS

| TERMINAL | | TYPE | DESCRIPTION |
|----------|------------------|----------------|---|
| NAME | NO. | | |
| COC+ | 6 | Analog | Offset cancellation filter capacitor plus terminal. An external 0.1 μF filter capacitor must be connected between this pin and COC– (pin 5). |
| COC– | 5 | Analog | Offset cancellation filter capacitor minus terminal. An external 0.1 μF filter capacitor must be connected between this pin and COC+ (pin 6). |
| DIN+ | 7 | Analog input | Noninverted data input. On-chip, 50-Ω terminated to COC+. Differentially 100-Ω terminated to DIN–. |
| DIN– | 8 | Analog input | Inverted data input. On-chip, 50-Ω terminated to COC–. Differentially 100-Ω terminated to DIN+. |
| DISABLE | 11 | CMOS input | Disables the output stage when set to a high level |
| DOU+ | 15 | CML out | Noninverted data output. On-chip, 50-Ω back-terminated to VCC. |
| DOU– | 14 | CML out | Inverted data output. On-chip, 50-Ω back-terminated to VCC. |
| GND | 3, 4, 13, 16, EP | Supply | Circuit ground. Exposed die pad (EP) must be grounded. |
| LOS | 10 | Open-drain MOS | High level indicates that the input signal amplitude is below the programmed threshold level. Open-drain output. Requires an external 10-kΩ pullup resistor to VCC for proper operation. |
| TH | 9 | Analog input | LOS threshold adjustment with resistor to GND |
| VAR | 12 | Analog input | Variable output amplitude control. Output amplitude can be reduced to 400 mV _{pp} by grounding the VAR pin. Output amplitude can be set from 400 mV _{pp} to 700 mV _{pp} by connecting a 0 to 100-kΩ resistor to GND or leaving the pin open. |
| VCC | 1, 2 | Supply | 3.3-V ±10% supply voltage |

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | VALUE | UNIT |
|---|--|-----------|----------|
| V_{CC} | Supply voltage ⁽²⁾ | –0.3 to 4 | V |
| V_{DIN+}, V_{DIN-} | Voltage at DIN+, DIN– ⁽²⁾ | 0.5 to 4 | V |
| $V_{LOS}, V_{COC+}, V_{COC-}, V_{TH}, V_{DOUT+}, V_{DOUT-}$ | Voltage at LOS, COC+, COC–, TH, DOUT+, DOUT– ⁽²⁾ | –0.3 to 4 | V |
| $V_{DIN,DIFF}$ | Differential voltage between DIN+ and DIN– | ±1.25 | V |
| I_{LOS} | Current into LOS | 1 | mA |
| $I_{DIN+}, I_{DIN-}, I_{DOUT+}, I_{DOUT-}$ | Continuous current at inputs and outputs | 20 | mA |
| ESD | ESD rating at all pins | 1.5 | kV (HBM) |
| $T_{J,max}$ | Maximum junction temperature | 125 | °C |
| T_{STG} | Storage temperature range | –65 to 85 | °C |
| T_A | Characterized free-air operating temperature range | –40 to 85 | °C |
| T_{LEAD} | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260 | °C |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

| | | MIN | TYP | MAX | UNIT |
|----------|--------------------------------|-----|-----|------|------------|
| V_{CC} | Supply voltage | 2.9 | 3.3 | 3.6 | V |
| T_A | Operating free-air temperature | –40 | | 85 | °C |
| | Disable input high voltage | 2 | | | V |
| | Disable input low voltage | | | 0.25 | V |
| | Optimum LOS threshold resistor | 32 | | 62 | k Ω |
| | R_{VAR} range | 0 | | open | k Ω |

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions, outputs connected to a 50- Ω load, R_{VAR} = open (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|------------------------|--|------|-----|----------|
| V_{CC} | Supply voltage | 2.9 | 3.3 | 3.6 | V |
| I_{VCC} | Supply current | | 33 | 49 | mA |
| R_{IN} | Data input resistance | | 50 | | Ω |
| R_{OUT} | Data output resistance | | 50 | | Ω |
| | Voltage at TH pin | | 1.25 | | V |
| | LOS HIGH voltage | 10-k Ω pullup to V_{CC} , $I_{SOURCE} = 50 \mu A$ | 2.4 | | |
| | LOS LOW voltage | 10-k Ω pullup to V_{CC} , $I_{SINK} = 200 \mu A$ | | 0.5 | V |

AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions, outputs connected to a 50-Ω load, R_{VAR} = open (unless otherwise noted). Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|----------------------------------|---|------|------|------|-------------------|
| f_{3dB-H} | High-frequency –3-dB bandwidth | | 8 | 11 | 15 | GHz |
| f_{3dB-L} | Low-frequency –3-dB bandwidth | $C_{OC} = 0.1 \mu F$, ac coupling capacitors = 0.1 μF | | 30 | | kHz |
| $V_{IN,MIN}$ | Data input sensitivity | $K28.5$ at 11.3 Gbps, BER < 10^{-12} | | 2.5 | 5 | mV _{pp} |
| | | $V_{OD-min} \geq 0.95 \times V_{OD}$ (output limited) | | 10 | 20 | |
| A | Small-signal gain | | 34 | 40 | 44 | dB |
| $V_{IN,MAX}$ | Data input overload | | 2000 | | | mV _{pp} |
| DJ | Deterministic jitter | $V_{IN} = 5 \text{ mV}_{pp}$, K28.5 at 11.3 Gbps | | 4 | 7 | ps _{pp} |
| | | $V_{IN} = 20 \text{ mV}_{pp}$, K28.5 at 11.3 Gbps | | 4 | 9 | |
| RJ | Random jitter | Input = 5 mV _{pp} | | 1.6 | | ps _{RMS} |
| | | Input = 20 mV _{pp} | | 0.7 | | |
| V_{OD} | Differential data output voltage | $V_{IN} \geq 20 \text{ mV}_{pp}$, DISABLE = LOW | 600 | 700 | 900 | mV _{pp} |
| | | DISABLE = HIGH | | 25 | 100 | |
| t_r | Output rise time | 20% to 80%, $V_{IN} \geq 20 \text{ mV}_{pp}$ | | 25 | 35 | ps |
| t_f | Output fall time | 20% to 80%, $V_{IN} \geq 20 \text{ mV}_{pp}$ | | 25 | 35 | ps |
| V_{TH} | LOS assert threshold range | K28.5 pattern at 10.7 Gbps, $R_{TH} = 62 \text{ k}\Omega$ | | 40 | | mV _{pp} |
| | | K28.5 pattern at 10.7 Gbps, $R_{TH} = 32 \text{ k}\Omega$ | | 65 | | |
| | LOS threshold variation | Versus temperature | | 3 | | dB |
| | | Versus supply voltage V_{CC} | | 1 | | dB |
| | LOS hysteresis | K28.5 pattern at 11.3 Gbps | 1.5 | | 7 | dB |
| t_{LOS_AST} | LOS assert time | | | 1300 | 2000 | ns |
| t_{LOS_DEA} | LOS deassert time | | | 120 | | ns |
| t_{DIS} | Disable response time | | | 90 | | ns |

TYPICAL OPERATION CHARACTERISTICS

Typical operating condition is at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, and $R_{VAR} = \text{open}$ (unless otherwise noted)

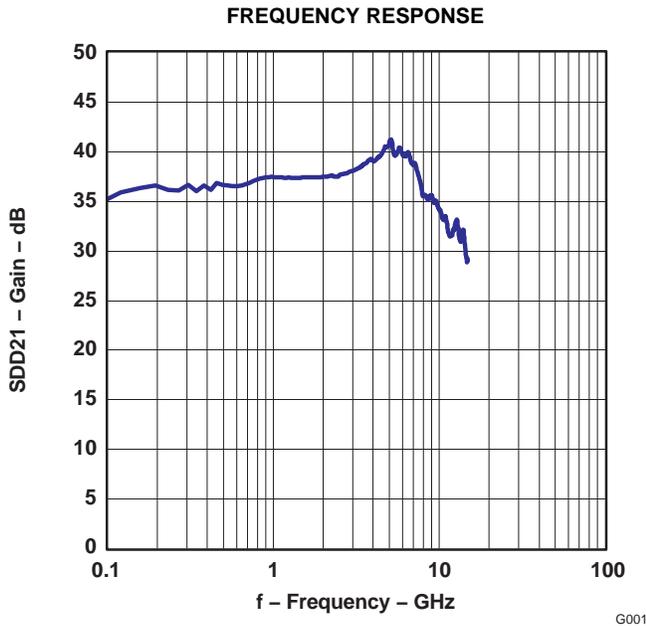


Figure 3.

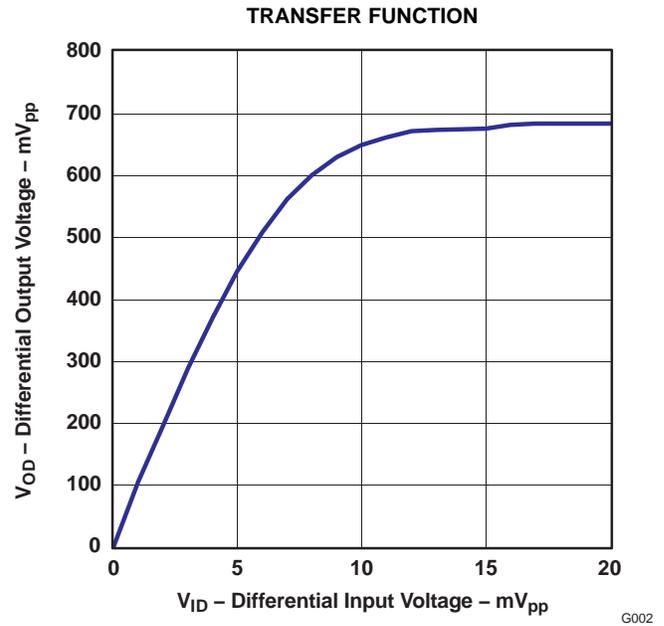


Figure 4.

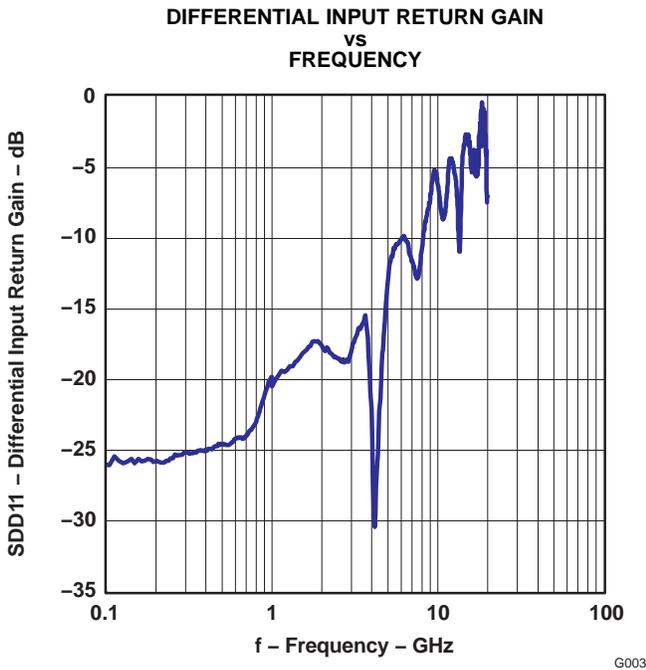


Figure 5.

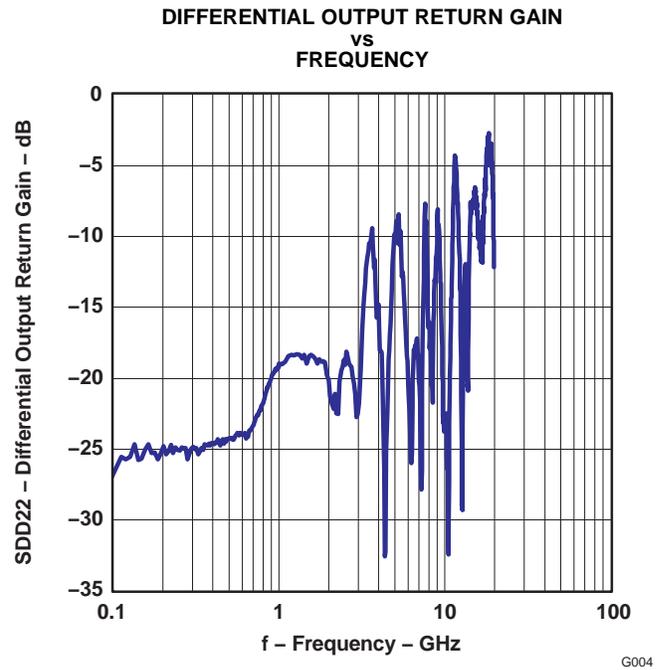


Figure 6.

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, and $R_{VAR} = \text{open}$ (unless otherwise noted)

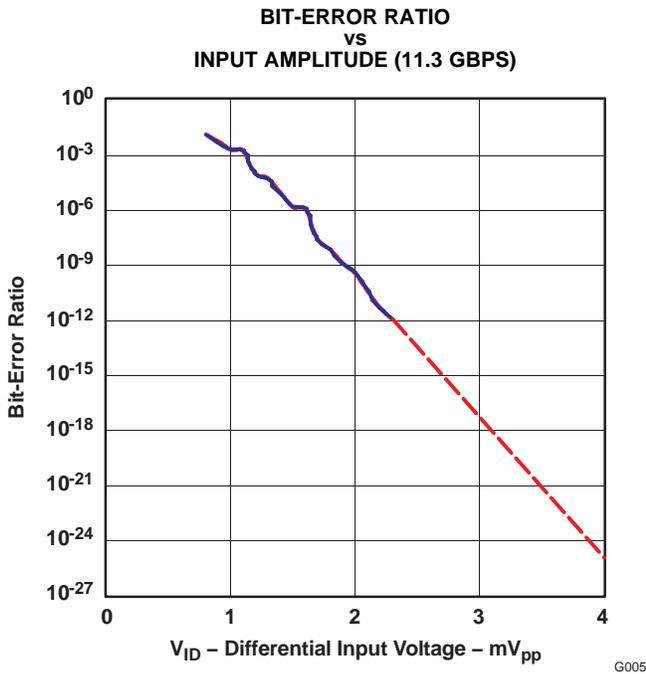


Figure 7.

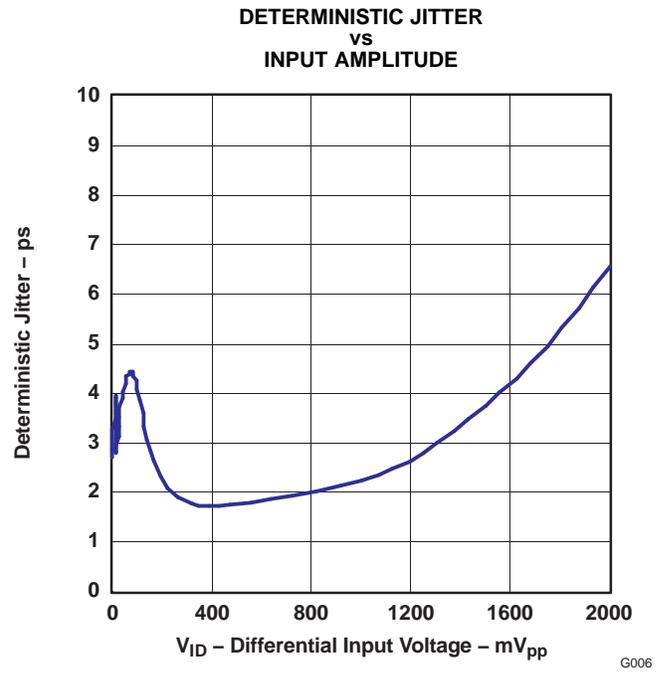


Figure 8.

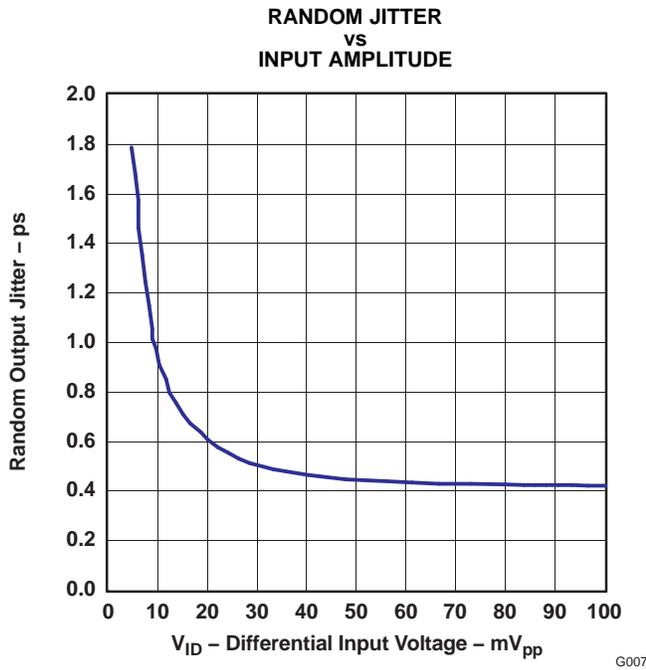


Figure 9.

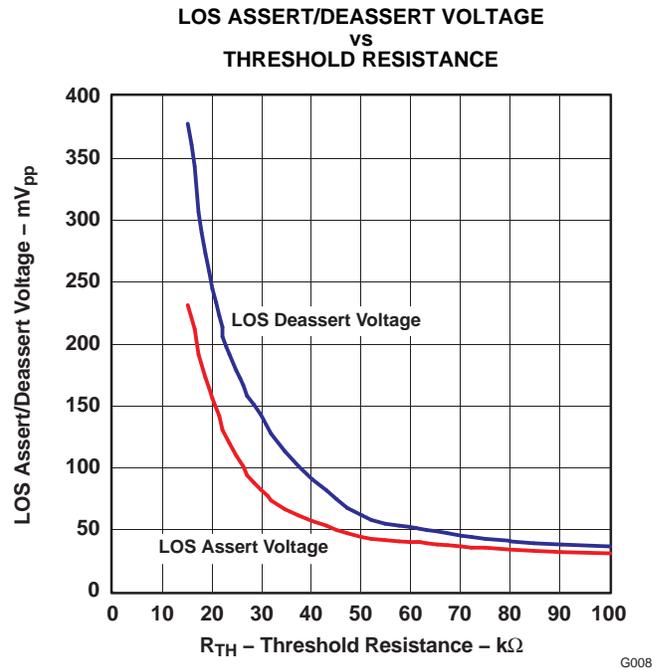


Figure 10.

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, and $R_{VAR} = \text{open}$ (unless otherwise noted)

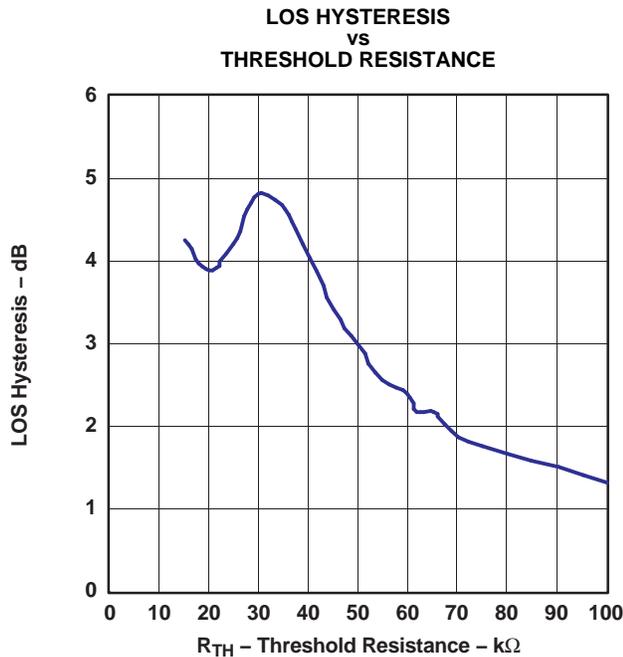


Figure 11.

G009

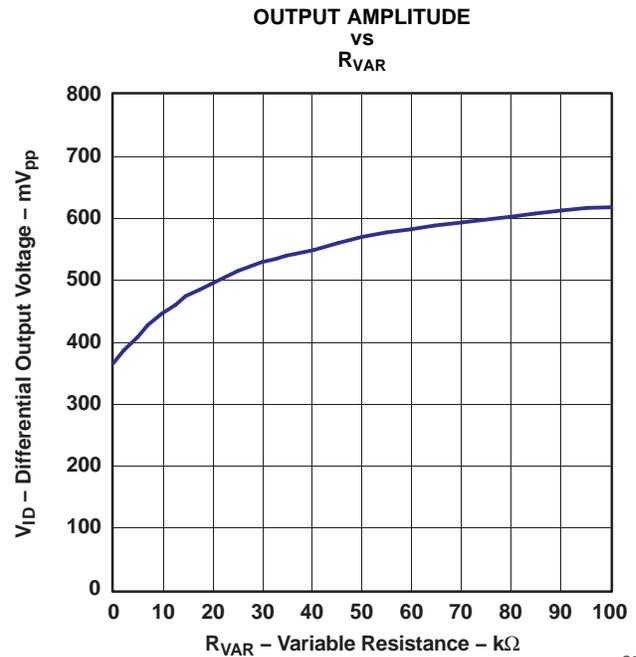


Figure 12.

G010

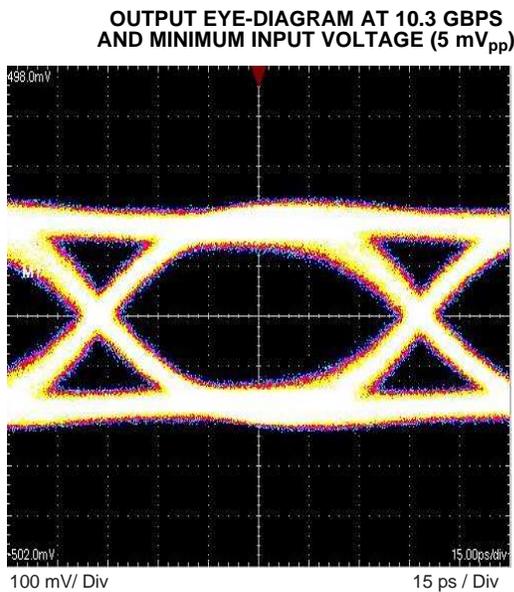


Figure 13.

G011

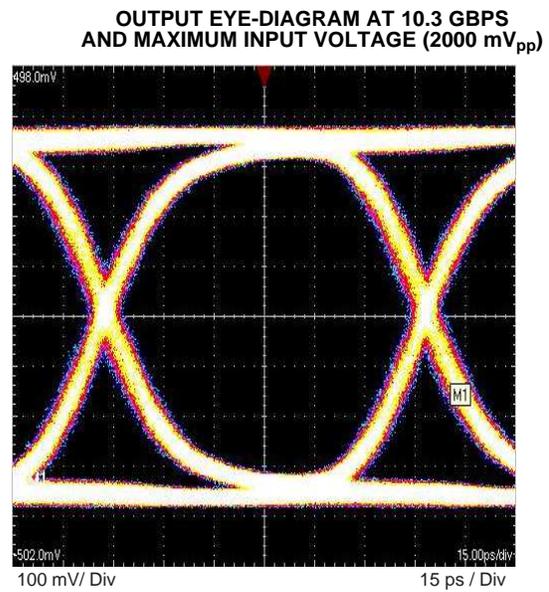


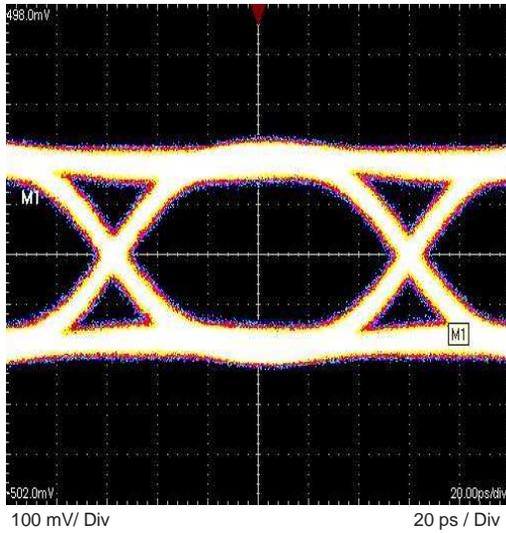
Figure 14.

G012

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, and $R_{VAR} = \text{open}$ (unless otherwise noted)

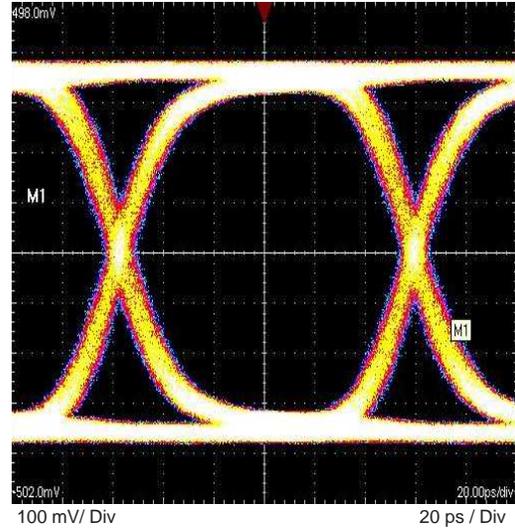
OUTPUT EYE-DIAGRAM AT 8.5 GBPS
AND MINIMUM INPUT VOLTAGE (5 mV_{pp})



G013

Figure 15.

OUTPUT EYE-DIAGRAM AT 8.5 GBPS
AND MAXIMUM INPUT VOLTAGE (2000 mV_{pp})

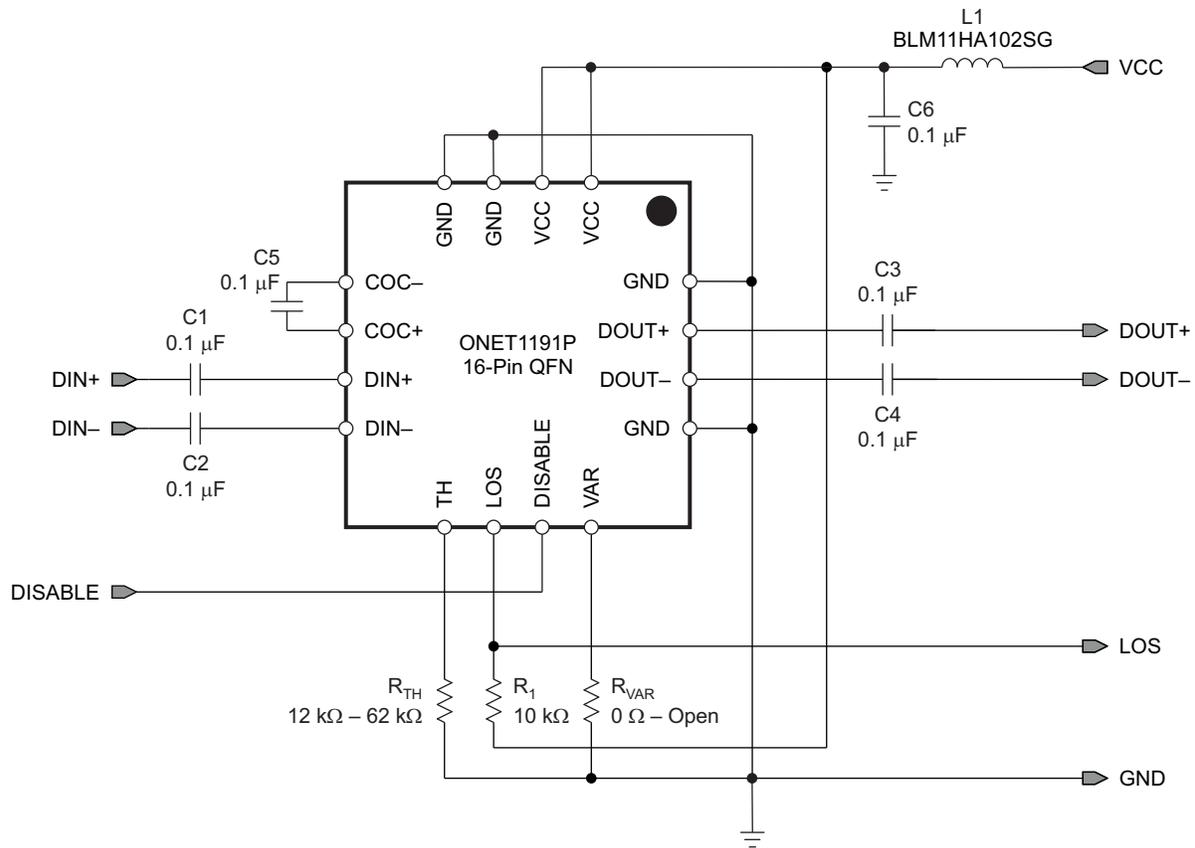


G014

Figure 16.

APPLICATION INFORMATION

Figure 17 shows a typical application circuit using the ONET1191P. The output amplitude can be adjusted with R_{VAR} and the LOS assert voltage is adjusted with R_{TH} .



S0099-03

Figure 17. Basic Application Circuit

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| ONET1191PRGTR | Obsolete | Production | VQFN (RGT) 16 | - | - | Call TI | Call TI | -40 to 85 | 191P |
| ONET1191PRGTT | Obsolete | Production | VQFN (RGT) 16 | - | - | Call TI | Call TI | -40 to 85 | 191P |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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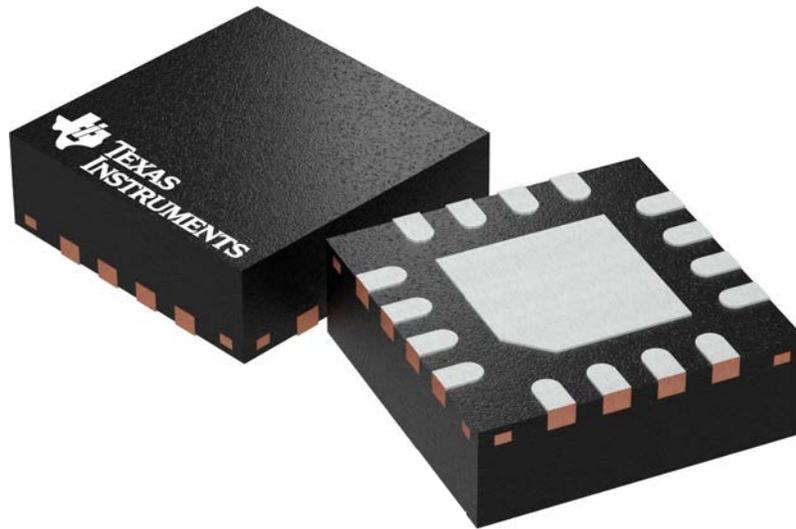
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RGT 16

GENERIC PACKAGE VIEW

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/1

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