

1.1 nV/ $\sqrt{\text{Hz}}$ Noise, Low Power, Precision Operational Amplifier

Check for Samples: [OPA211-HT](#)

FEATURES

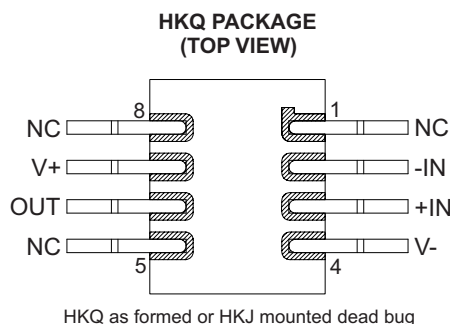
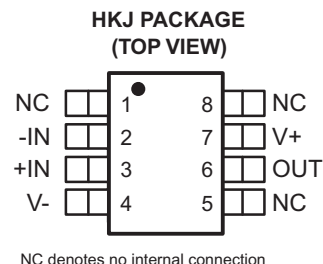
- Low Voltage Noise: 1.1 nV/ $\sqrt{\text{Hz}}$ at 1 kHz
- Input Voltage Noise: 80 nV_{PP} (0.1 Hz to 10 Hz)
- THD+N: –136dB (G = 1, f = 1 kHz)
- Offset Voltage: 240 μV (max)
- Offset Voltage Drift: 0.35 $\mu\text{V}/^\circ\text{C}$ (typ)
- Low Supply Current: 6 mA/Ch (typ)
- Unity-Gain Stable
- Gain Bandwidth Product: 80 MHz (G = 100)
45 MHz (G = 1)
- Slew Rate: 27 V/ μs
- 16-Bit Settling: 700 ns
- Wide Supply Range: $\pm 2.25\text{ V}$ to $\pm 18\text{ V}$, 4.5 V to 36 V
- Rail-to-rail output
- Output current: 30 mA

APPLICATIONS

- Down-Hole Drilling
- High Temperature Environments

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Extreme ($-55^\circ\text{C}/210^\circ\text{C}$) Temperature Range ⁽¹⁾
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability
- Texas Instruments high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.



(1) Custom temperature ranges available

DESCRIPTION

The OPA211 series of precision operational amplifiers achieves very low 1.1 nV/ $\sqrt{\text{Hz}}$ noise density with a supply current of only 3.6 mA. This series also offers rail-to-rail output swing, which maximizes dynamic range.

The extremely low voltage and low current noise, high speed, and wide output swing of the OPA211 series make these devices an excellent choice as a loop filter amplifier in PLL applications.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2009–2013, Texas Instruments Incorporated

In precision data acquisition applications, the OPA211 series of op amps provides 700-ns settling time to 16-bit accuracy throughout 10-V output swings. This ac performance, combined with only 240-μV of offset and 0.35-μV/°C of drift over temperature, makes the OPA211 ideal for driving high-precision 16-bit analog-to-digital converters (ADCs) or buffering the output of high-resolution digital-to-analog converters (DACs).

The OPA211 series is specified over a wide dual-power supply range of ±2.25 V to ±18 V, or for single-supply operation from 4.5 V to 36 V.

This series of op amps is specified from T_A = –55°C to 210°C.

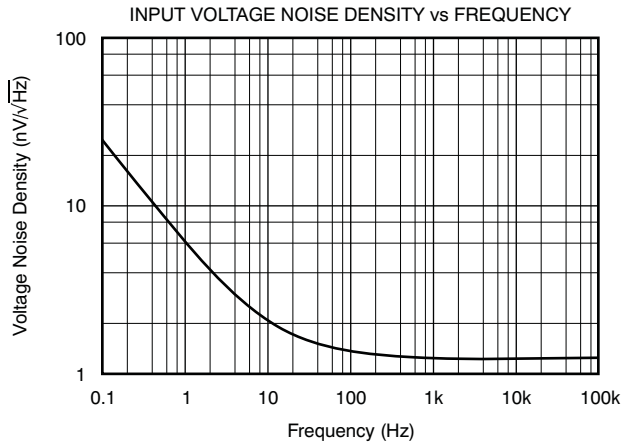


Table 1. ORDERING INFORMATION⁽¹⁾

TA	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 210°C	HKJ	OPA211SHKJ	OPA211SHKJ
	HKQ	OPA211SHKQ	OPA211SHKQ
	KGD	OPA211SKGD1	NA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION
15 mils.	Silicon with backgrind	V-	Al-Si-Cu (0.5%)

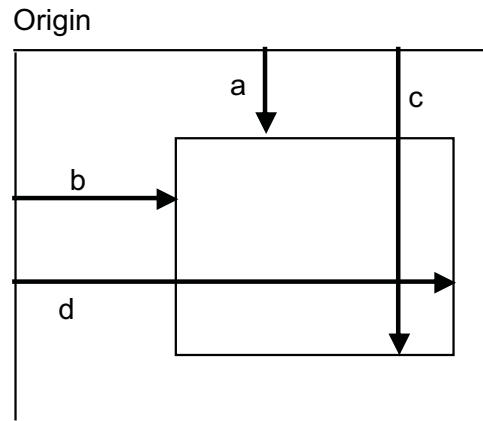
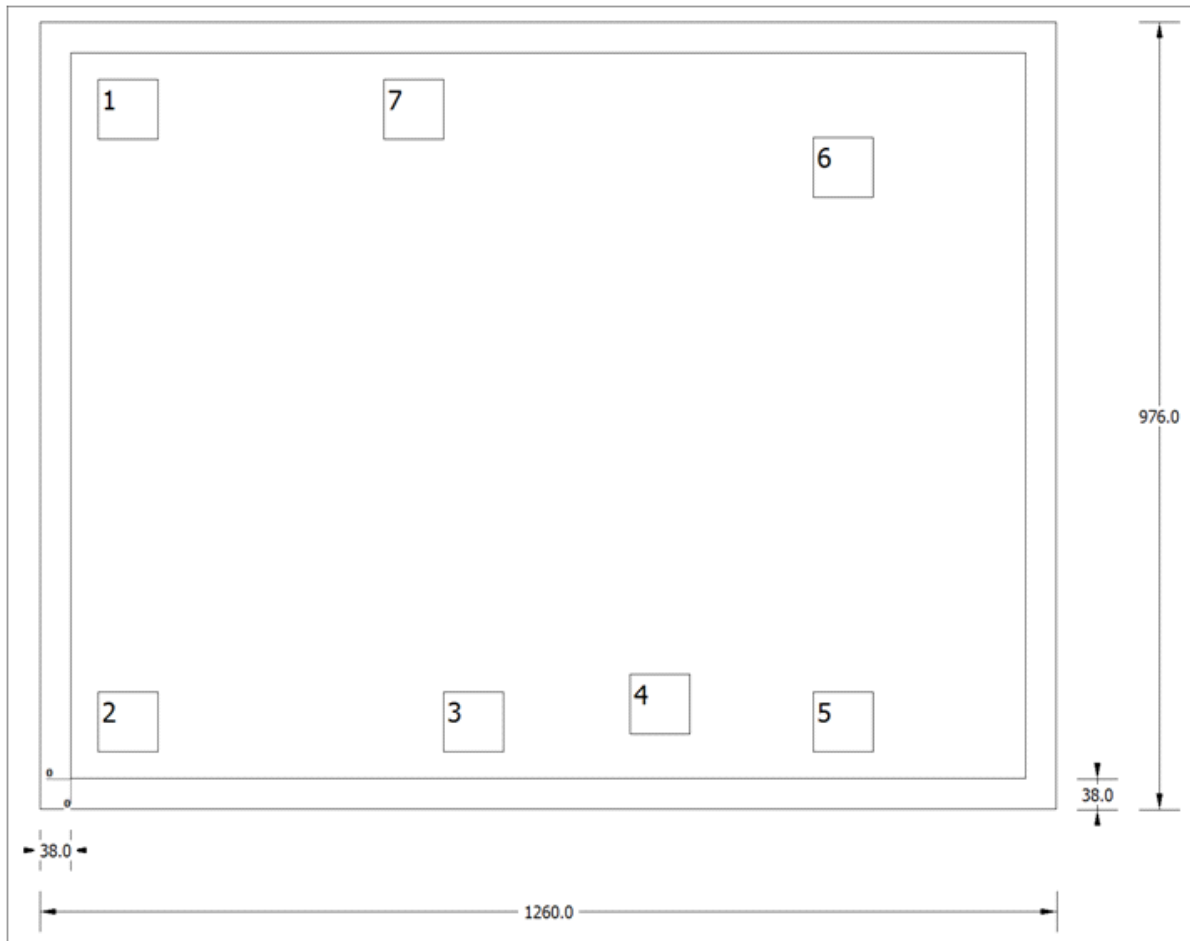


Table 2. BOND PAD COORDINATES

DESCRIPTION	PAD NUMBER	a	b	c	d
-IN	1	34.4000	792.000	109.400	867.000
+IN	2	34.4000	33.000	109.400	108.000
NC	3	461.850	33.000	536.850	108.000
V-	4	692.650	54.600	767.650	129.600
OUT	5	920.400	33.000	995.400	108.000
V+	6	920.400	720.150	995.400	795.150
NC	7	388.050	792.000	463.050	867.000



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range (unless otherwise noted).

		VALUE	UNIT
$V_S = (V=) - (V-)$	Supply Voltage	40	V
V_{IN}	Input Voltage	$(V-) - 0.5$ to $(V+) + 0.5$	V
I_{IN}	Input Current (Any pin except power-supply pins)	± 10	mA
	Output Short-Circuit ⁽²⁾	Continuous	
T_A	Operating Temperature	-55 to 210	°C
T_{STG}	Storage Temperature	-65 to 210	°C
T_J	Junction Temperature	210	°C
ESD Ratings	Human Body Model (HBM)	3000	V
	Charged Device Model (CDM)	1000	V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) Short-circuit to $V_S/2$ (ground in symmetrical dual supply setups), one amplifier per package.

THERMAL CHARACTERISTICS FOR HKJ OR HKQ PACKAGE

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
θ_{JC}	Junction-to-case thermal resistance	to ceramic side of case			5.7	°C/W
		to top of case lid (metal side of case)			13.7	

ELECTRICAL CHARACTERISTICS: $V_S = \pm 2.25\text{ V}$ to $\pm 18\text{ V}$

At $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

				T _A = −55 to 125°C			T _A = 210°C			
PARAMETER		CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE										
Input Offset Voltage	V _{OS}	V _S = ±15V			±30	±180		±70	±260	μV
Drift	dV _{OS} /dT				0.35	1.5		0.35	2.0	μV/°C
vs Power Supply	PSRR	V _S = ±2.25V to ±18V			0.1	3		0.1	3	μV/V
INPUT BIAS CURRENT										
Input Bias Current	I _B	V _{CM} = 0V			±60	±200		±60	±250	nA
Offset Current	I _{OS}	V _{CM} = 0V			±25	±150		±25	±150	nA
NOISE										
Input Voltage Noise	e _n	f = 0.1Hz to 10Hz			80			80		nV _{pp}
Input Voltage Noise Density		f = 10Hz			2			2		nV/√Hz
		f = 100Hz			1.4			1.4		nV/√Hz
		f = 1kHz			1.1			1.1		nV/√Hz
Input Current Noise Density	I _n	f = 10Hz			3.2			3.2		pA/√Hz
		f = 1kHz			1.7			1.7		pA/√Hz
INPUT VOLTAGE RANGE ⁽¹⁾										
Common-Mode Voltage Range	V _{CM}	V _S ≥ ±5V		(V−) + 1.8		(V+) − 1.4	(V−) + 1.8		(V+) − 1.4	V
		V _S < ±5V		(V−) + 2		(V+) − 1.4	(V−) + 2		(V+) − 1.4	V
Common-Mode Rejection Ratio	CMRR	V _S ≥ ±5V, (V−) + 2V ≤ V _{CM} ≤ (V+) − 2V		114	120		113	120		dB
		V _S < ±5V, (V−) + 2V ≤ V _{CM} ≤ (V+) − 2V		108	120		93	100		dB
INPUT IMPEDANCE										
Differential					20k 8			20k 8		Ω pF
Common-Mode					10 ⁹ 2			10 ⁹ 2		Ω pF
OPEN-LOOP GAIN										
Open-Loop Voltage Gain	A _{OL}	(V−) + 0.2V ≤ V _O ≤ (V+) − 0.2V, R _L = 10kΩ		114	130		112	118		dB
	A _{OL}	(V−) + 0.6V ≤ V _O ≤ (V+) − 0.6V, R _L = 600Ω		110	114		90	93		dB
FREQUENCY RESPONSE										
Gain-Bandwidth Product	GBW	G = 100			80			80		MHz
		G = 1			45			45		MHz
Slew Rate	SR				27			27		V/μs
Settling Time, 0.01%	t _S	V _S = ±15V, G = −1, 10V Step, C _L = 100pF			490			580		ns
0.0015% (16-bit)		V _S = ±15V, G = −1, 10V Step, C _L = 100pF			700			750		ns
Overload Recovery Time		G = −10			500			500		ns
Total Harmonic Distortion + Noise	THD+N	G = 1, f = 1kHz, V _O = 3V _{RMS} , R _L = 600Ω			0.000015			0.000015		%
					−136			−136		dB

(1) The OPA211-HT is not intended to be used as a comparator due to its limited differential input range capability.

ELECTRICAL CHARACTERISTICS: $V_S = \pm 2.25\text{ V}$ to $\pm 18\text{ V}$ (continued)

At $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

		$T_A = -55\text{ to }125^\circ\text{C}$			$T_A = 210^\circ\text{C}$					
PARAMETER		CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT	
OUTPUT										
Voltage Output	V_{OUT}	$R_L = 10\text{k}\Omega$, $A_{OL} \geq 114\text{dB}$	$(V-) + 0.2$		$(V+) - 0.2$	$(V-) + 0.2$		$(V+) - 0.2$	V	
		$R_L = 600\Omega$, $A_{OL} \geq 110\text{dB}$, $\pm 18\text{V}$	$(V-) + 0.6$		$(V+) - 0.6$	$(V-) + 1.2$		$(V+) - 0.6$	V	
Short-Circuit Current	I_{SC}		+35/−50			+30/−45			mA	
Capacitive Load Drive	C_{LOAD}		See Typical Characteristics							
Open-Loop Output Impedance	Z_O	$f = 1\text{MHz}$	5							Ω
POWER SUPPLY										
Specified Voltage	V_S		± 2.25		± 18	± 2.25		± 18	V	
Quiescent Current (per channel)	I_Q	$I_{OUT} = 0\text{A}$		3.6	6		6.0	7.5	mA	
TEMPERATURE RANGE										
Specified range		-55°C to 210°C								
Operating range		-55°C to 210°C								

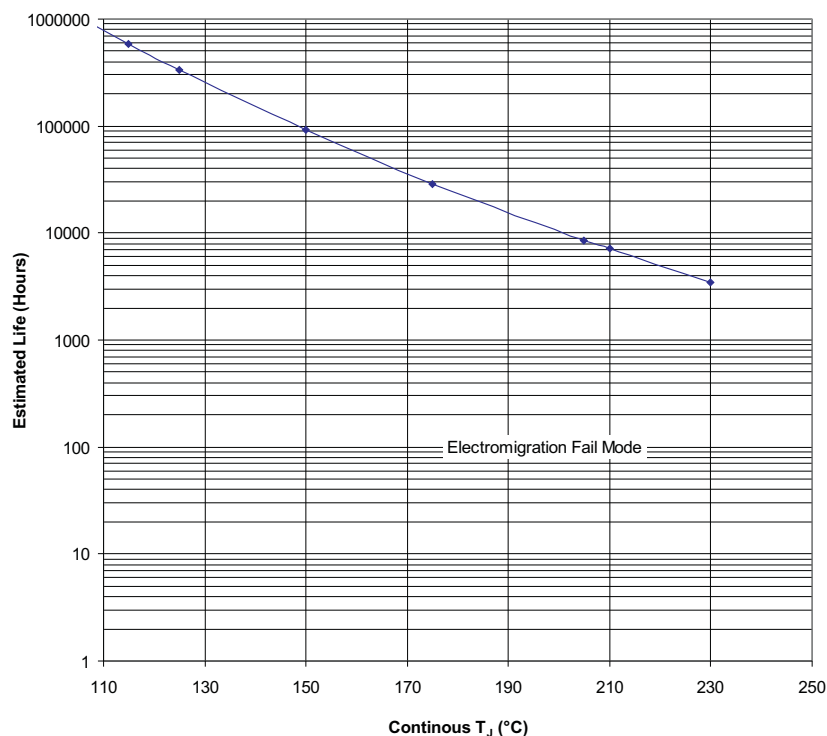


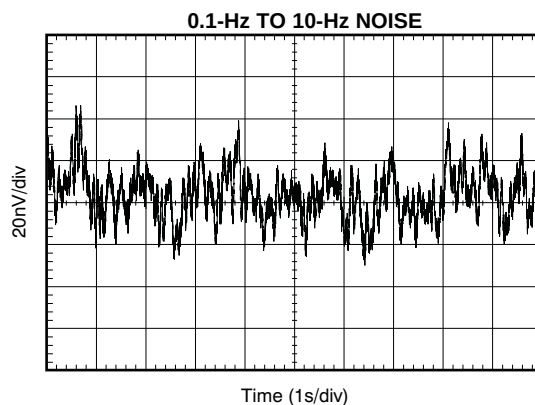
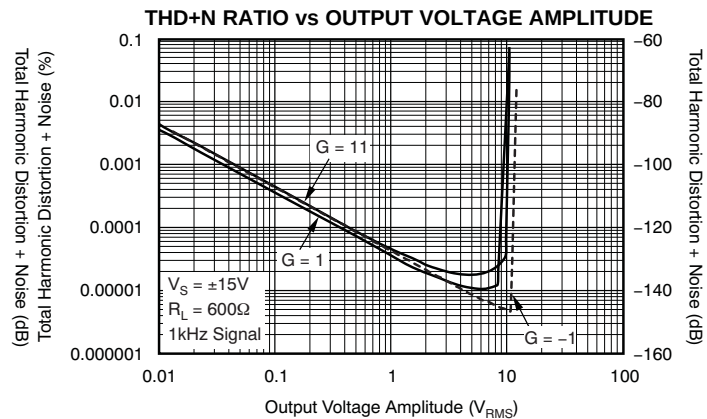
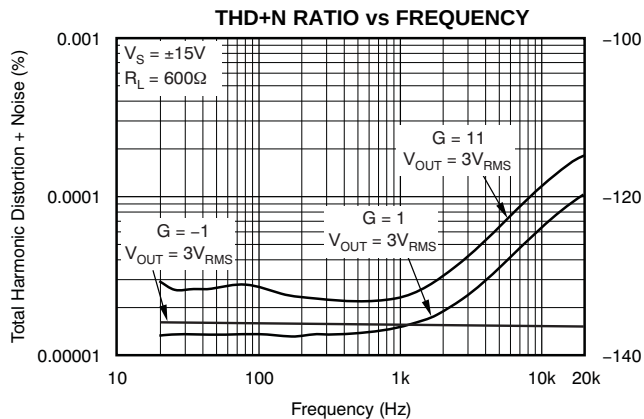
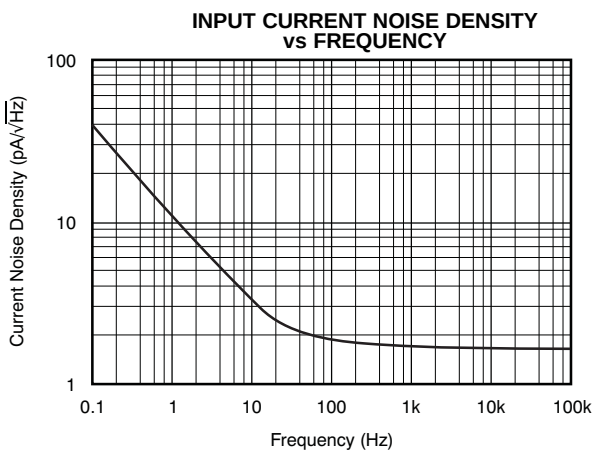
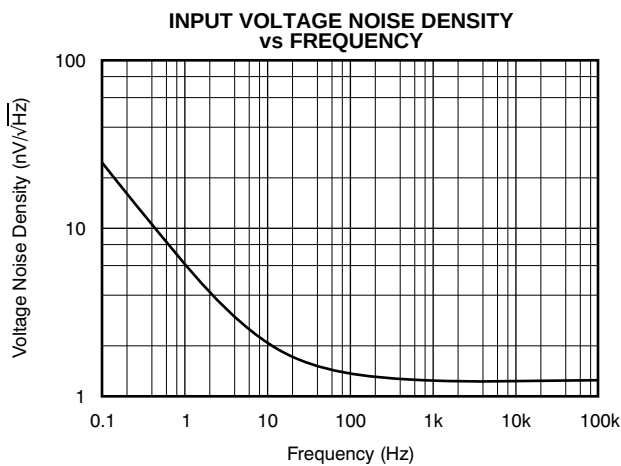
Figure 1. OPA211SKGD1 Operating Life Derating Chart

Notes:

- See datasheet for absolute maximum and minimum recommended operating conditions.
- Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

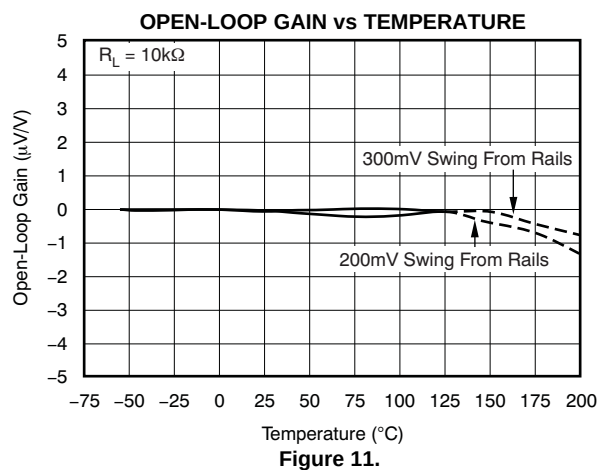
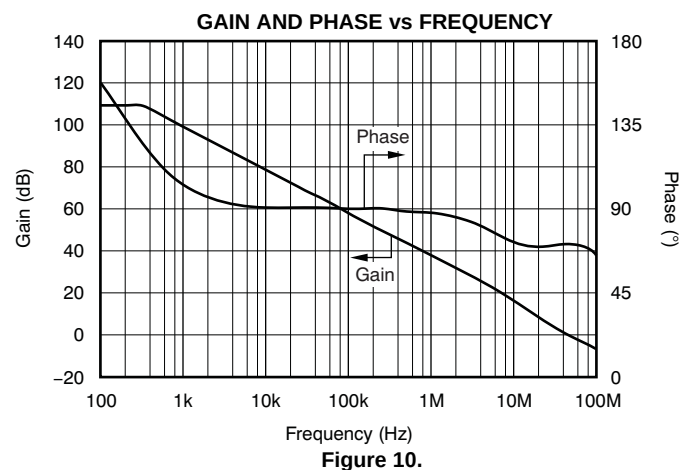
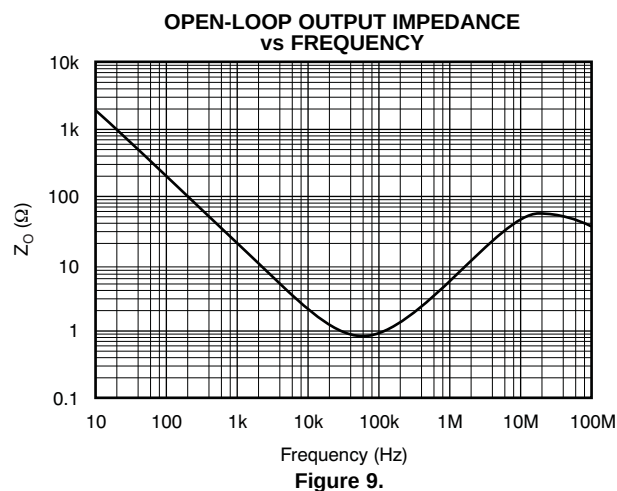
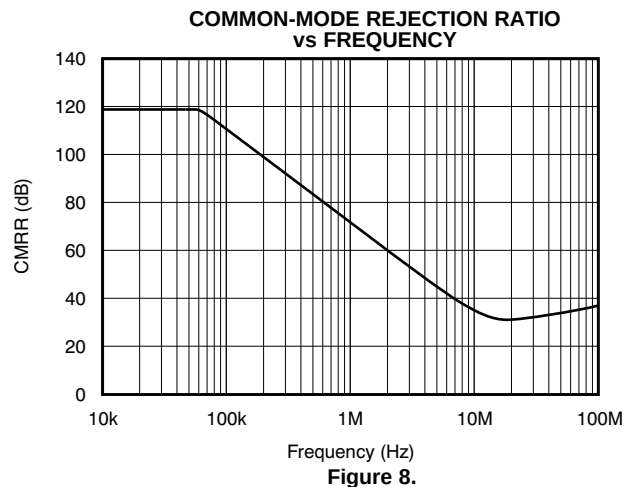
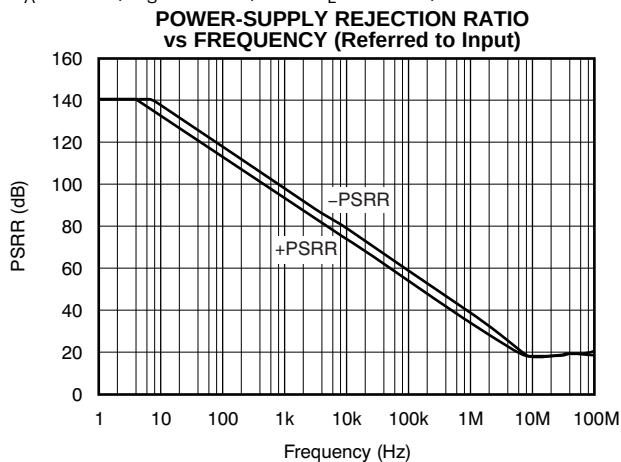
TYPICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.



TYPICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.



TYPICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

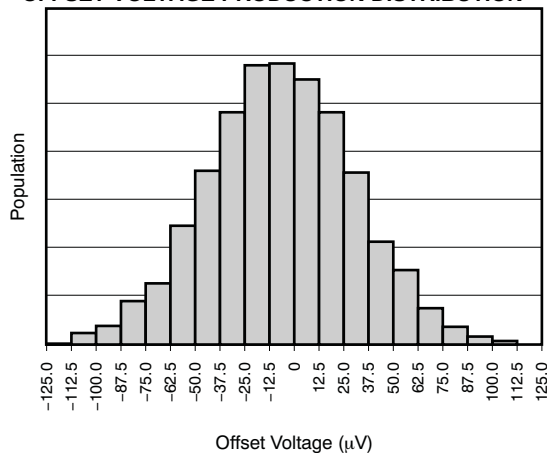


Figure 12.

OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION

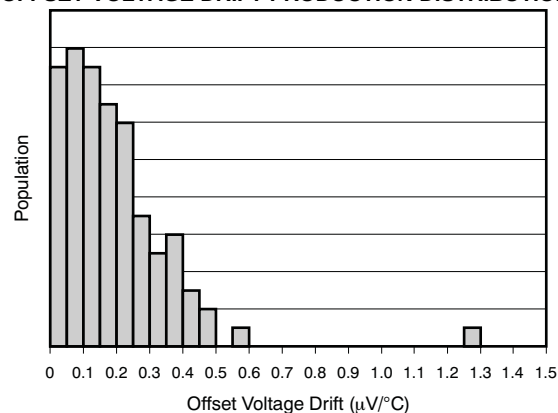


Figure 13.

**I_B AND I_{OS} CURRENT
vs
TEMPERATURE**

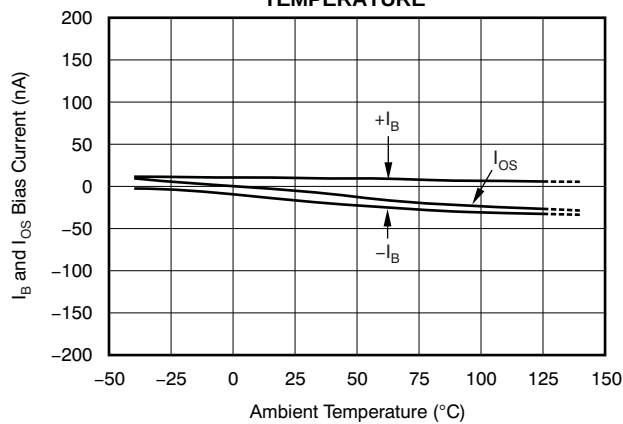


Figure 14.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

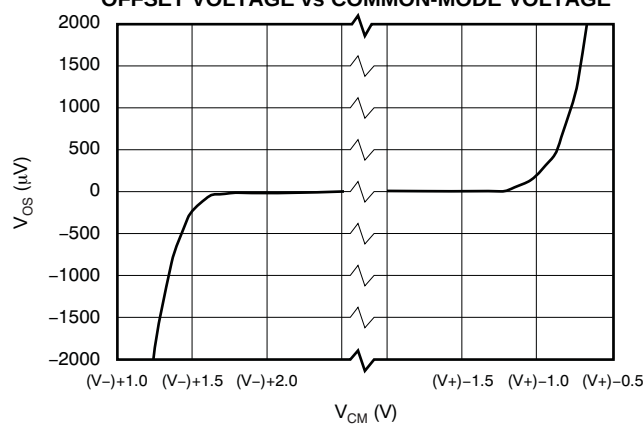


Figure 15.

V_{OS} WARMUP

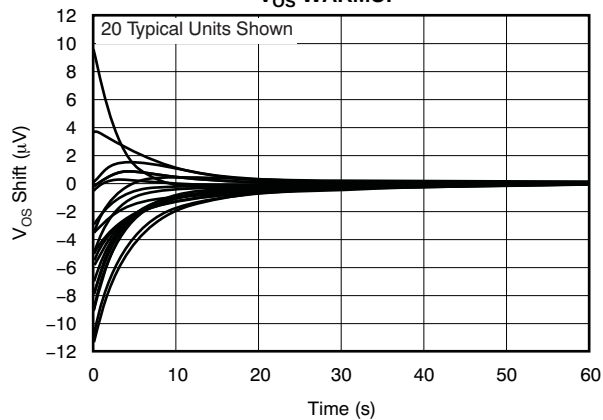


Figure 16.

INPUT OFFSET CURRENT vs SUPPLY VOLTAGE

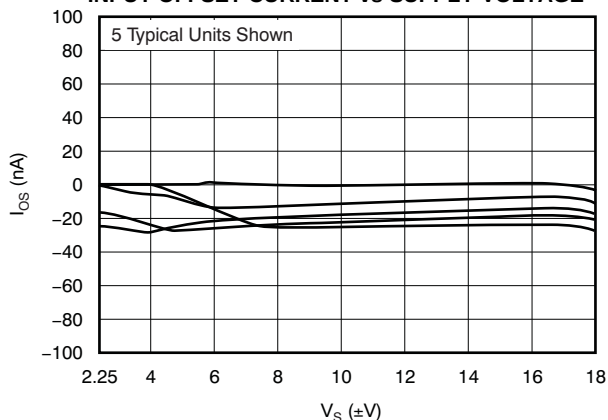


Figure 17.

TYPICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

INPUT OFFSET CURRENT vs COMMON-MODE VOLTAGE

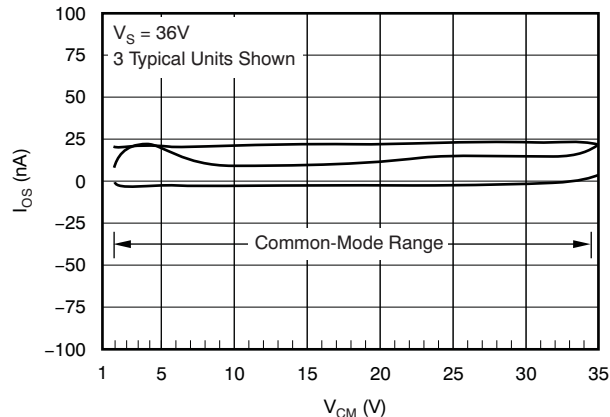


Figure 18.

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

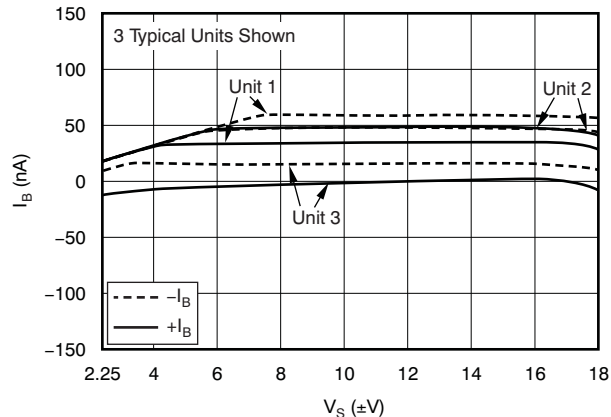


Figure 19.

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

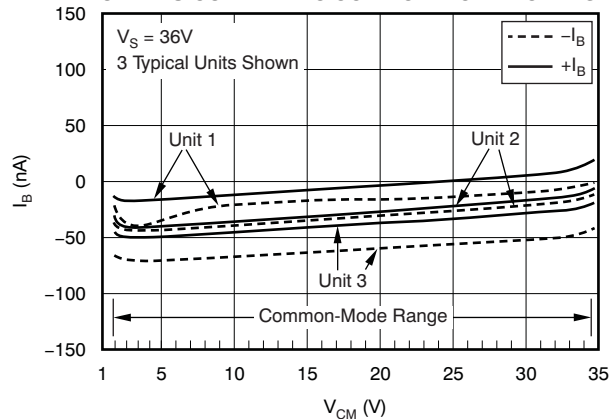


Figure 20.

QUIESCENT CURRENT vs TEMPERATURE

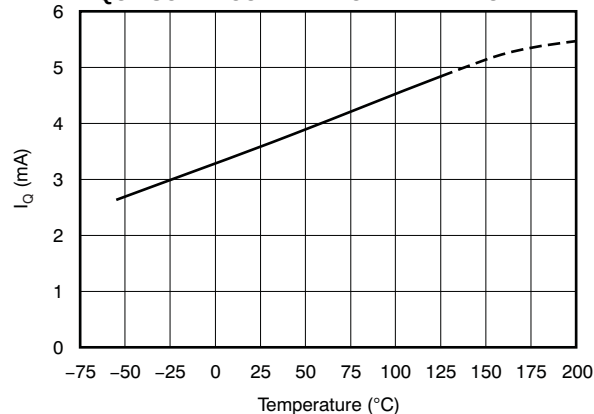


Figure 21.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

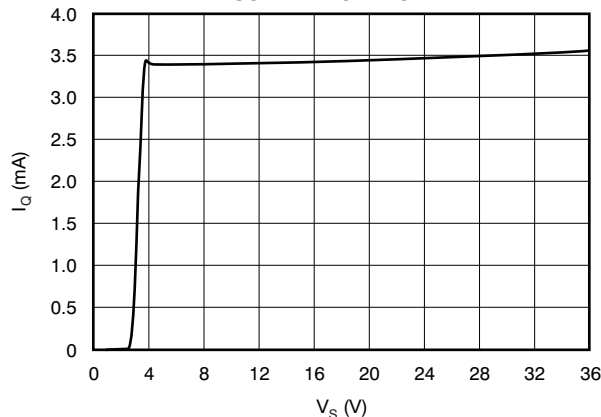


Figure 22.

NORMALIZED QUIESCENT CURRENT vs TIME

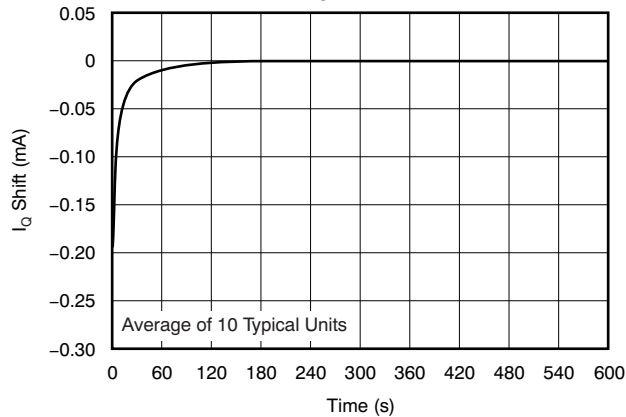


Figure 23.

TYPICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

**SHORT-CIRCUIT CURRENT
vs TEMPERATURE**

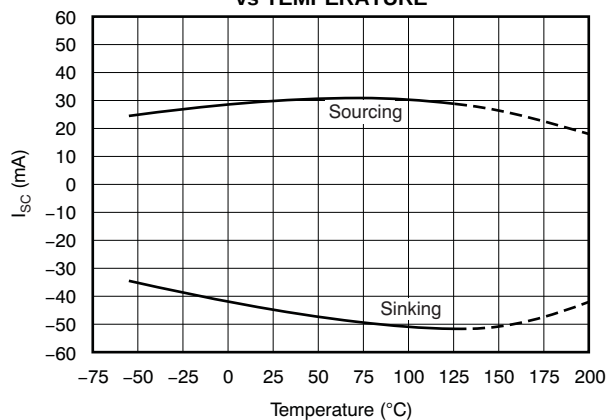


Figure 24.

**SMALL-SIGNAL STEP RESPONSE
(100 mV)**

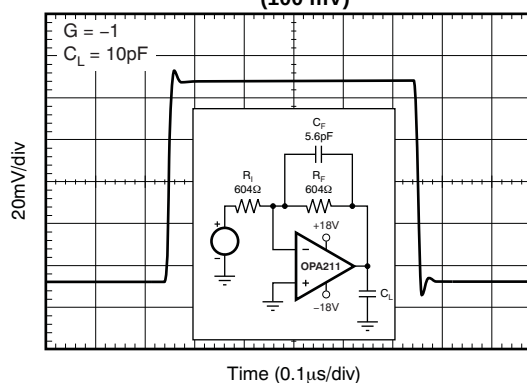


Figure 25.

**SMALL-SIGNAL STEP RESPONSE
(100 mV)**

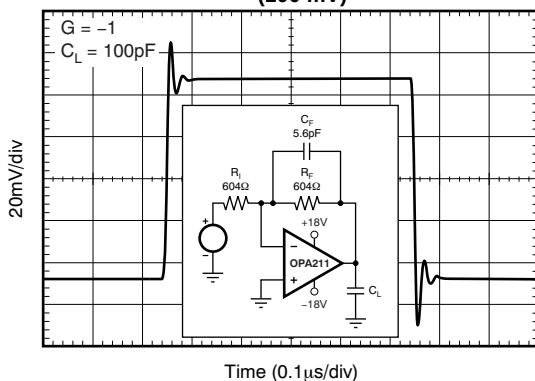


Figure 26.

**SMALL-SIGNAL STEP RESPONSE
(100 mV)**

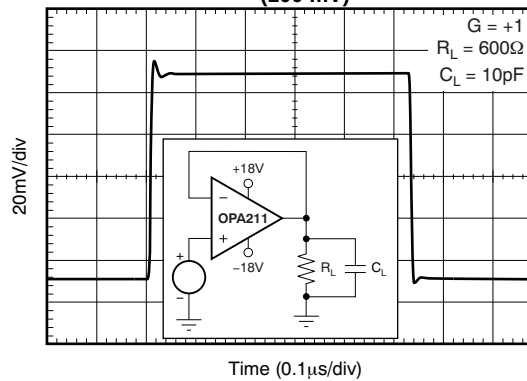


Figure 27.

**SMALL-SIGNAL STEP RESPONSE
(100 mV)**

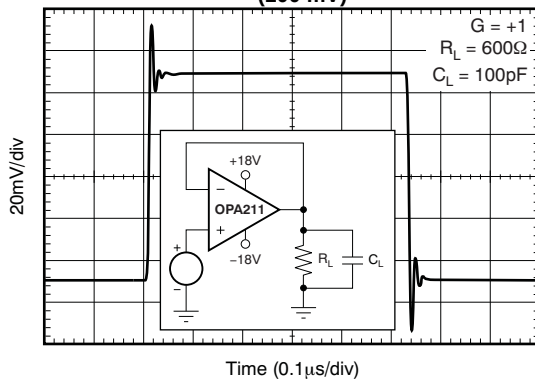


Figure 28.

**SMALL-SIGNAL OVERSHOOT
vs CAPACITIVE LOAD (100-mV Output Step)**

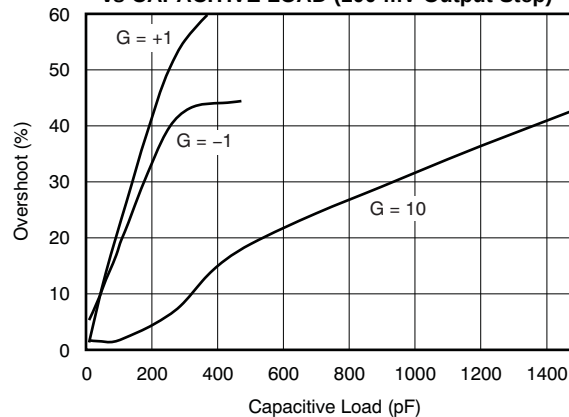


Figure 29.

TYPICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

LARGE-SIGNAL STEP RESPONSE

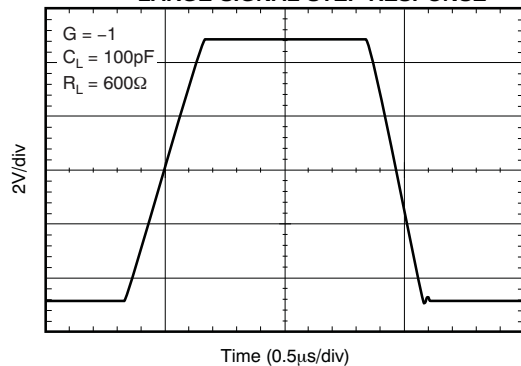


Figure 30.

LARGE-SIGNAL STEP RESPONSE

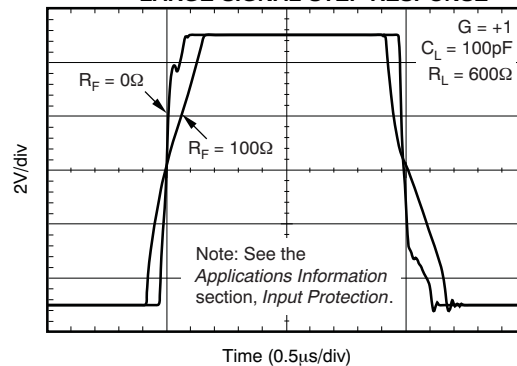


Figure 31.

LARGE-SIGNAL POSITIVE SETTLING TIME
(10 V_{PP} , $C_L = 100\text{ pF}$)

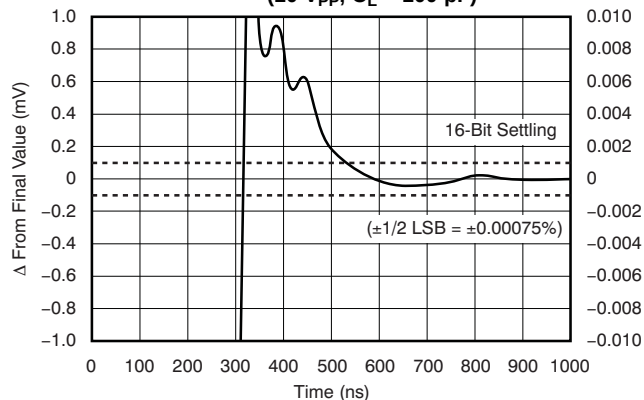


Figure 32.

LARGE-SIGNAL POSITIVE SETTLING TIME
(10 V_{PP} , $C_L = 10\text{ pF}$)

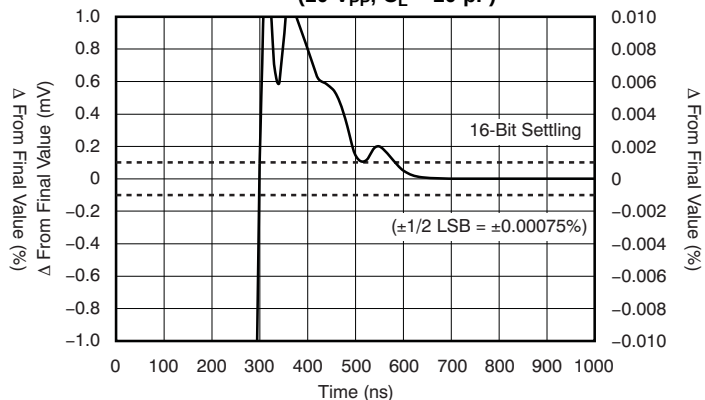


Figure 33.

LARGE-SIGNAL NEGATIVE SETTLING TIME
(10 V_{PP} , $C_L = 100\text{ pF}$)

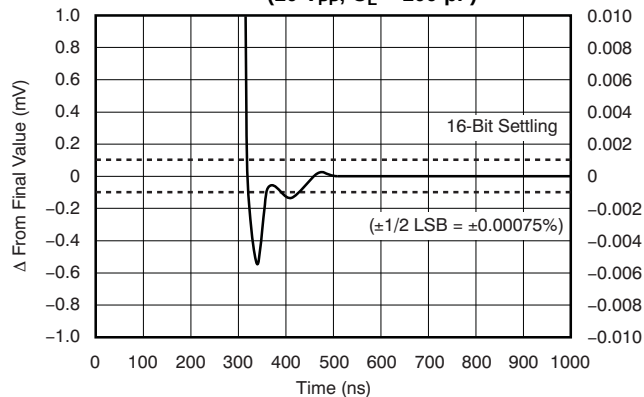


Figure 34.

LARGE-SIGNAL NEGATIVE SETTLING TIME
(10 V_{PP} , $C_L = 10\text{ pF}$)

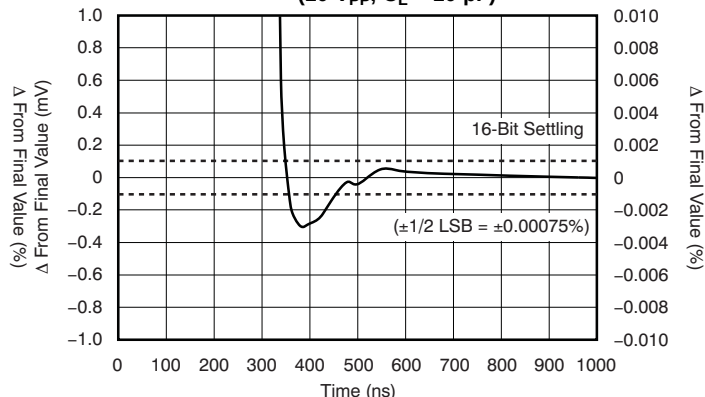


Figure 35.

TYPICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

NEGATIVE OVERLOAD RECOVERY

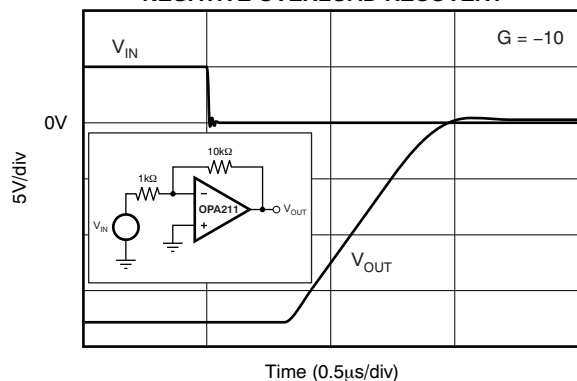


Figure 36.

POSITIVE OVERLOAD RECOVERY

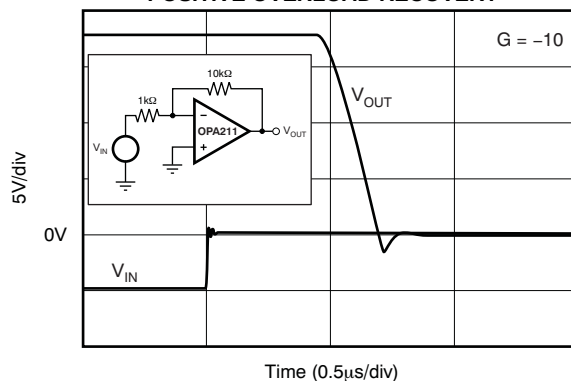


Figure 37.

OUTPUT VOLTAGE vs OUTPUT CURRENT

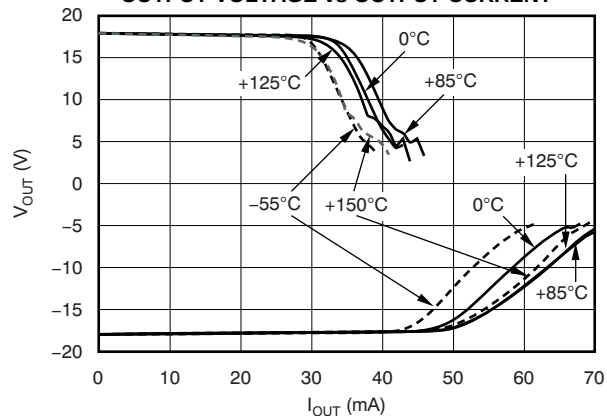


Figure 38.

NO PHASE REVERSAL

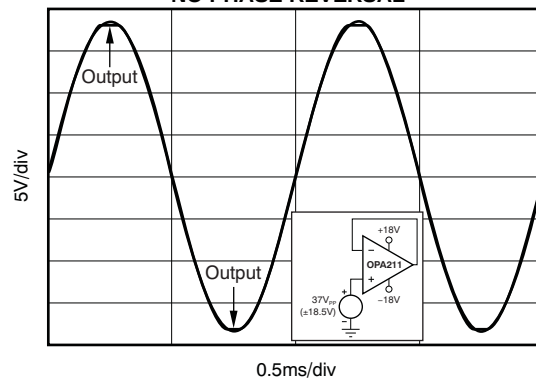


Figure 39.

TURN-OFF TRANSIENT

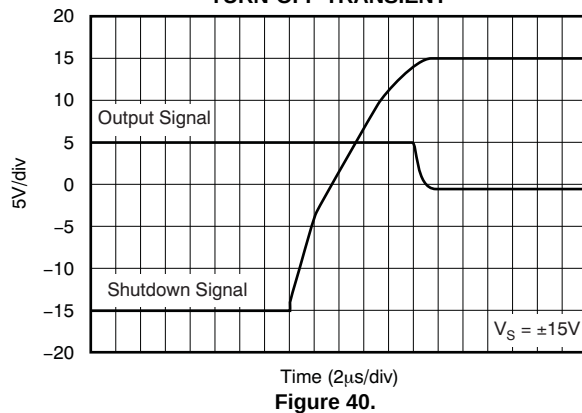


Figure 40.

TURN-ON TRANSIENT

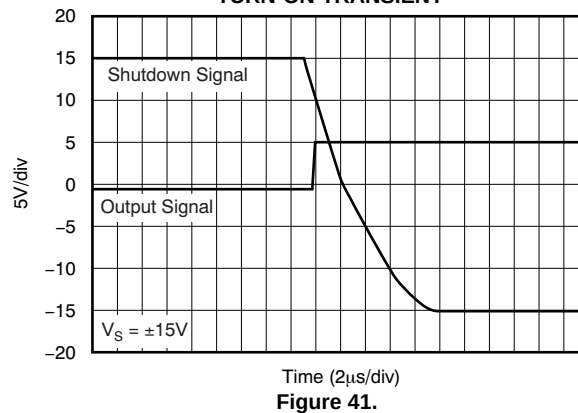


Figure 41.

TYPICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

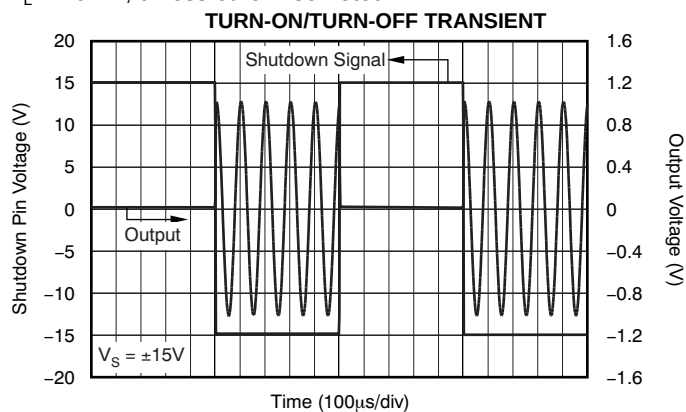


Figure 42.

APPLICATION INFORMATION

The OPA211 is a unity-gain stable, precision op amp with very low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1- μ F capacitors are adequate. [Figure 43](#) shows a simplified schematic of the OPA211. This die uses a SiGe bipolar process and contains 180 transistors.

OPERATING VOLTAGE

OPA211 series op amps operate from ± 2.25 -V to ± 18 -V supplies while maintaining excellent performance. The OPA211 series can operate with as little as 4.5 V between the supplies and with up to 36 V between the supplies. However, some applications

do not require equal positive and negative output voltage swing. With the OPA211 series, power-supply voltages do not need to be equal. For example, the positive supply could be set to 25 V with the negative supply at -5 V or vice-versa.

The common-mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range, $T_A = -55^\circ\text{C}$ to 210°C . Parameters that vary significantly with operating voltage or temperature are shown in the [Typical Characteristics](#).

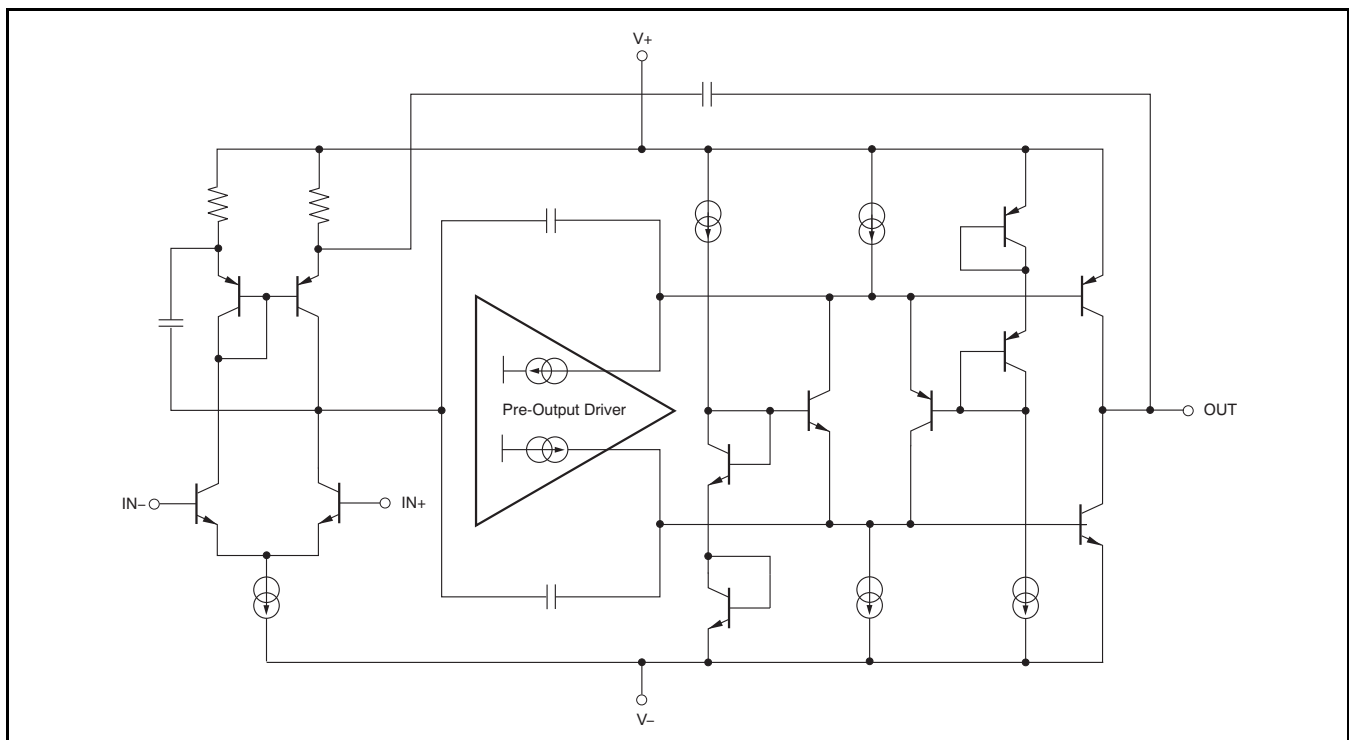


Figure 43. OPA211 Simplified Schematic

INPUT PROTECTION

The input terminals of the OPA211 are protected from excessive differential voltage with back-to-back diodes, as shown in Figure 44. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or $G = 1$ circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is illustrated in Figure 31 of the Typical Characteristics. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA211, and is discussed in the [Noise Performance](#) section of this data sheet. Figure 44 shows an example implementing a current-limiting feedback resistor.

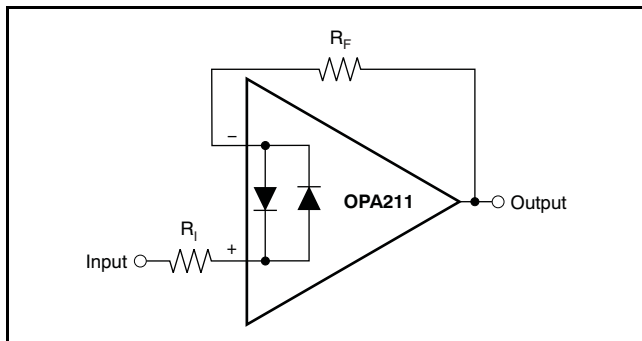


Figure 44. Pulsed Operation

NOISE PERFORMANCE ⁽¹⁾

Figure 45 shows total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). Two different op amps are shown with total circuit noise calculated. The OPA211 has very low voltage noise, making it ideal for low source impedances (less than 2 kΩ). A similar precision op amp, the OPA227, has somewhat higher voltage noise but lower current noise. It provides excellent noise performance at moderate source impedance (10 kΩ to 100 kΩ). Above 100 kΩ, a FET-input op amp such as the OPA132 (very low current noise) may provide improved performance. The equation in Figure 45 is shown for the calculation of the total circuit noise. Note that e_n = voltage noise, i_n = current noise, R_S = source impedance, k = Boltzmann's constant = 1.38×10^{-23} J/K, and T is temperature in K.

(1) OPA227 and OPA132 have not been characterized or tested at 210°C.

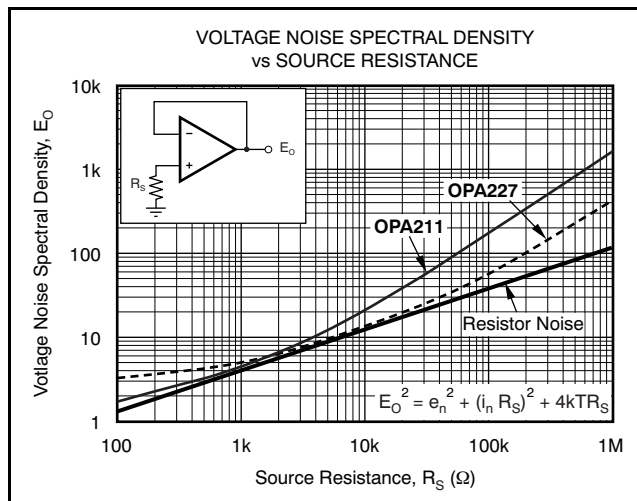


Figure 45. Noise Performance of the OPA211 and OPA227 in Unity-Gain Buffer Configuration

BASIC NOISE CALCULATIONS

Design of low-noise op amp circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the op amp, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 45. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 45 depicts total noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). The operational amplifier itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible and voltage noise generally dominates. For high source impedance, current noise may dominate.

Figure 46 illustrates both inverting and noninverting op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

TOTAL HARMONIC DISTORTION MEASUREMENTS

OPA211 series op amps have excellent distortion characteristics. THD + Noise is below 0.0001% ($G = 1$, $V_O = 3 V_{RMS}$) throughout the audio frequency range, 20 Hz to 20 kHz, with a 600- Ω load.

The distortion produced by OPA211 series op amps is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit illustrated in Figure 47 can be used to extend the measurement capabilities.

Op amp distortion can be considered an internal error source that can be referred to the input. Figure 47 shows a circuit that causes the op amp distortion to be 101 times greater than that normally produced by the op amp. The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of

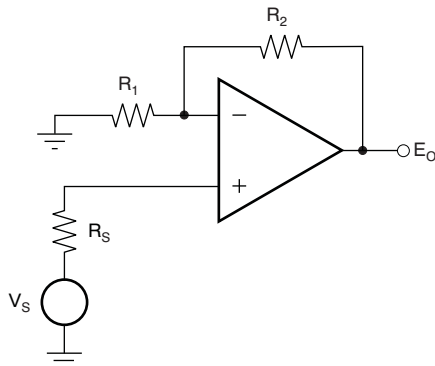
101, thus extending the resolution by 101. Note that the input signal and load applied to the op amp are the same as with conventional feedback without R_3 . The value of R_3 should be kept small to minimize its effect on the distortion measurements.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

SHUTDOWN

The shutdown (enable) function of the OPA211 is referenced to the positive supply voltage of the operational amplifier. A valid high disables the op amp. A valid high is defined as $(V+) - 0.35 V$ of the positive supply applied to the shutdown pin. A valid low is defined as $(V+) - 3 V$ below the positive supply pin. For example, with V_{CC} at $\pm 15 V$, the device is enabled at or below 12 V. The device is disabled at or above 14.65 V. If dual or split power supplies are used, care should be taken to ensure the valid high or valid low input signals are properly referred to the positive supply voltage. This pin must be connected to a valid high or low voltage or driven, and not left open-circuit. The enable and disable times are provided in the Typical Characteristics section (see Figure 40 through Figure 42). When disabled, the output assumes a high-impedance state.

Noise in Noninverting Gain Configuration



Noise at the output:

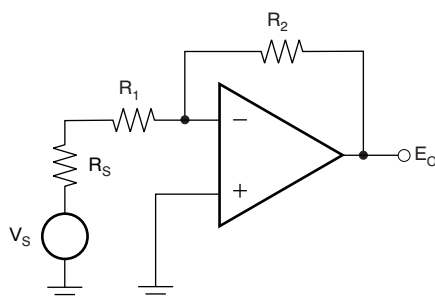
$$E_O^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2 + (i_n R_S)^2 \left(1 + \frac{R_2}{R_1}\right)^2$$

Where $e_S = \sqrt{4kTR_S} \times \left(1 + \frac{R_2}{R_1}\right)$ = thermal noise of R_S

$$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1}\right) = \text{thermal noise of } R_1$$

$$e_2 = \sqrt{4kTR_2} = \text{thermal noise of } R_2$$

Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1 + \frac{R_2}{R_1 + R_S}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2$$

Where $e_S = \sqrt{4kTR_S} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_S

$$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1 + R_S}\right) = \text{thermal noise of } R_1$$

$$e_2 = \sqrt{4kTR_2} = \text{thermal noise of } R_2$$

For the OPA211 series op amps at 1kHz, $e_n = 1.1\text{nV}/\sqrt{\text{Hz}}$ and $i_n = 1.7\text{pA}/\sqrt{\text{Hz}}$.

Figure 46. Noise Calculation in Gain Configurations

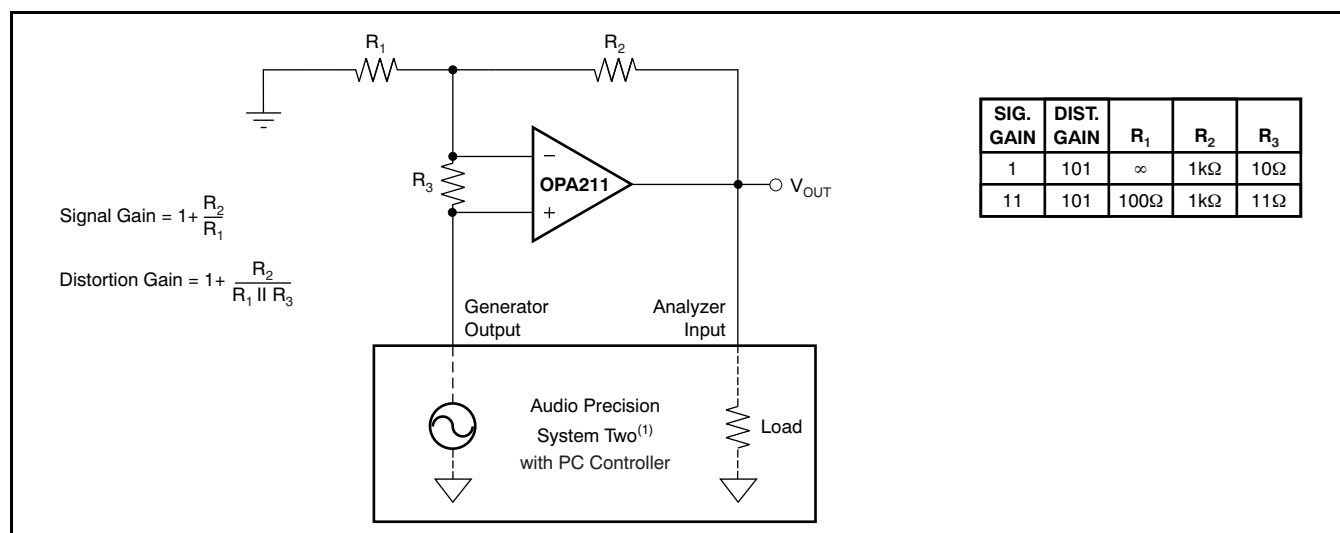


Figure 47. Distortion Test Circuit

ELECTRICAL OVERSTRESS

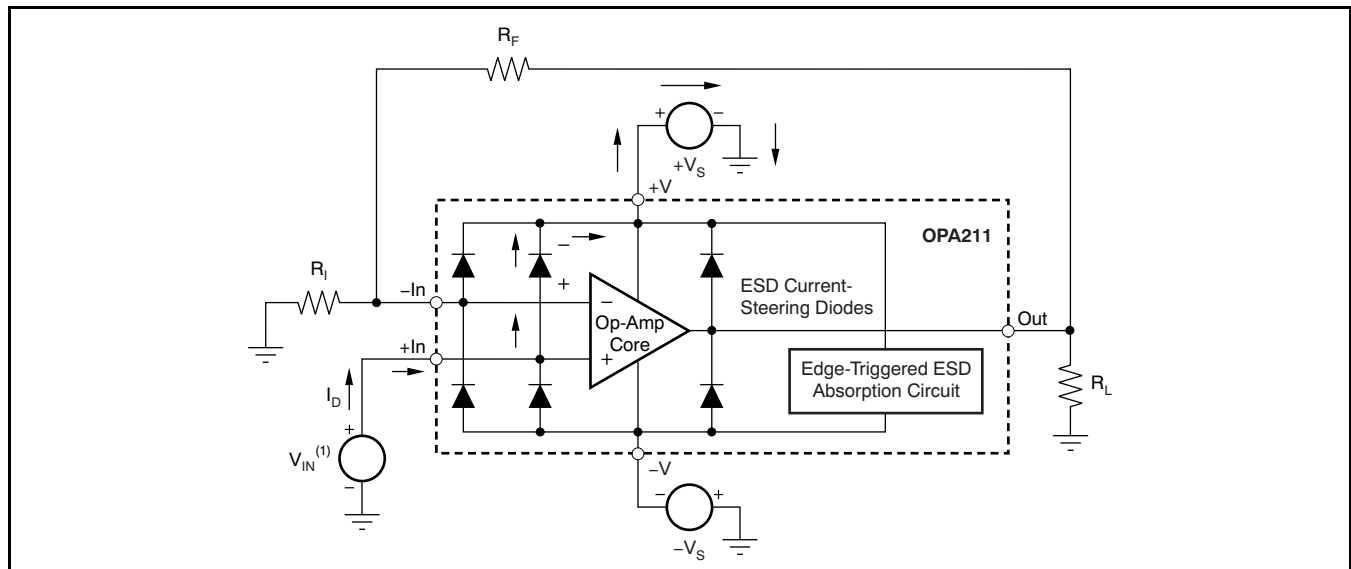
Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. Figure 48 illustrates the ESD circuits contained in the OPA211 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA211 but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as that illustrated in Figure 48, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.



(1) $V_{IN} = +V_S + 500\text{mV}$.

Figure 48. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application

Figure 48 depicts a specific example where the input voltage, V_{IN} , exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V_S can sink the current, one of the upper input steering diodes conducts and directs current to V_S . Excessively high current levels can flow with increasingly higher V_{IN} . As a result, the datasheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings. In extreme but rare cases, the absorption device triggers on while V_S and $-V_S$ are applied. If this event happens, a direct current path is established between the V_S and $-V_S$ supplies. The power dissipation of the absorption device is quickly exceeded, and the extreme internal heating destroys the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies V_S and/or $-V_S$ are at 0 V. Again, it depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

DFN PACKAGE

The OPA211 is offered in an DFN-8 package (also known as SON). The DFN package is a QFN package with lead contacts on only two sides of the bottom of the package. This leadless package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

DFN packages are physically small, and have a smaller routing area, improved thermal performance, and improved electrical parasitics. Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can be easily mounted using standard printed circuit board (PCB) assembly techniques. See Application Note *QFN/SON PCB Attachment* (SLUA271) and Application Report *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download at www.ti.com.

The exposed leadframe die pad on the bottom of the package must be connected to V-. Soldering the thermal pad improves heat dissipation and enables specified device performance.

DFN LAYOUT GUIDELINES

The exposed leadframe die pad on the DFN package should be soldered to a thermal pad on the PCB. A mechanical drawing showing an example layout is attached at the end of this data sheet. Refinements to this layout may be necessary based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heatsink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA211SHKJ	Active	Production	CFP (HKJ) 8	25 TUBE	Yes	Call TI	N/A for Pkg Type	-55 to 210	OPA211S HKJ
OPA211SHKQ	Active	Production	CFP (HKQ) 8	25 TUBE	Yes	AU	N/A for Pkg Type	-55 to 210	OPA211S HKQ
OPA211SKGD1	Active	Production	XCEPT (KGD) 0	400 NOT REQUIRED	Yes	Call TI	N/A for Pkg Type	-55 to 210	

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA211-HT :

- Catalog : [OPA211](#)
- Enhanced Product : [OPA211-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TUBE

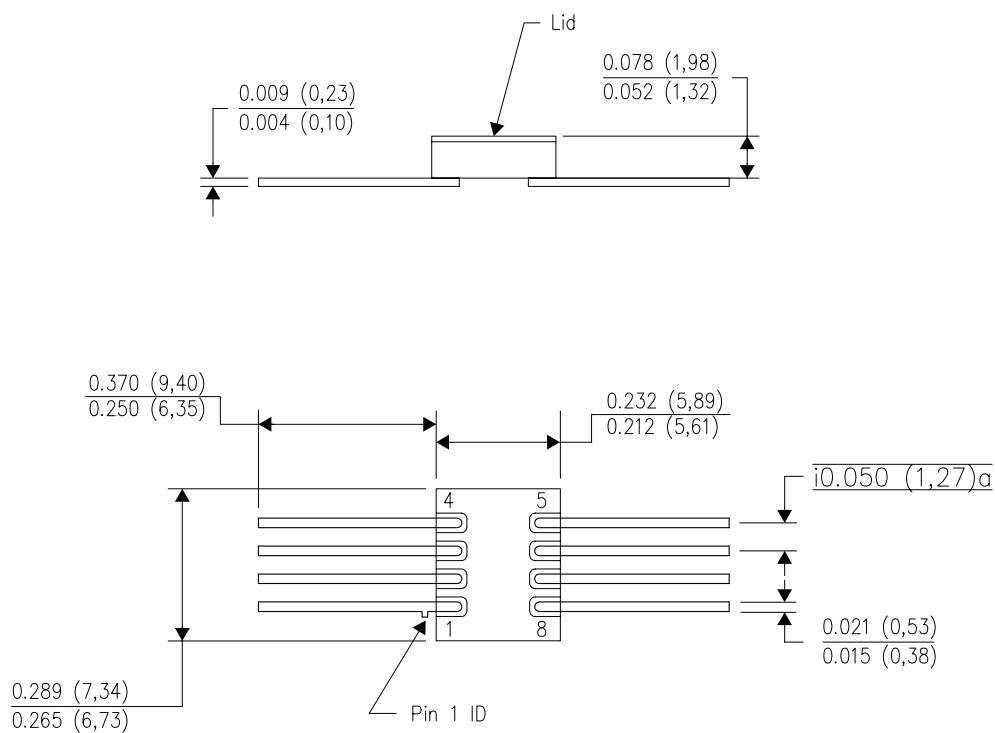


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA211SHKJ	HKJ	CFP	8	25	506.98	26.16	6220	NA
OPA211SHKQ	HKQ	CFP	8	25	506.98	26.16	6220	NA

HKJ (R-CDFP-F8)

CERAMIC DUAL FLATPACK



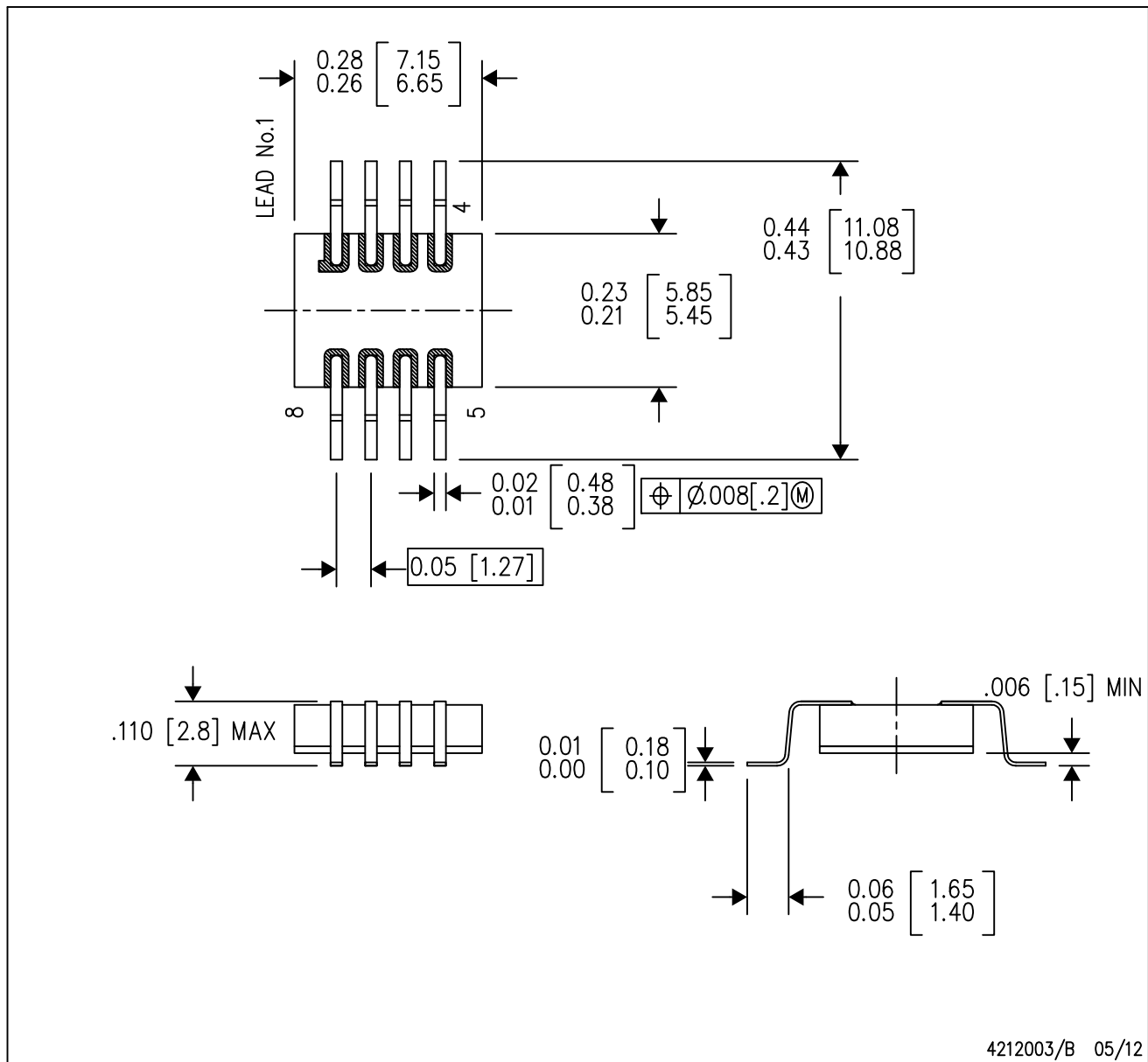
4209892/A 10/08

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals will be gold plated.

MECHANICAL DATA

HKQ (R-CDFP-G8)

CERAMIC GULL WING



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals will be gold plated.
 - E. Lid is not connected to any lead.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025