OPAx171 36V, Single-Supply, SOT-553, General-Purpose Operational Amplifiers

1 Features

- Supply range: 2.7V to 36V, ±1.35V to ±18V
- Low noise: 14nV/√Hz
- Low offset drift: ±0.3µV/°C (Typical)
- RFI filtered inputs
- Input range includes the negative supply
- Input range operates to positive supply
- Rail-to-rail output
- Gain bandwidth: 3MHz
- Low quiescent current: 475µA per amplifier
- High common-mode rejection: 120dB (typical)
- Low-input bias current: 8pA
- Industry-standard packages:
  - 5-pin SOT-23
  - 8-pin SOIC
  - 14-pin TSSOP
- *micro*Packages:
  - Single in SOT-553
  - Dual in VSSOP-8

2 Applications

- Tracking amplifier in power modules
- Merchant power supplies
- Transducer amplifiers
- Bridge amplifiers
- Temperature measurements
- Strain gauge amplifiers
- Precision integrators
- Battery-powered instruments
- Test equipment

3 Description

The OPA171, OPA2171, and OPA4171 (OPAx171) are a family of 36V, single-supply, low-noise operational amplifiers with the ability to operate on supplies ranging from 2.7V (±1.35V) to 36V (±18V). These devices are available in micro-packages and offer low offset, drift, and bandwidth with low quiescent current. The single, dual, and quad versions all have identical specifications for maximum design flexibility.

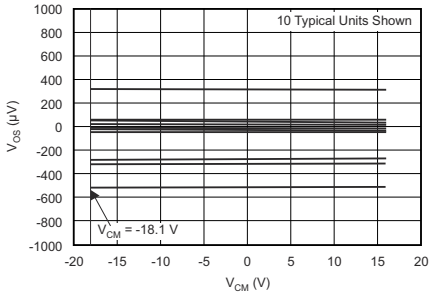
Unlike most operational amplifiers, which are specified at only one supply voltage, the OPAx171 family is specified from 2.7V to 36V. Input signals beyond the supply rails do not cause phase reversal. The OPAx171 family is stable with capacitive loads up to 300pF. The input can operate 100mV below the negative rail and within 2V of the top rail during normal operation. These devices can operate with full rail-to-rail input 100mV beyond the top rail, but with reduced performance within 2V of the top rail.

The OPAx171 series of operational amplifiers are specified from –40°C to +125°C.

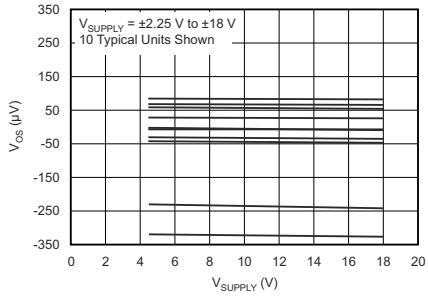
Package Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)	PACKAGE SIZE(2)
OPA171	Single	D (SOIC, 8)	4.9mm × 6mm
		DBV (SOT-23, 5)	2.9mm × 2.8mm
		DRL (SOT-5X3, 5)	1.6mm × 1.6mm
OPA2171	Dual	D (SOIC, 8)	4.9mm × 6mm
		DCU (VSSOP, 8)	2mm × 3.1mm
		DGK (VSSOP, 8)	3mm × 4.9mm
OPA4171	Quad	PW (TSSOP, 14)	5mm × 6.4mm
		D (SOIC, 14)	8.65mm × 6mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Offset Voltage vs Common-Mode Voltage



Offset Voltage vs Power Supply

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

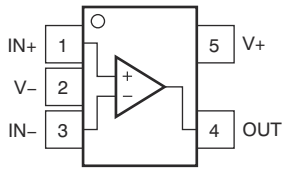


Figure 4-1. OPA171 DRL Package: 5-Pin SOT-553 (Top View)

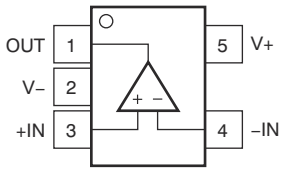
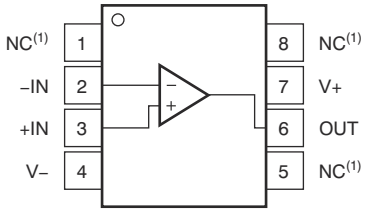


Figure 4-2. OPA171 DBV Package: 5-Pin SOT-23 (Top View)



A. NC- no internal connection

Figure 4-3. OPA171 D Package: 8-Pin SOIC (Top View)

Pin Functions: OPA171

PIN				TYPE	DESCRIPTION
NAME	DRL	DBV	D		
+IN	1	3	3	I	Noninverting input
–IN	3	4	2	I	Inverting input
OUT	4	1	6	O	Output
V+	5	5	7	—	Positive (highest) supply
V–	2	2	4	—	Negative (lowest) supply
NC	—	—	1, 5, 8	—	No internal connection (can be left floating)

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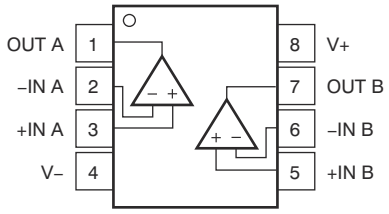


Figure 4-4. OPA2171 D, DCU, and DCK Packages: 8-Pin SO and VSSOP (Top View)

Table 4-1. Pin Functions: OPA2171

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input
+IN B	5	I	Noninverting input
–IN A	2	I	Inverting input
–IN B	6	O	Inverting input
OUT A	1	O	Output
OUT B	7	—	Output
V+	8	—	Positive (highest) supply
V–	4	—	Negative (lowest) supply

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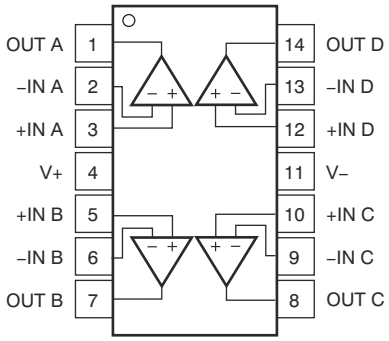


Figure 4-5. OPA4171 D and PW Packages: 14-Pin SO and TSSOP (Top View)

Table 4-2. Pin Functions: OPA4171

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input
+IN B	5	I	Noninverting input
+IN C	10	I	Noninverting input
+IN D	12	I	Noninverting input
–IN A	2	I	Inverting input
–IN B	6	I	Inverting input
–IN C	9	I	Inverting input
–IN D	13	I	Inverting input
OUT A	1	O	Output
OUT B	7	O	Output
OUT C	8	O	Output
OUT D	14	O	Output
V+	4	—	Positive (highest) supply
V–	11	—	Negative (lowest) supply

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range, (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage		0	40	V
Signal input terminals	Voltage	(V–) – 0.5	(V+) + 0.5	V
	Current	–10	10	mA
Output short circuit(2)		Continuous		
Operating temperature		–55	150	°C
Junction temperature			150	°C
Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V+ – V–)	4.5 (±2.25)		36 (±18)	V
Specified temperature	–40		125	°C

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5.4 Thermal Information: OPA171

THERMAL METRIC[1]		OPA171			UNIT
		D (SO)	DBV (SOT-23)	DRL (SOT-553)	
		8 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	149.5	245.8	208.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	97.9	133.9	0.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.7	83.6	42.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	35.5	18.2	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	89.5	83.1	42.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information: OPA2171

THERMAL METRIC[1]		OPA2171			UNIT
		D (SO)	DGK (VSSOP)	DCU (VSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.3	175.2	195.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	72.1	74.9	59.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.6	22.2	115.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.2	1.6	4.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.8	22.8	114.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report .

5.6 Thermal Information: OPA4171

THERMAL METRIC[1]		OPA4171		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.2	106.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	51.8	24.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	59.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.5	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.2	54.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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5.7 Electrical Characteristics

at T_A = 25°C, V_S = 2.7 to 36 V, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			0.25	±1.8	mV
	Over temperature	T_A = –40°C to +125°C		0.3	±2	mV
dV_{OS}/dT	Drift	T_A = –40°C to +125°C		0.3	±2	µV/°C
	vs power supply	V_S = 4 to 36 V T_A = –40°C to +125°C		1	±3	µV/V
	Channel separation, DC	DC		5		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current			±8	±15	pA
	Over temperature	T_A = –40°C to +125°C			±3.5	nA
I_{OS}	Input offset current			±4		pA
	Over temperature	T_A = –40°C to +125°C			±3.5	nA
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		3		μV_{PP}
e_n	Input voltage noise density	f = 100 Hz		25		nV/√Hz
		f = 1 kHz		14		nV/√Hz
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range		(V–) – 0.1 V		(V+) – 2 V	V
CMRR	Common-mode rejection ratio	V_S = ±2 V (V–) – 0.1 V < V_{CM} < (V+) – 2 V T_A = –40°C to +125°C	90	104		dB
		V_S = ±18 V (V–) – 0.1 V < V_{CM} < (V+) – 2 V T_A = –40°C to +125°C	104	120		dB
INPUT IMPEDANCE						
	Differential			100 || 3		MΩ || pF
	Common-mode			6 || 3		10^{12}Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 4 V to 36 V (V–) + 0.35 V < V_O < (V+) – 0.35 V T_A = –40°C to +125°C	110	130		dB
FREQUENCY RESPONSE						
GBP	Gain bandwidth product			3		MHz
SR	Slew rate	G = 1		1.5		V/µs
t_S	Settling time	To 0.1% V_S = ±18 V, G = 1 10-V step		6		µs
		To 0.01% (12 bit) V_S = ±18 V, G = 1 10-V step		10		µs
	Overload recovery time	V_{IN} × gain > V_S		2		µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz V_O = 3 V_{RMS}		0.0002%		
OUTPUT						

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at T_A = 25°C, V_S = 2.7 to 36 V, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Voltage output swing from rail	V_S = 5 V R_L = 10 kΩ		30		mV
	Over temperature	R_L = 10 kΩ A_{OL} ≥ 110 dB T_A = –40°C to +125°C	(V–) + 0.35		(V+) – 0.35	V
I_{SC}	Short-circuit current			+25/–35		mA
C_{LOAD}	Capacitive load drive			See *Section 5.9*		pF
R_O	Open-loop output resistance	f = 1 MHz I_O = 0 A		150		Ω
POWER SUPPLY						
V_S	Specified voltage range		2.7		36	V
I_Q	Quiescent current per amplifier	I_O = 0 A		475	595	µA
	Over temperature	I_O = 0 A T_A = –40°C to +125°C			650	µA
TEMPERATURE						
	Specified range		–40		125	°C
	Operating range		–55		150	°C

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5.8 Typical Characteristics: Table of Graphs

Table 5-1. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 5-1
Offset Voltage Drift Distribution	Figure 5-2
Offset Voltage vs Temperature	Figure 5-3
Offset Voltage vs Common-Mode Voltage	Figure 5-4
Offset Voltage vs Common-Mode Voltage (Upper Stage)	Figure 5-5
Offset Voltage vs Power Supply	Figure 5-6
I_B and I_{OS} vs Common-Mode Voltage	Figure 5-7
Input Bias Current vs Temperature	Figure 5-8
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 5-9
CMRR and PSRR vs Frequency (Referred-to Input)	Figure 5-10
CMRR vs Temperature	Figure 5-11
PSRR vs Temperature	Figure 5-12
0.1-Hz to 10-Hz Noise	Figure 5-13
Input Voltage Noise Spectral Density vs Frequency	Figure 5-14
THD+N Ratio vs Frequency	Figure 5-15
THD+N vs Output Amplitude	Figure 5-16
Quiescent Current vs Temperature	Figure 5-17
Quiescent Current vs Supply Voltage	Figure 5-18
Open-Loop Gain and Phase vs Frequency	Figure 5-19
Closed-Loop Gain vs Frequency	Figure 5-20
Open-Loop Gain vs Temperature	Figure 5-21
Open-Loop Output Impedance vs Frequency	Figure 5-22
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	Figure 5-23, Figure 5-24
No Phase Reversal	Figure 5-25
Positive Overload Recovery	Figure 5-26
Negative Overload Recovery	Figure 5-27
Small-Signal Step Response (100 mV)	Figure 5-28, Figure 5-29
Large-Signal Step Response	Figure 5-30, Figure 5-31
Large-Signal Settling Time (10-V Positive Step)	Figure 5-32
Large-Signal Settling Time (10-V Negative Step)	Figure 5-33
Short-Circuit Current vs Temperature	Figure 5-34
Maximum Output Voltage vs Frequency	Figure 5-35
Channel Separation vs Frequency	Figure 5-36

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5.9 Typical Characteristics

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

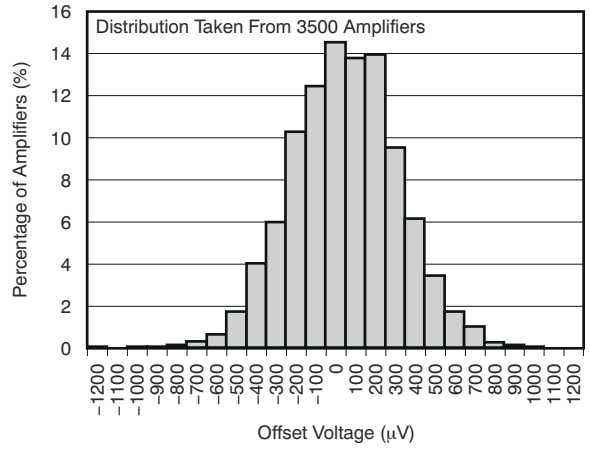


Figure 5-1. Offset Voltage Production Distribution

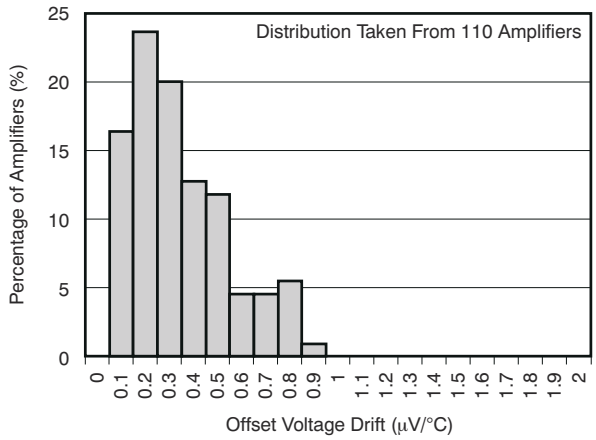


Figure 5-2. Offset Voltage Drift Distribution

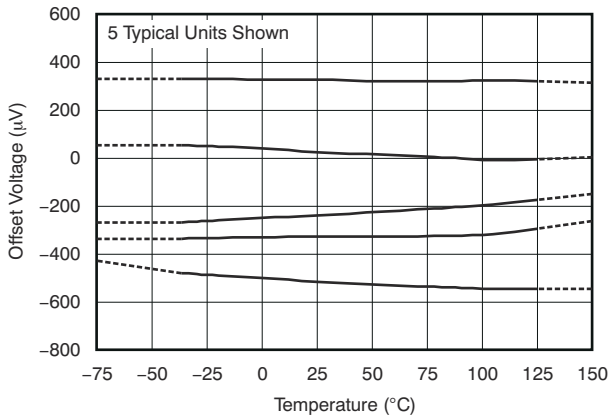


Figure 5-3. Offset Voltage vs Temperature

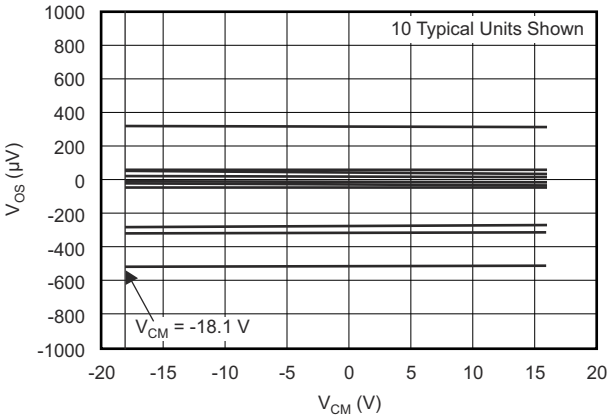


Figure 5-4. Offset Voltage vs Common-Mode Voltage

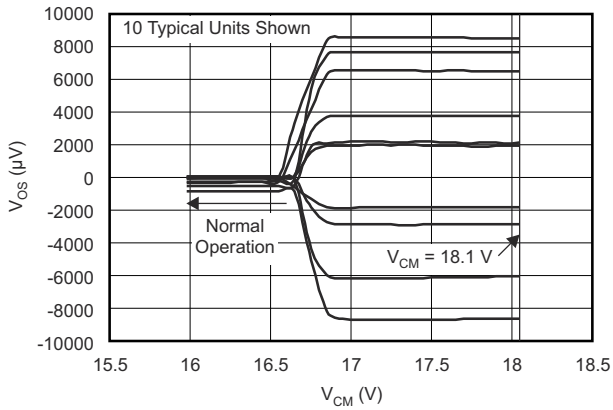


Figure 5-5. Offset Voltage vs Common-Mode Voltage (Upper Stage)

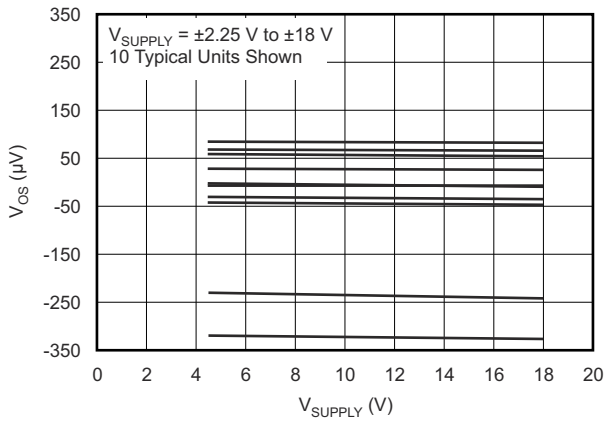


Figure 5-6. Offset Voltage vs Power Supply

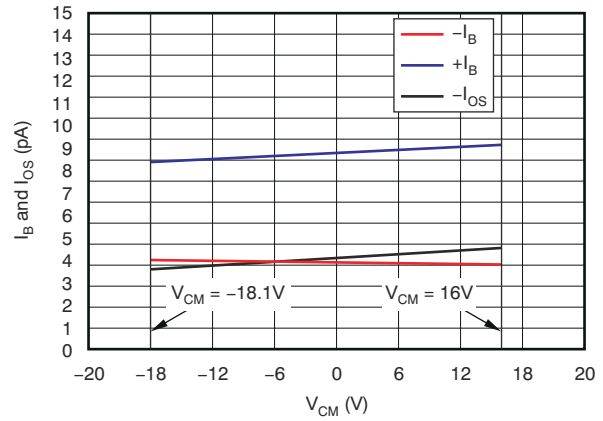


Figure 5-7. I_B and I_{OS} vs Common-Mode Voltage

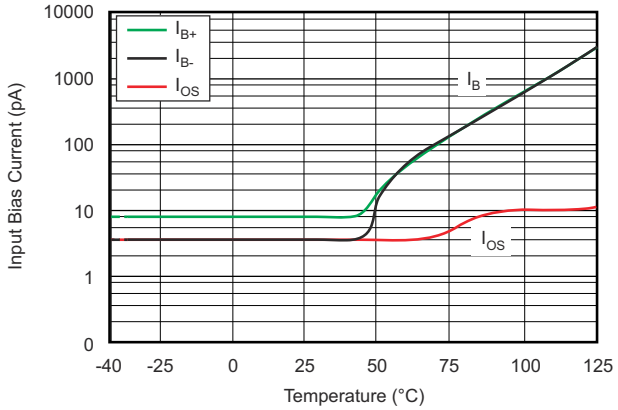


Figure 5-8. Input Bias Current vs Temperature

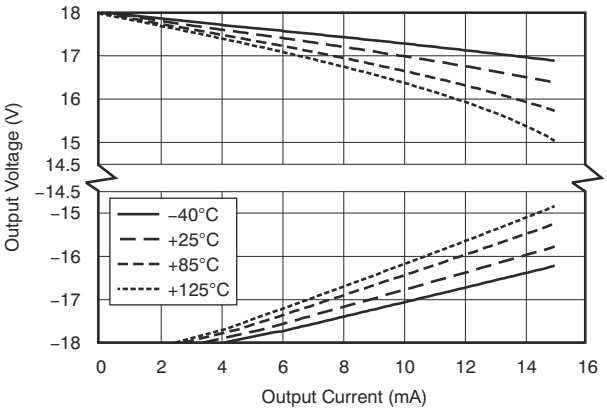


Figure 5-9. Output Voltage Swing vs Output Current (Maximum Supply)

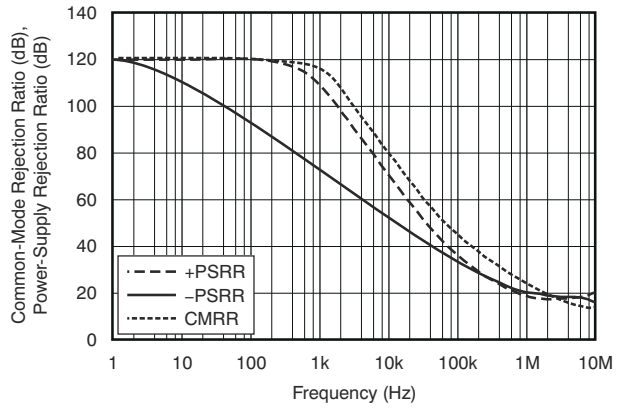


Figure 5-10. CMRR and PSRR vs Frequency (Referred-to Input)

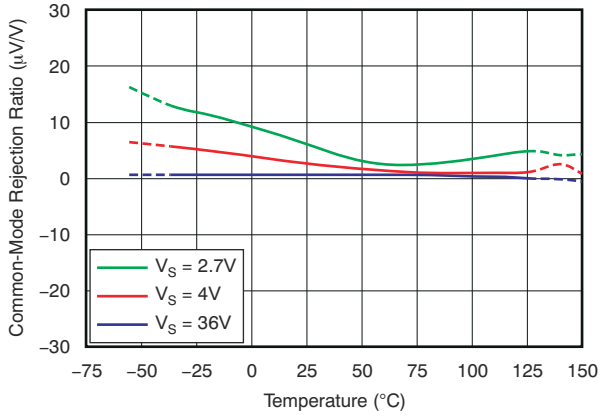


Figure 5-11. CMRR vs Temperature

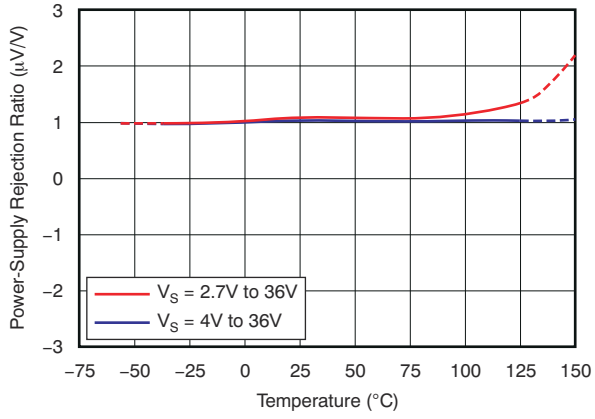


Figure 5-12. PSRR vs Temperature

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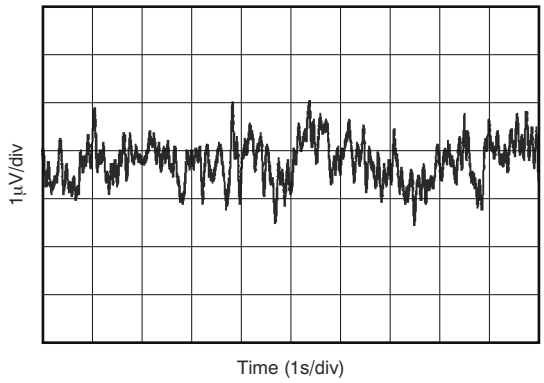


Figure 5-13. 0.1-Hz to 10-Hz Noise

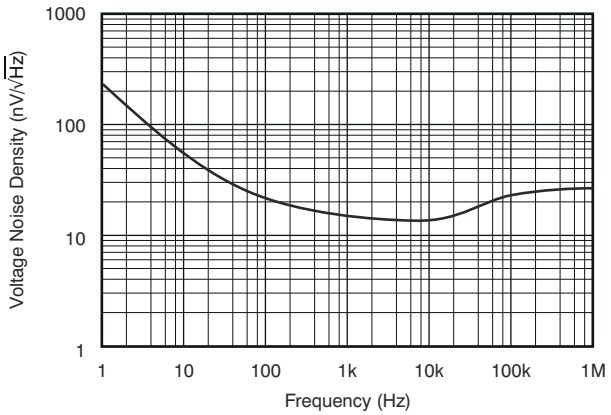


Figure 5-14. Input Voltage Noise Spectral Density vs Frequency

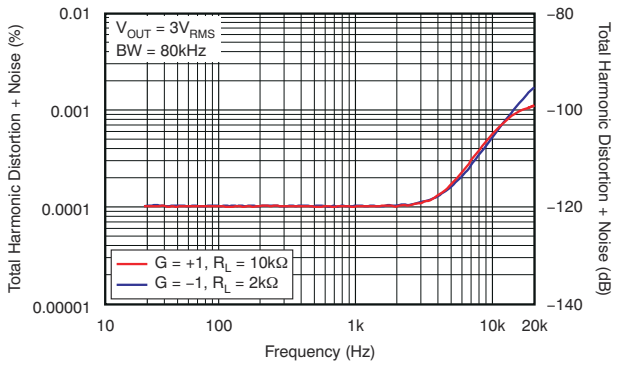


Figure 5-15. THD+N Ratio vs Frequency

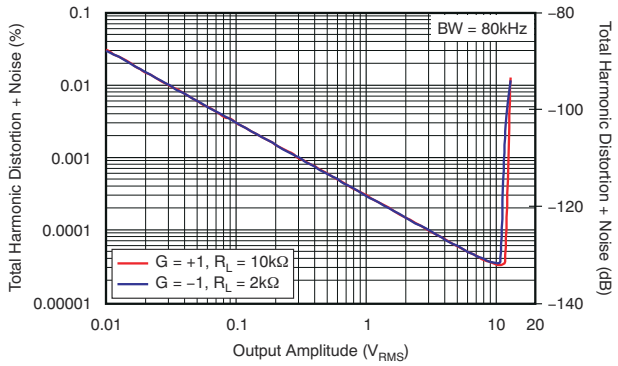


Figure 5-16. THD+N vs Output Amplitude

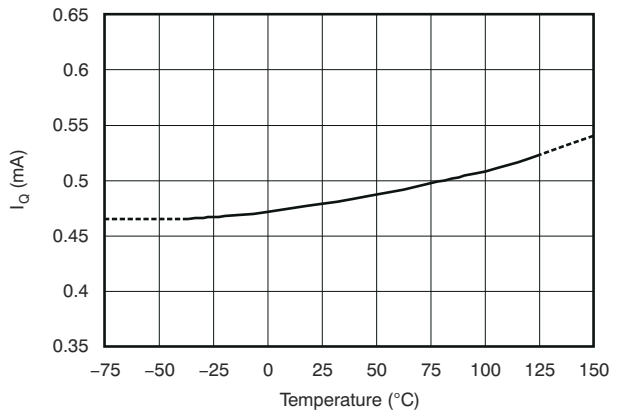


Figure 5-17. Quiescent Current vs Temperature

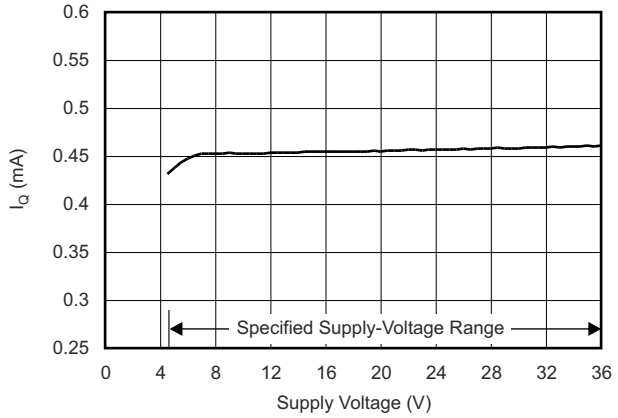


Figure 5-18. Quiescent Current vs Supply Voltage

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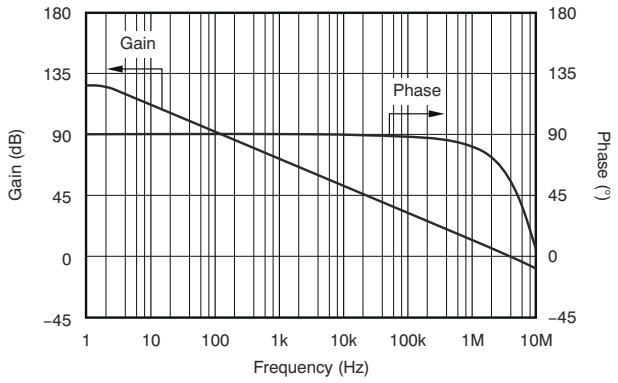


Figure 5-19. Open-Loop Gain and Phase vs Frequency

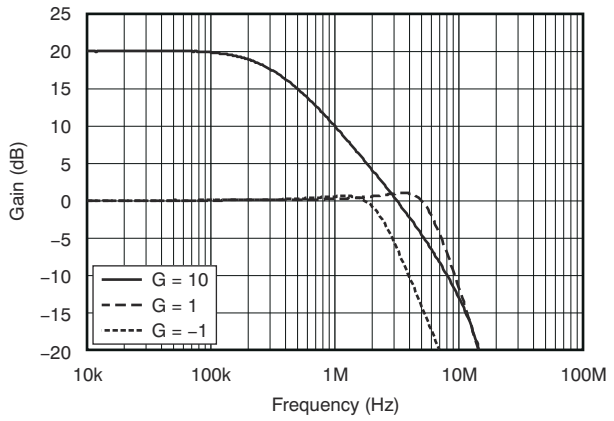


Figure 5-20. Closed-Loop Gain vs Frequency

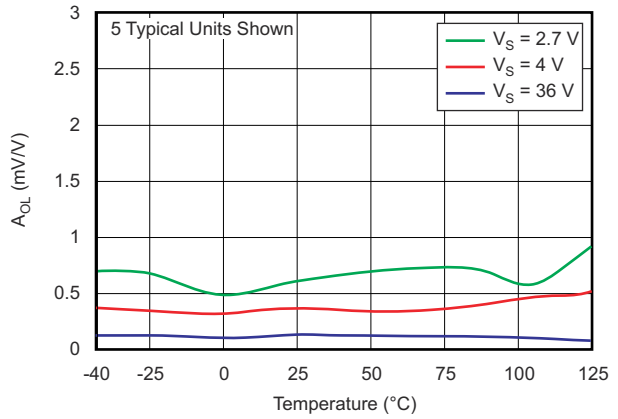


Figure 5-21. Open-Loop Gain vs Temperature

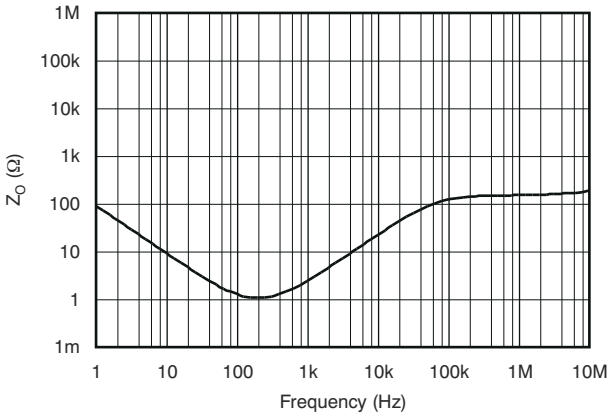


Figure 5-22. Open-Loop Output Impedance vs Frequency

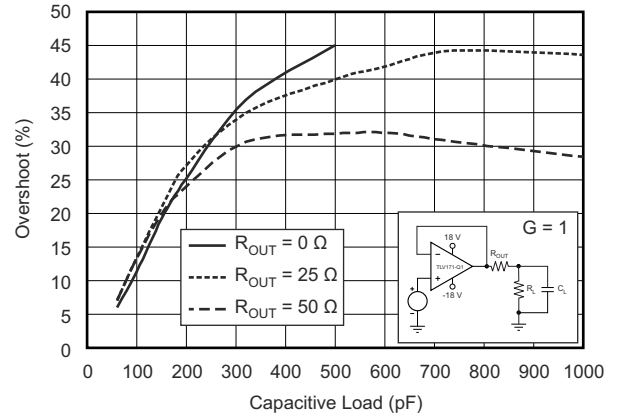


Figure 5-23. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

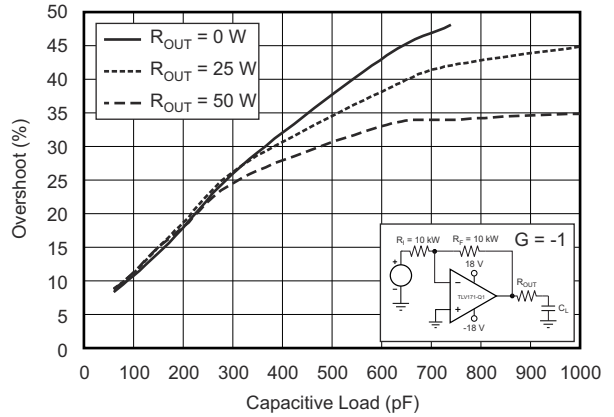


Figure 5-24. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

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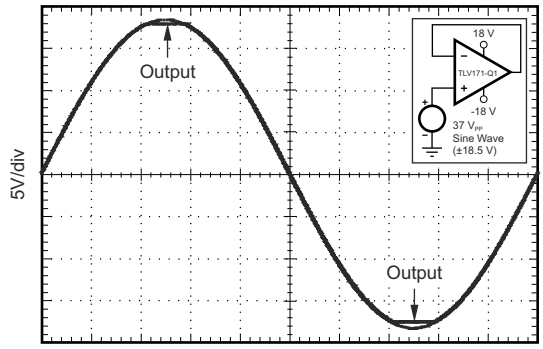


Figure 5-25. No Phase Reversal

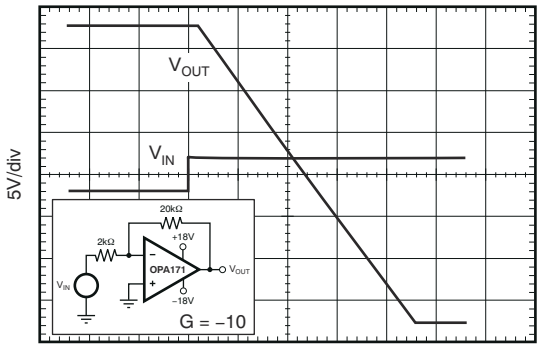


Figure 5-26. Positive Overload Recovery

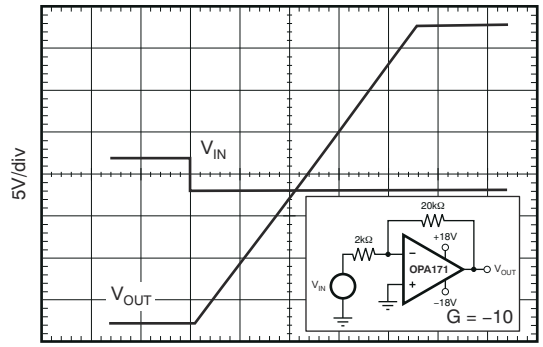


Figure 5-27. Negative Overload Recovery

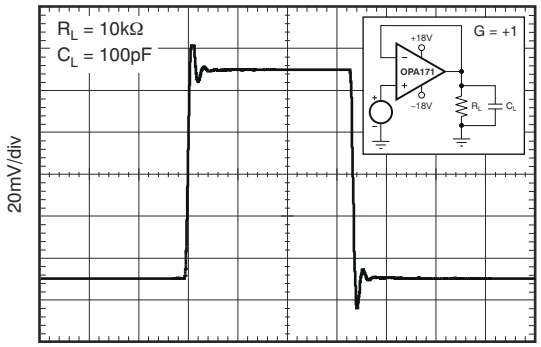


Figure 5-28. Small-Signal Step Response (100 mV)

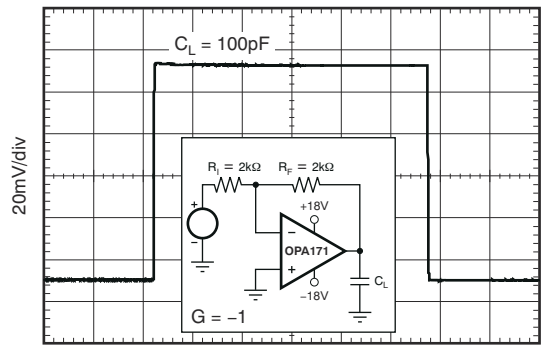


Figure 5-29. Small-Signal Step Response (100 mV)

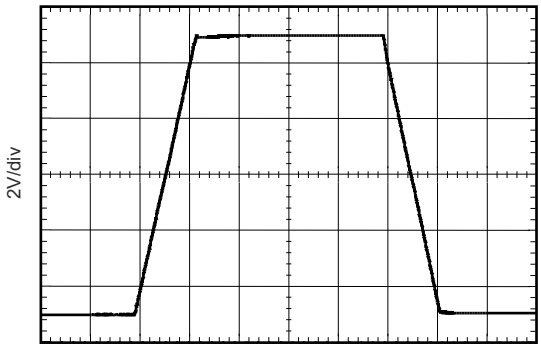


Figure 5-30. Large-Signal Step Response

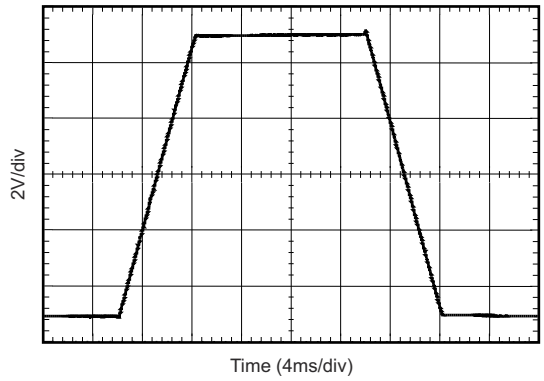


Figure 5-31. Large-Signal Step Response

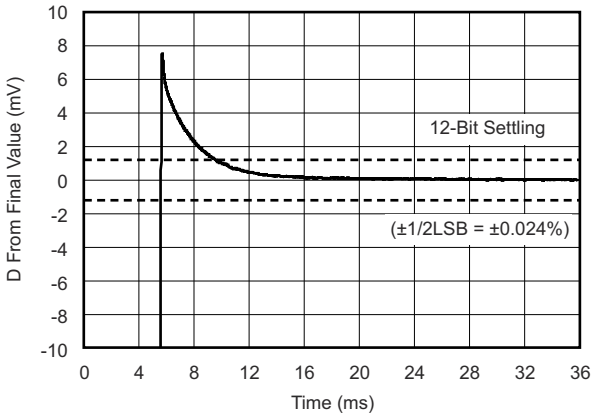


Figure 5-32. Large-Signal Settling Time (10-V Positive Step)

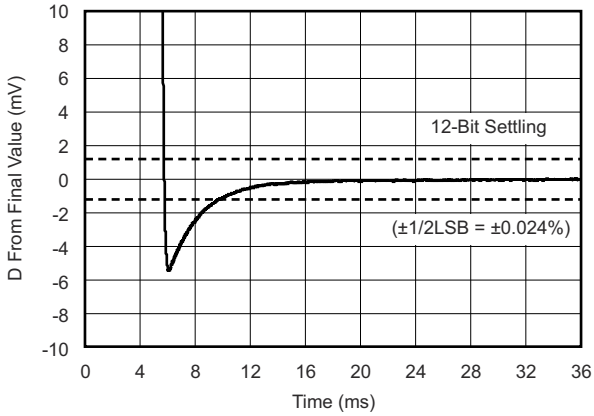


Figure 5-33. Large-Signal Settling Time (10-V Negative Step)

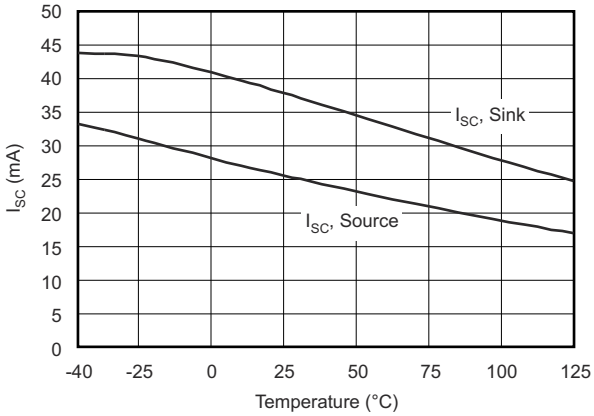


Figure 5-34. Short-Circuit Current vs Temperature

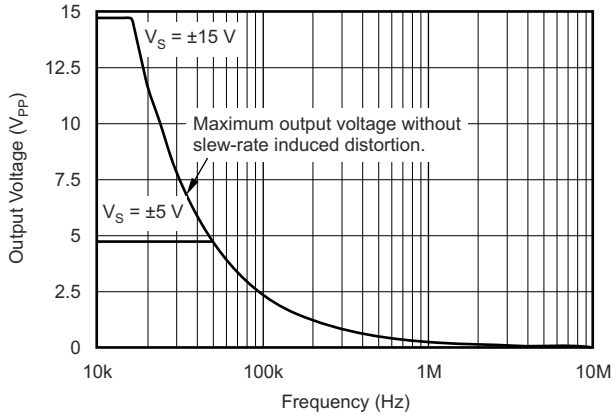


Figure 5-35. Maximum Output Voltage vs Frequency

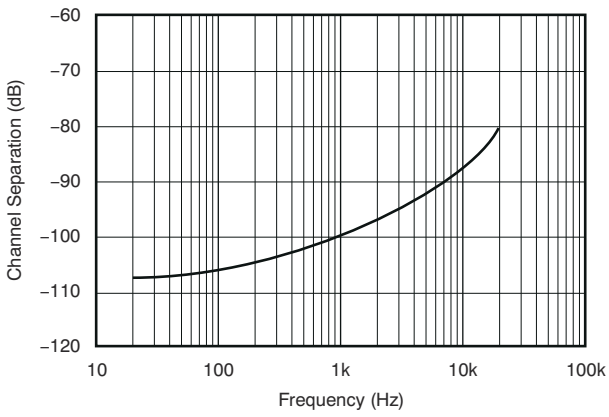


Figure 5-36. Channel Separation vs Frequency

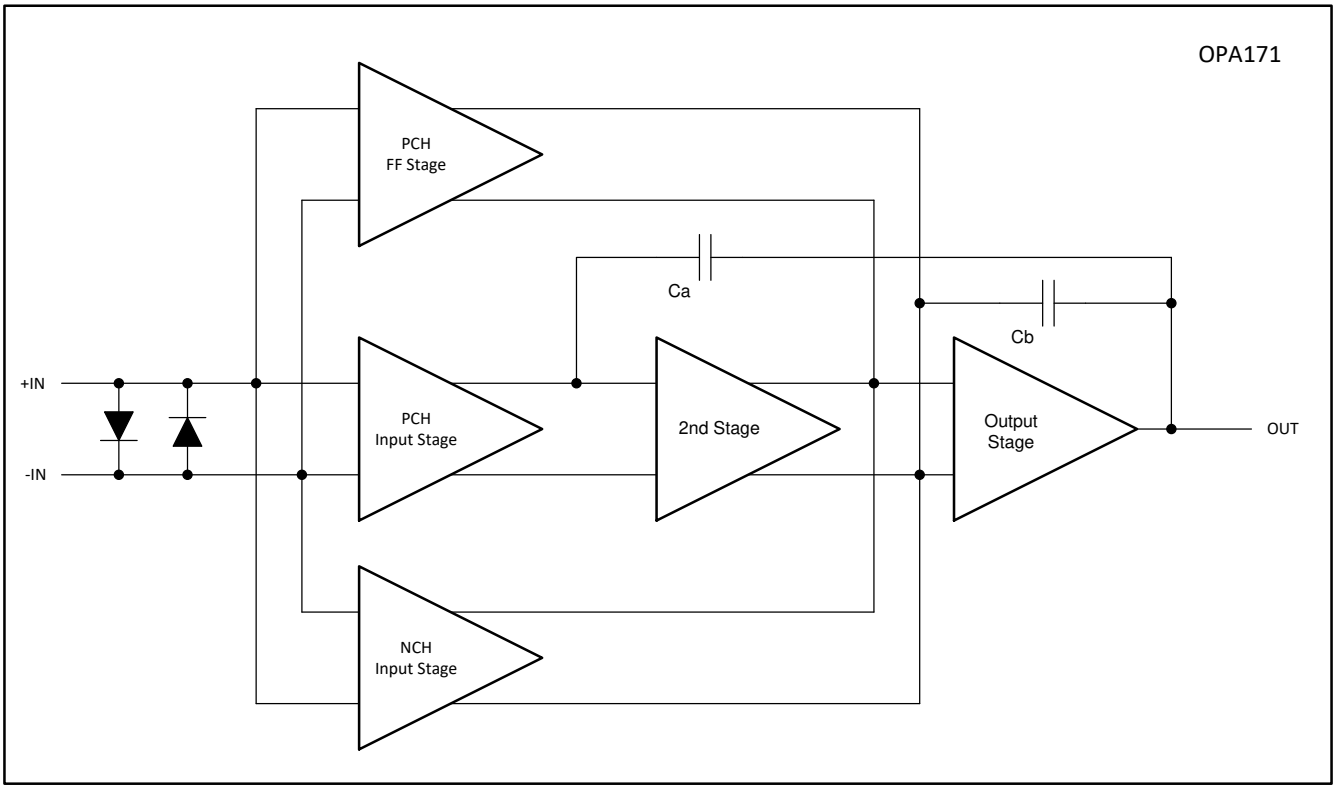
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6 Detailed Description

6.1 Overview

The OPAx171 operational amplifiers provide high overall performance, and are designed for many general-purpose applications. The excellent offset drift of only 2 µV/°C provides excellent stability over the entire temperature range. In addition, the series offers good overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Operating Characteristics

The OPAx171 family of amplifiers is specified for operation from 2.7 to 36 V (±1.35 to ±18 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Section 5.9*.

6.3.2 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx171 series extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This family can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in Table 6-1.

6.3.3 Phase-Reversal Protection

The OPAx171 family has an internal phase-reversal protection. Many operational amplifiers exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx171 prevents phase reversal with

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excessive common-mode voltage. Instead, the output limits into the appropriate rail. Figure 6-1 shows the performance.

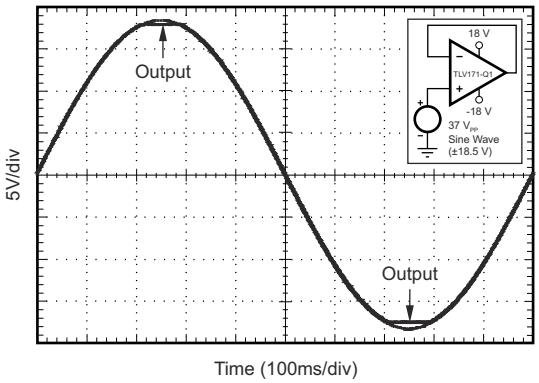


Figure 6-1. No Phase Reversal

Table 6-1. Typical Performance Range

PARAMETER	MIN	TYP	MAX	UNIT
Input common-mode voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		7		mV
vs temperature		12		µV/°C
Common-mode rejection		65		dB
Open-loop gain		60		dB
GBW		0.7		MHz
Slew rate		0.7		V/µs
Noise at f = 1 kHz		30		nV/√Hz

6.3.4 Capacitive Load and Stability

The dynamic characteristics of the OPAx171-Q1 family of devices have been optimized for commonly encountered operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. Figure 6-2 and Figure 6-3 show small-signal overshoot versus capacitive load for several values of R_{OUT}. For details of analysis techniques and application circuits, see *Applications Bulletin AB-028*, available for download from TI.com.

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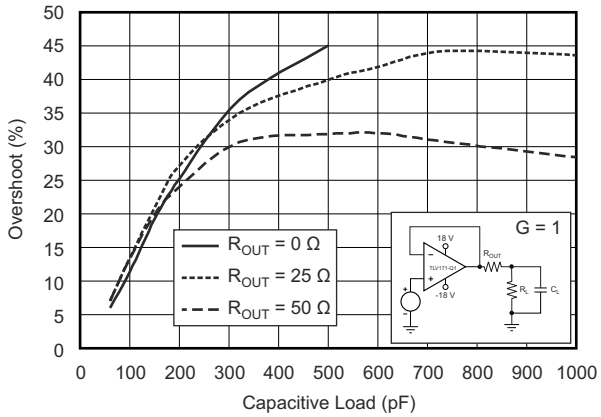


Figure 6-2. Small-Segment Overshoot vs Capacitive Load (100-mV Output Step)

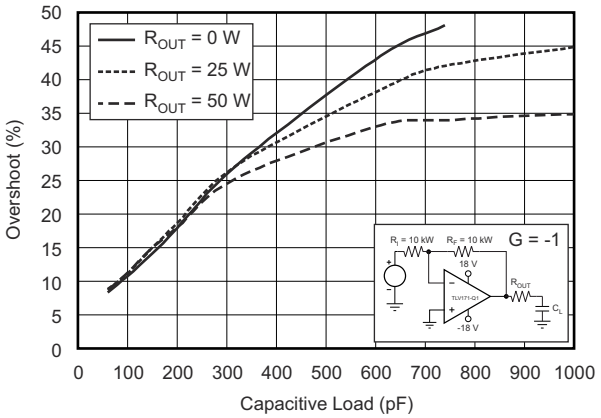


Figure 6-3. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

6.4 Device Functional Modes

6.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx171 family extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

These devices can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in Table 6-1.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPAx171 operational amplifiers provide high overall performance, and are designed for many general-purpose applications. The excellent offset drift of only 2 µV/°C provides excellent stability over the entire temperature range. In addition, the series offers good overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

7.1.1 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits for protection from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 7-1 shows the ESD circuits contained in the OPAx171 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

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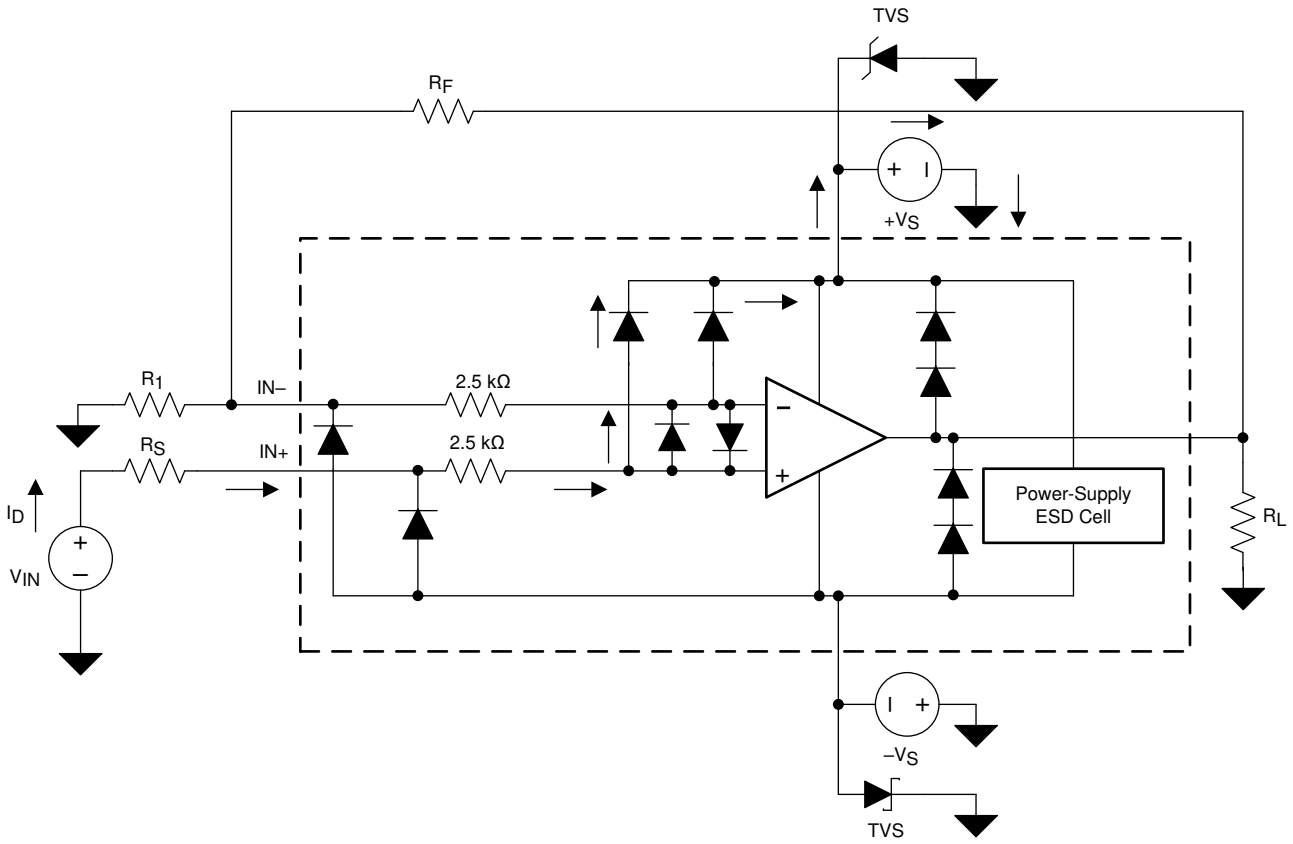


Figure 7-1. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device contains a trigger (or threshold voltage) that is above the normal operating voltage of the OPAx171 but below the device breakdown level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (as shown in Figure 7-1), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise when an applied voltage exceeds the operating voltage of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 7-1 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper steering diodes conducts and directs current to V+. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} begins sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

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Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies (V+ or V–) are at 0 V. This question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear to be high-impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition. Most likely, the amplifier does not operate normally. If the supplies are low-impedance, then the current through the steering diodes can be quite high. The current level depends on the ability of the input source to deliver current and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see Figure 7-1. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating, supply-voltage level.

The OPAx171 input pins are protected from excessive differential voltage with back-to-back diodes; see Figure 7-1. In most circuit applications, the input protection circuitry does not affect the application. However, in low gain or G = 1 circuits, fast-ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low noise performance of the OPAx171. Figure 7-1 shows an example configuration that implements a current-limiting feedback resistor.

7.2 Typical Application

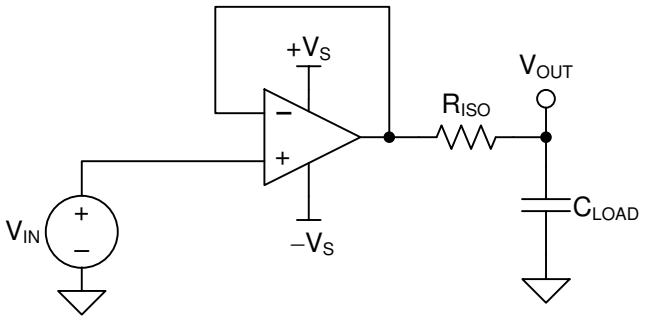


Figure 7-2. Unity-Gain Buffer With R_{ISO} Stability Compensation

7.2.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 µF, 0.1 µF, and 1 µF
- Phase margin: 45° and 60°

7.2.2 Detailed Design Procedure

Figure 7-3 shows a unity-gain buffer driving a capacitive load. Equation 1 shows the transfer function for the circuit in Figure 7-3. Not shown in Figure 7-3 is the open-loop output resistance of the operational amplifier, R_o.

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + \left(R_o + R_{ISO}\right) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in Equation 1 contains a pole and a zero. The frequency of the pole (f_p) is determined by (R_o + R_{ISO}) and C_{LOAD}. Components R_{ISO} and C_{LOAD} determine the frequency of the zero (f_z). Select R_{ISO} such that the rate of closure (ROC) between the open-loop gain (A_{OL}) and 1/β is 20 dB/decade to obtain a stable system. Figure 7-3 shows the concept. The 1/β curve for a unity-gain buffer is 0 dB.

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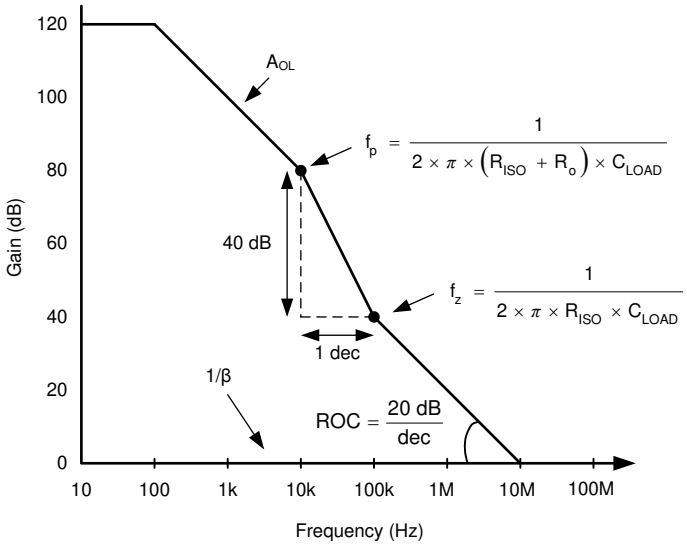


Figure 7-3. Unity-Gain Amplifier With R_{ISO} Compensation

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_o. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and AC gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. Table 7-1 shows the overshoot percentage and AC gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the OPAx171, see *Capacitive Load Drive Solution using an Isolation Resistor*.

Table 7-1. Phase Margin vs Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

7.2.2.1 Capacitive Load and Stability

The dynamic characteristics of the OPAx171 are optimized for commonly encountered operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. Figure 6-2 and Figure 6-3 illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. See *Applications Bulletin AB-028*, available for download from the TI website for details of analysis techniques and application circuits.

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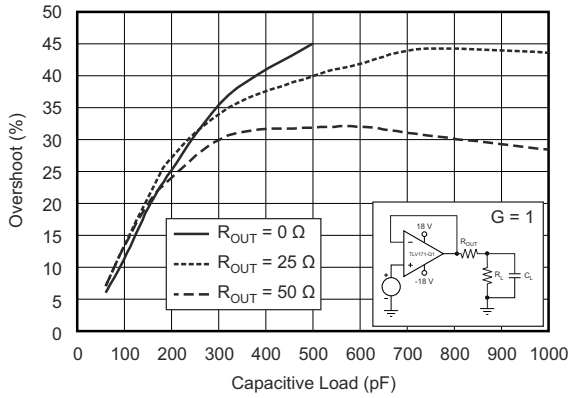


Figure 7-4. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

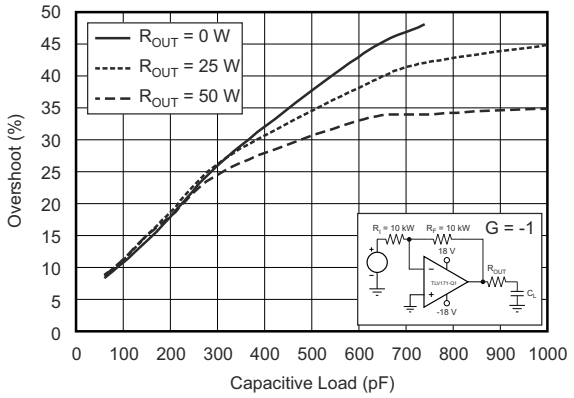


Figure 7-5. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

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7.2.3 Application Curve

The OPAx171 meets the supply voltage requirements of 30 V. The OPAx171 is tested for various capacitive loads and RISO is adjusted to get an overshoot corresponding to Table 7-1. The results of the these tests are summarized in Figure 7-6.

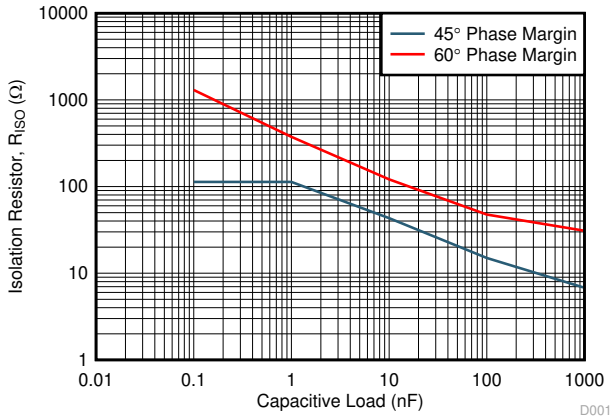


Figure 7-6. R_{ISO} vs C_{LOAD}

7.3 Power Supply Recommendations

The OPAx171 family is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Section 5* section.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Section 5.1* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For detailed information on bypass capacitor placement, see the *Section 7.4.1* section.

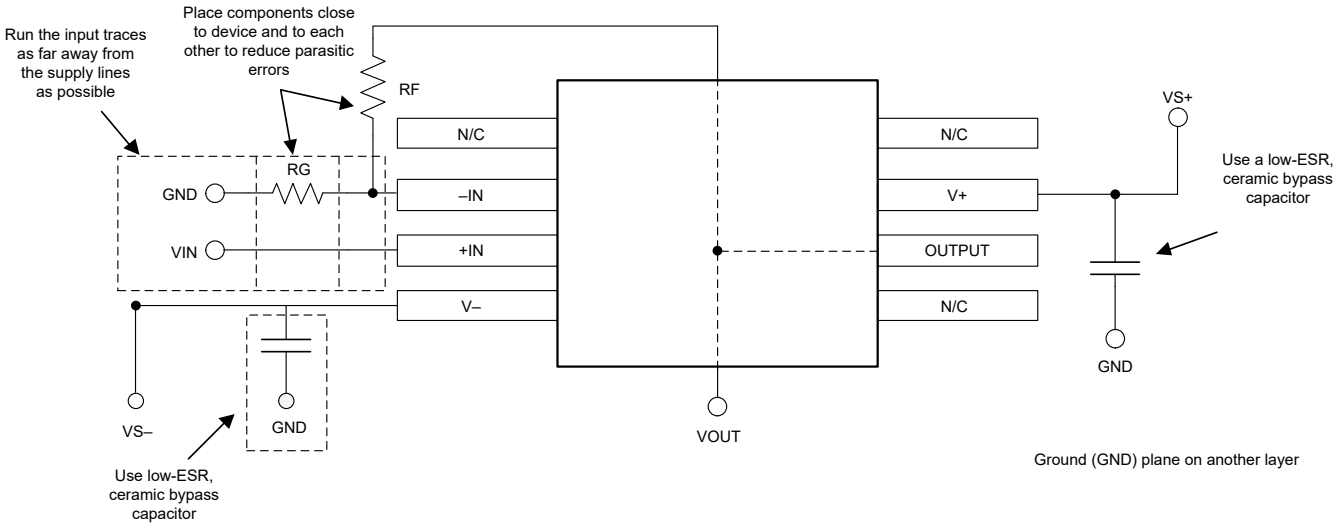
7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the devices, good printed circuit board (PCB) layout practices are recommended. Low-loss, 0.1-µF bypass capacitors must be connected between each supply pin and ground, placed as close to the devices as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.

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7.4.2 Layout Example



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Figure 7-7. Operational Amplifier Board Layout for Noninverting Configuration

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8 Device and Documentation Support

8.1 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.3 Trademarks

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8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (May 2020) to Revision H (June 2024)	Page
• Changed MSOP-8 package to VSSOP-8 throughout the data sheet	1
• Added the 5-pin SOT-23 package to the industry-standard package list in *Features*	1
• Removed the 8-pin MSOP package from the industry-standard package list in *Features*	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed Device Information table to Package Information	1

Changes from Revision F (April 2018) to Revision G (May 2020)	Page
• Added links to *Applications*	1
• Changed graphs with incorrect units (mV to µV) in the Typical Characteristics section	11

Changes from Revision E (April 2015) to Revision F (April 2018)	Page
• Changed minimum supply voltage value from ±20 V to 0 V in *Absolute Maximum Ratings* table	6
• Added maximum supply voltage value of 40 V to *Absolute Maximum Ratings* table	6
• Rewrote *Electrical Overstress* subsection content in *Application Information* section	20

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Changes from Revision D (September 2012) to Revision E (April 2015)	Page
• Changed device title (removed "Value Line Series")	1
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision C (June 2011) to Revision D (September 2012)	Page
• Added "Value Line Series" to title	1

Changes from Revision B (November 2010) to Revision June 2011 C ()	Page
• Added MSOP-8 package to device graphic	1
• Added MSOP-8 package to Features bullets	1
• Added MSOP-8 package to Product Family table	1
• Updated pinout configurations for OPA2171 and OPA4171	3
• Added MSOP-8 package to OPA2171 Thermal Information table	7
• Added new row for Voltage Output Swing from Rail parameter to *Output* subsection of *Electrical Characteristics*	8
• Changed Voltage Output Swing from Rail parameter to over temperature in *Output* subsection of *Electrical Characteristics*	8
• Changed Figure 5-9	11

Changes from Revision A (November 2010) to Revision B (November 2010)	Page
• Changed input offset voltage specification	8
• Changed input offset voltage, over temperature specification	8
• Changed quiescent current per amplifier, over temperature specification	8

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA171AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O171A
OPA171AID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O171A
OPA171AIDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	OSUI
OPA171AIDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OSUI
OPA171AIDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OSUI
OPA171AIDBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OSUI
OPA171AIDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	OSUI
OPA171AIDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OSUI
OPA171AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O171A
OPA171AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O171A
OPA171AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O171A
OPA171AIDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O171A
OPA171AIDRLR	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DAP
OPA171AIDRLR.A	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DAP
OPA171AIDRLT	Active	Production	SOT-5X3 (DRL) | 5	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DAP
OPA171AIDRLT.A	Active	Production	SOT-5X3 (DRL) | 5	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DAP
OPA2171AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2171A
OPA2171AID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2171A
OPA2171AIDCUR	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPOC
OPA2171AIDCUR.A	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPOC
OPA2171AIDCURG4	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPOC
OPA2171AIDCURG4.A	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPOC
OPA2171AIDCUT	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPOC
OPA2171AIDCUT.A	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPOC
OPA2171AIDGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OPMI
OPA2171AIDGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OPMI
OPA2171AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OPMI
OPA2171AIDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPMI

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2171AIDGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPMI
OPA2171AIDGKRG4.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPMI
OPA2171AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2171A
OPA2171AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2171A
OPA2171AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2171A
OPA2171AIDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2171A
OPA4171AID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4171
OPA4171AID.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4171
OPA4171AIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4171
OPA4171AIDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4171
OPA4171AIDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4171
OPA4171AIDRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4171
OPA4171AIPW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4171
OPA4171AIPW.A	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4171
OPA4171AIPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4171
OPA4171AIPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4171
OPA4171AIPWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4171
OPA4171AIPWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4171

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF OPA171, OPA2171, OPA4171 :

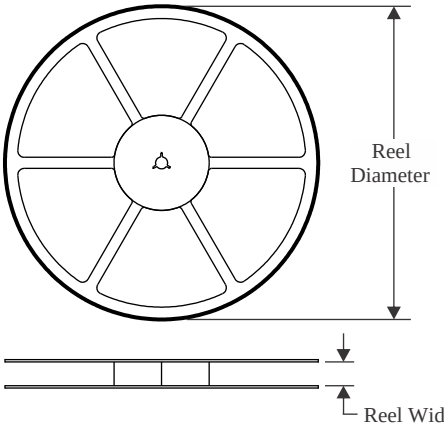
- Automotive : OPA171-Q1, OPA2171-Q1, OPA4171-Q1
- Enhanced Product : OPA2171-EP

NOTE: Qualified Version Definitions:

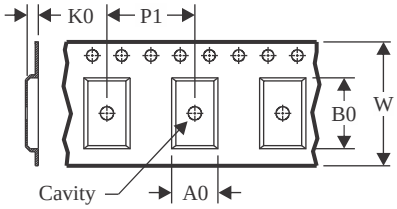
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

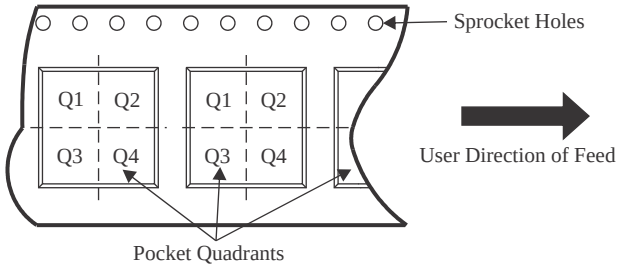


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

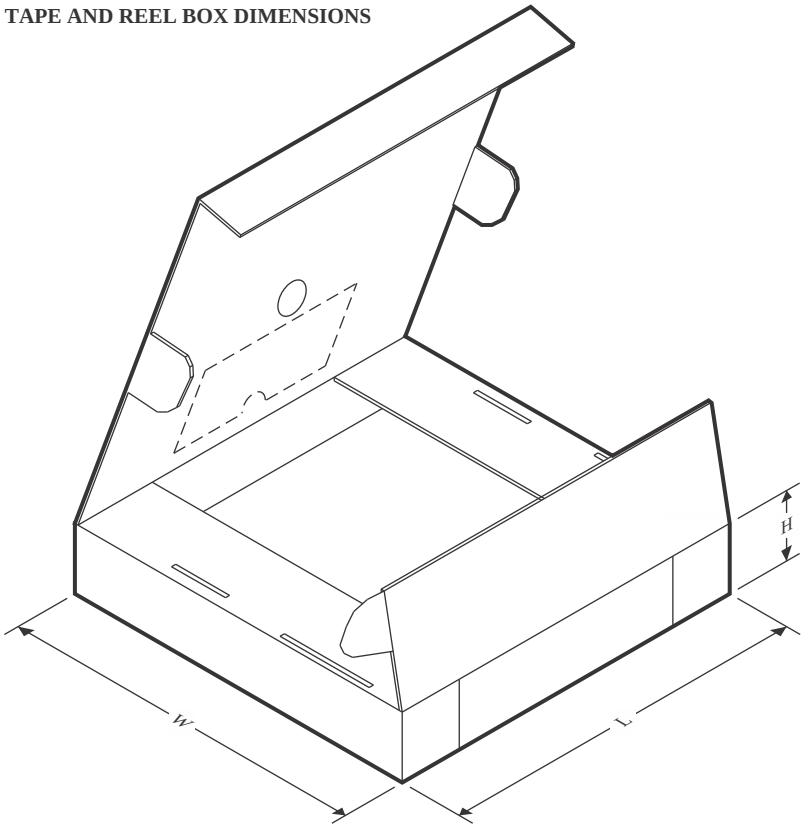


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA171AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA171AIDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA171AIDBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA171AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA171AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA171AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA171AIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA171AIDRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
OPA171AIDRLT	SOT-5X3	DRL	5	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
OPA2171AIDCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
OPA2171AIDCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
OPA2171AIDCUT	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
OPA2171AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2171AIDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2171AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2171AIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA4171AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4171AIDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4171AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4171AIPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

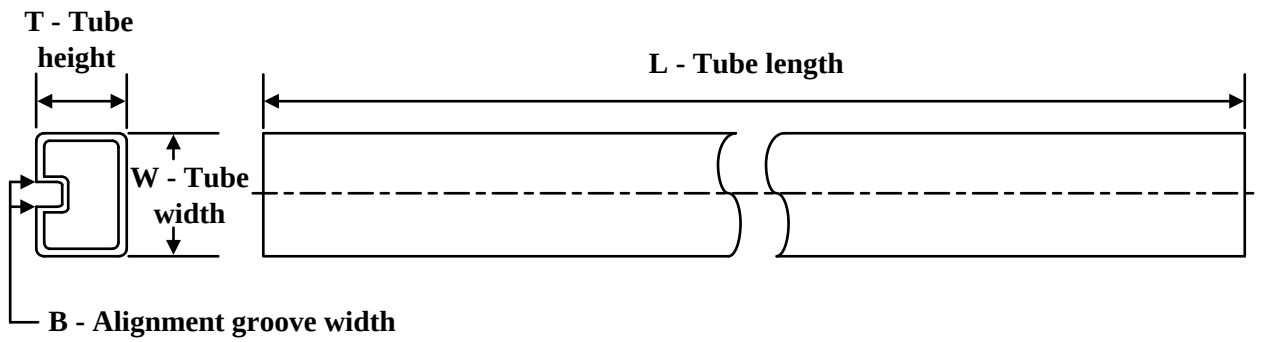


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA171AIDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA171AIDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
OPA171AIDBVRG4	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA171AIDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
OPA171AIDBVT	SOT-23	DBV	5	250	223.0	270.0	35.0
OPA171AIDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA171AIDRG4	SOIC	D	8	2500	353.0	353.0	32.0
OPA171AIDRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
OPA171AIDRLT	SOT-5X3	DRL	5	250	202.0	201.0	28.0
OPA2171AIDCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
OPA2171AIDCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
OPA2171AIDCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
OPA2171AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2171AIDGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2171AIDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA2171AIDRG4	SOIC	D	8	2500	353.0	353.0	32.0
OPA4171AIDR	SOIC	D	14	2500	353.0	353.0	32.0
OPA4171AIDRG4	SOIC	D	14	2500	353.0	353.0	32.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA4171AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
OPA4171AIPWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA171AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA171AID.A	D	SOIC	8	75	506.6	8	3940	4.32
OPA2171AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2171AID.A	D	SOIC	8	75	506.6	8	3940	4.32
OPA2171AIDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA2171AIDGK.A	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA4171AID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4171AID.A	D	SOIC	14	50	506.6	8	3940	4.32
OPA4171AIPW	PW	TSSOP	14	90	530	10.2	3600	3.5
OPA4171AIPW.A	PW	TSSOP	14	90	530	10.2	3600	3.5

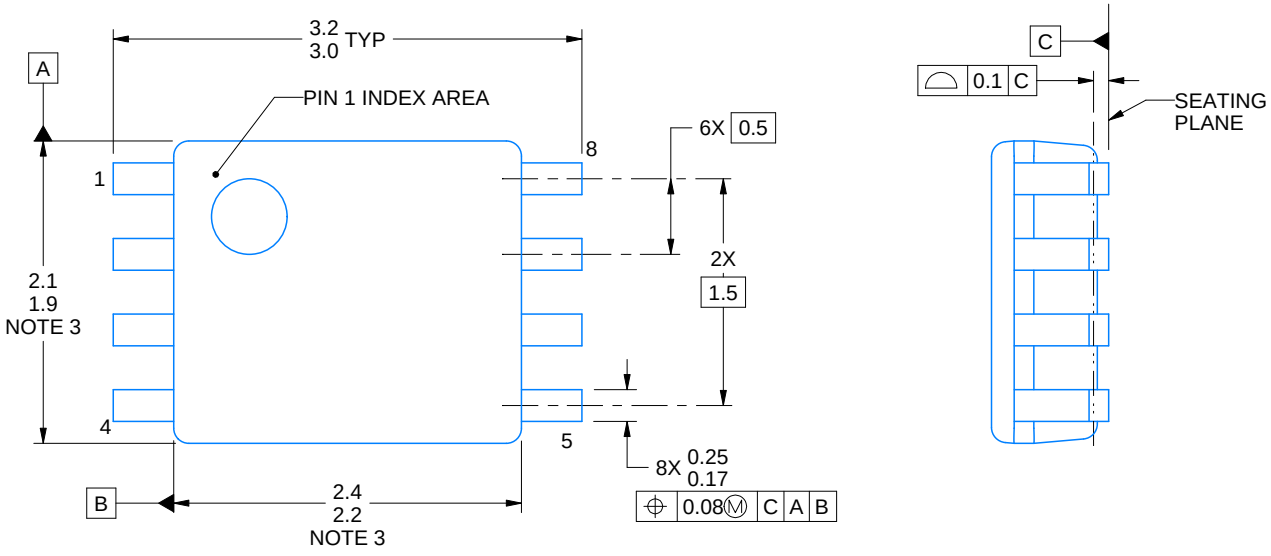
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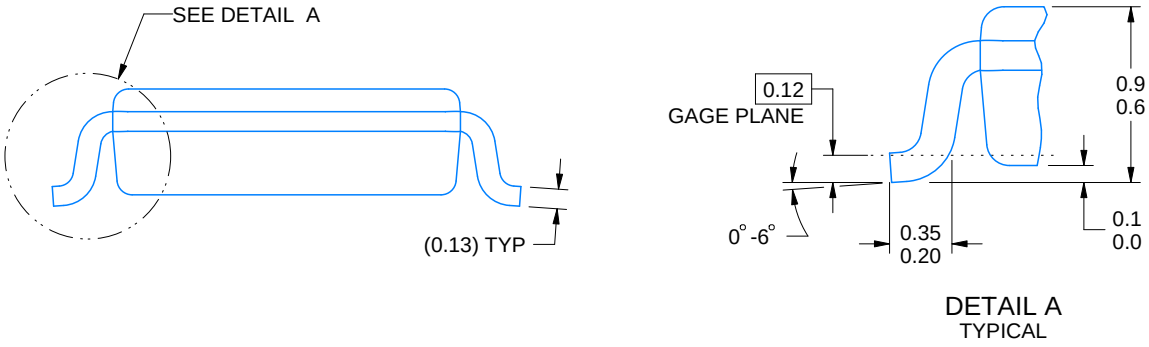


PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

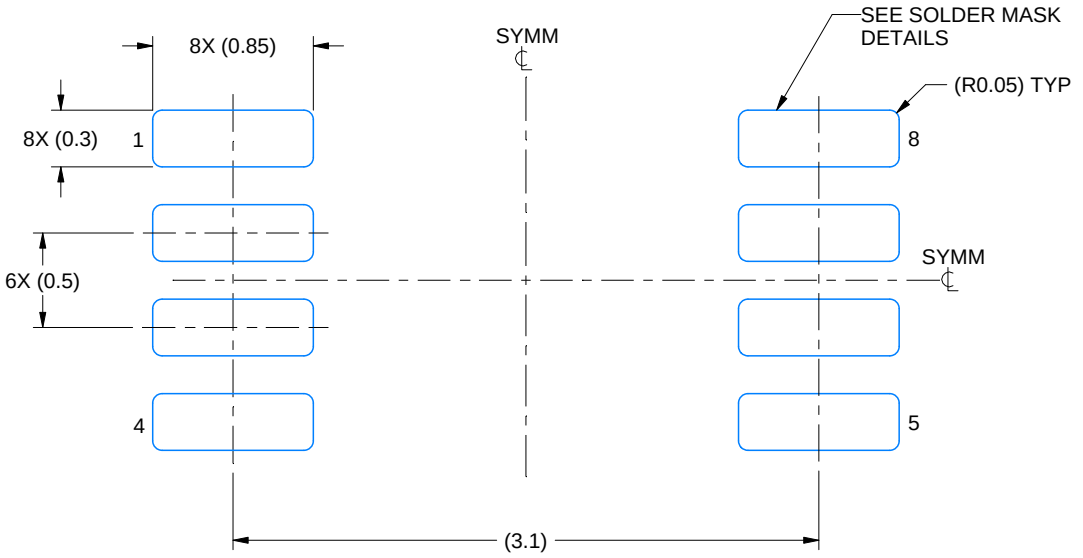




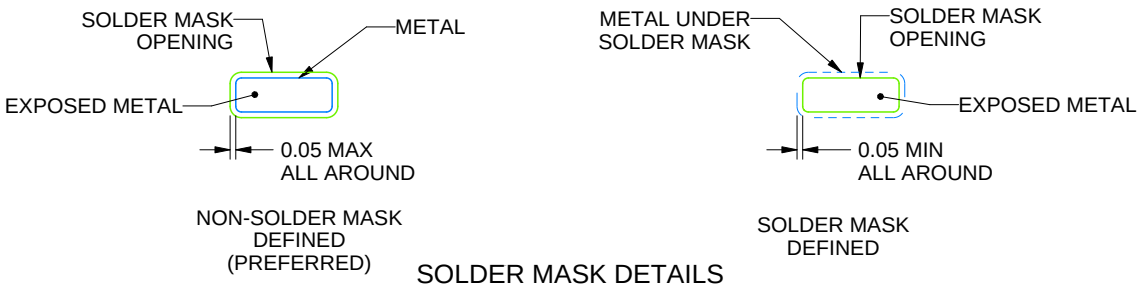
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

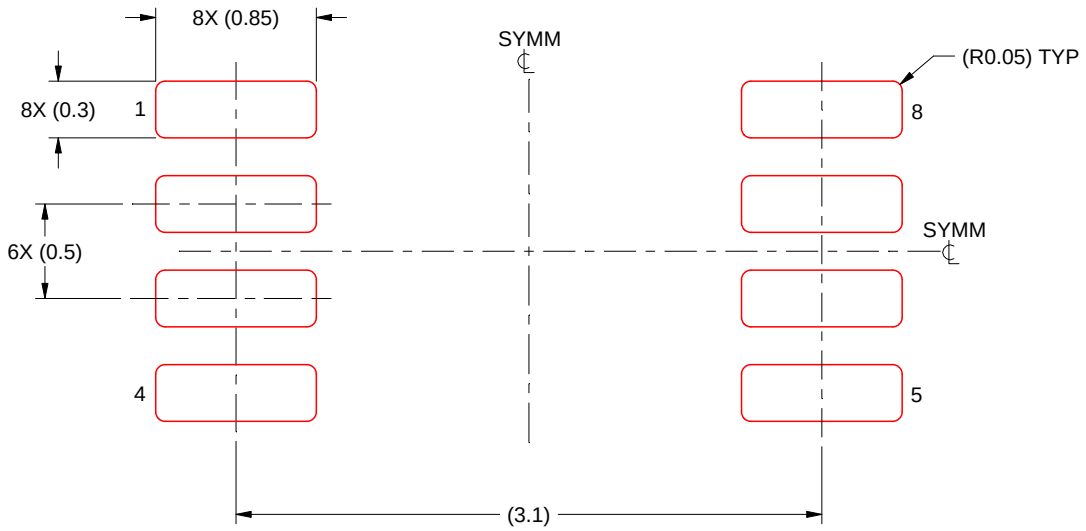


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

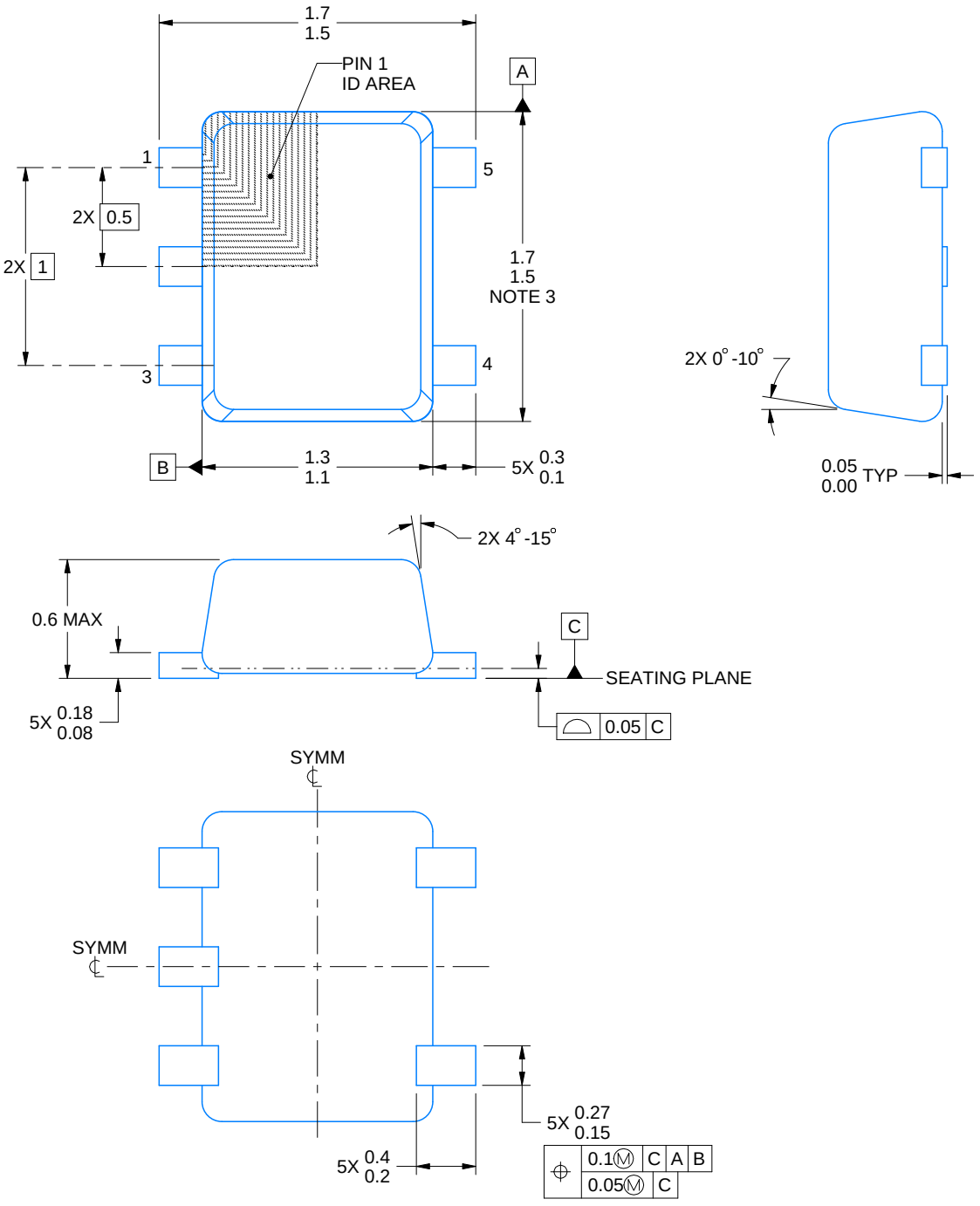
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DRL0005A

SOT - 0.6 mm max height

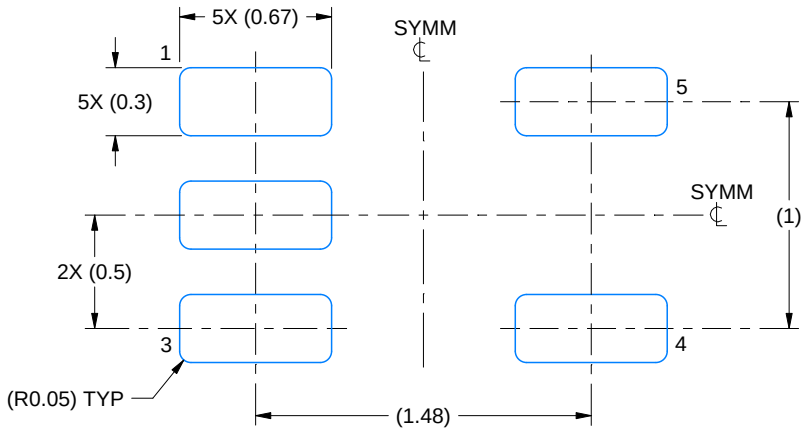
PLASTIC SMALL OUTLINE



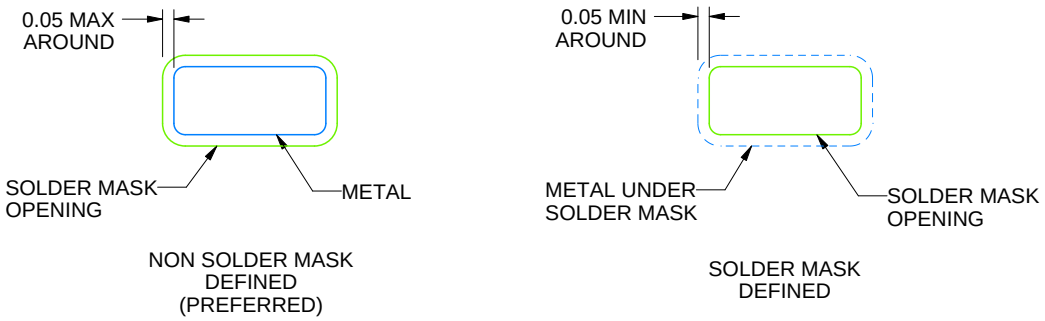
4220753/E 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1



LAND PATTERN EXAMPLE
SCALE:30X

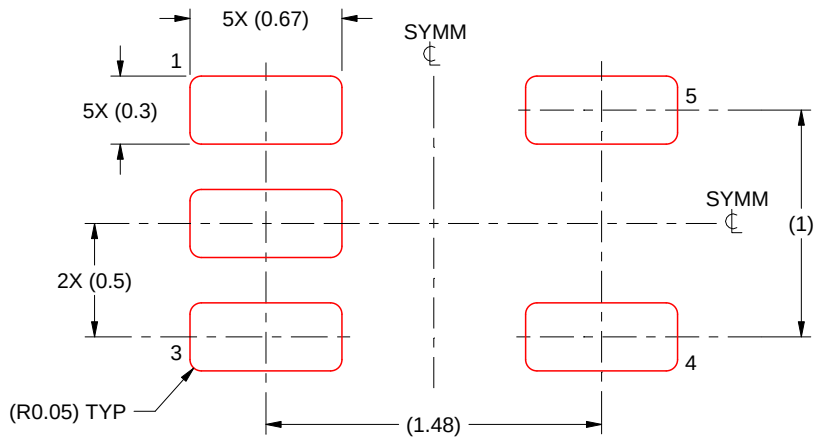


SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

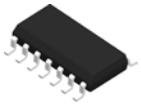


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

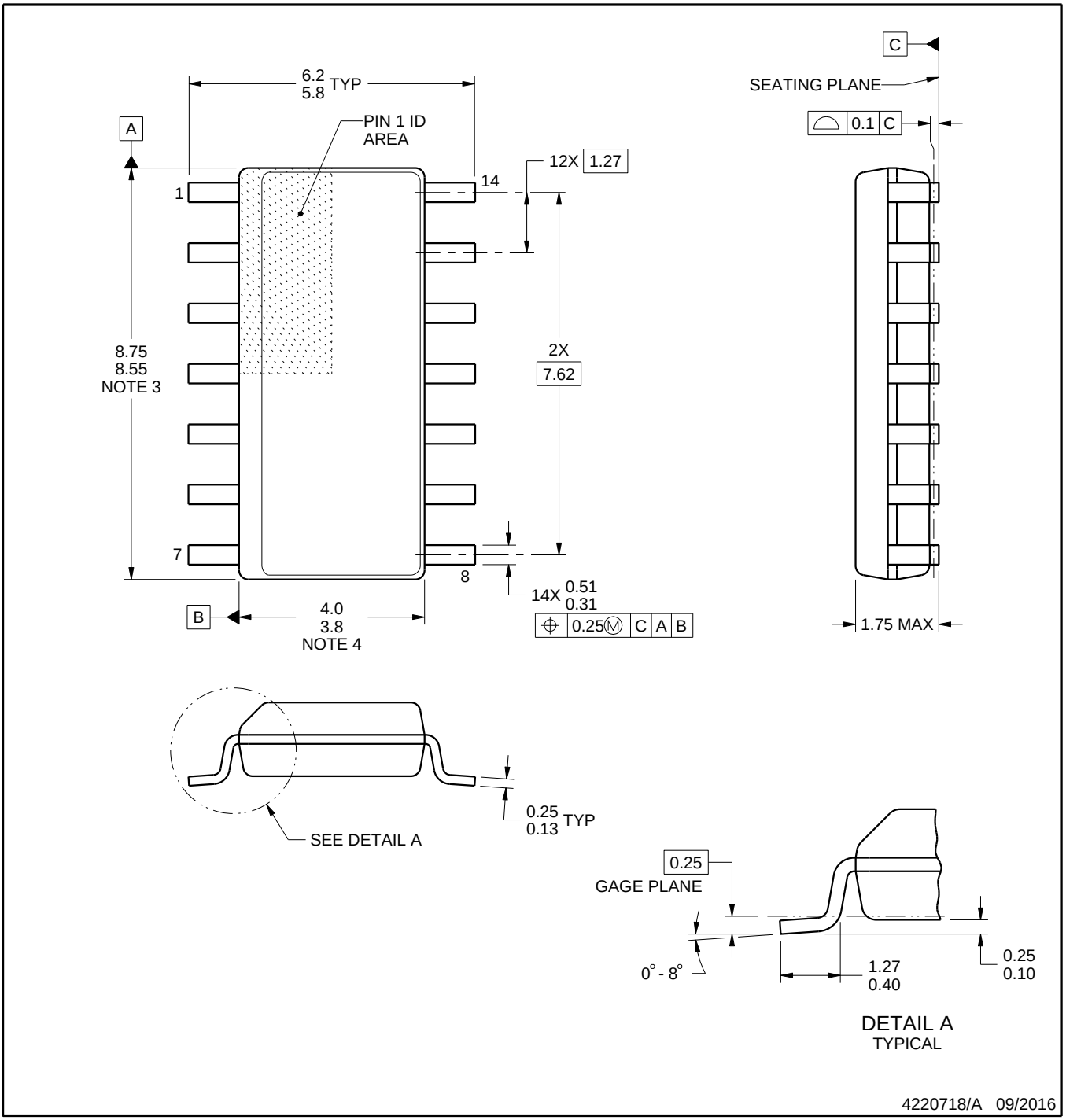


PACKAGE OUTLINE

D0014A

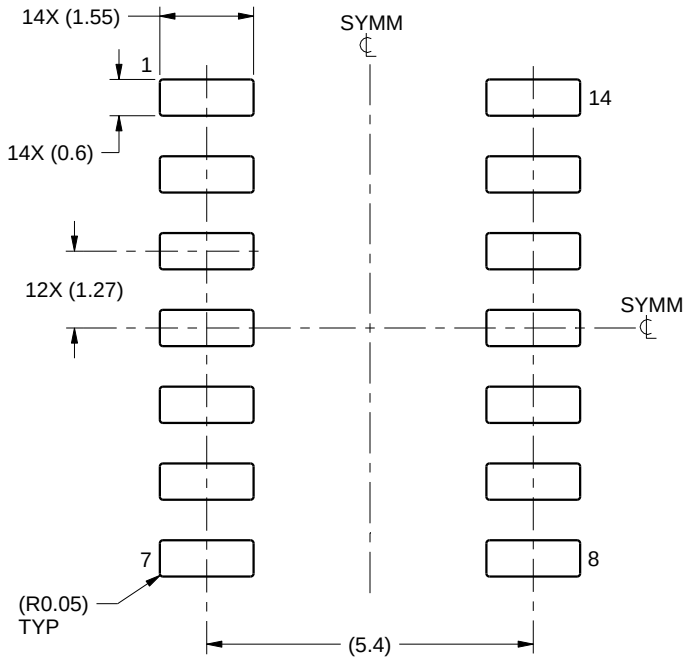
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

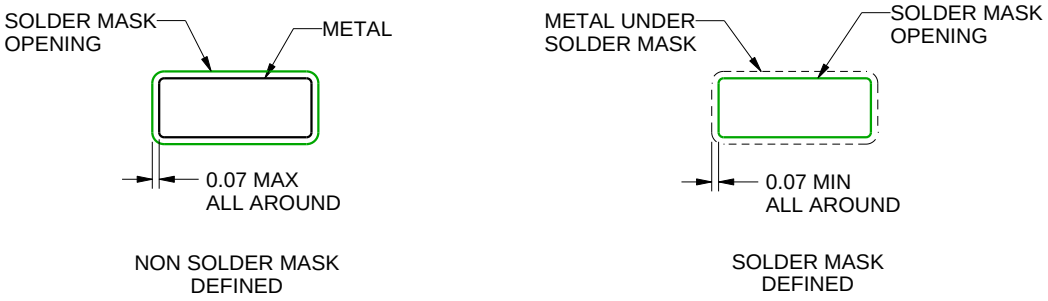


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

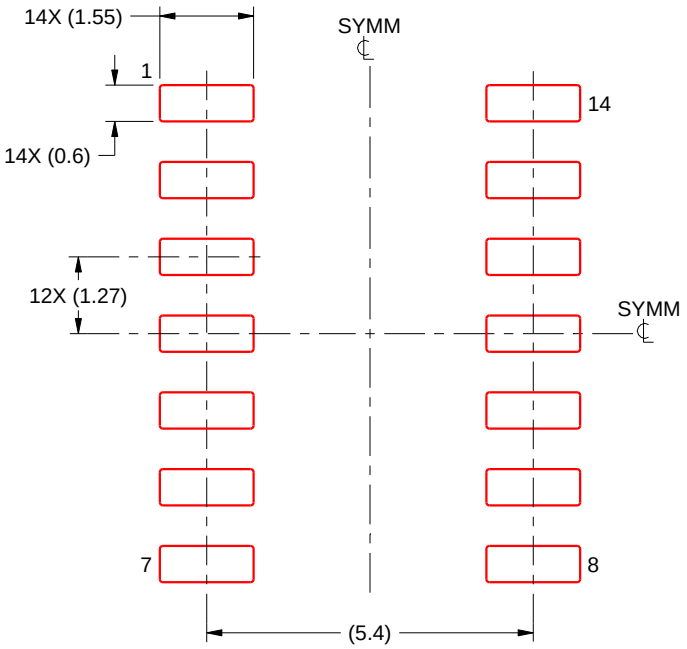
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

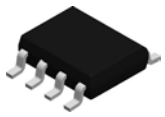


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

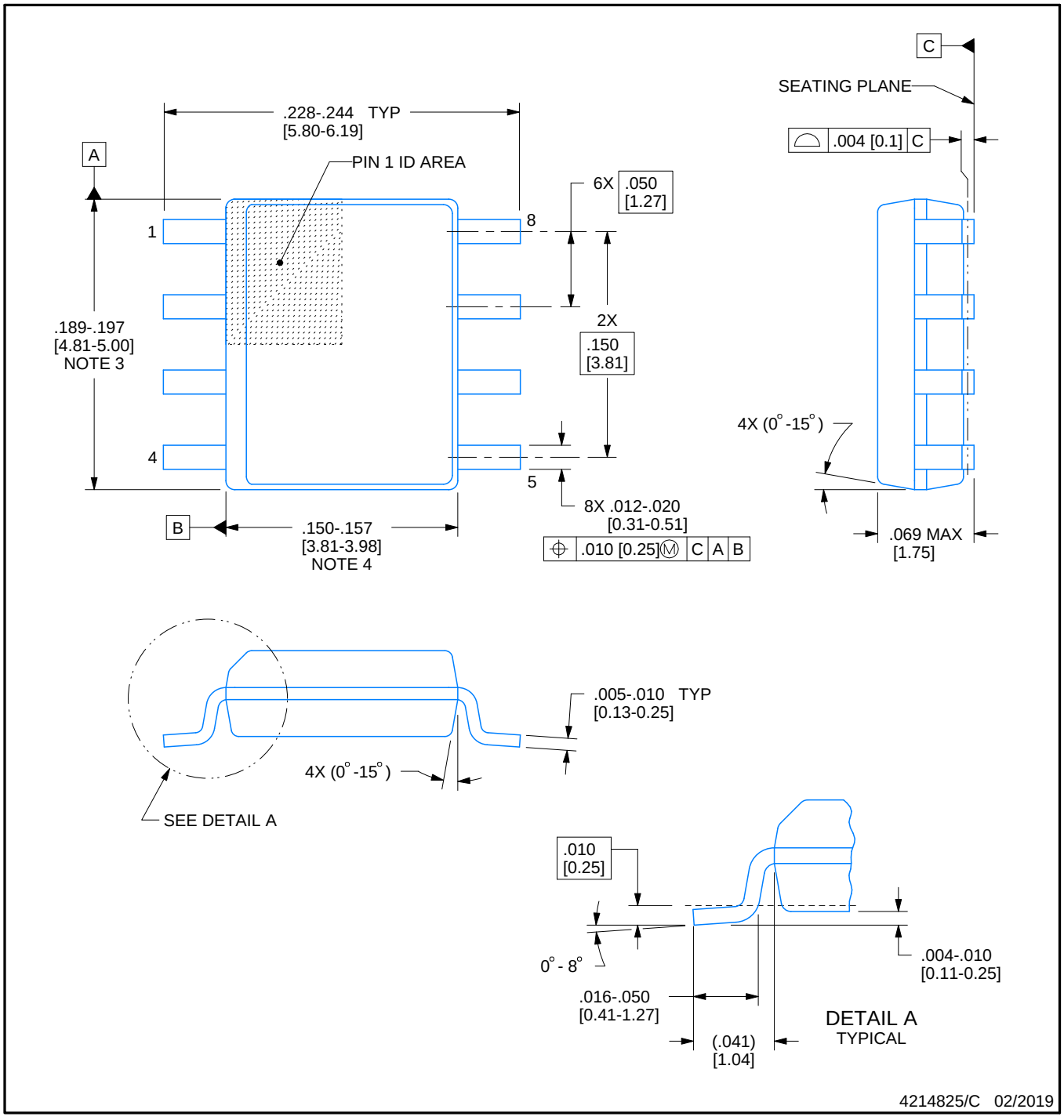


PACKAGE OUTLINE

D0008A

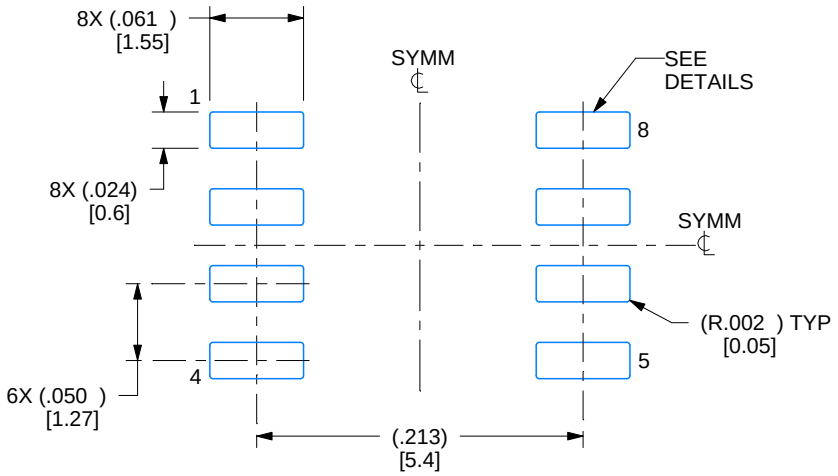
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

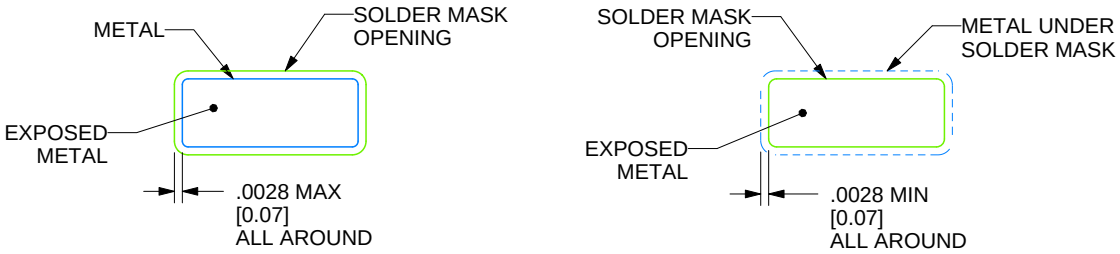


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

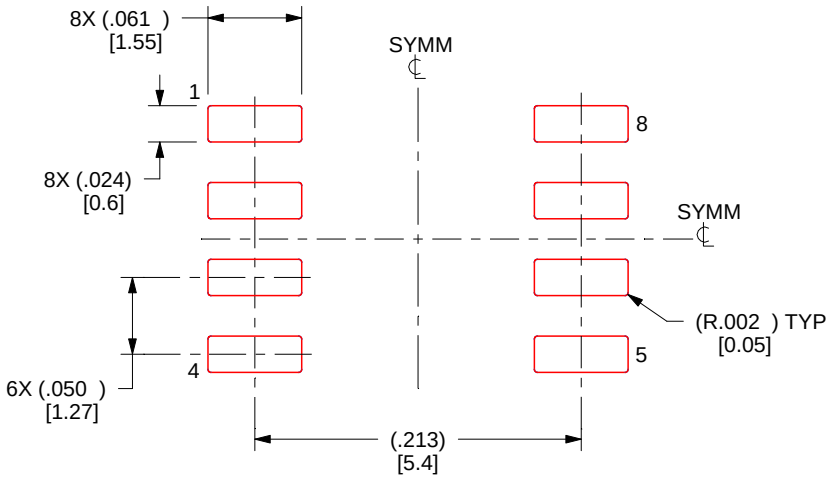
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

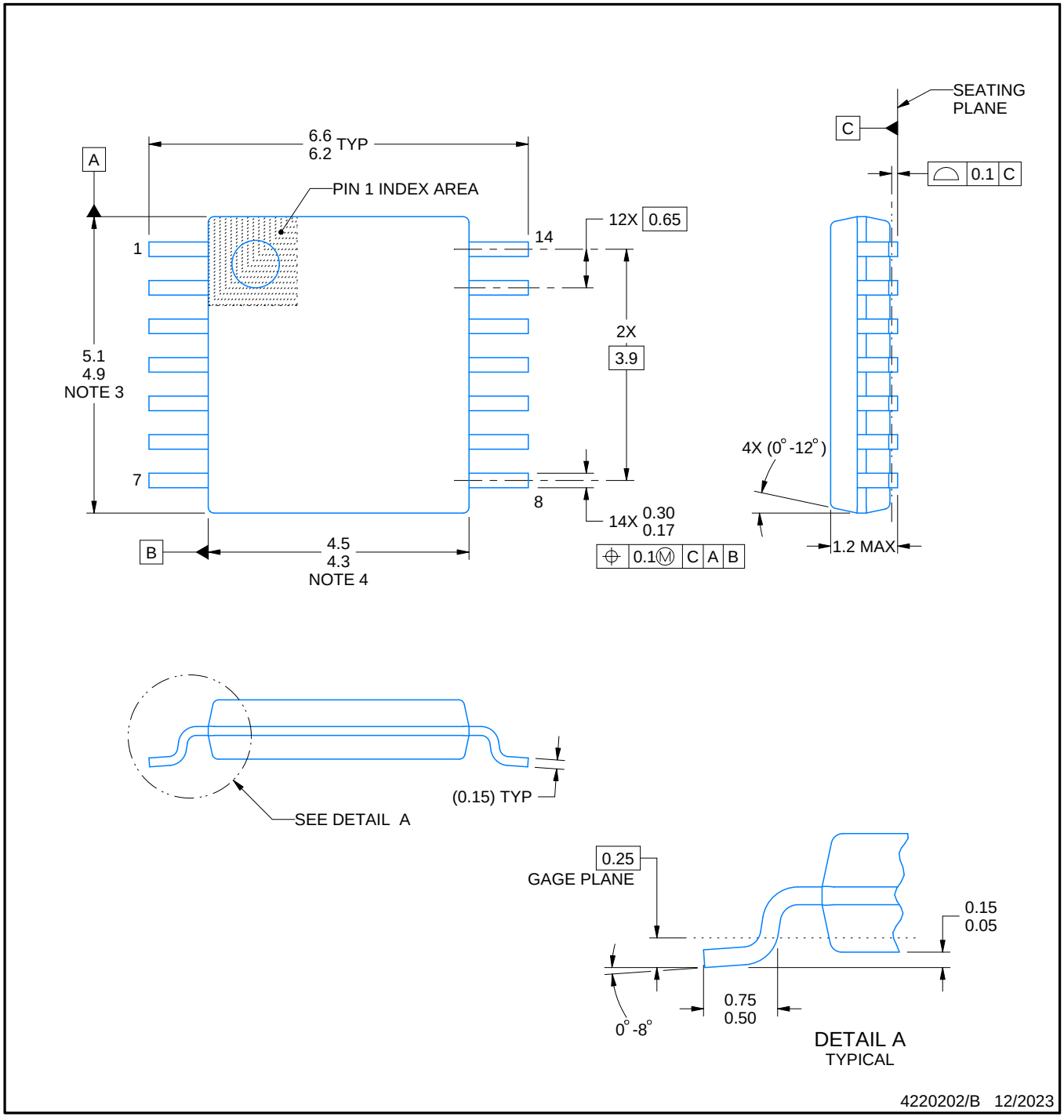
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

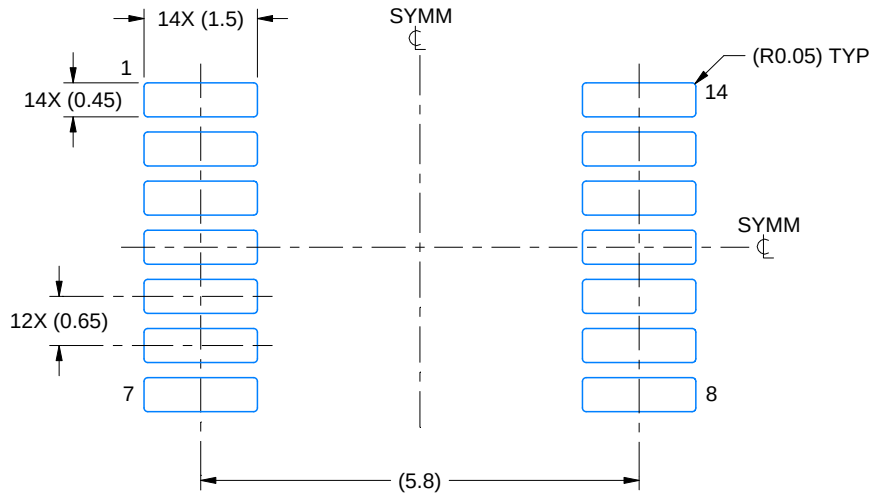
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

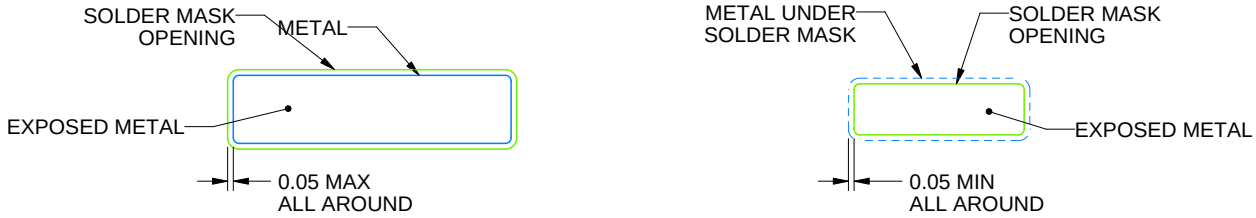


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

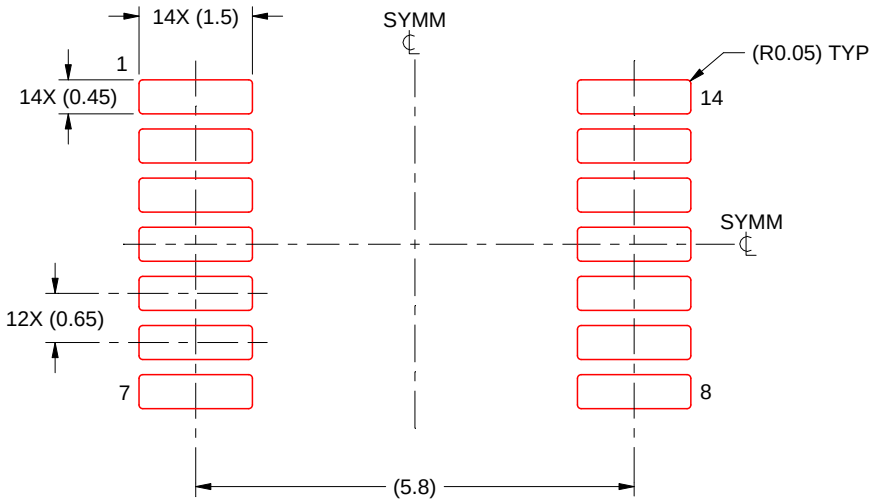


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

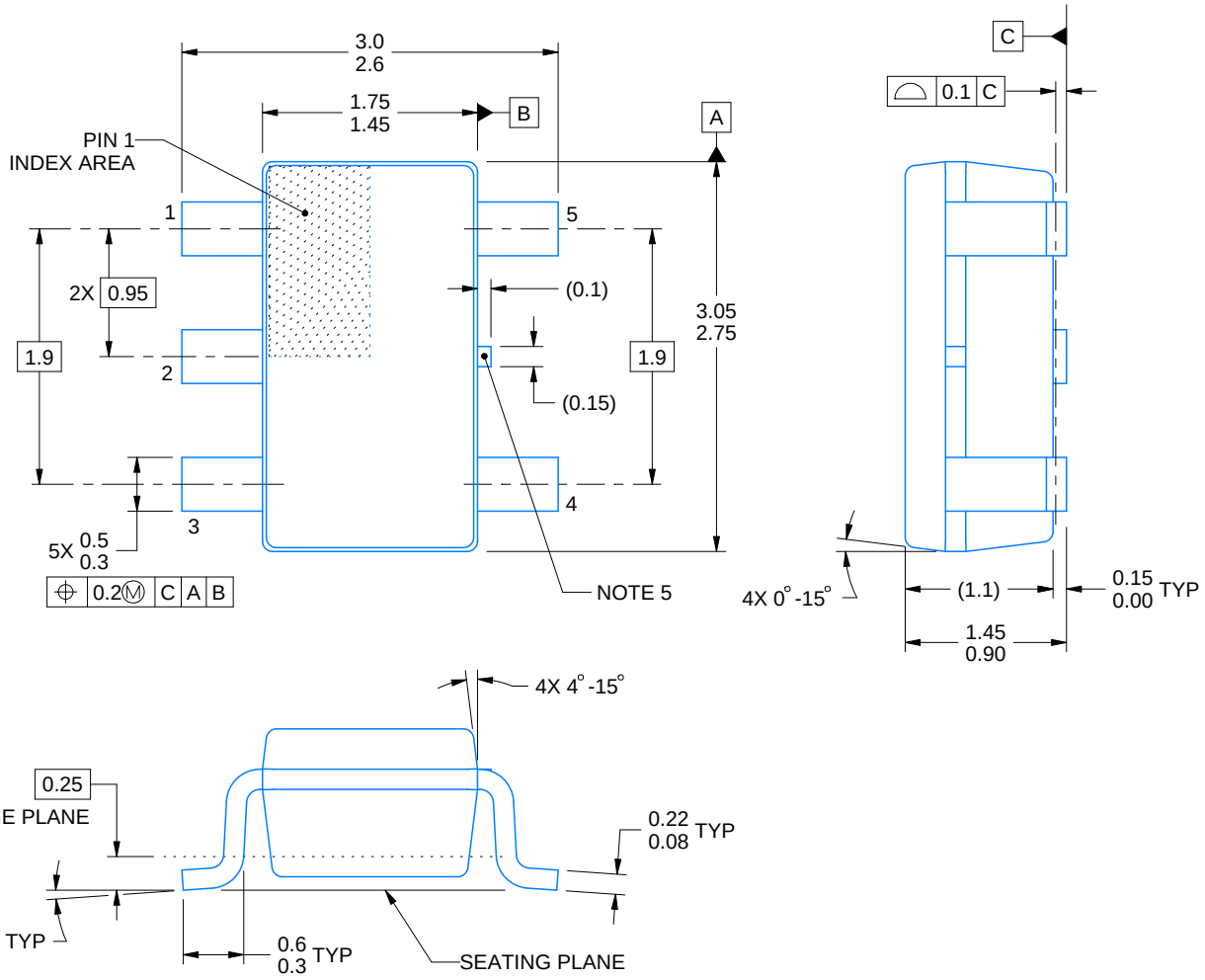
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

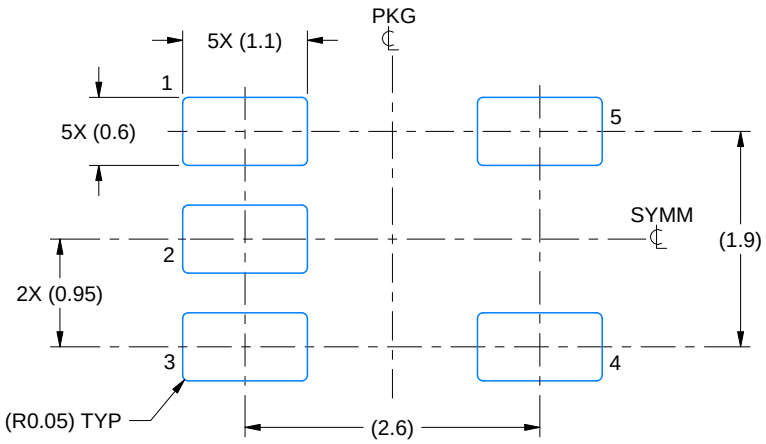
SMALL OUTLINE TRANSISTOR



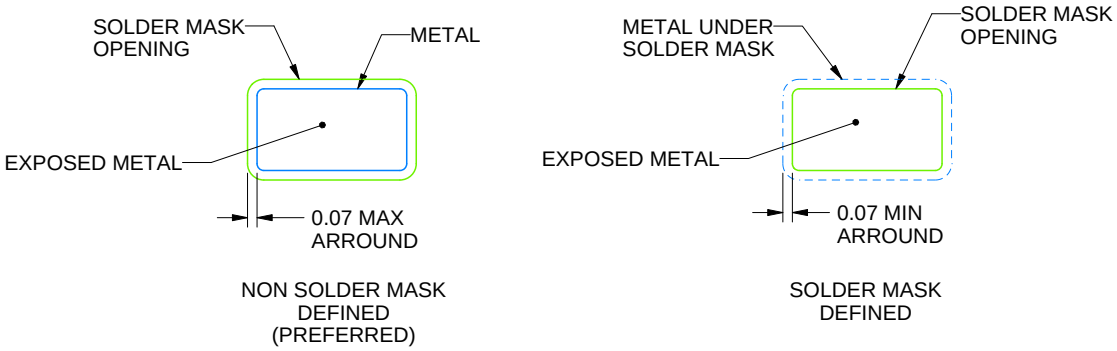
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

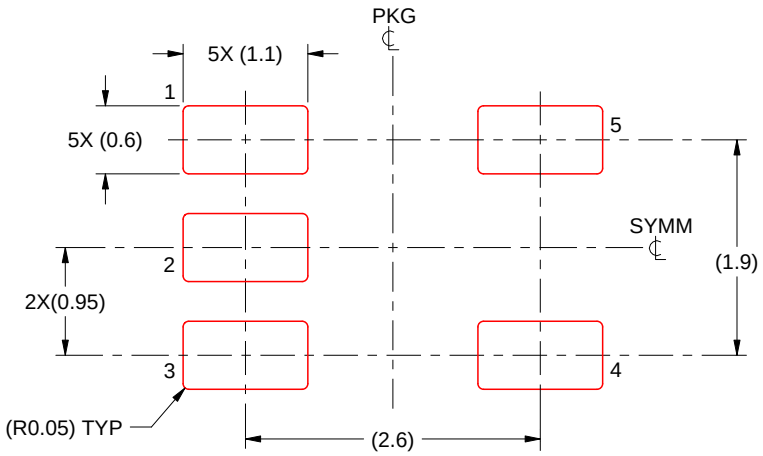


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

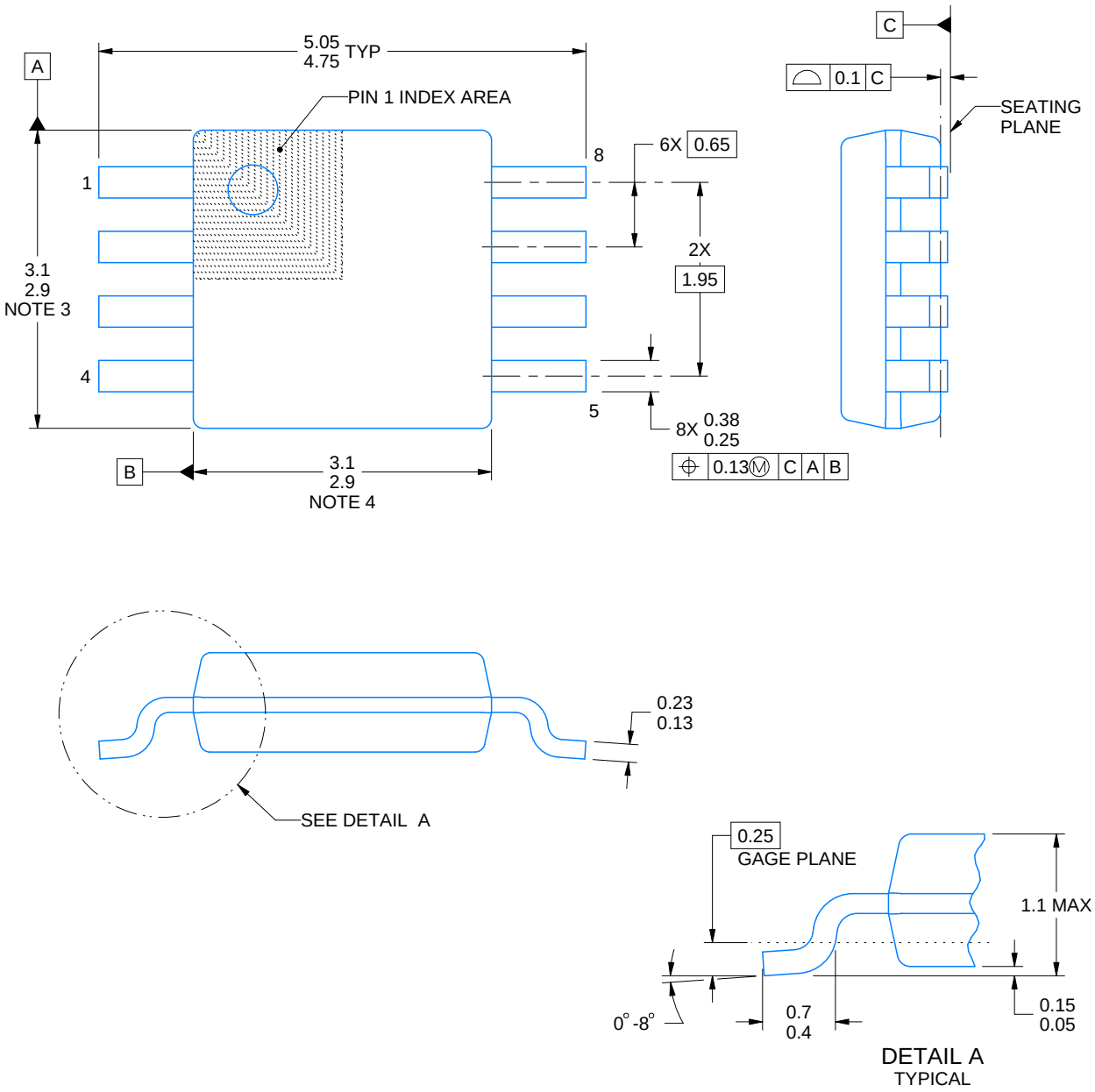
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

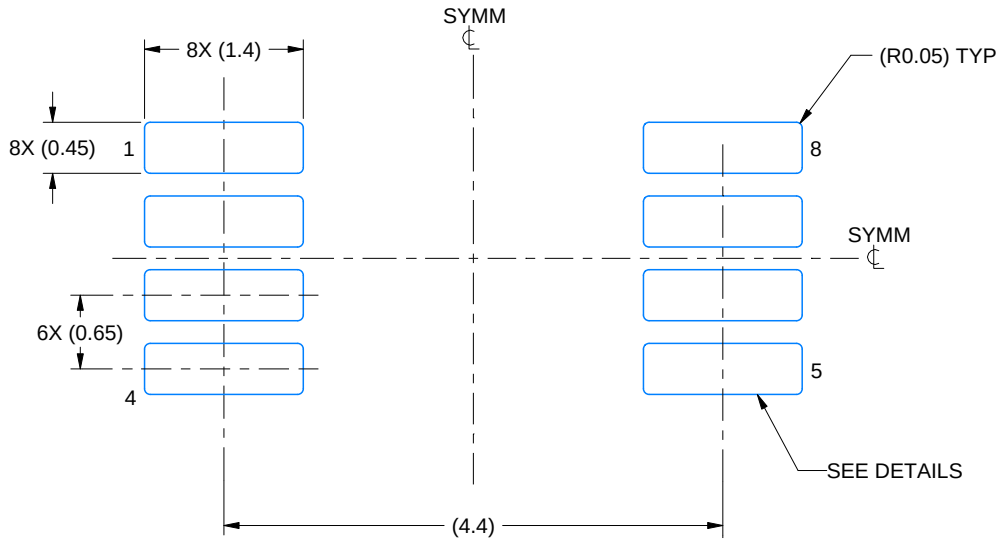
SMALL OUTLINE PACKAGE



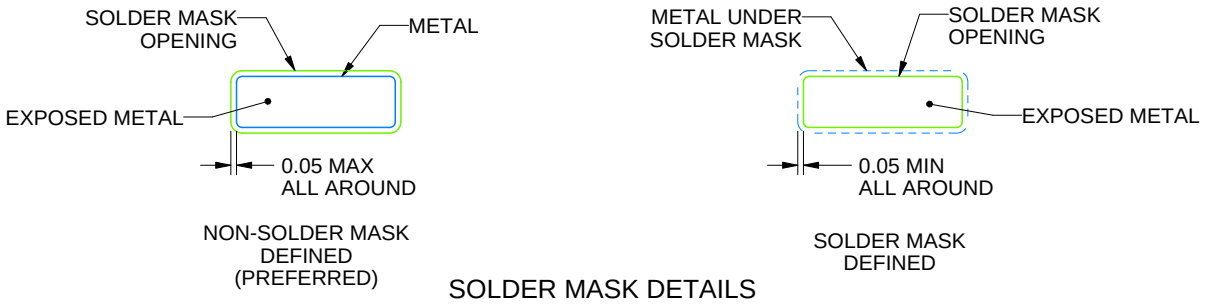
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

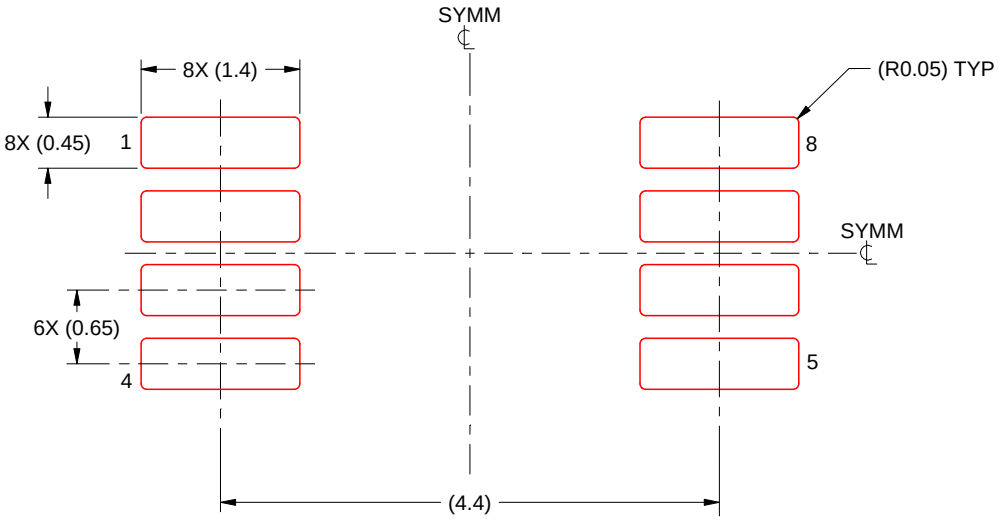


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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