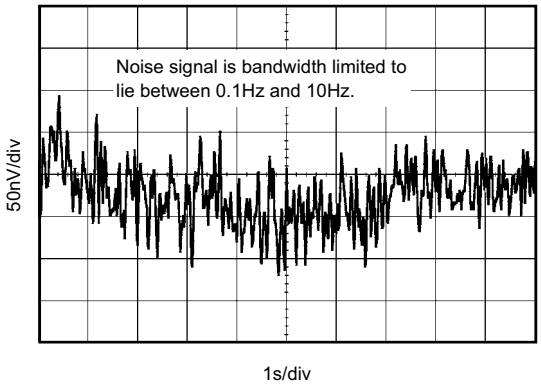
OPAx277 High-Precision Operational Amplifiers

1 Features

- Ultra-low offset voltage: 10 µV
- Ultra-low drift: ±0.1 µV/°C
- High open-loop gain: 134 dB
- High common-mode rejection: 140 dB
- High power-supply rejection: 130 dB
- Low bias current: 1-nA maximum
- Wide supply range: ±2 V to ±18 V
- Low quiescent current: 800 µA/amplifier
- Single, dual, and quad versions
- Replaces OP-07, OP-77, and OP-177
- For similar performance with ±40-V overvoltage protection, see the OPA2206

2 Applications

- Analog input module
- Weigh scale
- Temperature transmitter
- Pressure transmitter
- Data acquisition (DAQ)
- Lab and field instrumentation
- Battery test



0.1-Hz to 10-Hz Noise

3 Description

The OPAx277 series of precision operational amplifiers replace the industry standard OP-177. The OPAx277 devices offer improved noise, wider output voltage swing, and are twice as fast with half the quiescent current. Features include ultra-low offset voltage and drift, low bias current, high common-mode rejection, and high power supply rejection.

The OPAx277 operate from ±2-V to ±18-V supplies with excellent performance. Unlike most op amps that are specified at only one supply voltage, the OPAx277 series is specified for real-world applications; a single limit applies over the ±5-V (10-V) to ±15-V (30-V) supply range. High performance is maintained as the amplifiers swing to the specified limits. Because the initial offset voltage (±20 µV, maximum) is so low, user adjustment is usually not required. However, the single version (OPA277) provides external trim pins for special applications.

The OPAx277 are easy to use and free from phase inversion and the overload problems found in some other op amps. These devices are unity-gain stable and provide excellent dynamic behavior over a wide range of load conditions. Dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
OPA277, OPA2277	D (SOIC, 8)	3.91 mm × 4.90 mm
	DRM (VSON, 8)	4.00 mm × 4.00 mm
	P (PDIP, 8)	6.35 mm × 9.81 mm
OPA4277	D (SOIC, 14)	3.91 mm × 8.65 mm
	P (PDIP, 14)	6.35 mm × 19.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2015) to Revision C (February 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed *Applications* bullets to include links	1
• Deleted text regarding identical specification for the single, dual, and quad versions	1
• Changed Offset Trim pin type from "Input" to "—"	3
• Changed "DFN" to "DRM (VSON)" in *OPA2277 Pin Functions* table	3
• Added table note for 10-mA current limit on input pins in *Absolute Maxiimum Ratings*	6
• Deleted operating temperature from *Absolute Maximum Ratings*	6
• Deleted lead temperature from *Absolute Maximum Ratings*	6
• Changed *Thermal Information* values for OPA2277 and OPA4277 SOIC packages	7
• Added test conditions to *Electrical Characteristics* header	8
• Changed format of *Electrical Characteristcs* for readability	8
• Changed input offset voltage vs. time to long-term drift in *Electrical Characteristics*	8
• Changed input bias current test condition to separate over temperature specification	8
• Deleted redundant row in *open-loop gain* parameter	8
• Changed C_{LOAD} to C_L for consistency	8
• Changed Figure 6-14, *Change in Input Bias Current vs Common-Mode Voltage*, to correct typo in note	10
• Changed "DFN package" to "DRM package (8-pin VSON)"	21
• Changed "DFN package" to "DRM Package" and added "8-Pin VSON"	21
• Changed *Development Support* section to show updated links and resources	23

Changes from Revision A (April 2005) to Revision B (April 2015)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

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5 Pin Configuration and Functions

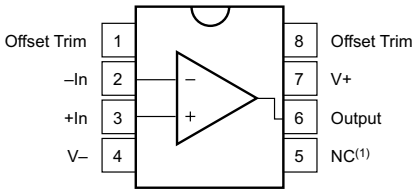

Figure 5-1. OPA277 P Package, 8-Pin PDIP and D Package, 8-Pin SOIC (Top View)

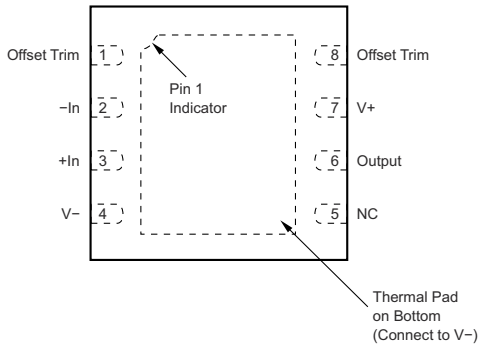

Figure 5-2. OPA277 DRM Package, 8-Pin VSON (Top View)

Table 5-1. Pin Functions: OPA277

PIN		TYPE	DESCRIPTION
NAME	NO.		
–In	2	Input	Inverting input
+In	3	Input	Noninverting input
NC	5	—	No internal connection (can be left floating)
Offset Trim	1	—	Input offset voltage trim (leave floating if not used)
Offset Trim	8	—	Input offset voltage trim (leave floating if not used)
Output	6	Output	Output
V–	4	—	Negative (lowest) power supply
V+	7	—	Positive (highest) power supply

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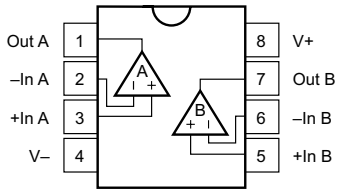

Figure 5-3. OPA2277 P Package, 8-Pin PDIP and D Package, 8-Pin SOIC (Top View)

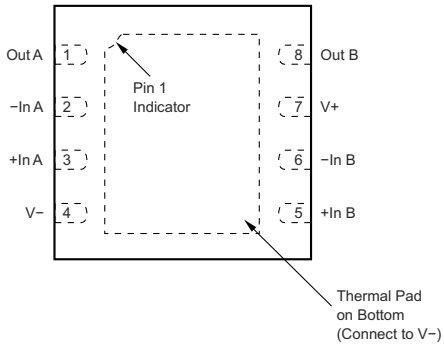

Figure 5-4. OPA2277 DRM Package, 8-Pin VSON (Top View)

Table 5-2. Pin Functions: OPA2277

PIN			TYPE	DESCRIPTION
NAME	D (SOIC), P (PDIP)	DRM (VSON)		
–In A	2	2	Input	Inverting input channel A
–In B	6	6	Input	Inverting input channel B
+In A	3	3	Input	Noninverting input channel A
+In B	5	5	Input	Noninverting input channel B
Out A	1	1	Output	Output channel A
Out B	7	8	Output	Output channel B
V–	4	4	—	Negative (lowest) power supply
V+	8	7	—	Positive (highest) power supply

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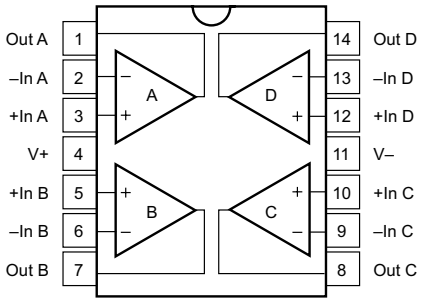

Figure 5-5. OPA4277 P Package, 14-Pin PDIP and D Package, 14-Pin SOIC (Top View)

Table 5-3. Pin Functions: OPA4277

PIN		TYPE	DESCRIPTION
NAME	NO.		
–In A	2	Input	Inverting input channel A
–In B	6	Input	Inverting input channel B
–In C	9	Input	Inverting input channel C
–In D	13	Input	Inverting input channel D
+In A	3	Input	Noninverting input channel A
+In B	5	Input	Noninverting input channel B
+In C	10	Input	Noninverting input channel C
+In D	12	Input	Noninverting input channel D
Out A	1	Output	Output channel A
Out B	7	Output	Output channel B
Out C	8	Output	Output channel C
Out D	14	Output	Output channel D
V+	4	—	Positive (highest) power supply
V–	11	—	Negative (lowest) power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)		36	V
	Input voltage(2)	(V–) – 0.7	(V+) + 0.7	V
I_{SC}	Output short circuit(3)	Continuous		
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Limit input signals that can swing more than 0.7 V beyond the supply rails to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single supply	4	30	36	V
		Dual supply	±2	±15	±18	
T_A	Ambient temperature		–40		85	°C

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6.4 Thermal Information: OPA277

THERMAL METRIC[1]		OPA277			UNIT
		D (SOIC)	DRM (VSON)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.1	40.7	49.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	52.2	41.3	39.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.3	16.7	26.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	0.6	15.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.5	16.9	26.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	3.3	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report

6.5 Thermal Information: OPA2277

THERMAL METRIC[1]		OPA2277			UNIT
		D (SOIC)	DRM (VSON)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.9	39.3	47.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	67.1	36.9	36.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.3	15.4	24.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.8	0.4	13.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.5	15.6	24.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	2.2	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report

6.6 Thermal Information: OPA4277

THERMAL METRIC[1]		OPA4277		UNIT
		D (SOIC)	P (PDIP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.5	66.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	38.5	20.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.5	26.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.9	26.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report

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6.7 Electrical Characteristics

at T_A = 25°C, V_S = 10 V to 30 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 2 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	OPA277P, U			±10	±20	µV
		OPA2277P, U			±10	±25	
		OPAx277PA, UA			±20	±50	
		OPAx277AIDRM			±35	±100	
		T_A = –40°C to +85°C	OPA277P, U			±30	
			OPA2277P, U			±50	
			OPAx277PA, UA			±100	
			OPAx277AIDRM			±165	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +85°C	OPA277P, U		±0.1	±0.15	µV/°C
			OPA2277P, U		±0.1	±0.25	
			OPAx277AIDRM, PA, UA		±0.15	±1	
	Long-term drift				0.2		µV/mo
PSRR	Power-supply rejection ratio	V_S = ±2 V to ±18 V	OPAx277P, U		±0.3	±0.5	µV/V
			OPAx277AIDRM, PA, UA		±0.3	±1	
		V_S = ±2 V to ±18 V, T_A = –40°C to +85°C	OPAx277P, U			±0.5	
			OPAx277AIDRM, PA, UA			±1	
	Channel separation (dual, quad)	dc			0.1		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current	OPAx277P, U			±0.5	±1	nA
		OPAx277AIDRM, PA, UA			±0.5	±2.8	
		T_A = –40°C to +85°C	OPAx277P, U			±2	
			OPAx277AIDRM, PA, UA			±4	
I_{OS}	Input offset current	OPAx277P, U			±0.5	±1	nA
		OPAx277AIDRM, PA, UA			±0.5	±2.8	
		T_A = –40°C to +85°C	OPAx277P, U			±2	
			OPAx277AIDRM, PA, UA			±4	
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			0.22		$µV_{PP}$
e_n	Input voltage noise density	f = 10 Hz			12		nV/√Hz
		f = 100 Hz			8		
		f = 1 kHz			8		
		f = 10 kHz			8		
i_n	Input current noise density	f = 1 kHz			0.2		pA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) + 2		(V+) – 2	V
CMRR	Common-mode rejection ratio	V_{CM} = (V–) + 2 V to (V+) – 2 V	OPAx277P, U	130	140		dB
			OPAx277AIDRM, PA, UA	115	140		
		V_{CM} = (V–) + 2 V to (V+) – 2 V, T_A = –40°C to +85°C	OPAx277P, U	128			
			OPAx277AIDRM, PA, UA	115			
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 3		MΩ || pF
Z_{IC}	Common-mode	V_{CM} = (V–) + 2 V to (V+) – 2 V			250 || 3		GΩ || pF

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6.7 Electrical Characteristics (continued)

at T_A = 25°C, V_S = 10 V to 30 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 2 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_O = (V–) + 0.5 V to (V+) – 1.2 V, R_L = 10 kΩ			140		dB
		V_O = (V–) + 1.5 V to (V+) – 1.5 V, R_L = 2 kΩ		126	134		
			T_A = –40°C to +85°C	126			
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				1		MHz
SR	Slew rate				0.8		V/µs
t_s	Settling time	V_S = ±15 V, G = 1, 10-V step	To 0.1%		14		µs
			To 0.01%		16		
t_{OR}	Overload recovery time	V_{IN} × G = V_S			3		µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.002%		
OUTPUT							
V_O	Voltage output	R_L = 10 kΩ		(V–) + 0.5		(V+) – 1.2	V
			T_A = –40°C to +85°C	(V–) + 0.5		(V+) – 1.2	
		R_L = 2 kΩ		(V–) + 1.5		(V+) – 1.5	
			T_A = –40°C to +85°C	(V–) + 1.5		(V+) – 1.5	
I_{SC}	Short-circuit current				±35		mA
C_L	Capacitive load drive				See Typical Characteristics		
Z_O	Open-loop output impedance	f = 1 MHz			40		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			±790	±825	µA
			T_A = –40°C to +85°C			±900	

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6.8 Typical Characteristics

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

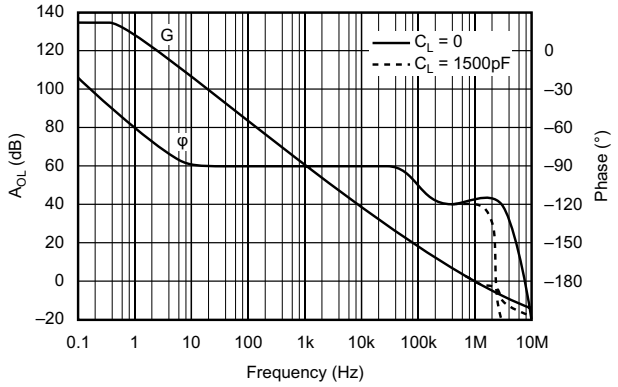

Figure 6-1. Open-Loop Gain and Phase vs Frequency

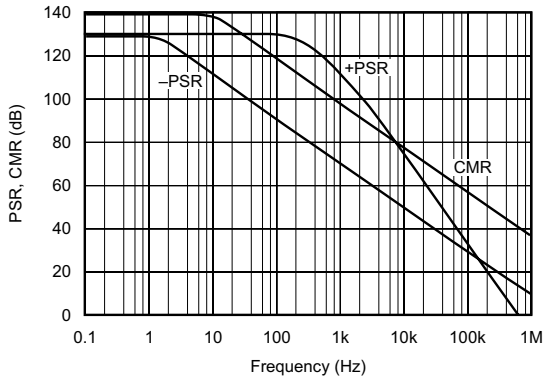

Figure 6-2. Power Supply and Common-Mode Rejection vs Frequency

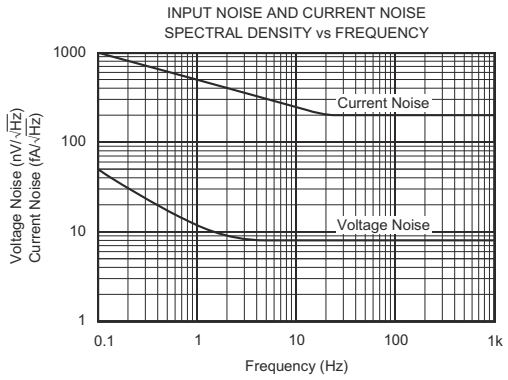

Figure 6-3. Input Noise and Current Noise Spectral Density vs Frequency

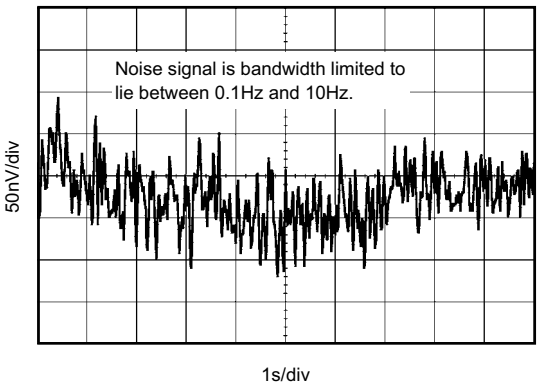

Figure 6-4. Input Noise Voltage vs Time

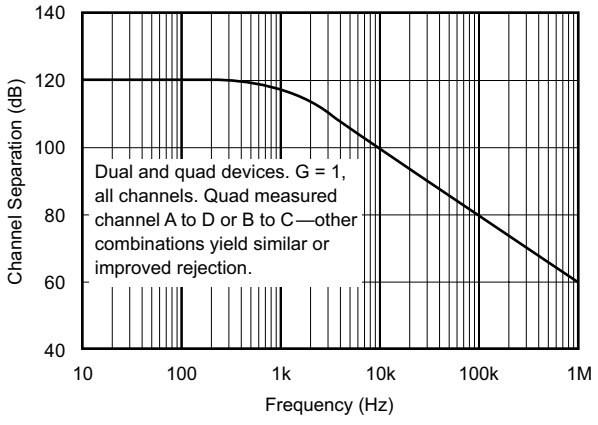

Figure 6-5. Channel Separation vs Frequency

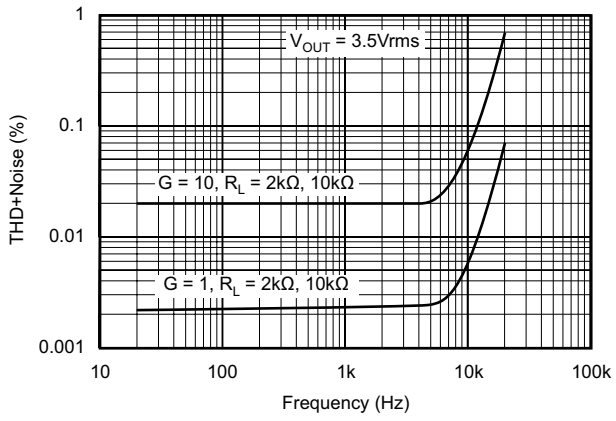

Figure 6-6. Total Harmonic Distortion + Noise vs Frequency

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6.8 Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

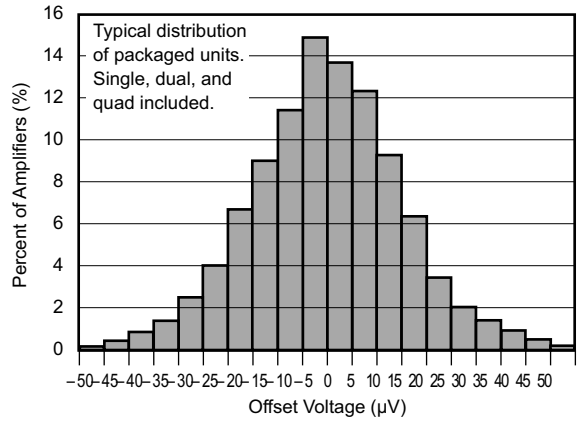

Figure 6-7. Offset Voltage Production Distribution

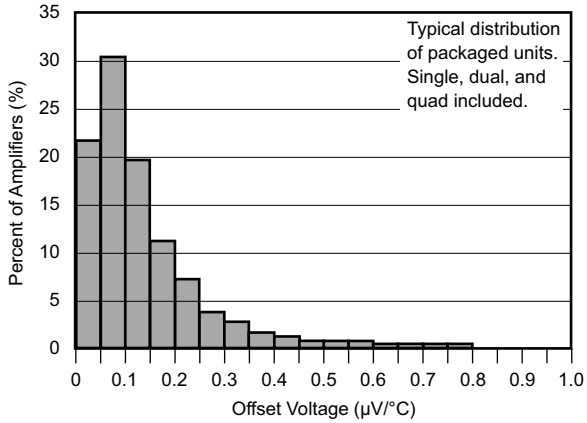

Figure 6-8. Offset Voltage Drift Production Distribution

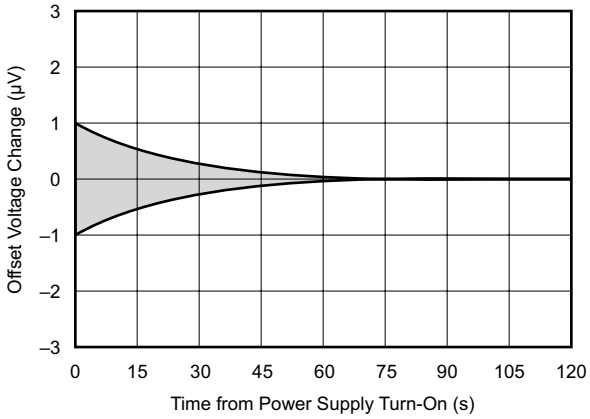

Figure 6-9. Warm-Up Offset Voltage Drift

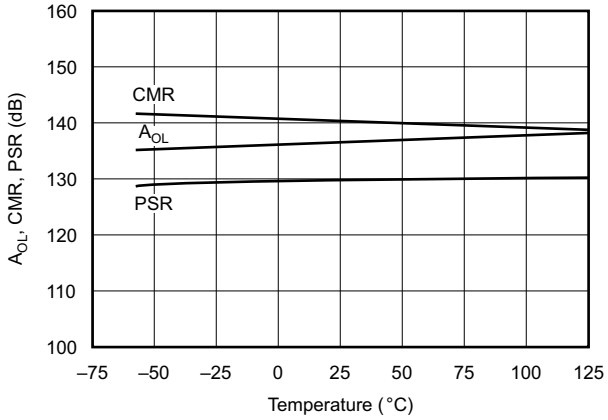

Figure 6-10. A_{OL}, CMR, PSR vs Temperature

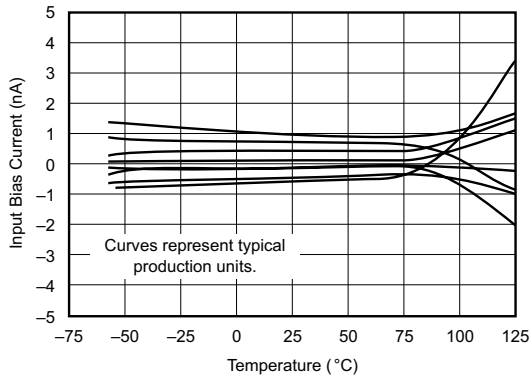

Figure 6-11. Input Bias Current vs Temperature

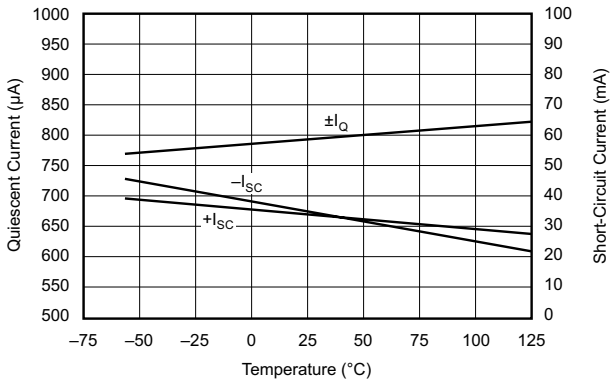

Figure 6-12. Quiescent Current and Short-Circuit Current vs Temperature

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6.8 Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

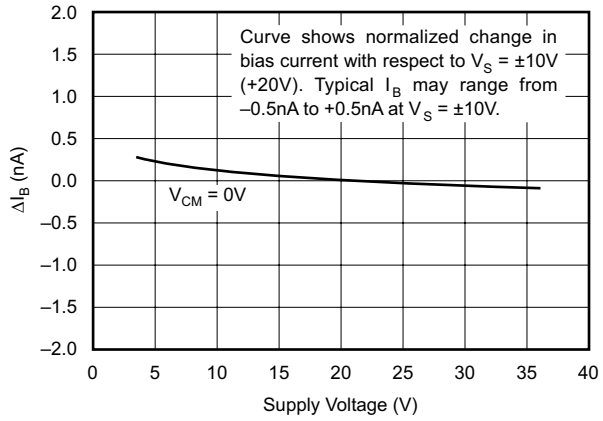

Figure 6-13. Change in Input Bias Current vs Power-Supply Voltage

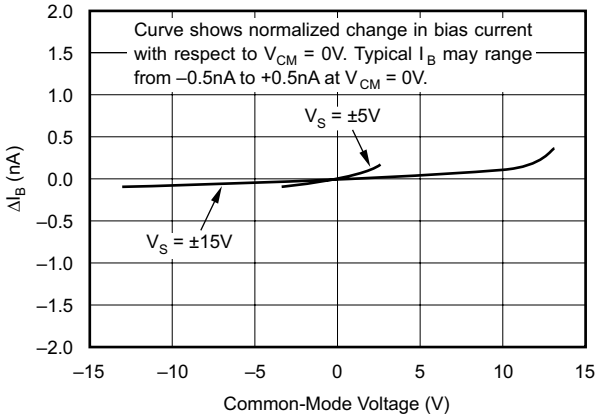

Figure 6-14. Change in Input Bias Current vs Common-Mode Voltage

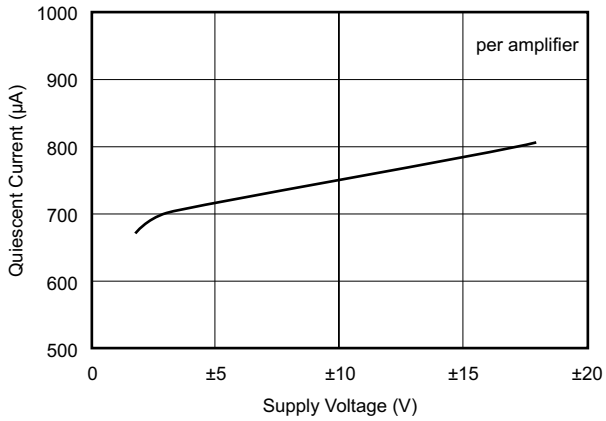

Figure 6-15. Quiescent Current vs Supply Voltage

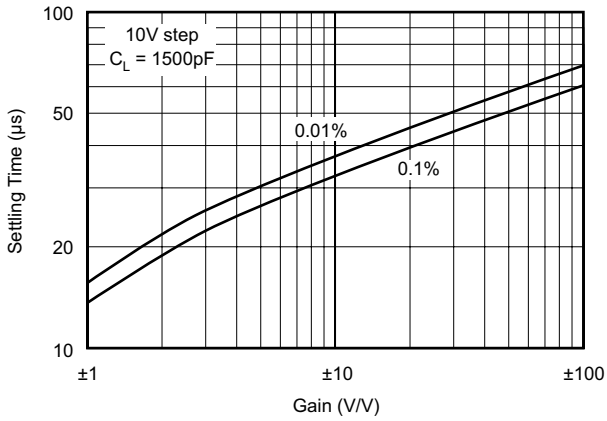

Figure 6-16. Settling Time vs Closed-Loop Gain

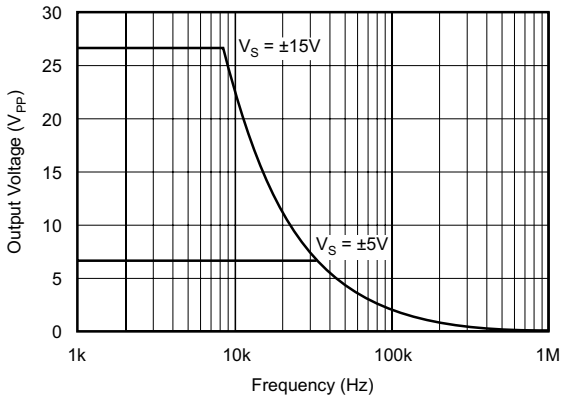

Figure 6-17. Maximum Output Voltage vs Frequency

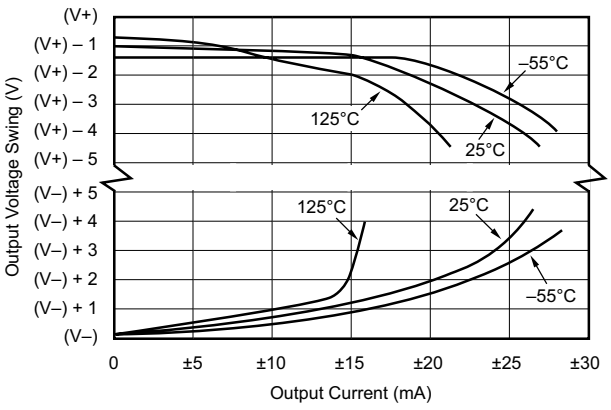

Figure 6-18. Output Voltage Swing vs Output Current

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6.8 Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

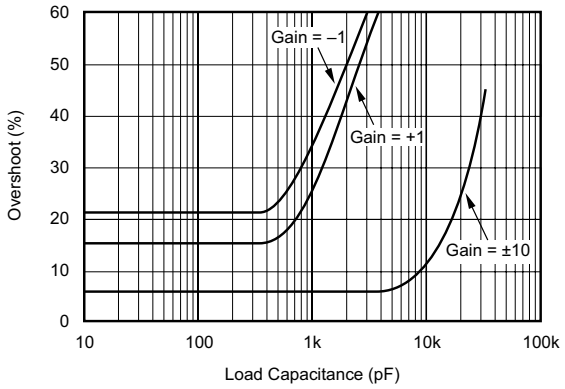
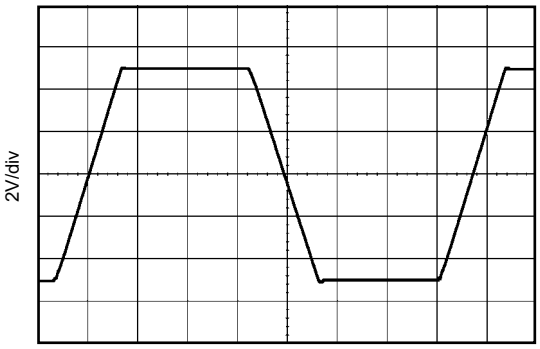
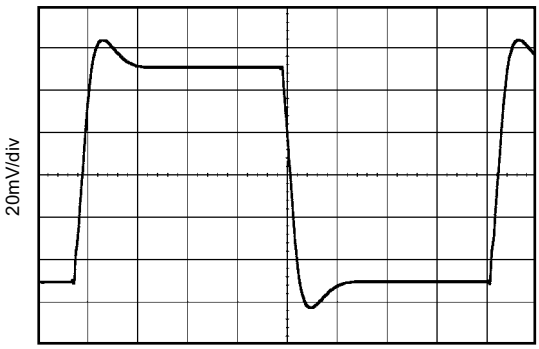


Figure 6-19. Small-Signal Overshoot vs Load Capacitance



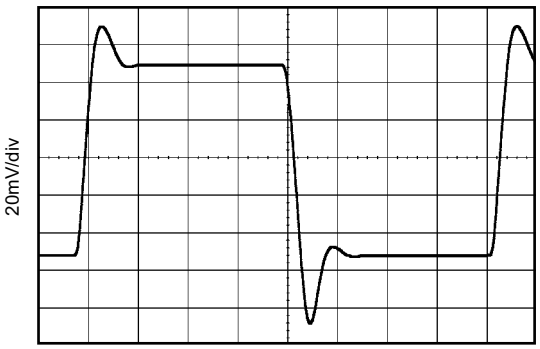
G = 1, C_L = 1500 pF, V_S = ±15 V

Figure 6-20. Large-Signal Step Response



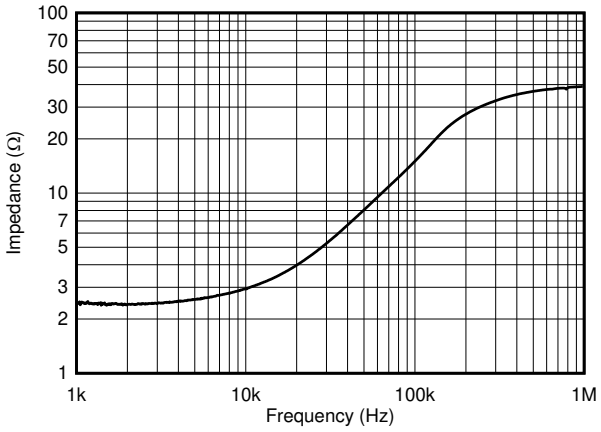
G = 1, C_L = 0, V_S = ±15 V

Figure 6-21. Small-Signal Step Response



G = 1, C_L = 1500 pF, V_S = ±15 V

Figure 6-22. Small-Signal Step Response



V_S = ±15 V

Figure 6-23. Open-Loop Output Impedance

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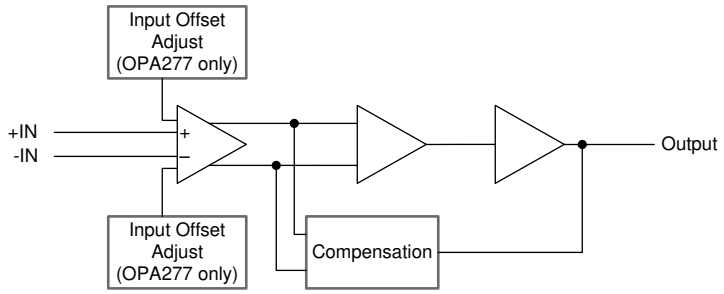
7 Detailed Description

7.1 Overview

The OPAx277 series precision operational amplifiers replace the industry standard OP-177. These devices offer improved noise, wider output voltage swing, and are twice as fast with half the quiescent current. Features include ultra-low offset voltage and drift, low bias current, high common-mode rejection, and high power-supply rejection.

7.2 Functional Block Diagram



7.3 Feature Description

The OPAx277 series is unity-gain stable and free from unexpected output phase reversal, making these devices easy to use in a wide range of applications. Applications with noisy or high-impedance power supplies can require decoupling capacitors close to the device pins. In most cases 0.1-µF capacitors are adequate.

The OPAx277 series has low offset voltage and drift. To achieve highest performance, optimize the circuit layout and mechanical conditions. Offset voltage and drift can be degraded by small thermoelectric potentials at the operational amplifier inputs. Connections of dissimilar metals generate thermal potential, which can degrade the ultimate performance of the OPAx277 series. To cancel these thermal potentials, make sure that the thermal potentials are equal in both input pins.

- Keep the thermal mass of the connections to the two input pins similar
- Locate heat sources as far as possible from the critical input circuitry
- Shield operational amplifier and input circuitry from air currents, such as cooling fans

7.3.1 Operating Voltage

The OPAx277 series of operational amplifiers operate from ±2-V to ±18-V supplies with excellent performance. Unlike most operational amplifiers, which are specified at only one supply voltage, the OPAx277 series is specified for real-world applications; a single limit applies over the ±5-V to ±15-V supply range. This single limit allows a customer operating at V_S = ±10 V to have the same specified performance as a customer using ±15-V supplies. In addition, key parameters are specified over the specified temperature range of –40°C to +85°C. Most behavior remains unchanged through the full operating voltage range of ±2 V to ±18 V. Parameters that vary significantly with operating voltage or temperature are shown in *Section 6.8*.

7.3.2 Offset Voltage Adjustment

The OPAx277 series is laser-trimmed for low offset voltage and drift, so most circuits do not require external adjustment. However, for the OPA277, offset voltage trim connections are provided on pins 1 and 8. Figure 7-1 shows how the offset voltage can be adjusted by connecting a potentiometer. Only use this adjustment to null the offset of the operational amplifier. Do not use this adjustment to compensate for offsets created elsewhere in a system, because additional temperature drift can be introduced.

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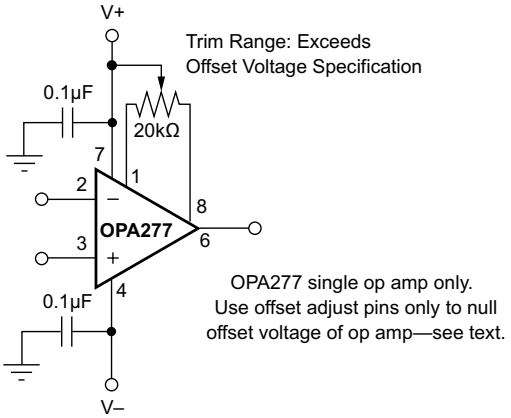


Figure 7-1. OPA277 Offset Voltage Trim Circuit

7.3.3 Input Protection

The inputs of the OPAx277 devices protected with 1-kΩ series input resistors and diode clamps. The inputs can withstand ±30-V differential inputs without damage. The protection diodes conduct current when the inputs are overdriven. This conducted current can disturb the slewing behavior of unity-gain follower applications, but does not damage the operational amplifier.

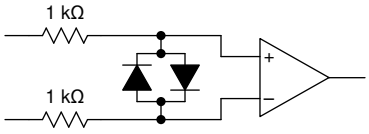
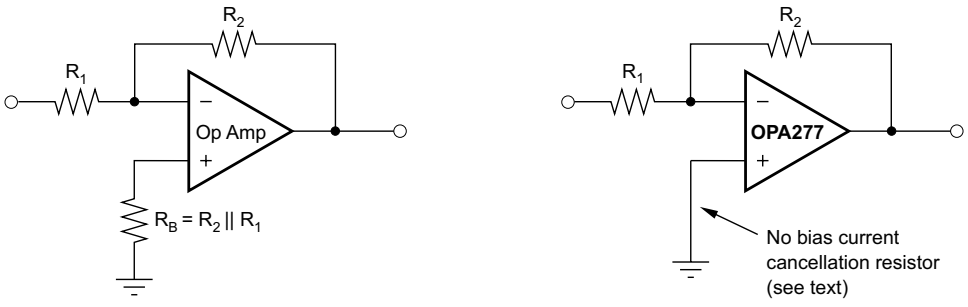


Figure 7-2. OPAx277 Input Protection

7.3.4 Input Bias Current Cancellation

The input stage base current of the OPAx277 series is internally compensated with an equal and opposite cancellation circuit. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

When the bias current is canceled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, a bias current cancellation resistor is not necessary, as is often done with other operational amplifiers. Figure 7-3 shows a conventional op amp with external bias current cancellation resistor compared to the OPA277 with no external bias current cancellation resistor. A resistor added to cancel input bias current errors can actually increase offset voltage and noise.



(a)

Conventional op amp with external bias current cancellation resistor.

(b)

OPA277 with no external bias current cancellation resistor.

Figure 7-3. Input Bias Current Cancellation

7.3.5 EMI Rejection Ratio (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many operational amplifiers is a change in the offset voltage as a result of RF signal rectification. An operational amplifier that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this report provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the operational amplifier. In general, only the noninverting input is tested for EMIRR for the following three reasons:

1. Operational amplifier input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
2. The noninverting and inverting operational amplifier inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
3. EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a printed circuit board (PCB). This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.

A more formal discussion of the EMIRR IN+ definition and test method is provided in the *EMI Rejection Ratio of Operational Amplifiers* application note, available for download at www.ti.com. Figure 7-4 shows the EMIRR IN+ of the OPA277 plotted versus frequency.

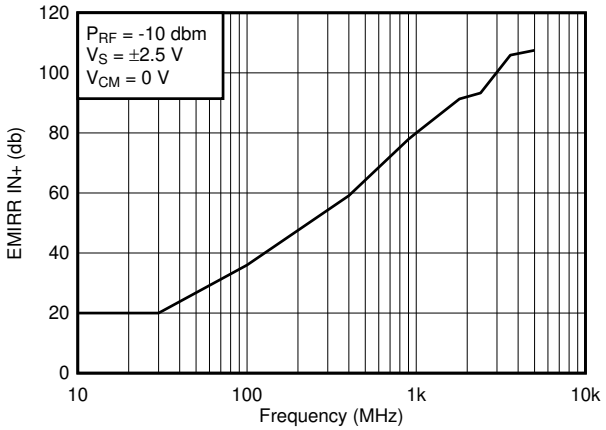


Figure 7-4. OPA277 EMIRR IN+ vs Frequency

If available, any dual and quad operational amplifier device versions have nearly similar EMIRR IN+ performance. The OPA277 unity-gain bandwidth is 1 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the operational amplifier bandwidth.

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Table 7-1 shows the EMIRR IN+ values for the OPA277 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 7-1 can be centered on or operated near the particular frequency shown. This information is of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

Table 7-1. OPA277 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION/ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite-space operation, weather, radar, UHF	59.1 dB
900 MHz	GSM, radio com-nav-GPS (to 1.6 GHz), ISM, aeronautical mobile, UHF	77.9 dB
1.8 GHz	GSM, mobile personal comm. broadband, satellite, L-band	91.3 dB
2.4 GHz	802.11b/g/n, Bluetooth®, mobile personal comm, ISM, amateur radio-satellite, S-band	93.3 dB
3.6 GHz	Radiolocation, aero comm-nav, satellite, mobile, S-band	105.9 dB
5.0 GHz	802.11a/n, aero comm-nav, mobile comm, space-satellite operation, C-band	107.5 dB

7.3.5.1 EMIRR IN+ Test Configuration

Figure 7-5 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the operational amplifier noninverting input terminal using a transmission line. The operational amplifier is configured in a unity-gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the operational amplifier input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting dc offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that can interfere with multimeter accuracy. See the *EMI Rejection Ratio of Operational Amplifiers* application note for more details.

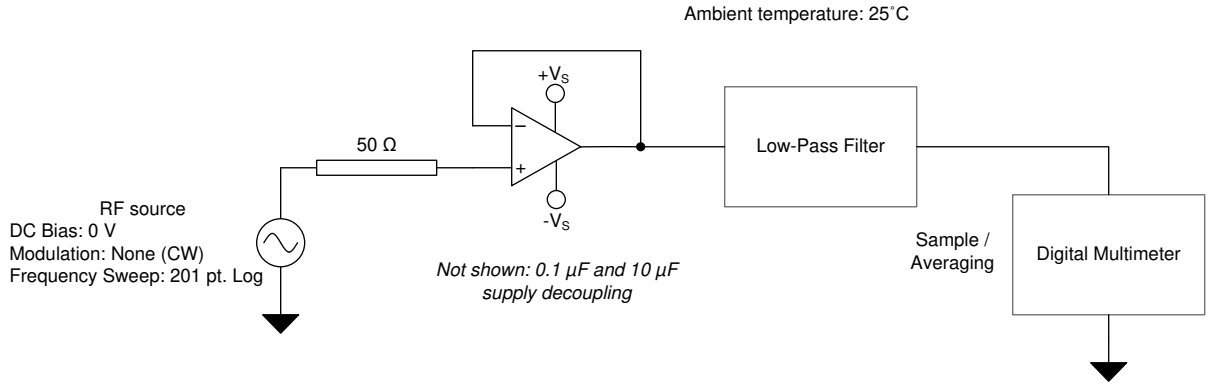

Figure 7-5. EMIRR IN+ Test Configuration Schematic

7.4 Device Functional Modes

The OPAx277 has a single functional mode and is operational when the power-supply voltage is greater than 4 V (±2 V). The maximum power supply voltage for the OPAx277 is 36 V (±18 V).

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The OPAx277 family offers outstanding dc precision and ac performance. These devices operate up to 36-V supply rails and offer ultralow offset voltage and offset voltage drift, as well as 1-MHz bandwidth and high capacitive load drive. These features make the OPAx277 a robust, high-performance operational amplifier for high-voltage industrial applications.

8.2 Typical Applications

8.2.1 Second-Order, Low-Pass Filter

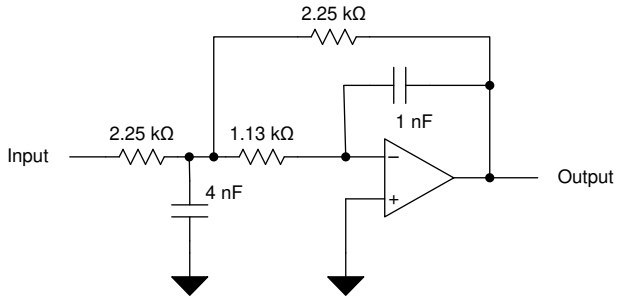

Figure 8-1. Second-Order, Low-Pass Filter

8.2.1.1 Design Requirements

- Gain = 1 V/V
- Low-pass cutoff frequency = 50 kHz
- –40 db/dec filter response
- Maintain less than 3-dB gain peaking in the gain versus frequency response

8.2.1.2 Detailed Design Procedure

The Filter Design Tool is a simple, powerful, and easy-to-use active filter design program. The Filter Design Tool lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the Design tools and simulation website, the Filter Design Tool allows you to design, optimize, and simulate complete multistage active-filter solutions within minutes.

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8.2.1.3 Application Curve

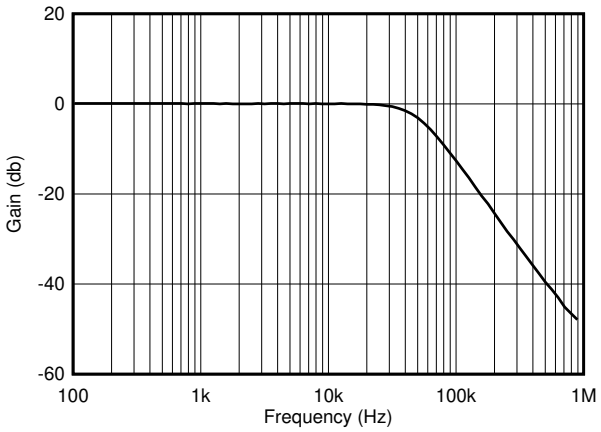
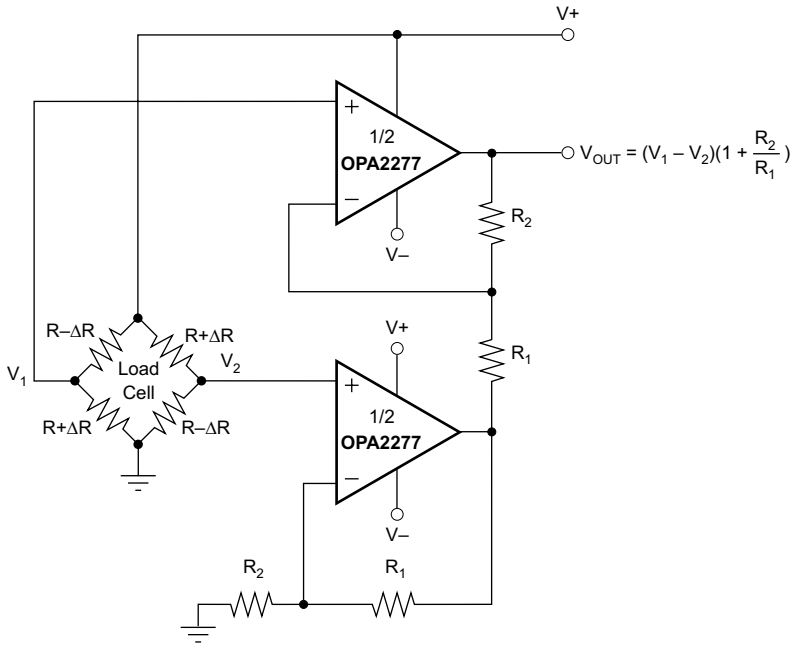


Figure 8-2. OPA277 Second-Order, 50-kHz, Low-Pass Filter

8.2.2 Load Cell Amplifier



For integrated solution see: INA126, INA2126 (dual)
INA125 (on-board reference)
INA122 (single-supply)

Figure 8-3. Load Cell Amplifier

8.2.3 Thermocouple Low-Offset, Low-Drift Loop Measurement With Diode Cold Junction Compensation

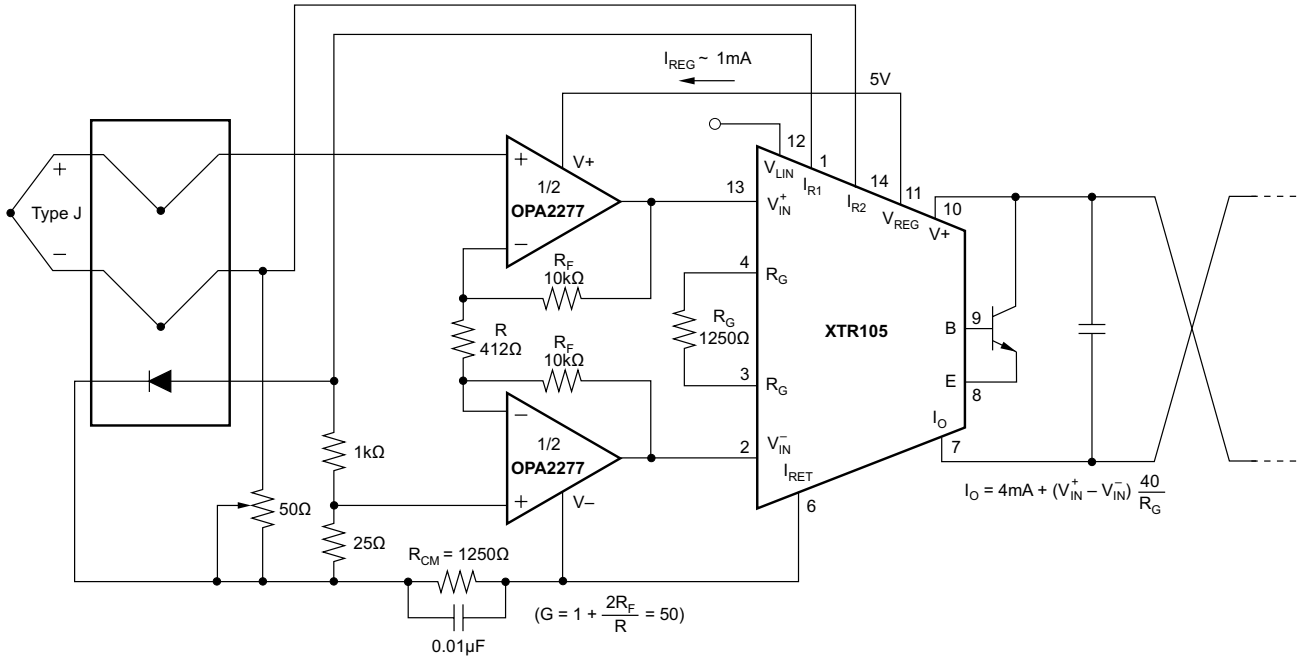


Figure 8-4. Thermocouple Low-Offset, Low-Drift Loop Measurement With Diode Cold Junction Compensation

8.3 Power Supply Recommendations

The OPAx277 is specified for operation from 4 V to 36 V (±2 V to ±18 V); many specifications apply from –40°C to 85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Section 6.8*.

CAUTION

Supply voltages larger than 36 V can permanently damage the device; see *Section 6.1*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Section 8.4.1*.

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8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in *Section 8.4.2*, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.
- *DRM package (8-pin VSON) only:* Solder the leadframe die pad to a thermal pad on the PCB. The mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad.
- *DRM package (8-pin VSON) only:* Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long term reliability.

8.4.1.1 DRM Package (8-Pin VSON)

The OPAx277 series uses the DRM package (also known as an 8-pin VSON), a leadless package with contacts on only two sides of the package bottom. This near-chip-scale package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

DRM packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics, with a pinout scheme that is consistent with other commonly-used packages, such as SOIC and VSSOP. Additionally, the absence of external leads eliminates bent-lead issues.

The DRM package can be easily mounted using standard printed-circuit-board (PCB) assembly techniques. See the *QFN/SON PCB Attachment* and *Quad Flatpack No-Lead Logic Packages* application notes, both available for download at www.ti.com.

The exposed leadframe die pad on the bottom of the package must be connected to V–.

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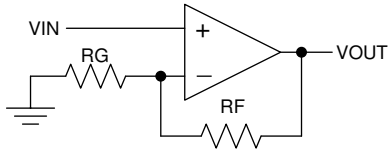
8.4.2 Layout Example



(Schematic Representation)

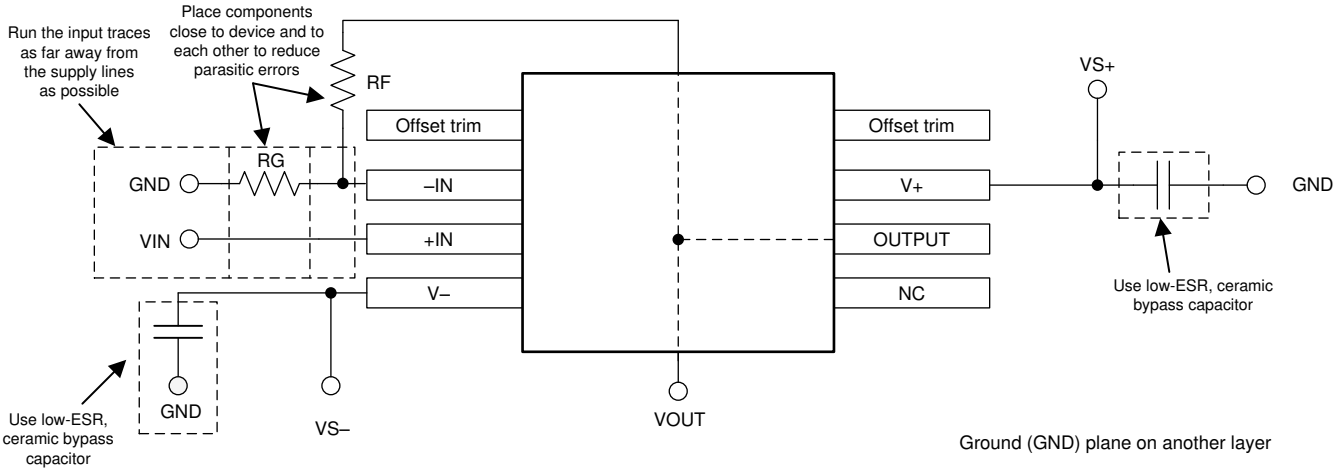


Figure 8-5. OPA277 Layout Example for the Noninverting Configuration

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9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

9.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design tools and simulation web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

9.1.1.3 DIP-Adapter-EVM

Speed up your op amp prototyping and testing with the DIP-Adapter-EVM, which provides a fast, easy and inexpensive way to interface with small, surface-mount devices. Connect any supported op amp using the included Samtec terminal strips or wire them directly to existing circuits. The DIP-Adapter-EVM kit supports the following industry-standard packages: D or U (SOIC-8), PW (TSSOP-8), DGK (VSSOP-8), DBV (SOT-23-6, SOT-23-5 and SOT-23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6).

9.1.1.4 DIYAMP-EVM

The DIYAMP-EVM is a unique evaluation module (EVM) that provides real-world amplifier circuits, enabling the user to quickly evaluate design concepts and verify simulations. This EVM is available in three industry-standard packages (SC70, SOT23, and SOIC) and 12 popular amplifier configurations, including amplifiers, filters, stability compensation, and comparator configurations for both single and dual supplies.

9.1.1.5 TI Reference Designs

TI reference designs are analog solutions created by TI's precision analog applications experts. TI reference designs offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI reference designs are available online at https://www.ti.com/reference-designs.

9.1.1.6 Filter Design Tool

The filter design tool is a simple, powerful, and easy-to-use active filter design program. The filter design tool allows the user to create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the Design tools and simulation web page, the filter design tool allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

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9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following application reports and publications (available for download from www.ti.com):

- Texas Instruments, *QFN/SON PCB Attachment*
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages*
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers*

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2277AIDRMT	Active	Production	VSON (DRM) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	BHZ
OPA2277AIDRMT.B	Active	Production	VSON (DRM) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BHZ
OPA2277AIDRMT1G4	Active	Production	VSON (DRM) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BHZ
OPA2277AIDRMT1G4.B	Active	Production	VSON (DRM) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BHZ
OPA2277P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-	OPA2277P
OPA2277P.B	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA2277P
OPA2277PA	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-	OPA2277PA
OPA2277PA.B	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA2277PA
OPA2277U	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Level-3-260C-168 HR	-	OPA 2277U
OPA2277U.B	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 2277U
OPA2277U/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 2277U
OPA2277U/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 2277U
OPA2277UA	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 2277U A
OPA2277UA.B	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 2277U A
OPA2277UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2277U A
OPA2277UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2277U A
OPA2277UA1G4	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Call TI	-40 to 85	OPA 2277U A
OPA277AIDRMR	Active	Production	VSON (DRM) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	NSS
OPA277AIDRMR.A	Active	Production	VSON (DRM) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NSS

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA277AIDRMT	Active	Production	VSON (DRM) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	NSS
OPA277AIDRMT.A	Active	Production	VSON (DRM) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NSS
OPA277P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	Call TI	N/A for Pkg Type	-	OPA277P
OPA277P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 85	OPA277P
OPA277PA	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	Call TI	N/A for Pkg Type	-	OPA277P A
OPA277PA.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 85	OPA277P A
OPA277PAG4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	Call TI	N/A for Pkg Type	See OPA277PA	OPA277P A
OPA277U	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Level-3-260C-168 HR	-	OPA 277U
OPA277U.B	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 277U
OPA277U/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-	OPA 277U
OPA277U/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 277U
OPA277UA	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-40 to 85	OPA 277U A
OPA277UA.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 277U A
OPA277UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 277U A
OPA277UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 277U A
OPA277UA/2K51G4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	OPA 277U A
OPA277UAG4	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Call TI	-40 to 85	
OPA4277PA	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-	OPA4277PA

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA4277PA.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA4277PA
OPA4277UA	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4277UA
OPA4277UA/2K5	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4277UA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2277, OPA4277 :

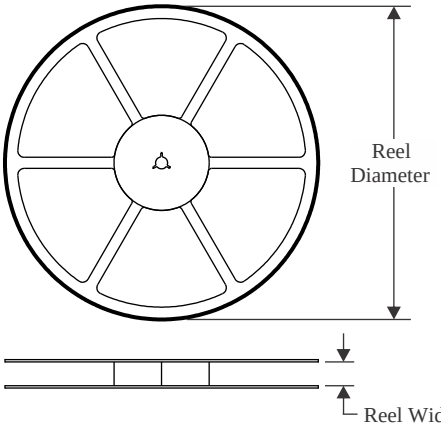
- Enhanced Product : OPA2277-EP, OPA4277-EP
- Space : OPA4277-SP

NOTE: Qualified Version Definitions:

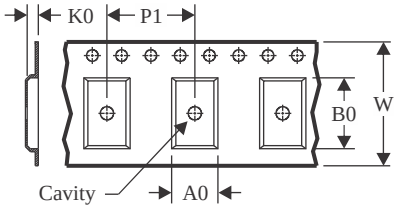
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

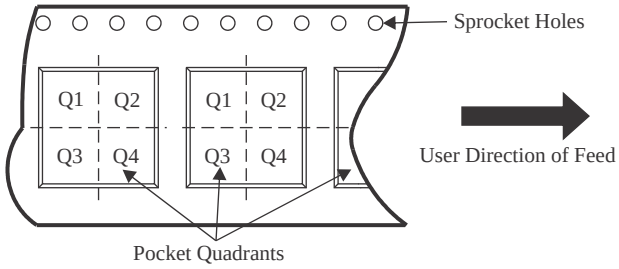


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

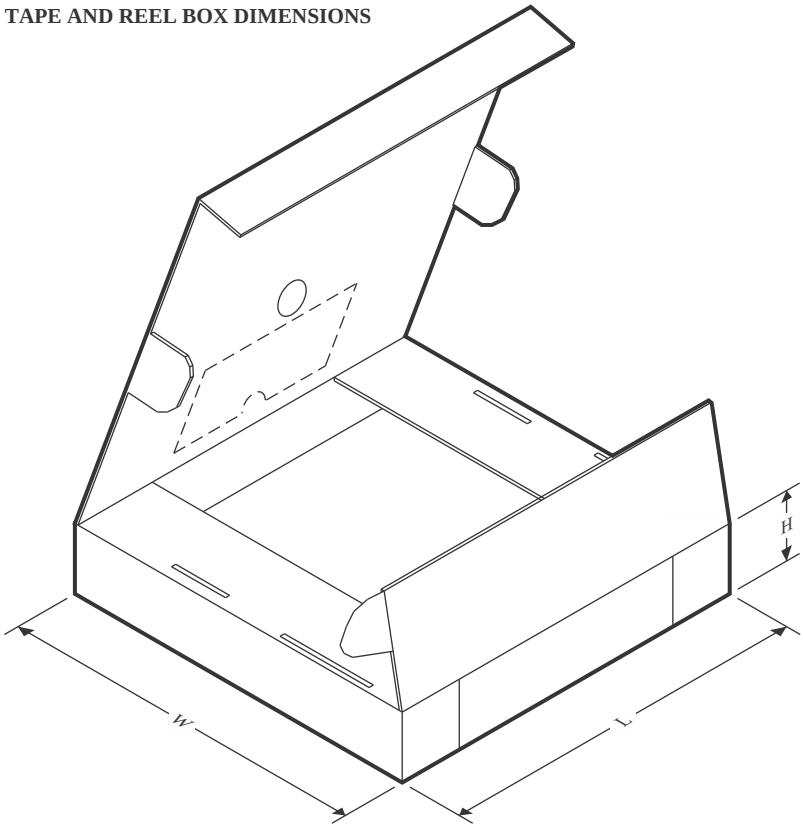
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2277AIDRMT	VSON	DRM	8	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA2277AIDRMT1G4	VSON	DRM	8	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA2277U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2277UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA277AIDRMR	VSON	DRM	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA277AIDRMT	VSON	DRM	8	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA277U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA277UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4277UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

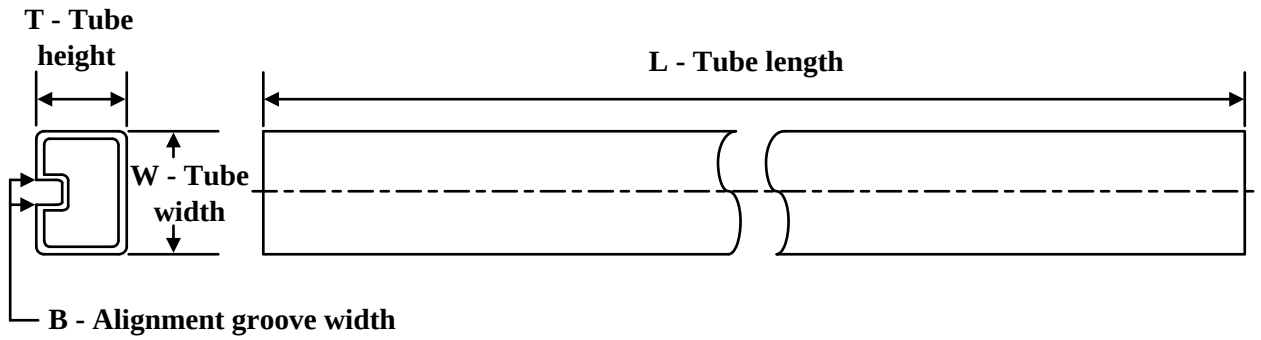
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2277AIDRMT	VSON	DRM	8	250	210.0	185.0	35.0
OPA2277AIDRMT1G4	VSON	DRM	8	250	210.0	185.0	35.0
OPA2277U/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA2277UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA277AIDRMR	VSON	DRM	8	3000	353.0	353.0	32.0
OPA277AIDRMT	VSON	DRM	8	250	213.0	191.0	35.0
OPA277U/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA277UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA4277UA/2K5	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

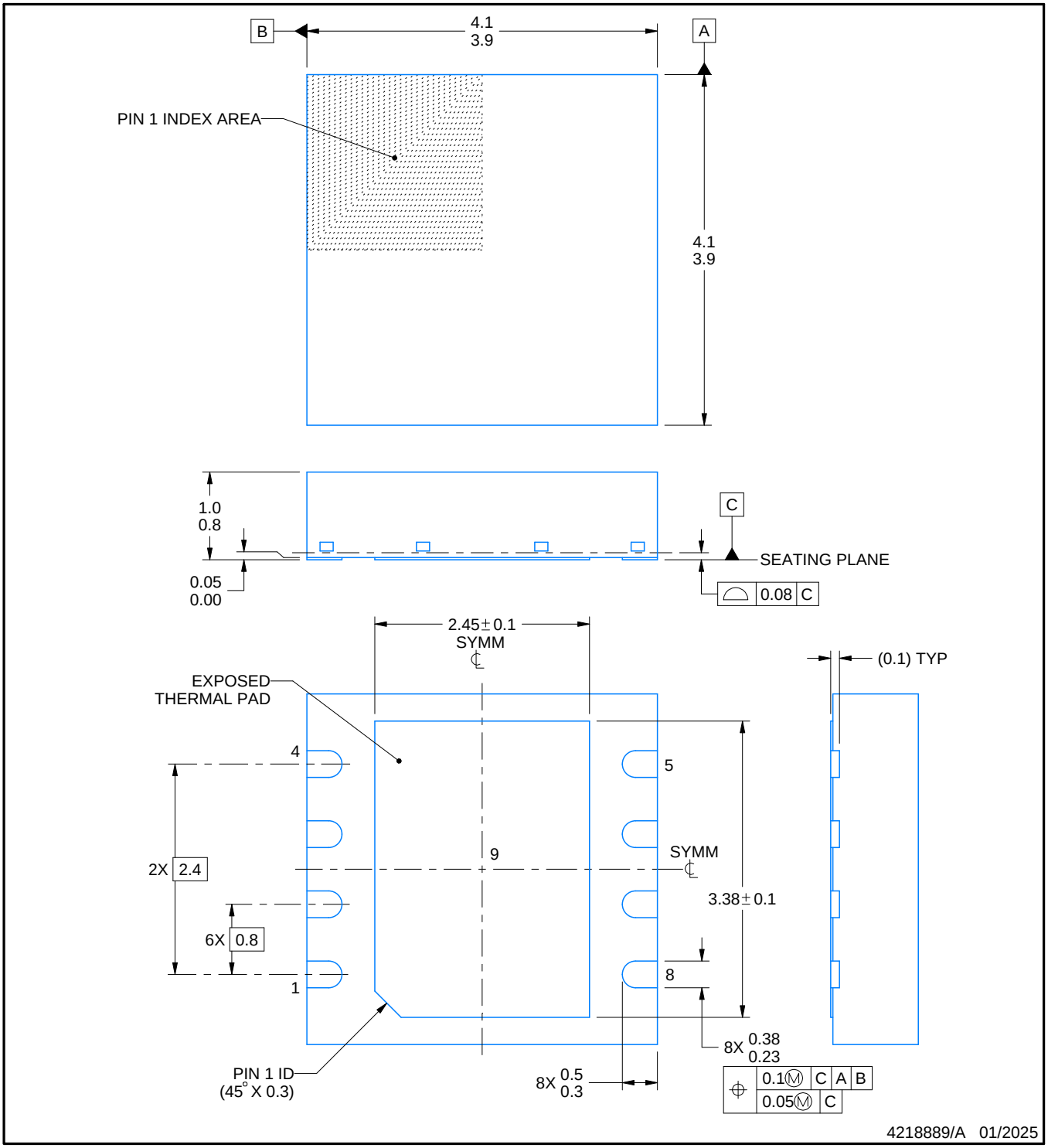
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2277P	P	PDIP	8	50	506	13.97	11230	4.32
OPA2277P.B	P	PDIP	8	50	506	13.97	11230	4.32
OPA2277PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA2277PA.B	P	PDIP	8	50	506	13.97	11230	4.32
OPA2277U	D	SOIC	8	75	506.6	8	3940	4.32
OPA2277U.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2277UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2277UA.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA277P	P	PDIP	8	50	506	13.97	11230	4.32
OPA277P.A	P	PDIP	8	50	506	13.97	11230	4.32
OPA277PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA277PA.A	P	PDIP	8	50	506	13.97	11230	4.32
OPA277PAG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA277U	D	SOIC	8	75	506.6	8	3940	4.32
OPA277U.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA277UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA277UA.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA4277PA	N	PDIP	14	25	506	13.97	11230	4.32
OPA4277PA.A	N	PDIP	14	25	506	13.97	11230	4.32
OPA4277UA	D	SOIC	14	50	506.6	8	3940	4.32

PACKAGE OUTLINE

DRM0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

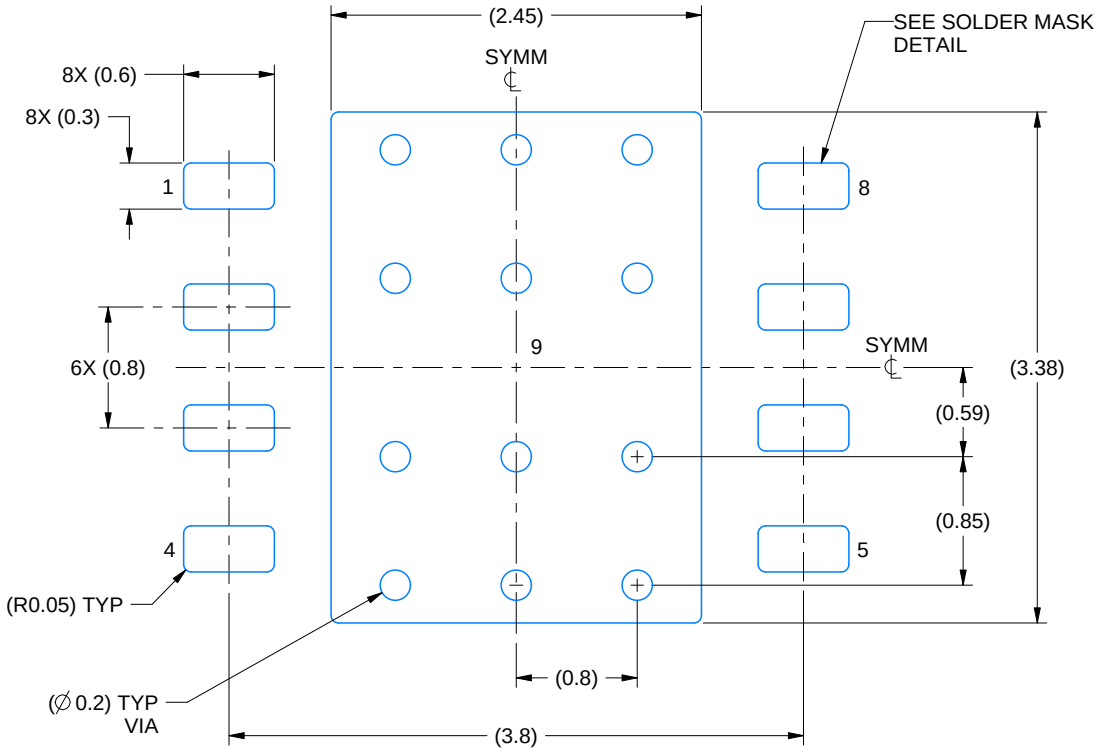
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

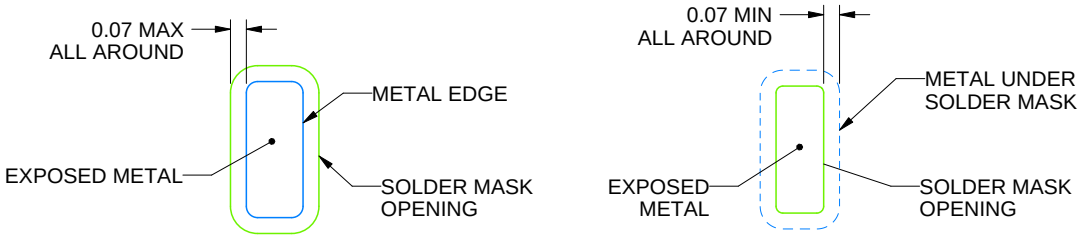
DRM0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

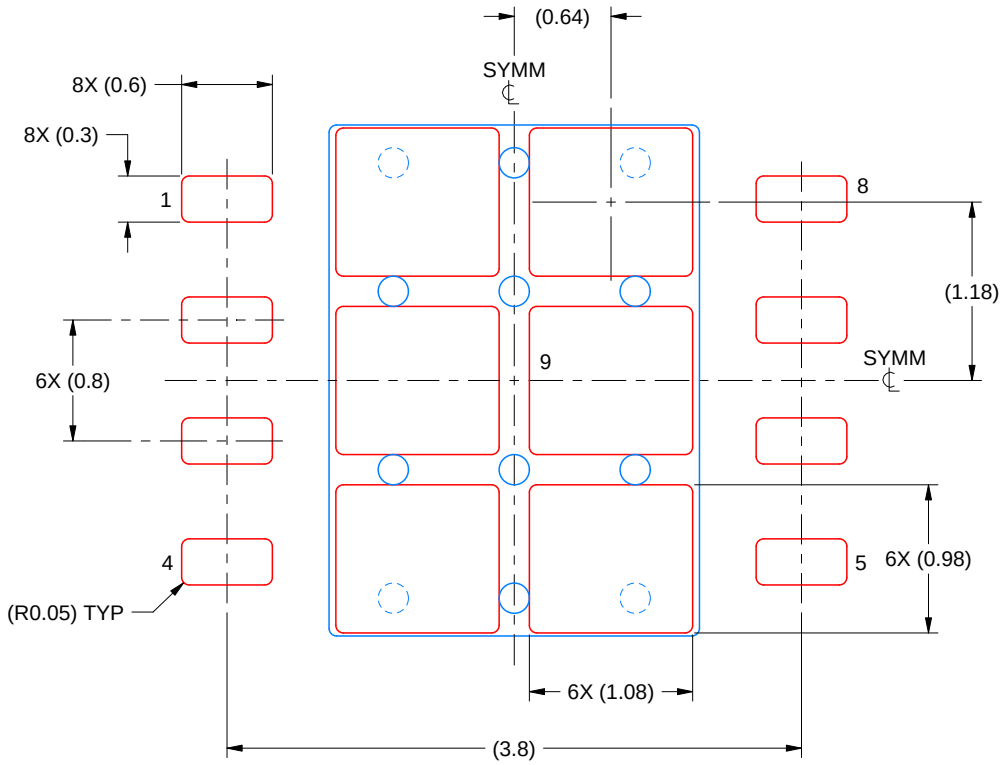
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4218889/A 01/2025

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



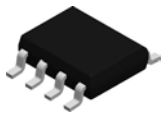
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 9
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4218889/A 01/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

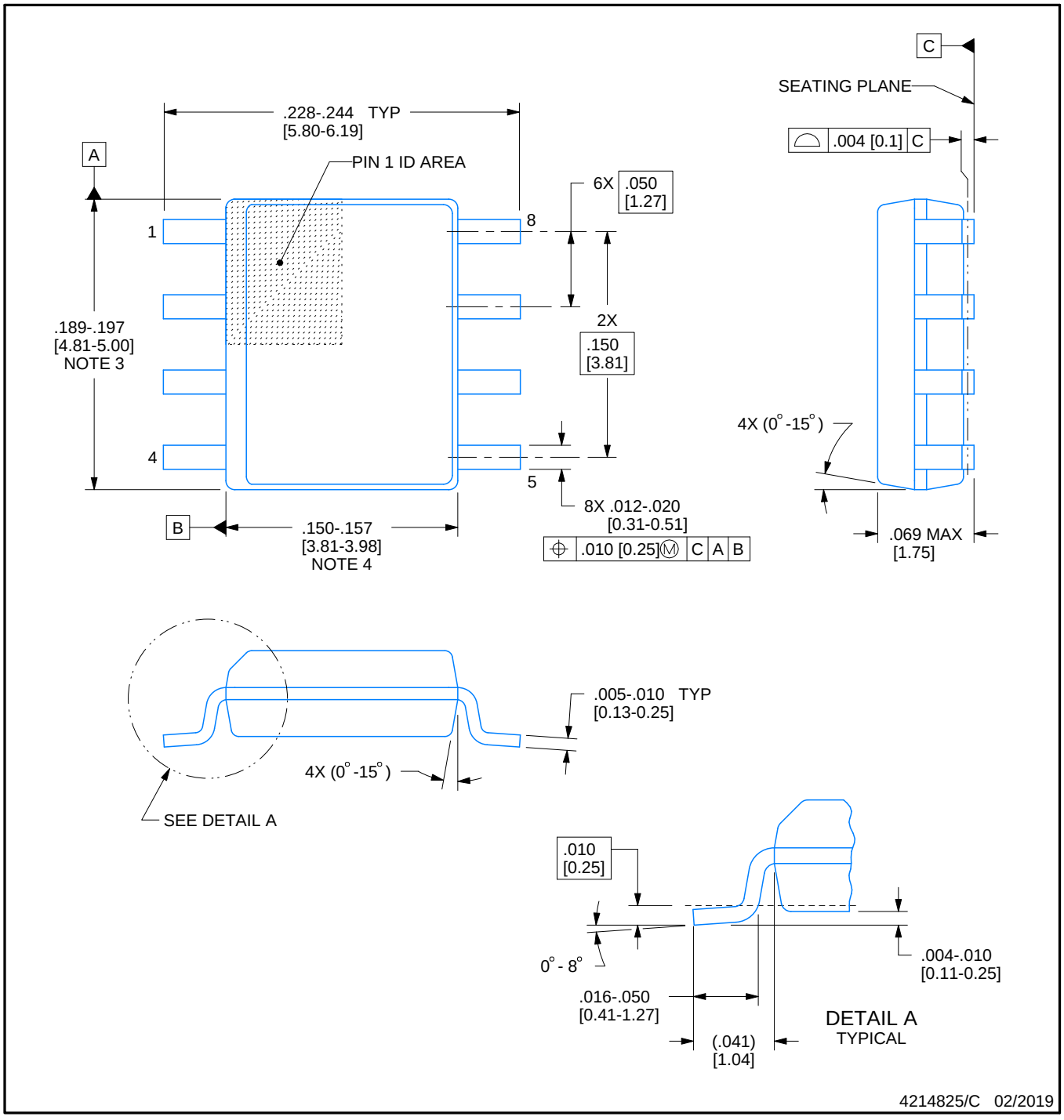


PACKAGE OUTLINE

D0008A

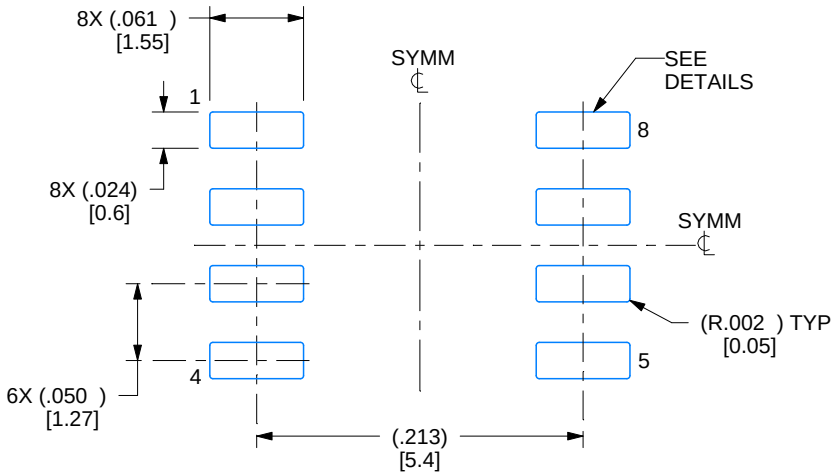
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

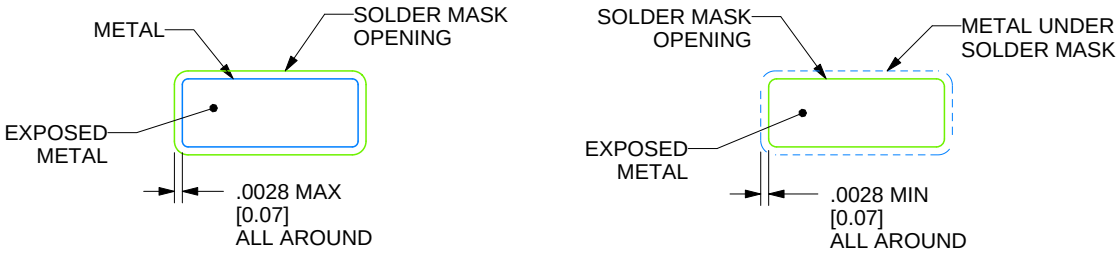


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

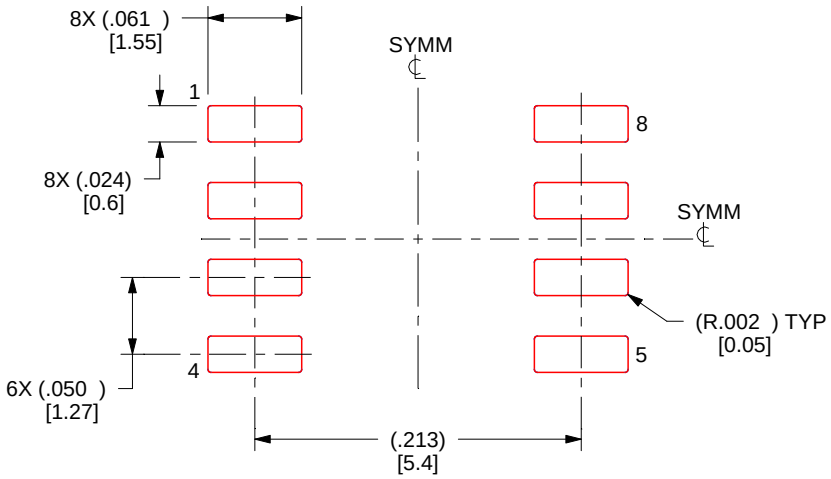
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



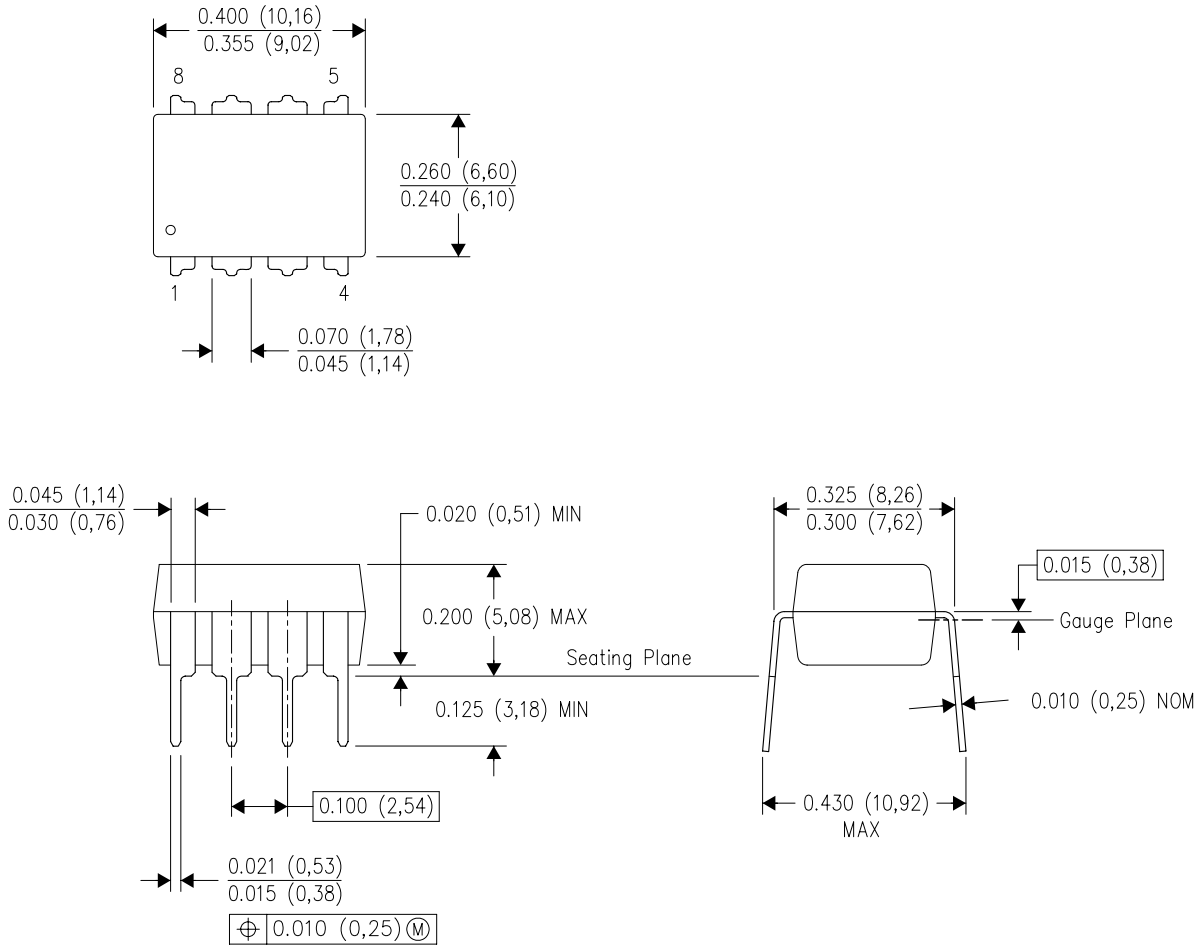
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

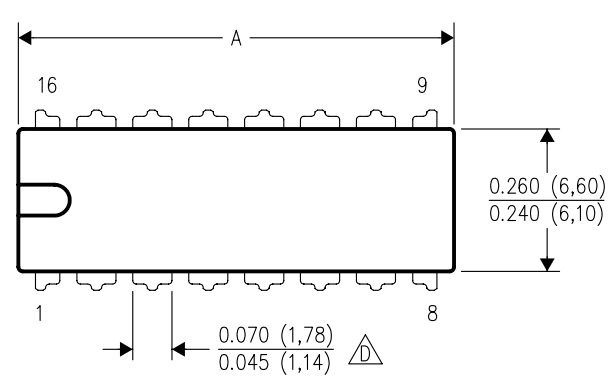


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

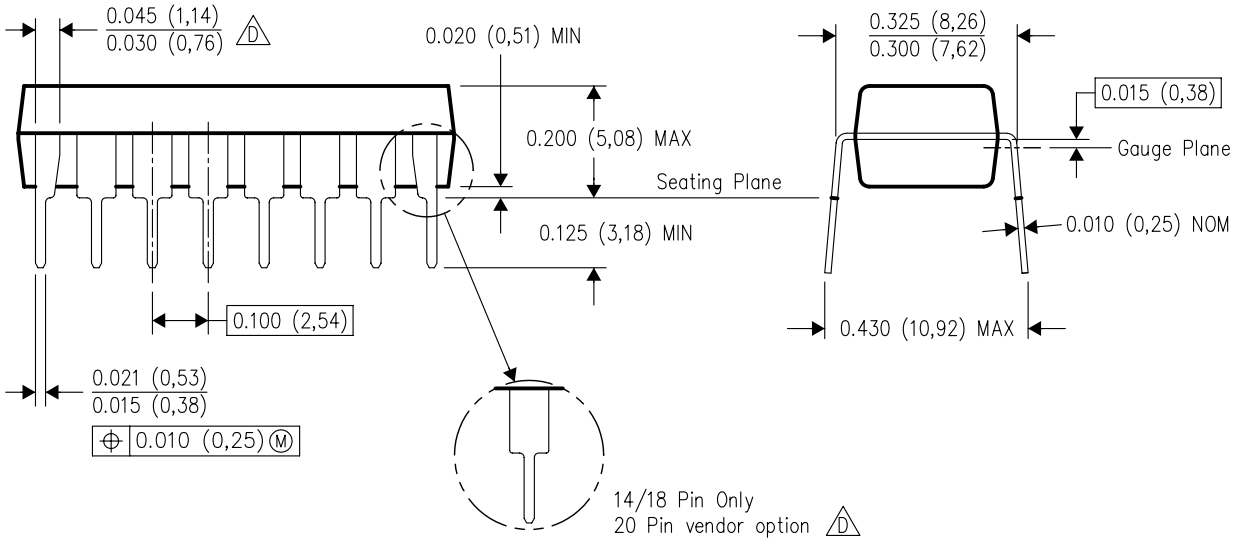
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

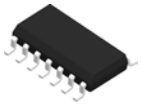


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

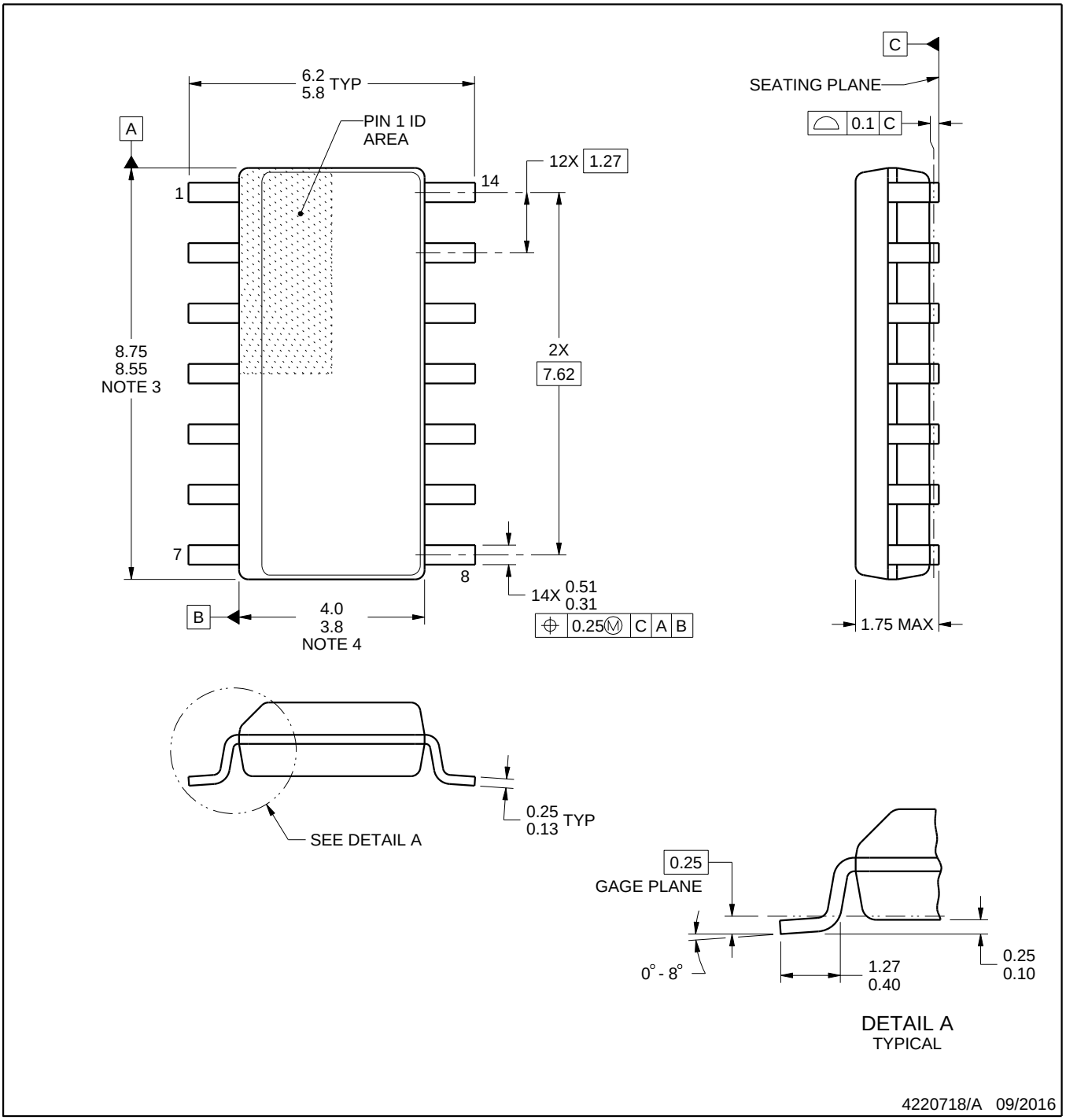


PACKAGE OUTLINE

D0014A

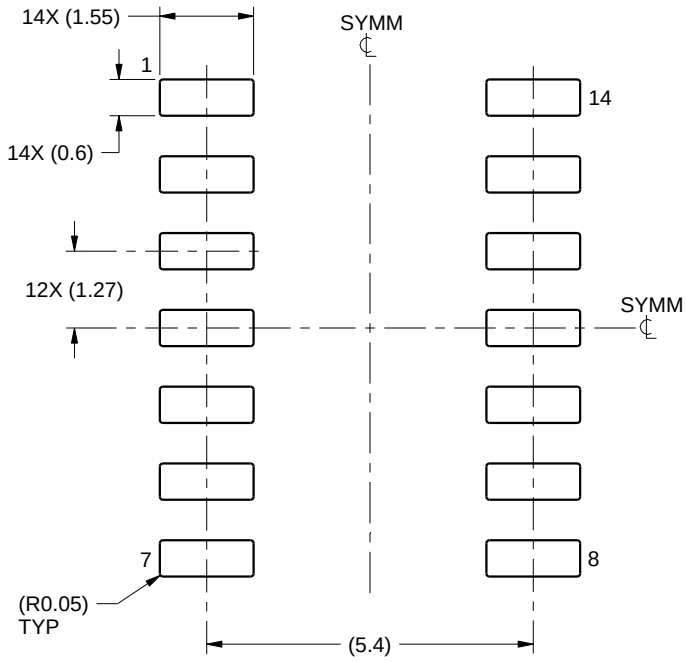
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

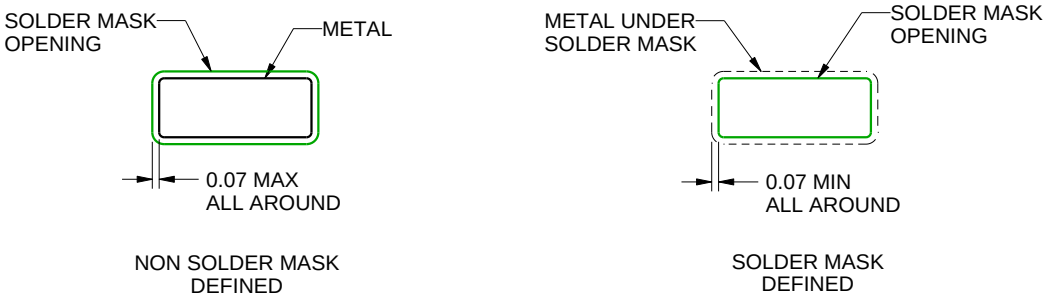


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

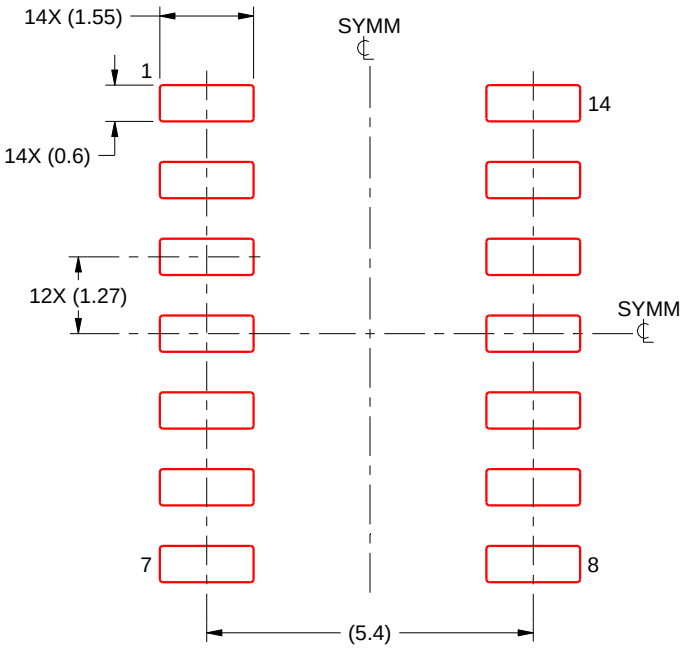
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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