OPAx985 48V, High Precision (1.2µV/°C), Low-Power (750µA), Low Noise (9nV/√Hz) CMOS Op Amps

1 Features

- Wide power-supply range:
  - 4.5V to 48V (±2.25V to ±24V)
- Low input offset voltage drift: 1.2µV/°C, max
- Low input offset voltage: 50µV, max
- Low input bias current: 10pA, max
- Low noise: 9nV/√Hz
- Low power consumption: 800µA, max
- Gain bandwidth: 5.6MHz
- High slew rate: 15V/µs
- Mux-Friendly inputs
- Rail-to-rail input and output
- Output current drive: +42/−50mA
- Wide temperature range: –40°C to +125°C

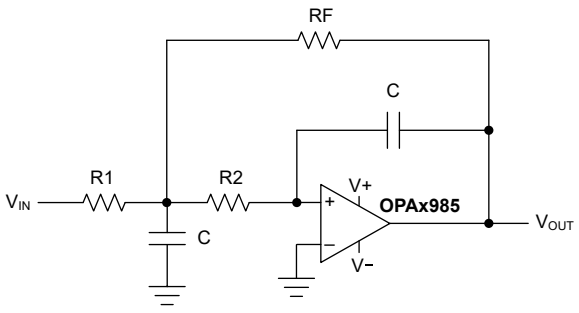
2 Applications

- AC/DC power supply unit (PSU) - 12V DC & 48V/54V DC output
- Battery backup unit (BBU)-12V DC/48V DC
- Battery cell formation & test equipment
- Analog input module
- Precision multifunction input & output DAQ

3 Description

The OPA985, OPA2985, and OPA4985 (OPAx985) are next generation operational amplifiers (op amps) that are 48V capable, and are equipped with dual temperature e-Trim™ to achieve very high precision. The OPAx985 are pin compatible replacement with many legacy amplifiers that can benefit from a higher operating voltage and improved performance.

The OPAx985 feature novel design techniques to achieve excellent ac and dc performance. These op amps offer very low offset (50µV, max) and offset drift (1.2µV/°C, max).



Sallen-Key Low-Pass Filter

The high common-mode rejection (CMRR) and power-supply rejection (PSRR) ratios help maintain precision across a variety of different operating conditions. With only 800µA (max) of supply current, the OPAx985 provides 9nV/√Hz of voltage noise and 5.6MHz of gain bandwidth.

The OPAx985 excel in a wide range of precision applications. The high input impedance, rail-to-rail input and output, mux-friendly input architecture, and wide operating voltage range makes these devices easy to design in. The combination of features make the OPAx985 an excellent choice for analog input module, common-redundant power supply (CRPS), and lab instrumentation applications. Low power consumption and industry-standard small packages allow the device to be used in high-density systems that are size constrained, while reducing the thermal management requirements for the system.

The OPAx985 are available in industry-standard packages and operate across the temperature range of –40°C to +125°C.

Device Information

PART NUMBER	CHANNELS	PACKAGE(1)
OPA985(2)	Single	DBV (SOT-23, 5)
		D (SOIC, 8)
OPA2985(2)	Dual	D (SOIC, 8)
		DGK (VSSOP, 8)
		DSG (WSON, 8)
OPA4985(2)	Quad	D (SOIC, 14)
		PW (TSSOP, 14)

(1) For more information, see Section 10.
(2) Preview information (not Production Data).

Related 48V Products

PART NUMBER	INPUT OFFSET DRIFT	BANDWIDTH	QUIESCENT CURRENT	INPUT BIAS
OPAx488	0.025µV/°C	14MHz	1.8mA	350pA
OPAx486	0.025µV/°C	5.6MHz	0.65mA	250pA
OPAx986	1.2µV/°C	14MHz	1.8mA	10pA

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4 Pin Configuration and Functions

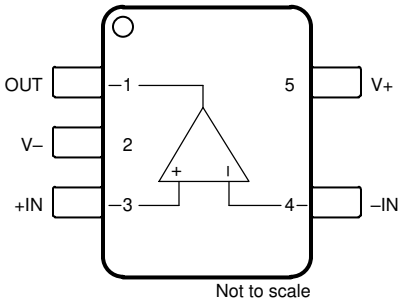


Figure 4-1. OPA985 DBV (Preview) Package, 5-Pin SOT-23 (Top View)

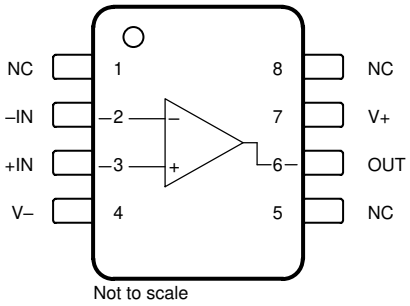


Figure 4-2. OPA985 D (Preview) Package, 8-Pin VSSOP (Top View)

Table 4-1. Pin Functions: OPA985

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN	3	Input	Noninverting input
–IN	4	Input	Inverting input
OUT	1	Output	Output
V+	5	Power	Positive (highest) power supply
V–	2	Power	Negative (lowest) power supply

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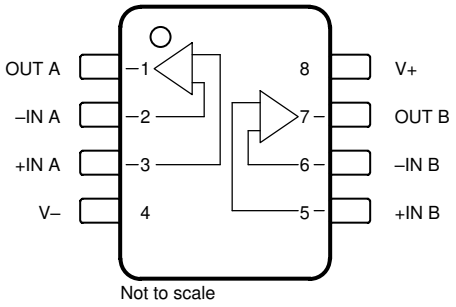


Figure 4-3. OPA2985 D (Preview) Package, 8-Pin SOIC and DGK (Preview) Package, 8-Pin VSSOP (Top View)

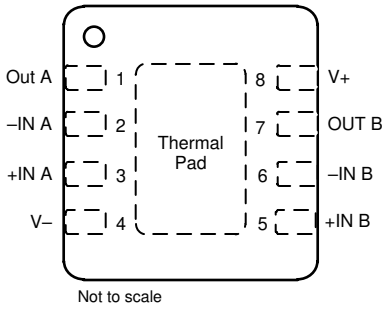


Figure 4-4. OPA2985 DSG (Preview) Package, 8-Pin WSON (Top View)

Table 4-2. Pin Functions: OPA2985

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V+	8	Power	Positive (highest) power supply
V–	4	Power	Negative (lowest) power supply
Thermal Pad	—	—	Exposed thermal die pad on underside; connect thermal die pad to V–. Soldering the thermal pad to the printed circuit board is required and improves heat dissipation and provides specified performance.

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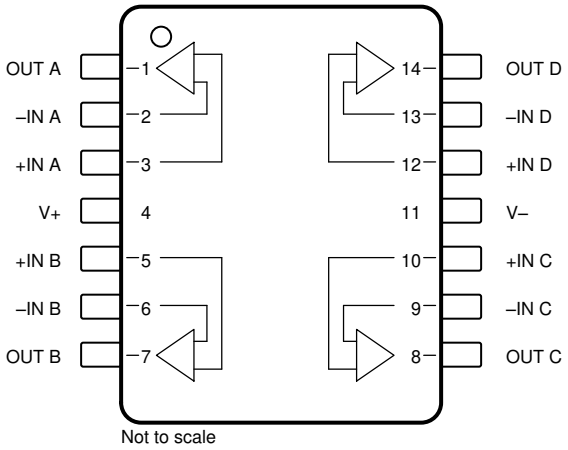


Figure 4-5. OPA4985 D (Preview) Package, 14-Pin SOIC and PW (Preview) Package, 14-Pin TSSOP (Top View)

Table 4-3. Pin Functions: OPA4985

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input channel A
–IN B	6	Input	Inverting input channel B
–IN C	9	Input	Inverting input channel C
–IN D	13	Input	Inverting input channel D
+IN A	3	Input	Noninverting input channel A
+IN B	5	Input	Noninverting input channel B
+IN C	10	Input	Noninverting input channel C
+IN D	12	Input	Noninverting input channel D
OUT A	1	Output	Output channel A
OUT B	7	Output	Output channel B
OUT C	8	Output	Output channel C
OUT D	14	Output	Output channel D
V–	11	Power	Negative supply
V+	4	Power	Positive supply

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)				60	V
Signal input pins	Voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Current			±10	mA
Output short circuit(2)			Continuous	Continuous	Continuous
Temperature	Operating		–40	150	°C
	Junction			150	
	Storage, T_{stg}		–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	4.5 (±2.25)		48 (±24)	V
Specified temperature	–40		125	°C

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5.4 Thermal Information for OPA985

THERMAL METRIC(1)		OPA985		UNIT
		D (SOIC)	DBV (SOT)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.8	158.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	60.1	60.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.4	44.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.8	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.9	4.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information for OPA2985

THERMAL METRIC(1)		OPA2985			UNIT
		D (SOIC)	DGK (VSSOP)	DSG (SON)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.9	107.9	158	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	53.9	53.9	48.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.9	48.9	78.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.6	6.6	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.3	48.3	77.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Thermal Information for OPA4985

THERMAL METRIC(1)		OPA4985		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.4	33.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	46.3	25.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.0	11.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.3	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.7	11.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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5.7 Electrical Characteristics for V_S = 8V to 48V

at T_A = +25°C, V_S = 8V to 48V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±10	±50	µV
		T_A = –40°C to +125°C				±170	
		V_{CM} = (V+) – 1V			±20	±100	
			T_A = –40°C to +125°C			±1000	
		(V+) – 3.0V < V_{CM} < (V+) – 1V			See Typical Characteristics		
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			±0.2	±1.2	µV/°C
			V_{CM} = (V+) – 1V			±9	
PSRR	Power-supply rejection ratio				±0.3	±1.0	µV/V
		T_A = –40°C to +125°C				±1.0	
INPUT BIAS CURRENT							
I_B	Input bias current				±5	±10	pA
		T_A = –40°C to +125°C				±5	nA
I_{OS}	Input offset current				±0.2	±10	pA
		T_A = –40°C to +125°C				±5	nA
NOISE							
E_n	Input voltage noise	f = 0.1Hz to 10Hz	(V–) < V_{CM} < (V+) – 3V		2		μV_{PP}
			(V+) – 1V < V_{CM} < (V+)		6.2		
e_n	Input voltage noise density	(V–) < V_{CM} < (V+) – 3V	f = 1kHz		14		nV/√Hz
			f = 10kHz		9		
		(V+) – 1V < V_{CM} < (V+)	f = 1kHz		30		
			f = 10kHz		15		
i_n	Input current noise density	f = 1kHz			4		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			V–		V+	V
CMRR	Common-mode rejection ratio	V_S = 48V, (V–) + 1V < V_{CM} < (V+) – 3V		116	140		dB
		V_S = 48V, (V–) < V_{CM} < (V+) – 3V		100	120		
		V_S = 48V, (V+) – 1V < V_{CM} < (V+)		100	120		
		(V+) – 3V < V_{CM} < (V+) – 1V			See Typical Characteristics		
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || TBD		MΩ || pF
Z_{IC}	Common-mode				10 || TBD		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 48V, (V–) + 0.3V < V_O < (V+) – 0.3V, R_L = 10kΩ		130	140		dB
		V_S = 48V, (V–) + 1V < V_O < (V+) – 1V, R_L = 2kΩ		130	140		

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5.7 Electrical Characteristics for V_S = 8V to 48V (continued)

at T_A = +25°C, V_S = 8V to 48V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain bandwidth	G = 1V/V			5		MHz
		G = 100V/V			5.6		
SR	Slew rate	V_S = 36V, G = 1, 10V step			15		V/µs
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load			25	mV
			R_L = 10kΩ			150	
			R_L = 2kΩ			800	
		Negative rail	No load			25	
			R_L = 10kΩ			150	
			R_L = 2kΩ			800	
I_{SC}	Short-circuit current	Sink			50		mA
		Source			42		
C_L	Capacitive load drive				See Typical Characteristics		
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0A OPA985			0.8	0.85	mA
		I_O = 0A OPA2985, OPA4985			0.75	0.80	
TEMPERATURE							
	Thermal protection				175		°C
	Thermal hysteresis				20		°C

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5.8 Electrical Characteristics for V_S = 4.5V to 8V

at T_A = +25°C, V_S = 4.5V to 8V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = (V+) – 3V			±10	±50	µV
			T_A = –40°C to +125°C			±130	
		V_{CM} = (V+) – 1V			±20	±100	
			T_A = –40°C to +125°C			±1000	
		(V+) – 3.0V < V_{CM} < (V+) – 1V			See Typical Characteristics		
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C	V_{CM} = (V+) – 3V		±0.2	±1.2	µV/°C
			V_{CM} = (V+) – 1.5V			±9	
PSRR	Power-supply rejection ratio	V_{CM} = (V+) – 3V			±0.3	±1.0	µV/V
		T_A = –40°C to +125°C				±1.5	
INPUT BIAS CURRENT							
I_B	Input bias current				±5	±10	pA
		T_A = –40°C to +125°C				±1	nA
I_{OS}	Input offset current				±0.2	±10	pA
		T_A = –40°C to +125°C				±1	nA
NOISE							
E_n	Input voltage noise	f = 0.1Hz to 10Hz	(V–) < V_{CM} < (V+) – 3V		2		$µV_{PP}$
			(V+) – 1V < V_{CM} < (V+) + 0.1V		6		
e_n	Input voltage noise density	(V–) – 0.1V < V_{CM} < (V+) – 3V	f = 1kHz		14		$nV/\sqrt{Hz}$
			f = 10kHz		9		
		(V+) – 1V < V_{CM} < (V+) + 0.1V	f = 1kHz		30		
			f = 10kHz		15		
i_n	Input current noise density	f = 1kHz			4		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			V–		V+	V
CMRR	Common-mode rejection ratio	(V–) + 1V < V_{CM} < (V+) – 3V		116	136		dB
		(V+) – 1V < V_{CM} < (V+)		100	120		
		(V+) – 3V < V_{CM} < (V+) – 1V		See Typical Characteristics			
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || TBD		MΩ || pF
Z_{IC}	Common-mode				10 || TBD		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 5V, (V–) + 0.3V < V_O < (V+) – 0.3V, R_L = 10kΩ		124	134		dB
		V_S = 5V, (V–) + 0.6V < V_O < (V+) – 0.6V, R_L = 2kΩ		126	140		

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5.8 Electrical Characteristics for V_S = 4.5V to 8V (continued)

at T_A = +25°C, V_S = 4.5V to 8V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain bandwidth	G = 1V/V			5		MHz
		G = 100V/V			5.4		
SR	Slew rate	V_S = 5V, G = 1, 1V step			14		V/µs
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load			25	mV
			R_L = 10kΩ			150	
			R_L = 2kΩ			800	
		Negative rail	No load			25	
			R_L = 10kΩ			150	
			R_L = 2kΩ			800	
I_{SC}	Short-circuit current	Sink			50		mA
		Source			42		
C_L	Capacitive load drive				See Typical Characteristics		
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0A OPA985			0.800	0.850	mA
		I_O = 0A OPA2985, OPA4985			0.750	0.800	
TEMPERATURE							
	Thermal protection				180		°C
	Thermal hysteresis				20		°C

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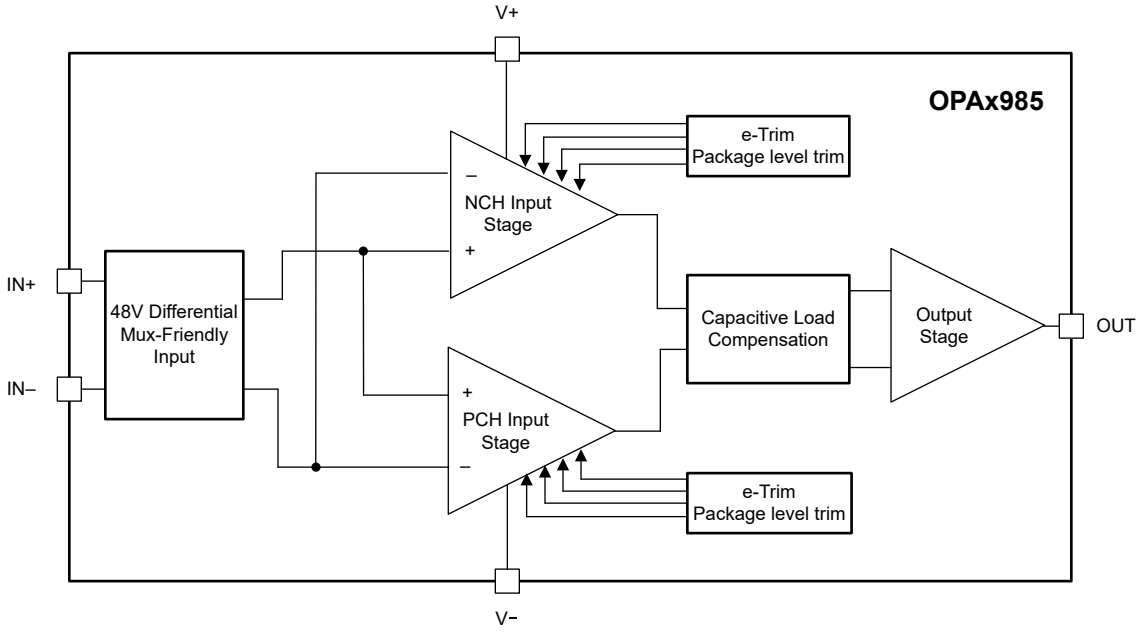
6 Detailed Description

6.1 Overview

The OPAx985 are 48V high precision, rail-to-rail amplifiers with e-Trim to achieve high precision. These amplifiers are have a mere 50µV of offset at room temperature and drift only 1.2µV/°C over temperature. The high common-mode rejection and power-supply rejection of these amplifiers help preserve precision across a variety of operating conditions.

In addition to stellar dc performance, the OPAx985 achieve outstanding ac performance. The OPAx985 offers ample speed for a variety of different applications with 5.6MHz of bandwidth and 15V/µs slew rate. The low 9nV/√Hz broadband voltage noise, and 4fA/√Hz current noise make these amplifiers easy to design with. The speed and noise performance is achieved with very little quiescent current, 750µA. The OPAx985 are an excellent choice for designing a high performance active filter, a transimpedance amplifier (TIA), a high accuracy current monitor, or a high impedance sensor interface amplifier.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 e-Trim™

The OPAx985 of operational amplifiers is manufactured using the Texas Instruments (TI) e-trim™ technology. Each amplifier input offset voltage and input offset voltage drift is trimmed in production, thereby minimizing errors associated with input offset voltage and input offset voltage drift. The e-trim technology is a TI proprietary method of trimming internal device parameters during final testing. This trimming method avoids the package stress related offset voltage effects experienced by other trimmed op amps. When trimming input offset voltage drift, the systematic or linear drift error on each device is trimmed to zero. The remaining errors associated with input offset drift are minimal and are the result from only nonlinear error sources. For more information on the e-Trim™ technology, please see the Offset Correction Methods: Laser Trim, e-Trim™, and Chopper application brief.

6.3.2 Mux-Friendly Inputs

The OPAx985 use a unique input architecture to eliminate the need for input protection diodes but still provide robust input protection under transient conditions. Conventional input diode protection schemes shown in Figure 6-1 can be activated by fast transient step responses and can introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 6-2. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes that cause an increase in input current and result in extended settling time.

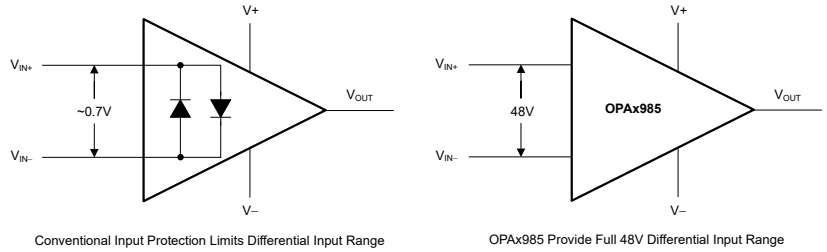


Figure 6-1. OPAx985 Input Protection Does Not Limit Differential Input Capability

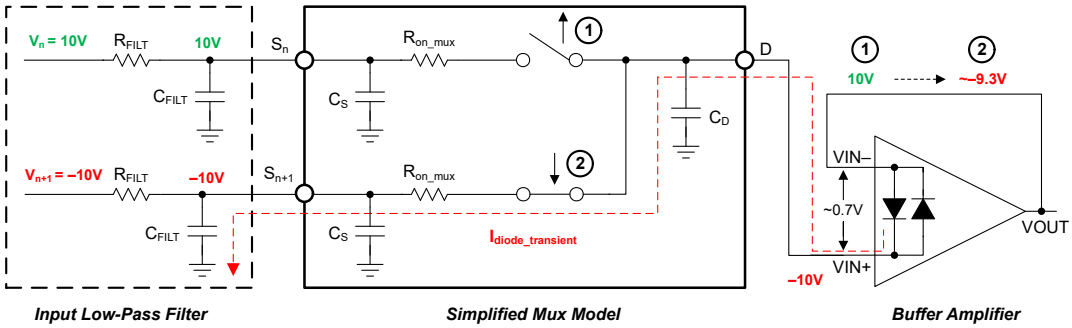


Figure 6-2. Back-to-Back Diodes Create Settling Issues

The OPAx985 feature a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making these devices an excellent choice for multichannel, high-switched, input applications. The OPAx985 tolerate a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 48V, making these devices a great choice for use as a comparator or in applications with fast-ramping or switched input signals.

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6.3.3 Thermal Protection

The OPAx985 has a thermal protection feature that prevents damage from self heating. When the junction temperature (T_J) reaches approximately 175ºC, the op amp output stage disables. This thermal protection works by monitoring the temperature of the output stage and turning off the op amp output drive. Thermal protection forces the output to a high-impedance state. The OPAx985 is designed with approximately 20°C of thermal hysteresis and returns to normal operation when the output stage temperature becomes less than approximately 155°C.

This thermal protection is not designed to prevent this device from exceeding absolute maximum ratings, but rather from excessive thermal overload.

6.3.4 Slew Rate

Slew rate is the maximum rate of change of output voltage change with respect to time and is typically specified in units of volts per microsecond, V/µs. Op amps can enter a slew condition when a large, rapid moving signal is applied at the input. While slewing, the op amp enters an open loop condition and significant slew induced distortion can be seen on the output signal.

Equation 1 shows that the slew rate, SR, of an op amp is typically determined by the saturation current of the input stage, I_{TAIL}, and the compensation capacitor, C_C.

$$SR = \frac{I_{TAIL}}{C_C} \tag{1}$$

Modern op amps are equipped with slew boost technology that increases I_{SAT} to improve slew rate. Slew boost circuits can vary in implementation, but designers must take into account the increase in supply current during slew events. In some cases, the op amp can exhibit distortion from slew boost as the circuit is turned on and off. For more information on this topic, see the Full Power Bandwidth and Op Amp Distortion application report.

The OPAx985 uses a proprietary design to achieve very high slew rate without the use of any slew boost circuitry. Thie op amps consumes no additional power during slew events.

Table 6-1 shows a comparison of slew rates and quiescent currents of different op amps.

Table 6-1. Op Amp Slew Rates and Quiescent Current

PART NUMBER	SLEW RATE	QUIESCENT CURRENT	SLEW BOOST
OPAx985	15V/µs	750µA	No
OPAx991	21V/µs	560µA	Yes
OPAx202	0.35V/µs	580µA	No
OPAx192	20V/µs	1mA	Yes
OPAx986	40V/µs	1.6mA	No

6.3.5 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time.

6.4 Device Functional Modes

The OPAx985 has a single functional mode and is operational when the power-supply voltage is between 4.5V (±2.25V) and 48V (±24V).

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPAx985 are high voltage, high precision, e-Trim™ op amps. The OPAx985 represent the ultimate toolbox amplifiers. These amplifiers offer low input bias current (±10pA, max) to interface with high source impedances, rail-to-rail input and output, wide operating voltage range extending from 4.5V to 48V, low broadband noise (9nV/√Hz), wide bandwidth (5.6MHz), low quiescent current (750µA). The combination of specifications and features like Mux-Friendly make the OPAx985 an excellent choice for both general purpose and precision applications.

7.2 Typical Applications

7.2.1 Piezoelectric Force Sensor

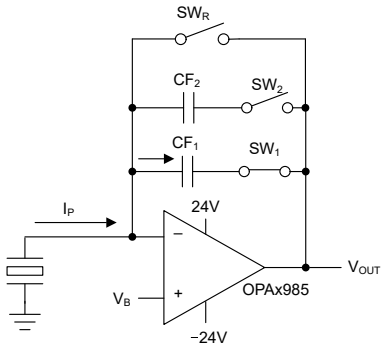


Figure 7-1. Piezoelectric Force Sensor

7.2.1.1 Design Requirements

The OPAx985 is used as the signal conditioning amplifier for a piezoelectric force sensor. Force sensors are critical in industries like robotics and industrial automation. The sensors can be used, for example, to monitor and record data on vibrations on a motor. This data is critical for the longevity and reliability of heavy machinery.

Force sensors made with piezoelectric material are common because the piezoelectric properties provide extremely high sensitivity and wide dynamic range. Piezoelectric sensors output a charge that is proportional to the force applied. Depending on the force applied, the charge output can be very small, typically in the pC/N and nC/N range. An amplifier with high precision, low input bias current, and wide dynamic range is required to achieve high accuracy measurements.

Table 7-1. Design Parameters

PARAMETER	VALUE
Power supply voltage	±24V
Piezoelectric sensitivity	5pC/N
Force range	1N to 1,000N
Operating frequency	120Hz
Output voltage	$23V_{PP}$

7.2.1.2 Detailed Design Procedure

The charge produced by a force sensor can be tiny and can make the analog signal chain design challenging. To measure the tiny signal from the sensor, a charge amplifier like that in Figure 7-1 is used. The OPAx985 is an

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excellent choice because the amplifiers provide very low input bias current, high precision, and wide operating supply voltage.

Low input bias current is critical in this application, as the input bias current directly adds to the output of the force sensor. If the input bias current is too large, then the sensor signal is drowned out and the capacitor is driven to the rail very quickly. OPAx985 feature ±10pA of bias current. The charge output is given by Equation 2.

$$Q = F_N \times \left(5.3\frac{pC}{N}\right)\sin(2\pi ft)\delta t \quad (2)$$

The charge can be converted to a current using Equation 3. The given a frequency of 120Hz, the current can be calculated to be approximately 4nA.

$$I_{charge} = \frac{\delta Q}{\delta t} = \pm\left[F \times 5.3\frac{pC}{N} \times 2\pi\left(120Hz\right)\right] \quad (3)$$

High precision is also necessary for this application. While the output is generated directly from the charging the capacitor of the charge amplifier, the offset voltage appears across the sensor. If the offset voltage is 5mV, for example, even a 500MΩ resistance at the source or across the input pins can degrade the input bias performance of the amplifier. The OPAx985 features 50µV of offset and 1.2µV/°C of offset drift, essentially eliminating any potential offset voltage related current errors.

Equally important for this application is the capability of the signal conditioning circuit to span a wide range of force values on the sensor. A span of 1N to 1,000N means the charge amplifier must support an input voltage range from 40nA to 4µA. To support this wide input range with a single integrating capacitor, the amplifier must be able have a wide linear output voltage swing. Using ±24V power supplies, the OPAx985 can swing to ±23.4V even under a heavy 2kΩ load.

7.2.1.3 Application Curves

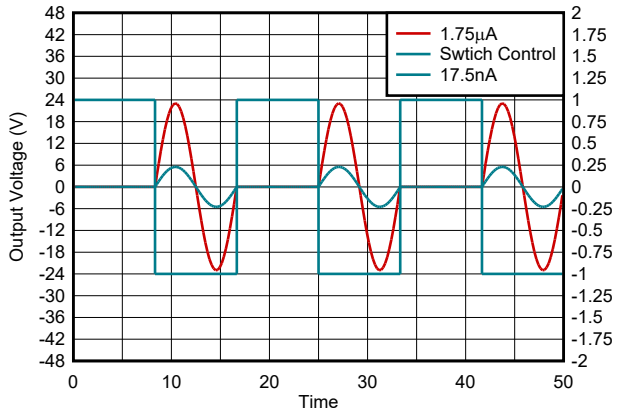


Figure 7-2. Charge Amplifier Output Voltage

7.2.2 High-Side Current Sense

The OPAx985 enables high voltage current sense measurements. High-side voltage measurements of 36V batteries can be elegantly implemented using the OPAx985. The voltage capability is proportional to the gain of the sense circuit and the input common-mode range of the amplifier. Figure 7-3 shows the OPA985 configured for to monitor a 36V battery common in many electric scooters, e-bikes, and heavy duty power tools. The circuit shown here provides a differential voltage gain of 4V/V. Use high precision, matched resistors like the RES11A series to achieve high precision.

Make the input resistors large enough to avoid any loading related errors. The low input bias current of the OPAx985 allows for the use of larger resistors when compared to other amplifiers and is not a major contribution to the total error in this application. Special consideration of input bias current, thermal noise, and input common-mode range is warranted when choosing resistors for this design.

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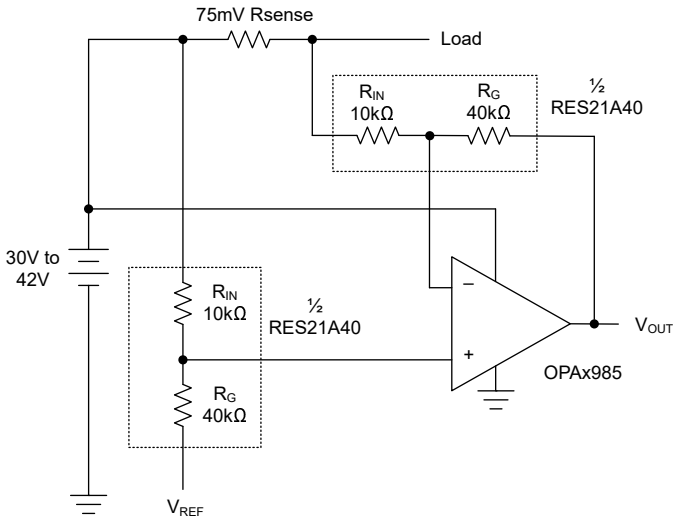


Figure 7-3. High-Side Current Sense for 36V Batteries

7.2.3 Wide Compliance Current Source

As sensor precision sensor demand increases, so does the need for precision current sources. Figure 7-4 shows a high precision current source. The circuit is a Howland Current Pump and requires 5 precision resistors. The current is set by Equation 4.

$$I_L = \frac{V_{IN}}{R_{SET}} \tag{4}$$

The compliance voltage is limited by the output capability of the amplifier. The amplifier is required to support the maximum output voltage for a given R_{SET} as given by Equation 5. High compliance current sources can be designed using the OPAx985 due to the high operating voltage of 48V. The circuit provides a very precise current source and sink, but is limited by the current drive of the amplifier. The OPAx985 can source and sink about 40mA.

$$V_{OUT_{max}} = \left(I_{L_{max}} \times R_{SET}\right) + V_{L_{max}} \tag{5}$$

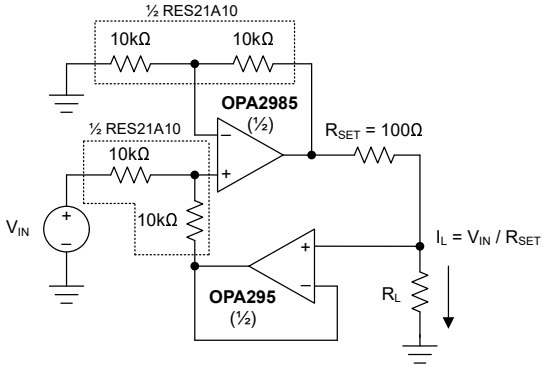


Figure 7-4. High Compliance Howland Current Pump

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7.3 Power Supply Recommendations

The OPAx985 operates from power supplies up to ±24V (48V), and as little as ±2.25V (4.5V) with excellent performance. Most behavior remains unchanged throughout the full operating voltage range, but the Typical Charachteristics show parameters that vary with operating voltage. A power-supply bypass capacitor of at least 0.1µF is recommended. Make sure that the capacitor voltage is rated for high voltage across the full operating temperature range. The OPAx985 can be powered with asymmetrical supplies to optimize power dissipation in applications that do not require an equal positive and negative output voltage swing.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including the following guidelines:

- Noise can propagate into analog circuitry through the power pins of the op amp and the circuit as a whole. Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground. Place the capacitors as close to the device as possible. A single bypass capacitor from V+ to ground is sufficient for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

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7.4.2 Layout Example

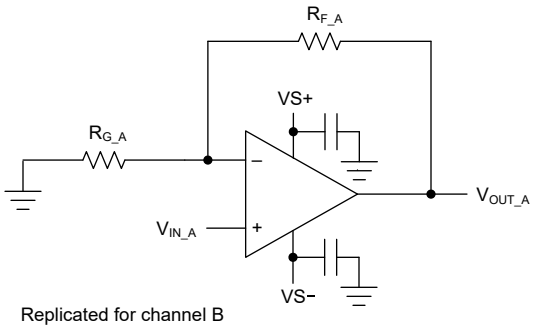


Figure 7-5. Schematic Representation of Noninverting Configuration

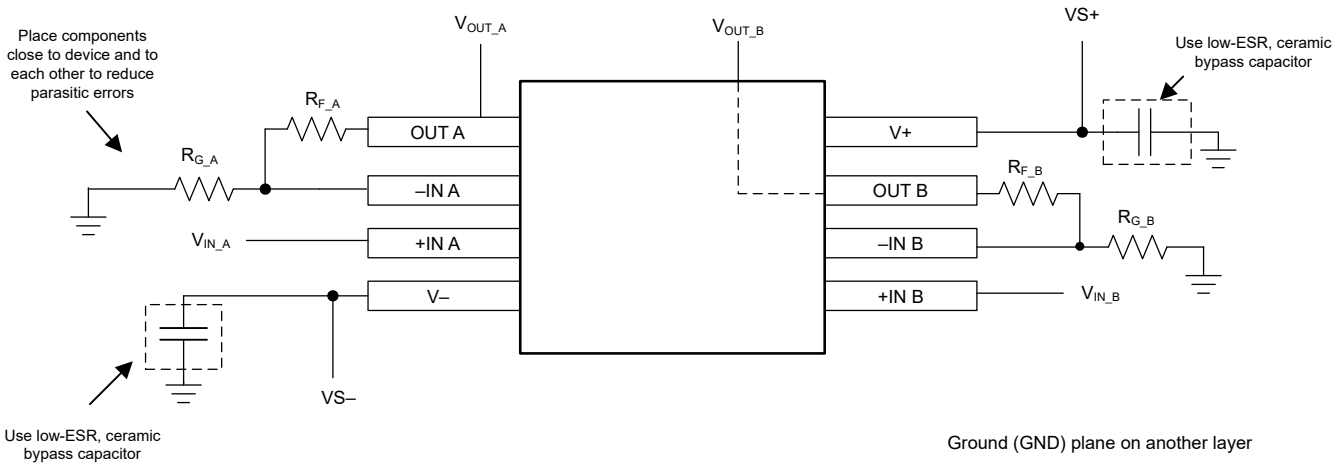


Figure 7-6. Board Layout for Noninverting Configuration of the VSSOP-8 Package

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8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2026	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
POPA2985DGKR	Active	Preproduction	VSSOP (DGK) | 8	3500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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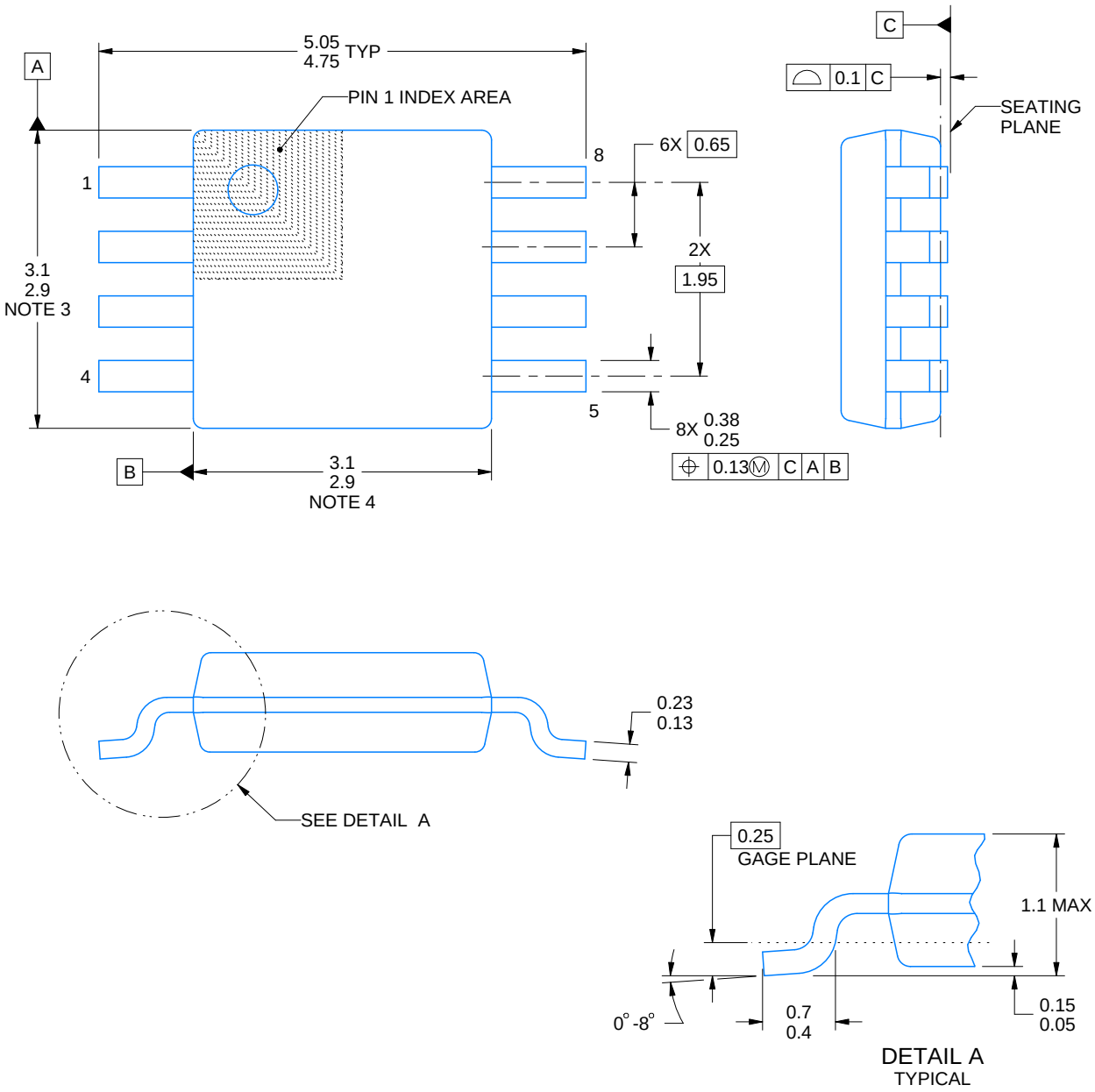
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

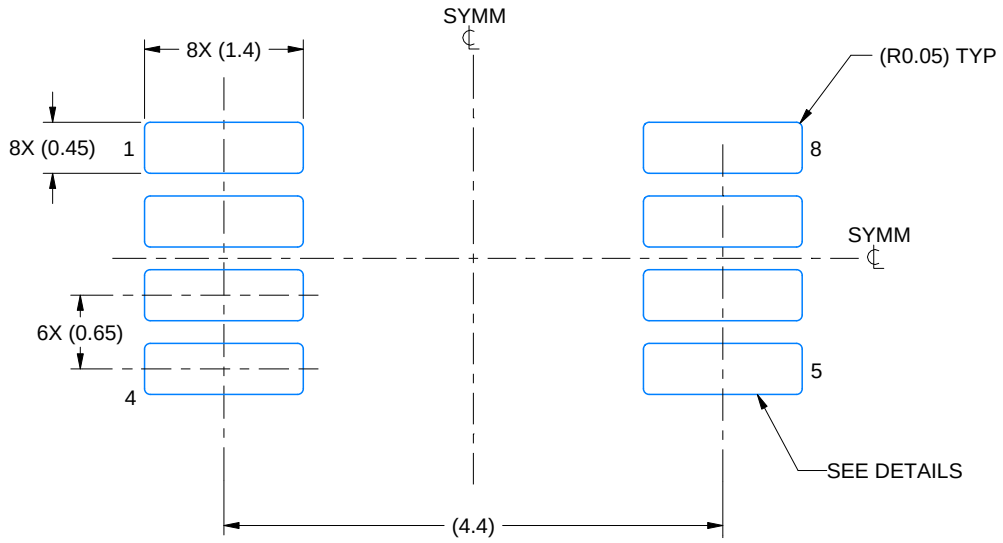
SMALL OUTLINE PACKAGE



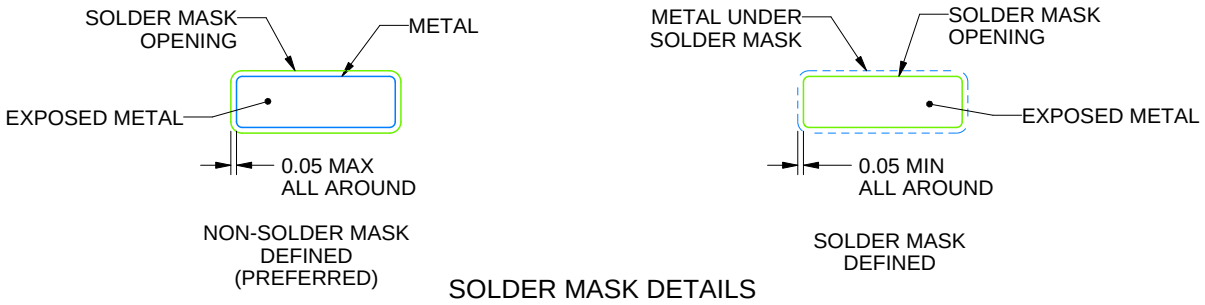
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

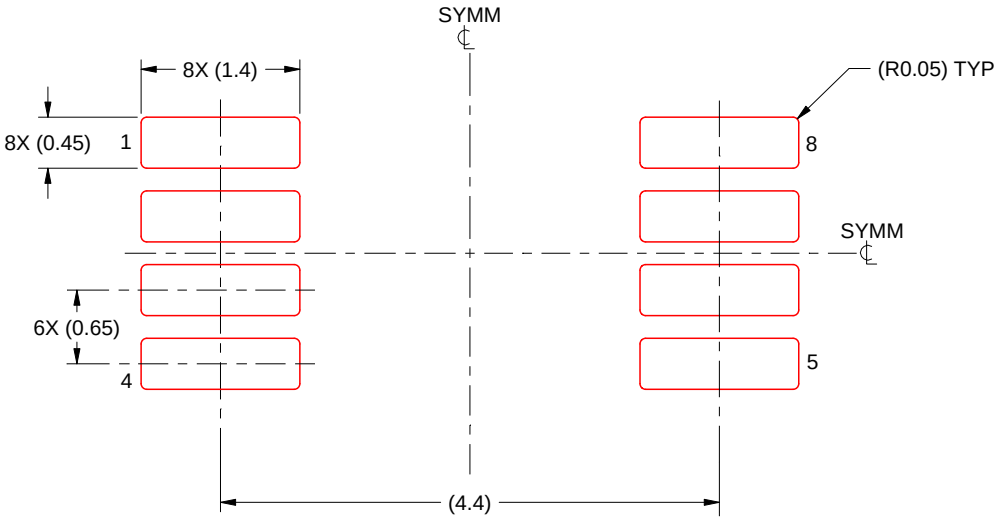


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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