

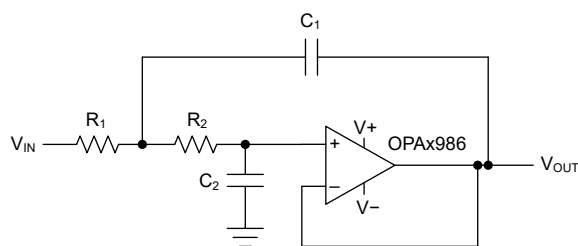
OPAx986 High-Voltage (48V), Wide-Bandwidth (14MHz), High Precision (1.2μV/°C), CMOS Op Amp

1 Features

- Wide power supply operation:
 - 4.5V to 48V ($\pm 2.25\text{V}$ to $\pm 24\text{V}$)
- Rail-to-rail input and output
- High accuracy and precision:
 - Input offset voltage: $\pm 50\mu\text{V}$, max
 - Input offset voltage drift: $\pm 1.2\mu\text{V}/^\circ\text{C}$, max
 - Common-mode rejection ratio: 120dB, min
- Very low noise:
 - Input voltage noise density: $7.5\text{nV}/\sqrt{\text{Hz}}$ at 10kHz
 - Input current noise density: $4\text{fA}/\sqrt{\text{Hz}}$ at 1kHz
- High gain bandwidth: 14MHz at $G = 100\text{V/V}$
- Unity gain bandwidth: 12MHz
- High slew rate: $40\text{V}/\mu\text{s}$
- Low power consumption: 1.6mA
- Mux-friendly inputs
- Low input bias current: $\pm 10\text{pA}$, max
- Specified across a wide temperature range:
 - -40°C to $+125^\circ\text{C}$

2 Applications

- Programmable DC power supply
- AC/DC power supply unit (PSU) - 12V DC and 48V/54V DC output
- Analog input module
- Optical module
- Multiple parameter patient monitor



Sallen-Key Low-Pass Filter

3 Description

The OPA986 and OPA2986 (OPAx986) are 48V capable, low noise, high precision, rail-to-rail, CMOS operational amplifiers on Texas Instruments latest process technology.

The OPAx986 enables next generation platforms supporting a wider input and output dynamic range. These systems can benefit from improved signal integrity and accuracy. The combination of high input impedance, rail-to-rail inputs, low noise, and wide bandwidth make these devices an excellent choice for data acquisition systems that interface with a wide range of sensors. The Mux-Friendly technology of these op amps provide a robust input stage that can improve settling behavior in multiplexed applications.

The OPAx986 are available in industry standard packages and can provide a drop-in upgrade to existing legacy sockets. These op amps are also available in industry leading, tiny packages to fit a variety of space constrained applications.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
OPA986	D (SOIC, 8) ⁽³⁾	4.90mm × 6.00mm
	DBV (SOT-23, 5) ⁽³⁾	2.90mm × 2.80mm
	DRL (SOT-23, 5) ⁽³⁾	1.60mm × 1.60mm
OPA2986	D (SOIC-8) ⁽³⁾	4.90mm × 6.00mm
	DGK (VSSOP-8) ⁽³⁾⁽⁴⁾	3.00mm × 4.90mm
	DSG (WSON) ⁽³⁾	2.00mm × 2.00mm
OPA4986	D (SOIC-14) ⁽³⁾	8.65mm × 6.00mm
	PW (TSSOP-14) ⁽³⁾	5.00mm × 6.40mm

- (1) For more information, see [Section 10](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) Preview information (not Production Data).
- (4) Samples available.



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4 Pin Configuration and Functions

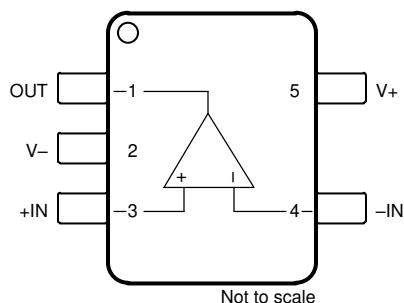


Figure 4-1. OPA986 DBV Package, 5-Pin SOT-23 (Top View)

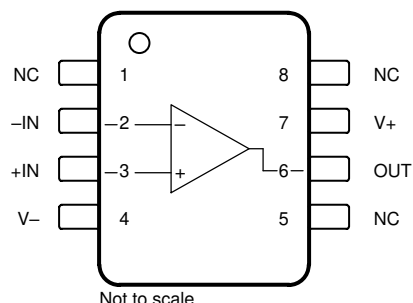


Figure 4-2. OPA986 D Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions: OPA986

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN	3	Input	Noninverting input
–IN	4	Input	Inverting input
OUT	1	Output	Output
V+	5	Power	Positive (highest) power supply
V–	2	Power	Negative (lowest) power supply

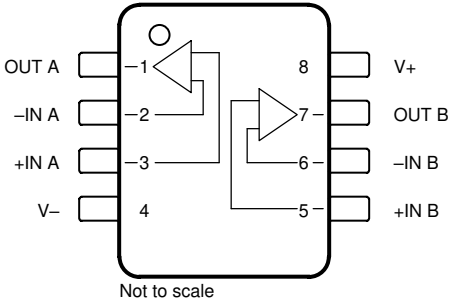


Figure 4-3. OPA2986 D (Preview) Package, 8-Pin SOIC and DGK (Preview) Package, 8-Pin VSSOP (Top View)

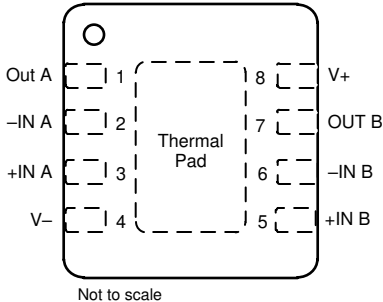


Figure 4-4. OPA2596 DSG (Preview) Package, 8-Pin WSON (Top View)

Table 4-2. Pin Functions: OPA2986

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
-IN A	2	Input	Inverting input, channel A
-IN B	6	Input	Inverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V+	8	Power	Positive (highest) power supply
V-	4	Power	Negative (lowest) power supply
Thermal Pad	-	-	Connect thermal pad to the negative supply (V-). See also Packages with an Exposed Thermal Pad for more information

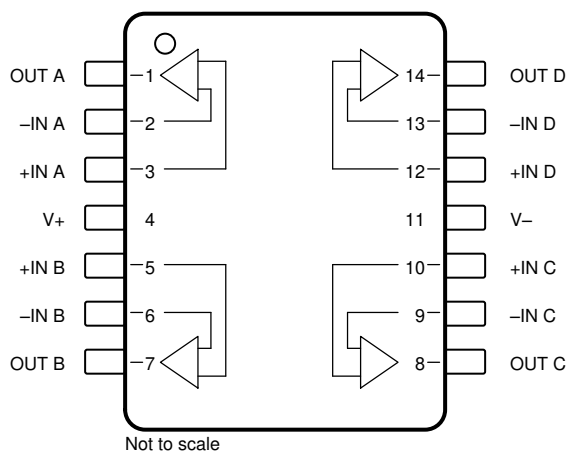


Figure 4-5. OPA4986: D Package, 14-Pin SOIC and PW Package, 14-Pin TSSOP (Top View)

Table 4-3. Pin Functions: OPA4986

PIN		TYPE	DESCRIPTION
NAME	NO.		
-IN A	2	Input	Inverting input channel A
-IN B	6	Input	Inverting input channel B
-IN C	9	Input	Inverting input channel C
-IN D	13	Input	Inverting input channel D
+IN A	3	Input	Noninverting input channel A
+IN B	5	Input	Noninverting input channel B
+IN C	10	Input	Noninverting input channel C
+IN D	12	Input	Noninverting input channel D
OUT A	1	Output	Output channel A
OUT B	7	Output	Output channel B
OUT C	8	Output	Output channel C
OUT D	14	Output	Output channel D
V-	11	Power	Negative supply
V+	4	Power	Positive supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$				60	V
Signal input pins	Voltage	Common-mode	$(V-) - 0.5$	$(V+) + 0.5$	V
		Differential	$(V+) - (V-) + 0.2$		
	Current		± 10		mA
Output short circuit ⁽²⁾			Continuous	Continuous	Continuous
Temperature	Operating		-40	150	°C
	Junction			150	
	Storage, T_{stg}		-65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	± 250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$	4.5 (± 2.25)		48 (± 24)	V
Specified temperature	-40		125	°C

5.4 Thermal Information for OPA986

THERMAL METRIC ⁽¹⁾		OPA986		UNIT
		D (SOIC)	DBV (SOT)	
		8 PINS	5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	115.8	158.8	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	60.1	60.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	56.4	44.8	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	12.8	1.6	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	55.9	4.2	°C/W
R _{θJC(bot)}	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Thermal Information for OPA2986

THERMAL METRIC ⁽¹⁾		OPA2986			UNIT
		D (SOIC)	DGK (VSSOP)	DSG (SON)	
		8 PINS	8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	107.9	107.9	158	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	53.9	53.9	48.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	48.9	48.9	78.7	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	6.6	6.6	3.9	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	48.3	48.3	77.3	°C/W
R _{θJC(bot)}	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.6 Thermal Information for OPA4986

THERMAL METRIC ⁽¹⁾		OPA4986		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	86.4	33.0	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	46.3	25.1	°C/W
R _{θJB}	Junction-to-board thermal resistance	41.0	11.6	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	11.3	0.2	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	40.7	11.5	°C/W
R _{θJC(bot)}	Junction-to-case(bottom) thermal resistance	N/A	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.7 Electrical Characteristics for $V_S = 8V$ to $48V$

at $T_A = +25^\circ C$, $V_S = 8V$ to $48V$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_L = 10k\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage			±10	±50	μV	
		T _A = −40°C to +125°C		±170			
		V _{CM} = (V+) − 1V	T _A = −40°C to +125°C	±30	±150	μV	
				±1050			
(V+) − 3.0V < V _{CM} < (V+) − 1V				See Typical Characteristics			
dV _{OS} /dT	Input offset voltage drift	T _A = −40°C to +125°C		±0.2	±1.2	μV/°C	
			V _{CM} = (V+) − 1V		±9		
PSRR	Power-supply rejection ratio			±0.3	±1.0	μV/V	
		T _A = −40°C to +125°C		±1.0			
INPUT BIAS CURRENT							
I _B	Input bias current			±2	±10	pA	
		T _A = −40°C to +125°C			±1	nA	
I _{OS}	Input offset current			±1	±10	pA	
		T _A = −40°C to +125°C			1	nA	
NOISE							
E _n	Input voltage noise	f = 0.1Hz to 10Hz	(V−) < V _{CM} < (V+) − 3V	4		μV _{PP}	
			(V+) − 1V < V _{CM} < (V+)	9			
e _n	Input voltage noise density	(V−) < V _{CM} < (V+) − 3V	f = 1kHz	14		nV/√Hz	
			f = 10kHz	7.5			
		(V+) − 1V < V _{CM} < (V+)	f = 1kHz	26			
			f = 10kHz	14			
i _n	Input current noise density	f = 1kHz		4		fA/√Hz	
INPUT VOLTAGE							
V _{CM}	Common-mode voltage			V−		V+	V
CMRR	Common-mode rejection ratio	V _S = 48V, (V−) + 0.1V < V _{CM} < (V+) − 3V	T _A = −40°C to +125°C	120	140	dB	
				114			
		V _S = 48V, (V+) − 1V < V _{CM} < (V+)	T _A = −40°C to +125°C	100	120		
				96			
INPUT IMPEDANCE							
Z _{ID}	Differential			100 TBD			MΩ pF
Z _{IC}	Common-mode			10 TBD			TΩ pF
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	V _S = 48V, (V−) + 0.4V < V _O < (V+) − 0.4V, R _L = 10kΩ	T _A = −40°C to +125°C	124	134	dB	
				120			
		V _S = 48V, (V−) + 1.5V < V _O < (V+) − 1.5V, R _L = 2kΩ	T _A = −40°C to +125°C	120	130		
				110			

5.7 Electrical Characteristics for $V_S = 8V$ to $48V$ (continued)

at $T_A = +25^\circ\text{C}$, $V_S = 8V$ to $48V$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_L = 10k\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain bandwidth	G = 1V/V		12		MHz	
		G = 100V/V		14			
		T _A = −40°C to +125°C		10			
SR	Slew rate	V _S = 48V, G = 1, 10V step		40		V/μs	
OUTPUT							
V _O	Voltage output swing from rail	Positive rail	No load	25		mV	
			R _L = 10kΩ	150			
			R _L = 2kΩ	800			
		Negative rail	No load	10			
			R _L = 10kΩ	150			
			R _L = 2kΩ	800			
I _{SC}	Short-circuit current	Sink		50		mA	
		Source		50			
C _L	Capacitive load drive			See Typical Characteristics			
I _Q	Quiescent current per amplifier	I _O = 0A		1.6	1.8	mA	
			T _A = −40°C to +125°C		1.9		
POWER SUPPLY							
TEMPERATURE							
	Thermal protection			180		°C	
	Thermal hysteresis			20		°C	

5.8 Electrical Characteristics for $V_S = 4.5V$ to $8V$

at $T_A = +25^\circ C$, $V_S = 4.5V$ to $8V$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_L = 10k\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage	V _{CM} = (V+) – 3V		±10	±50	μV	
			T _A = –40°C to +125°C	±170			
		V _{CM} = (V+) – 1V		±30	±150		
			T _A = –40°C to +125°C	±1050			
		(V+) – 3.0V < V _{CM} < (V+) – 1V			See Typical Characteristics		
dV _{OS} /dT	Input offset voltage drift	T _A = –40°C to +125°C	V _{CM} = (V+) – 3V	±0.2	±1.2	μV/°C	
			V _{CM} = (V+) – 1V		±9		
PSRR	Power-supply rejection ratio	V _{CM} = (V+) – 3V		±0.3	±1.0	μV/V	
		T _A = –40°C to +125°C			±1.0		
INPUT BIAS CURRENT							
I _B	Input bias current			±2	±10	pA	
		T _A = –40°C to +125°C			±1	nA	
I _{OS}	Input offset current			±2	±10	pA	
		T _A = –40°C to +125°C			±1	nA	
NOISE							
E _n	Input voltage noise	f = 0.1Hz to 10Hz	(V–) < V _{CM} < (V+) – 3V	4		μV _{PP}	
			(V+) – 1V < V _{CM} < (V+)	9			
e _n	Input voltage noise density	(V–) < V _{CM} < (V+) – 3V	f = 1kHz	14		nV/√Hz	
			f = 10kHz	7.5			
		(V+) – 1V < V _{CM} < (V+)	f = 1kHz	26			
			f = 10kHz	14			
i _n	Input current noise density	f = 1kHz		4		fA/√Hz	
INPUT VOLTAGE							
V _{CM}	Common-mode voltage			V–		V+	V
CMRR	Common-mode rejection ratio	(V–) < V _{CM} < (V+) – 3V		120	140	dB	
		(V–) < V _{CM} < (V+) – 3V, T _A = –40°C to +125°C		114			
		(V+) – 1V < V _{CM} < (V+)		100	120		
			T _A = –40°C to +125°C	94			
INPUT IMPEDANCE							
Z _{ID}	Differential			100 TBD			MΩ pF
Z _{IC}	Common-mode			10 TBD			TΩ pF

5.8 Electrical Characteristics for $V_S = 4.5V$ to $8V$ (continued)

at $T_A = +25^\circ C$, $V_S = 4.5V$ to $8V$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_L = 10k\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	V _S = 5V, R _L = 10kΩ (V−) + 0.2V < V _O < (V+) − 0.2V		124	134		dB
			T _A = −40°C to +125°C	118			
		V _S = 5V, R _L = 2kΩ (V−) + 0.8V < V _O < (V+) − 0.8V		110	120		dB
			T _A = −40°C to +125°C	104		dB	
FREQUENCY RESPONSE							
GBW	Gain bandwidth	G = 1V/V		12			MHz
		G = 100V/V		14			
SR	Slew rate	V _S = 5V, G = 1, 1V step		40			V/μs
OUTPUT							
V _O	Voltage output swing from rail	Positive rail	No load	15		mV	
			R _L = 10kΩ	100			
			R _L = 2kΩ	500			
		Negative rail	No load	15			
			R _L = 10kΩ	100			
			R _L = 2kΩ	500			
I _{SC}	Short-circuit current	Sink	±50		mA		
		Source	±50				
POWER SUPPLY							
I _Q	Quiescent current per amplifier	I _O = 0A		1.6	1.8	mA	
			T _A = −40°C to +125°C		1.9		
TEMPERATURE							

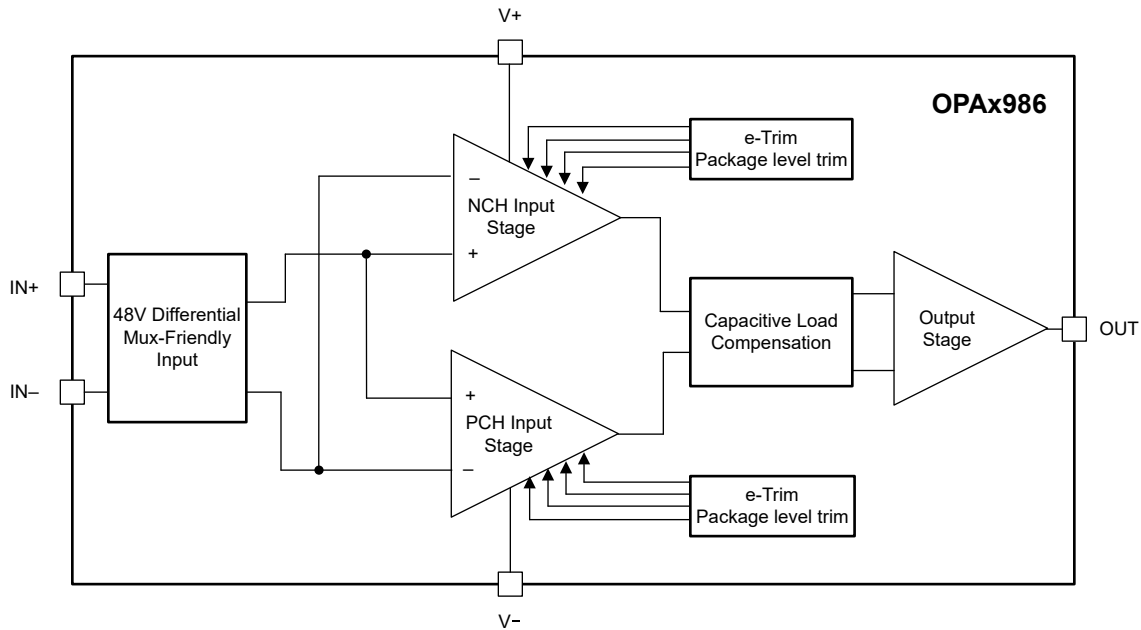
6 Detailed Description

6.1 Overview

The OPAx986 are wide bandwidth (14MHz), high slew rate (40V/ μ s), high precision (1.2 μ V/ $^{\circ}$ C, max), 48V operational amplifiers (op amps). These op amps are designed with e-Trim, a proprietary, post-package offset trimming technology, to achieve very low offset across a wide range of operating conditions. These amplifiers feature the latest state-of-the-art CMOS technology that enables rail-to-rail input and output operation, low input bias current, and tiny packages.

In addition to stellar dc performance, the OPAx986 achieve outstanding ac performance. The OPAx986 strengths also include 14MHz bandwidth, 40V/ μ s slew rate, 7.5nV/ $\sqrt{\text{Hz}}$ broadband voltage noise, and 4fA/ $\sqrt{\text{Hz}}$ of current noise. The combination of ac and dc performance make these amplifiers easy to design with in a variety of different applications. The OPAx986 are an excellent choice for designing a high performance active filter, a transimpedance amplifier (TIA), a high accuracy current monitor, or a high impedance sensor interface amplifier.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Mux-Friendly Inputs

The OPAx986 use a unique input architecture to eliminate the need for input protection diodes but still provide robust input protection under transient conditions. Conventional input diode protection schemes shown in Figure 6-1 can be activated by fast transient step responses and can introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 6-2. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes that cause an increase in input current and result in extended settling time.

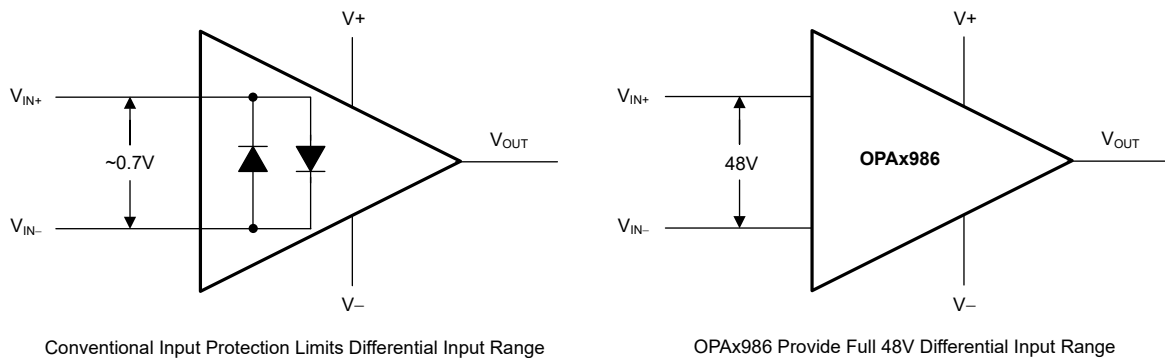


Figure 6-1. OPAx986 Input Protection Does Not Limit Differential Input Capability

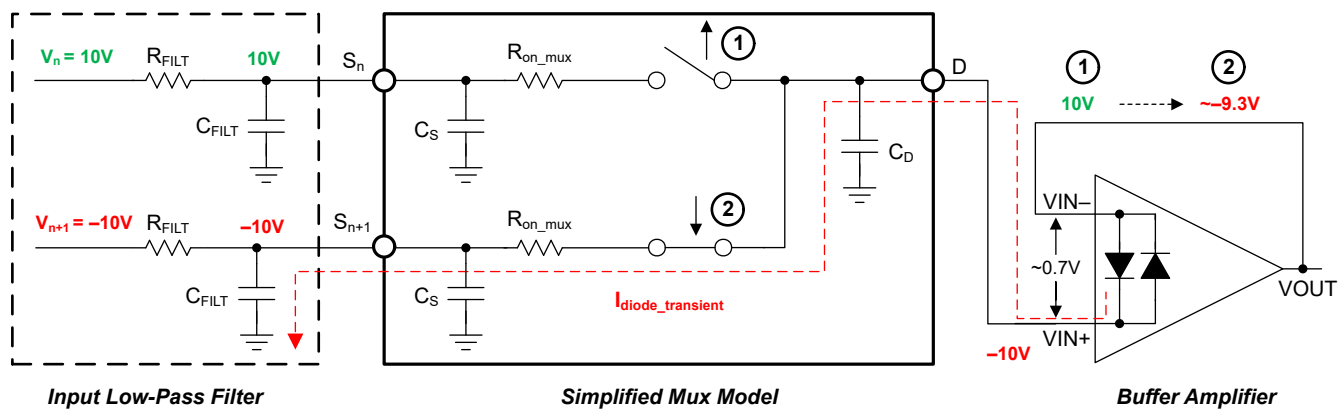


Figure 6-2. Back-to-Back Diodes Create Settling Issues

The OPAx986 feature a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making these devices an excellent choice for multichannel, high-switched, input applications. The OPAx986 tolerate a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 48V, making these devices a great choice for use as a comparator or in applications with fast-ramping or switched input signals.

6.3.2 Thermal Protection

The OPAx986 has a thermal protection feature that prevents damage from self heating. When the junction temperature (T_J) reaches approximately 175°C, the op amp output stage disables. This thermal protection works by monitoring the temperature of the output stage and turning off the op amp output drive. Thermal protection forces the output to a high-impedance state. The OPAx986 is designed with approximately 20°C of thermal hysteresis and returns to normal operation when the output stage temperature becomes less than approximately 155°C.

This thermal protection is not designed to prevent this device from exceeding absolute maximum ratings, but rather from excessive thermal overload.

6.3.3 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time.

6.3.4 Slew Rate

Slew rate is the maximum rate of change of output voltage change with respect to time and is typically specified in units of volts per microsecond, V/μs. Op amps can enter a slew condition when a large, rapid moving signal is applied at the input. While slewing, the op amp enters an open loop condition and significant slew induced distortion can be seen on the output signal.

Equation 1 shows that the slew rate, SR, of an op amp is typically determined by the saturation current of the input stage, I_{TAIL} , and the compensation capacitor, C_C .

$$SR = \frac{I_{TAIL}}{C_C} \quad (1)$$

Slew rate usually scales with the quiescent current, I_Q , of the op amp. There are several ways that designers have overcome slew rate limitation. For example, lowering C_C , commonly known as decompensation, improves slew rate at the expense of stability. Decompensated op amps require a minimum gain and are not stable at unity gain. More commonly, modern op amps are equipped with slew boost technology that increases I_{SAT} to improve slew rate. Slew boost circuits can vary in implementation, but designers can typically expect about a 4 fold improvement over comparable unboosted op amps. Slew boost can have drawbacks as well, often manifesting as increased supply current and unexpected distortion.

The OPAx986 uses proprietary design circuitry to achieve very high slew rate to I_Q ratio without the use of slew boost circuitry. The OPAx986 is unity-gain stable. See the [Full Power Bandwidth and Op Amp Distortion](#) application note to learn more about slew rate and distortion.

Table 6-1 shows a comparison of slew rates and quiescent currents of different op amps.

Table 6-1. Op Amp Slew Rates

PART NUMBER	SLEW RATE	QUIESCENT CURRENT	SLEW BOOST
OPA986	40V/μs	1.8mA	No
LMP7707	5.9V/μs	1.1mA	No, decompensated
LMP7701	1.1V/μs	1.1mA	No
OPA4986	20V/μs	1mA	Yes

6.3.5 Full-Power Bandwidth Improved

The full-power bandwidth curve has been a staple in data sheets for decades. The full-power bandwidth of an op amp provides some indication about where designers can expect slew-induced distortion on a signal of a given amplitude and frequency. The full-power bandwidth curve is generated using [Equation 2](#).

$$FPBW = \frac{SR}{2\pi V_{OUT_MAX}} \quad (2)$$

[Figure 6-3](#) shows the full-power bandwidth of the OPAX986. The curve is a good reference for designers that need to achieve high-voltage, high-frequency output swings with little concern for distortion performance. Unfortunately, the curve provides little indication of the true distortion at any given point on the curve. The full-power bandwidth curve is, after all, only a theoretical value and slew-induced distortion appears gradually as the output nears the maximum rate of change. The interpretation of the curve is further complicated by the use of different slew boost circuitry that is ever so common in modern op amps. Additionally, slew-induced distortion is only one of several sources of op amp distortion. Therefore, the curve is a decent starting point, but not a reliable source for distortion performance.

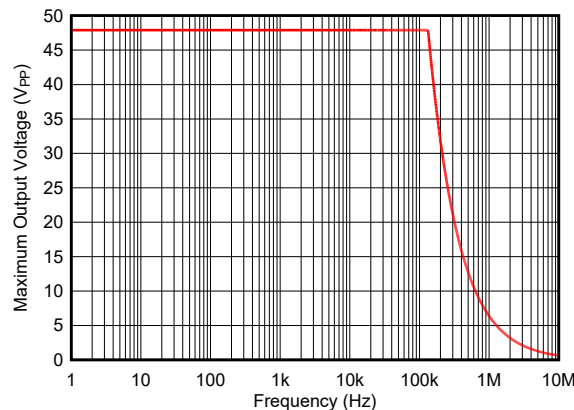


Figure 6-3. Full-Power Bandwidth

6.3.6 e-Trim™

OPAX986 of operational amplifiers is manufactured using the Texas Instruments (TI) e-trim™ technology. Each amplifier input offset voltage and input offset voltage drift is trimmed in production, thereby minimizing errors associated with input offset voltage and input offset voltage drift. The e-trim technology is a TI proprietary method of trimming internal device parameters during final testing. This trimming method avoids the package stress related offset voltage effects experienced by other trimmed op amps. When trimming input offset voltage drift, the systematic or linear drift error on each device is trimmed to zero. The remaining errors associated with input offset drift are minimal and are the result from only nonlinear error sources. For more information on the e-Trim™ technology, please see the [Offset Correction Methods: Laser Trim, e-Trim™, and Chopper application brief](#).

6.4 Device Functional Modes

The OPAX986 has a single functional mode and is operational when the power-supply voltage is between 4.5V (±2.25V) and 48V (±42.5V).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPAx986 are wide bandwidth (14MHz), high-slew rate (40V/μs), high-precision (1.2μV/°C) operational amplifiers (op amps). These op amps are designed in the latest CMOS process technology and are equipped with a variety of proprietary design techniques to achieve very high dc and ac performance, including e-Trim™, Mux-Friendly, and novel compensation circuitry.

7.2 Typical Applications

7.2.1 2nd Order Low Pass Filter

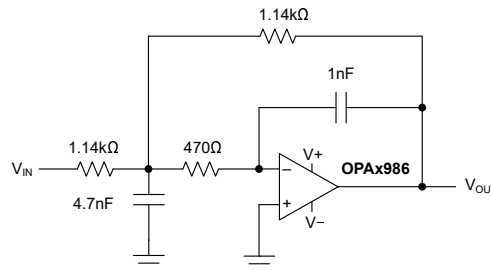


Figure 7-1. 2nd Order, Multiple Feedback Bessel Response Low Pass Filter

7.2.1.1 Design Requirements

Low pass filters are critical circuits in almost every analog signal chain design. Low pass filters isolate desired signal frequency components from high frequency components that are undesirable, such as noise and aliased signals. In some demanding applications, steep roll-off of -40dB/decade or greater are required.

Table 7-1. Design Parameters

PARAMETER	VALUE
Power supply voltage	±24V
Response	Bessel
-3dB cut-off frequency	100kHz

7.2.1.2 Detailed Design Procedure

OPA986 is an excellent choice for active filter design. The OPA986 offers a few advantages over existing amplifiers, such as ample gain bandwidth and slew rate, low noise, rail-to-rail inputs, low input bias current, and low input offset voltage.

A multiple feedback filter (MFB) topology is used for the topology's improved high frequency performance compared to other topologies. There are different filter response options to select from, but a Bessel response is chosen here to preserve phase linearity. The MFB topology provides a -40dB/decade roll off and an inverting gain. The transfer function is given by Equation 3.

$$H(s) = -\frac{R_2}{R_1} \times \left(\frac{1}{s^2(R_2C_1R_3C_2) + s(R_2C_2 + R_3C_2 + \frac{R_2R_3C_2}{R_1}) + 1} \right) \quad (3)$$

Where the ratio of R_2 and R_1 set the inverting gain of the filter. The frequency response is determined by the combination of the resistors and the capacitors in the filter. Converting to the standard form of the transfer function given by Equation 4 provides for a more straight forward analysis of the filter response.

$$H(s) = \left(\frac{K\omega_0^2}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2} \right) \quad (4)$$

The standard form of the transfer function yields the following equations.

$$K = -\frac{R_2}{R_1} \quad (5)$$

$$Q = \frac{\sqrt{R_2C_1R_3C_2}}{R_2C_2 + R_3C_2 + \frac{R_2R_3C_2}{R_1}} \quad (6)$$

$$\omega_0 = \frac{1}{\sqrt{R_2C_1R_3C_2}} \quad (7)$$

The best approach is to select the capacitor values in such a way that the roots of the transfer function yield real resistor values. Using Equation 5, Equation 6, Equation 7, and the quadratic formula, an inequality for C_1 can be derived. Selecting a standard capacitor value for C_2 , the capacitor, C_1 , is calculated using Equation 8.

$$C_1 \geq C_2 \times 4Q^2(1 + K) \quad (8)$$

Setting C_2 to 1nF, means that C_1 must be ≥ 2.66 nF. A standard 4.7nF capacitor is chosen for C_2 . Recall that 2nd order Bessel filter response is achieved with a quality factor (Q) of 0.577. With C_1 , C_2 , Q, and K fixed, the resistor R_2 can be found using Equation 9.

$$R_2 = \frac{1}{4\pi f_c Q C_2 (1 + K)} \times \left(1 + \sqrt{1 - \frac{4C_2 Q^2 (1 + K)}{C_1}} \right) \quad (9)$$

Substituting the known values into Equation 9 yields a resistor value of 1.143k Ω . A standard value of 1.14k Ω is chosen. Note that $R_1 = R_2$ for an inverting gain of 1. To solve for R_3 , use Equation 7 and the component values found in previous steps. The calculated value for R_3 is 471 Ω so a standard 470 Ω resistor is used.

The circuit is then verified using TINA-Spice for TI with the gain and transient response are shown in Figure 7-2 and Figure 7-3, respectively. The cut-off frequency is calculated to be approximately 100.3kHz with the calculated component values and matches well with simulated curve.

7.2.1.3 Application Curves

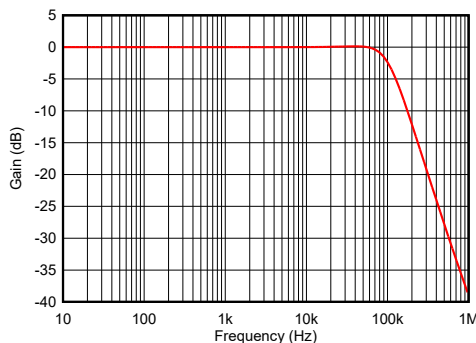


Figure 7-2. Gain over Frequency Response

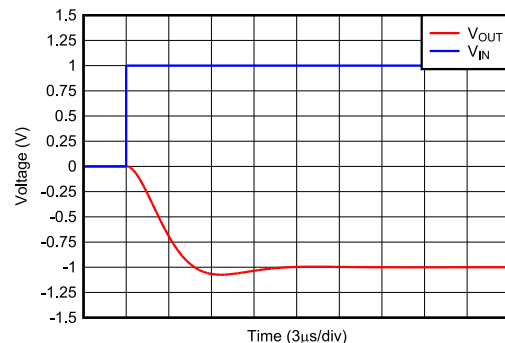


Figure 7-3. Transient Response

7.2.2 High-Side Current Sense

The OPAx986 enables high voltage current sense measurements. High-side voltage measurements of 48V can be easily implemented using the OPAx986. The voltage capability is proportional to the gain of the sense circuit and the input common-mode range of the amplifier. Figure 7-4 shows the OPA986 configured for a 36V battery high side current measurement and a gain of 40V/V to generate a 3V full-scale output. A high precision amplifier gain stage is not needed in this design.

Make the input resistors large enough to avoid any loading related errors. The low input bias current of the OPAx986 allows for the use of larger resistors when compared to other power amplifiers and is not a major contribution to the total error in this application. Special consideration of input bias current, thermal noise, and input common-mode range is warranted when choosing resistors for this design.

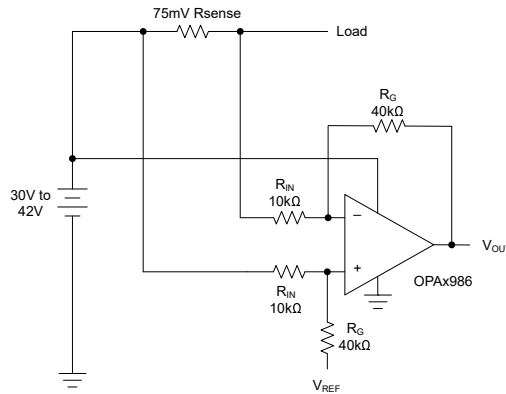


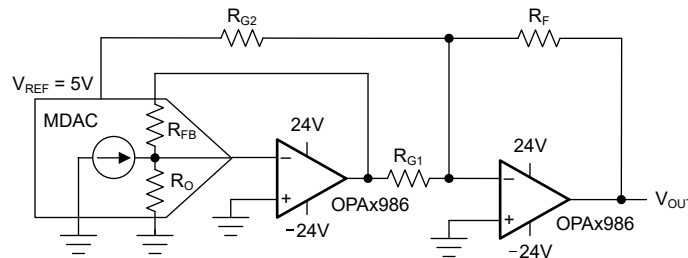
Figure 7-4. 36V Battery High-Side Current Sense

Consider using the RES21A matched resistor pair to achieve high common-mode rejection ratio (CMRR) in a ready to use package.

7.2.3 MDAC Output Gain and Buffer

Digital to analog converters (DACs) are used in a wide variety of electronic systems. Specific DAC architectures, like multiplying DACs or MDACs often require an amplifier to convert an output current into a voltage. Essentially, the amplifier is connected as a transimpedance amplifier and any additional current degrades the accuracy of the MDAC. A low input bias current amplifier is critical to maintain a low error budget. Another challenge with MDACs is that the output impedance changes with a given output code, and increases the noise gain of the amplifier. Higher noise gain not only reduces the op amp's usable bandwidth, but also amplifies the input offset voltage errors of the op amp. A high precision op amp with ample bandwidth helps preserve the MDACs specified performance.

The OPAx986 is an excellent choice given the combination of dc and ac performance characteristics. The high bandwidth and slew rate enable faster settling, and the low input bias current and low input offset and input offset drift maintain high accuracy across a variety of different operating conditions. An added benefit of the OPAx986 is the 48V ($\pm 24V$) operating capability that enables wider output voltages to be generated compared to other traditional amplifiers.



7.3 Power Supply Recommendations

The OPAx986 operates from power supplies up to 48V ($\pm 24V$), and as little as 4.5V ($\pm 2.25V$) with excellent performance. Most behavior remains unchanged throughout the full operating voltage range, but the Typical Characteristics section shows parameters that vary with operating voltage. A power-supply bypass capacitor of at least 0.1 μ F is recommended. The OPAx986 can be powered with asymmetrical supplies to optimize power dissipation in applications that do not require an equal positive and negative output voltage swing.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including the following guidelines:

- Noise can propagate into analog circuitry through the power pins of the op amp and the circuit as a whole. Connect low-ESR, 0.1 μ F ceramic bypass capacitors between each supply pin and ground. Place the capacitors as close to the device as possible. A single bypass capacitor from V+ to ground is sufficient for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example

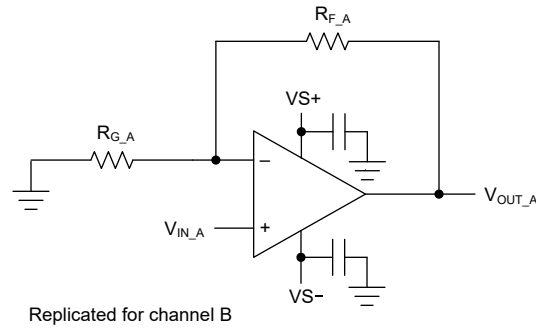


Figure 7-5. Schematic Representation of Noninverting Configuration

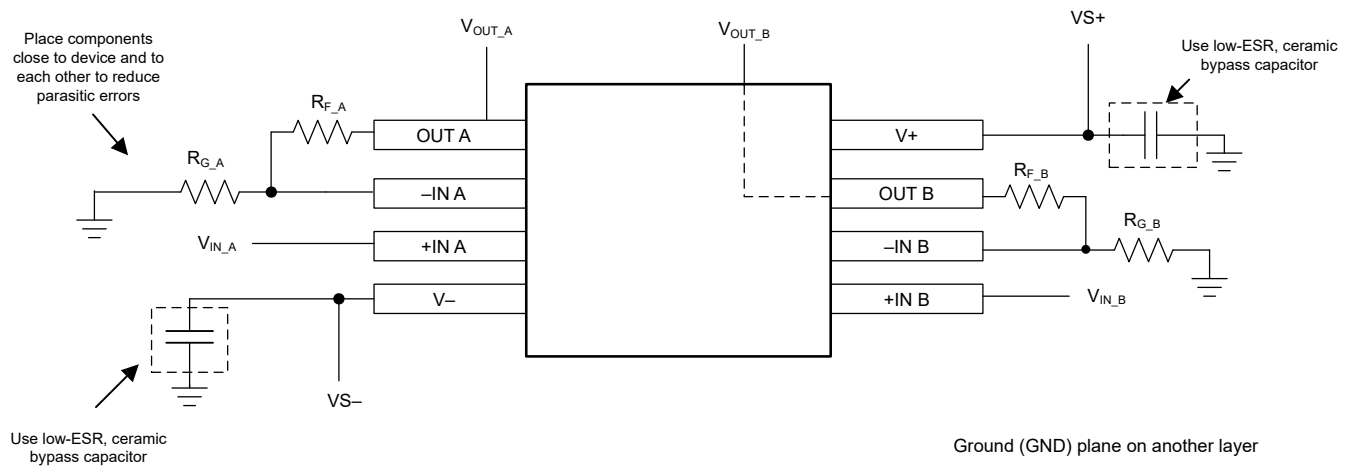


Figure 7-6. Board Layout for Noninverting Configuration of the VSSOP-8 Package

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.3 Trademarks

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8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2026	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
POPA2986DGKR	Active	Preproduction	VSSOP (DGK) 8	3500 LARGE T&R	-	Call TI	Call TI	-40 to 125	

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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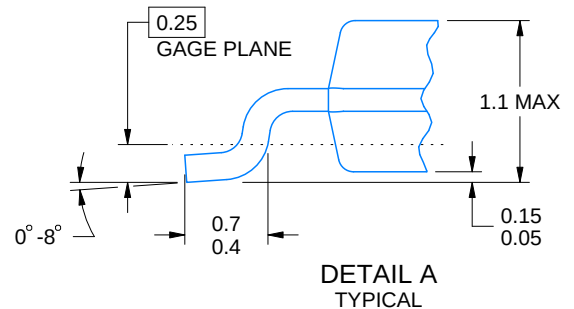
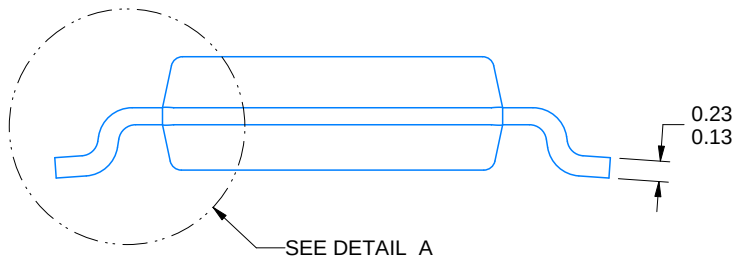
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VSSOP - 1.1 mm max height

Technical drawing of a 6-pin connector. The drawing includes a top view and a side view. The top view shows a rectangular component with six pins on the right side. Dimensions include a total width of 5.05 (typical) and 4.75, a pin pitch of 1.95 (2X), and a pin width of 0.65 (6X). A circular feature is labeled "PIN 1 INDEX AREA". The side view shows the component's profile with a height of 3.1 (typical) and 2.9, and a pin height of 0.38 (typical) and 0.25. A "SEATING PLANE" is indicated. Callouts A, B, and C are present. A table of values is provided at the bottom right:

⊕	0.13	Ⓜ	C	A	B
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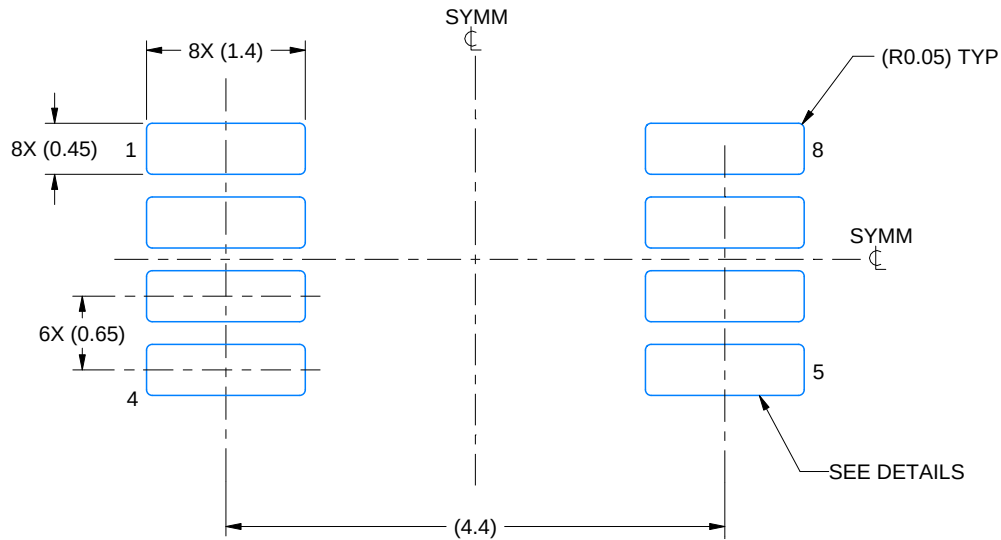


EXAMPLE BOARD LAYOUT

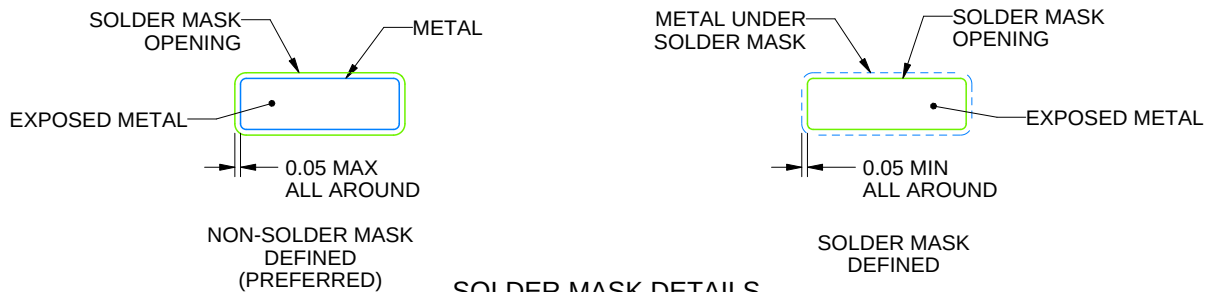
DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

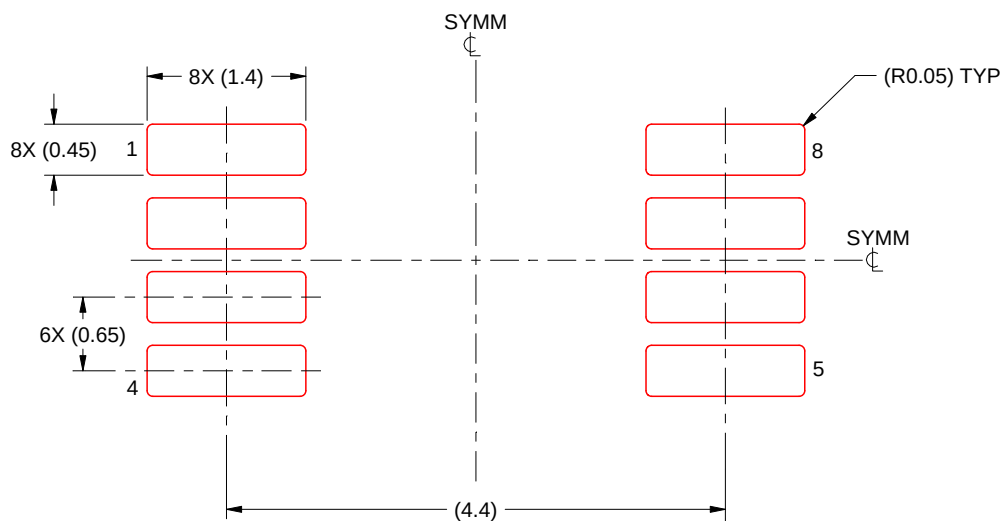
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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