

# OPAx990 40-V Rail-to-Rail Input/Output, Low Offset Voltage, Low Power Op Amp

## 1 Features

- Low offset voltage:  $\pm 300 \mu\text{V}$
- Low offset voltage drift:  $\pm 0.6 \mu\text{V}/^\circ\text{C}$
- Low noise:  $30 \text{nV}/\sqrt{\text{Hz}}$  at 1 kHz
- High common-mode rejection: 115 dB
- Low bias current:  $\pm 10 \text{ pA}$
- Rail-to-rail input and output
- MUX-friendly/comparator inputs
  - Amplifier operates with differential inputs up to supply rail
  - Amplifier can be used in open-loop or as comparator
- Wide bandwidth: 1.1-MHz GBW
- High slew rate:  $4.5 \text{ V}/\mu\text{s}$
- Low quiescent current:  $120 \mu\text{A}$  per amplifier
- Wide supply:  $\pm 1.35 \text{ V}$  to  $\pm 20 \text{ V}$ ,  $2.7 \text{ V}$  to  $40 \text{ V}$
- Robust EMI/RF performance: 78 dB at 1.8 GHz
- Differential and common-mode input voltage range to supply rail

## 2 Applications

- Multiplexed data-acquisition systems
- Test and measurement equipment
- Motor drive: power stage and control modules
- Power delivery: UPS, server, and merchant network power
- ADC driver and reference buffer amplifier
- Programmable logic controllers
- Analog input and output modules
- High-side and low-side current sensing
- High precision comparator

## 3 Description

The OPAx990 family (OPA990, OPA2990, and OPA4990) is a family of high voltage (40 V) general purpose operational amplifiers. These devices offer excellent DC precision and AC performance, including rail-to-rail input/output, low offset ( $\pm 300 \mu\text{V}$ , typ), and low offset drift ( $\pm 0.6 \mu\text{V}/^\circ\text{C}$ , typ).

Unique features such as differential and common-mode input voltage range to the supply rail, high short-circuit current ( $\pm 80 \text{ mA}$ ), high slew rate ( $4.5 \text{ V}/\mu\text{s}$ ), and shutdown make the OPAx990 an extremely flexible, robust, and high-performance op amp for high-voltage industrial applications.

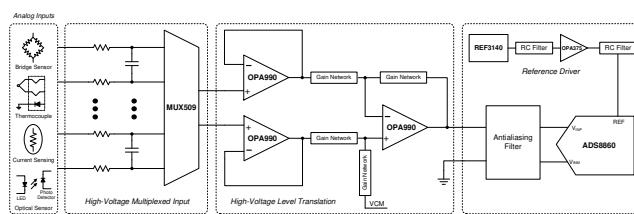
The OPAx990 family of op amps is available in micro-size packages (such as X2QFN, WSON, and SOT-553), as well as standard packages (such as SOT-23, SOIC, and TSSOP), and is specified from  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

## Device Information

| PART NUMBER <sup>(1)</sup> | PACKAGE                    | BODY SIZE (NOM)          |
|----------------------------|----------------------------|--------------------------|
| OPA990                     | SOT-23 (5)                 | 2.90 mm $\times$ 1.60 mm |
|                            | SOT-23 (6)                 | 2.90 mm $\times$ 1.60 mm |
|                            | SC70 (5)                   | 2.00 mm $\times$ 1.25 mm |
|                            | SOT-553 (5) <sup>(2)</sup> | 1.60 mm $\times$ 1.20 mm |
| OPA2990                    | SOIC (8)                   | 4.90 mm $\times$ 3.90 mm |
|                            | SOT-23 (8)                 | 2.90 mm $\times$ 1.60 mm |
|                            | TSSOP (8)                  | 3.00 mm $\times$ 4.40 mm |
|                            | VSSOP (8)                  | 3.00 mm $\times$ 3.00 mm |
|                            | VSSOP (10)                 | 3.00 mm $\times$ 3.00 mm |
|                            | WSON (8)                   | 2.00 mm $\times$ 2.00 mm |
|                            | X2QFN (10)                 | 2.00 mm $\times$ 1.50 mm |
| OPA4990                    | SOIC (14)                  | 8.65 mm $\times$ 3.90 mm |
|                            | TSSOP (14)                 | 5.00 mm $\times$ 4.40 mm |
|                            | WQFN (16)                  | 3.00 mm $\times$ 3.00 mm |
|                            | X2QFN (14)                 | 2.00 mm $\times$ 2.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) This package is preview only.



## OPAx990 in a High-Voltage, Multiplexed, Data-Acquisition System



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision H (May 2021) to Revision I (August 2021)</b>  | <b>Page</b> |
|--|-------------|
| • Removed preview notation from OPA2990 VSSOP-8 package (DGK) from <i>Device Information</i> table.....  | 1           |
| • Removed preview notation from OPA2990 VSSOP-8 package (DGK) in the <i>Pin Configuration and Functions</i> section.....   | 4           |
| • Added note explaining difference between DDF and TDDF packages in the <i>Pin Configuration and Functions</i> section.....  | 4           |
| • Corrected typo describing shutdown region in <i>Recommended Operating Conditions</i> to match rest of data sheet.....  | 10          |
| • Changed Junction-to-ambient thermal resistance value for SOT-23-6 (DBV-6) from 1174.5°C/W to 174.5°C/W in the <i>Thermal Information for Single Channel</i> section.....                                   | 11          |
| • Added clarifying statement regarding logic low signal for SHDN pin in the <i>Shutdown</i> section.....   | 32          |
| • Corrected statement on shutdown enable and disable times in the <i>Shutdown</i> section from 30 µs and 3 µs to 11 µs and 2.5 µs, respectively, to match the <i>Electrical Characteristics</i> section..... | 32          |

| <b>Changes from Revision G (December 2020) to Revision H (May 2021)</b>  | <b>Page</b> |
|--|-------------|
| • Removed preview notation from OPA4990 WQFN (16) package from <i>Device Information</i> table.....                                | 1           |
| • Removed preview notation from OPA4990 X2QFN (14) package from <i>Device Information</i> table.....                               | 1           |
| • Removed preview notation from OPA4990 and OPA4990S RTE package (WQFN) in the <i>Pin Configuration and Functions</i> section..... | 4           |
| • Removed Table of Graphs from <i>Specifications</i> section.....  | 10          |
| • Clarified threshold and maximum voltage levels of the shutdown pin in the <i>Shutdown</i> section.....                           | 32          |
| • Removed <i>Related Links</i> from <i>Device and Documentation</i> section.....   | 39          |

| <b>Changes from Revision F (May 2020) to Revision G (December 2020)</b>                               | <b>Page</b> |
|---|-------------|
| • Updated the numbering format for tables, figures and cross-references throughout the document ..... | 1           |
| • Removed preview notation from OPA2990 SOT-23 (8) package from <i>Device Information</i> table.....  | 1           |
| • Added OPA2990 VSSOP (10) package to <i>Device Information</i> table.....                            | 1           |
| • Clarified SHDN notation on OPA4990S <i>Pin Functions</i> .....                                      | 4           |

|  |   |
|--|---|
| • Removed preview notation from OPA2990 DDF package (SOT-23) in the <i>Pin Configuration and Functions</i> section.....  | 4 |
| • Removed preview notation from OPA2990S DGS package (VSSOP) in the <i>Pin Configuration and Functions</i> section ..... | 4 |
| • Clarified SHDN notation for OPA2990S in the <i>Pin Functions</i> section .....   | 4 |
| • Clarified SHDN notation for OPA4990S in the <i>Pin Functions</i> section .....   | 4 |

| <b>Changes from Revision E (December 2019) to Revision F (May 2020)</b>  | <b>Page</b> |
|--|-------------|
| • Removed preview notation from OPA2990 X2QFN (10) package from <i>Device Information</i> table .....                    | 1           |
| • Removed preview notation from OPA2990S RUG package (X2QFN) in the <i>Pin Configuration and Functions</i> section ..... | 4           |
| • Changed RUG (X2QFN) in <i>Thermal Information for Dual Channel</i> section.....  | 4           |

| <b>Changes from Revision D (July 2019) to Revision E (December 2019)</b>  | <b>Page</b> |
|---|-------------|
| • Changed the OPA990 and OPA4990 device statuses from <i>Advance Information</i> to <i>Production Data</i> .....                    | 1           |
| • Removed preview notation from OPA990 SOT-23 (5) package from <i>Device Information</i> table.....                                 | 1           |
| • Removed preview notation from OPA990S SOT-23 (6) package from <i>Device Information</i> table.....                                | 1           |
| • Removed preview notation from OPA990 SC70 (5) package from <i>Device Information</i> table.....                                   | 1           |
| • Removed preview notation from OPA4990 SOIC (14) package from <i>Device Information</i> table.....                                 | 1           |
| • Removed preview notation from OPA4990 TSSOP (14) package from <i>Device Information</i> table.....                                | 1           |
| • Removed preview notation from OPA990 DBV package (SOT-23) in the <i>Pin Configuration and Functions</i> section.....              | 4           |
| • Removed preview notation from OPA990 DCK package (SC70) in the <i>Pin Configuration and Functions</i> section.....                | 4           |
| • Removed preview notation from OPA4990 D (SOIC) and TSSOP (PW) packages in the <i>Pin Configuration and Functions</i> section..... | 4           |
| • Removed preview notation from OPA990S DBV package (SOT-23) in the <i>Pin Configuration and Functions</i> section.....             | 4           |

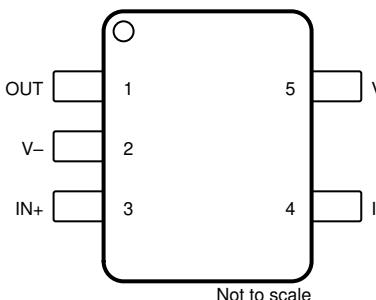
| <b>Changes from Revision C (May 2019) to Revision D (July 2019)</b>   | <b>Page</b> |
|---|-------------|
| • Removed preview notation from OPA2990 WSON (8) package from <i>Device Information</i> table.....                    | 1           |
| • Removed preview notation from OPA2990 DSG package (WSON) in the <i>Pin Configuration and Functions</i> section..... | 4           |
| • Added SHUTDOWN to <i>Electrical Characteristics</i> table.....  | 13          |
| • Added <i>Shutdown</i> section to the <i>Detailed Description</i> section.....                                       | 32          |

| <b>Changes from Revision B (April 2019) to Revision C (May 2019)</b>  | <b>Page</b> |
|---|-------------|
| • Removed preview notation from OPA2990 TSSOP (8) package from <i>Device Information</i> table.....                   | 1           |
| • Removed preview notation from OPA2990 PW package (TSSOP) in the <i>Pin Configuration and Functions</i> section..... | 4           |

| <b>Changes from Revision A (March 2019) to Revision B (April 2019)</b>   | <b>Page</b> |
|--|-------------|
| • Removed preview notation from OPA2990 SOIC (8) package from <i>Device Information</i> table.....               | 1           |
| • Removed preview notation from OPA2990 D package (SOIC) in the <i>Pin Configuration and Functions</i> section.. | 4           |

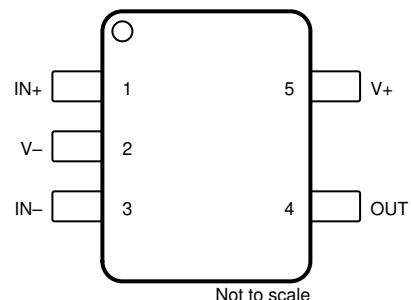
| <b>Changes from Revision * (February 2019) to Revision A (March 2019)</b>                           | <b>Page</b> |
|---|-------------|
| • Changed the OPA2990 device status from <i>Advance Information</i> to <i>Production Data</i> ..... | 1           |

## 5 Pin Configuration and Functions



A. DRL package is preview only.

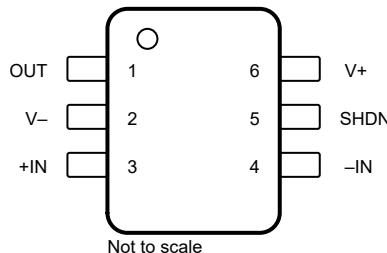
**Figure 5-1. OPA990 DBV and DRL Package<sup>(A)</sup>**  
**5-Pin SOT-23 and SOT-553**  
**Top View**



**Figure 5-2. OPA990 DCK Package**  
**5-Pin SC70**  
**Top View**

**Table 5-1. Pin Functions: OPA990**

| PIN  |             |     | I/O | DESCRIPTION                     |
|------|-------------|-----|-----|---------------------------------|
| NAME | DBV and DRL | DCK |     |                                 |
| IN+  | 3           | 1   | I   | Noninverting input              |
| IN-  | 4           | 3   | I   | Inverting input                 |
| OUT  | 1           | 4   | O   | Output                          |
| V+   | 5           | 5   | —   | Positive (highest) power supply |
| V-   | 2           | 2   | —   | Negative (lowest) power supply  |

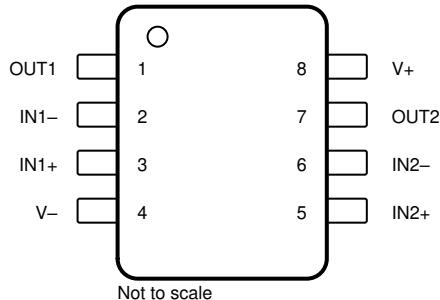


A. DRL package is preview only.

**Figure 5-3. OPA990S DBV and DRL Package<sup>(A)</sup>**  
**6-Pin SOT-23 and SOT-563**  
**Top View**

**Table 5-2. Pin Functions: OPA990S**

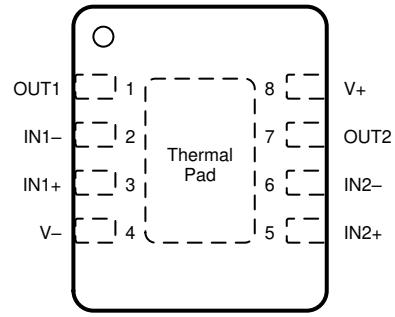
| PIN  |     | I/O | DESCRIPTION   |
|------|-----|-----|---|
| NAME | NO. |     |   |
| IN+  | 3   | I   | Noninverting input  |
| IN-  | 4   | I   | Inverting input   |
| OUT  | 1   | O   | Output  |
| SHDN | 5   | I   | Shutdown: low = amplifier enabled, high = amplifier disabled. See <i>Shutdown</i> section for more information. |
| V+   | 6   | —   | Positive (highest) power supply   |
| V-   | 2   | —   | Negative (lowest) power supply  |



A. DDF and TDDF differ in pin 1 orientation within tape and reel.

See [Mechanical, Packaging, and Orderable Information](#) section for more information.

**Figure 5-4. OPA2990 D, DDF, DGK, PW, and TDDF Package<sup>(A)</sup>**  
8-Pin SOIC, SOT-23-8, TSSOP, and VSSOP  
Top View

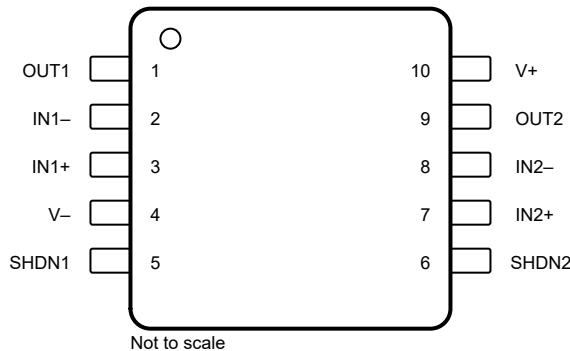


A. Connect thermal pad to V-. See [Packages with an Exposed Thermal Pad](#) section for more information.

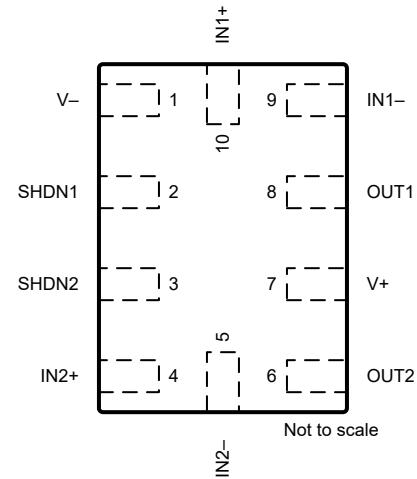
**Figure 5-5. OPA2990 DSG Package<sup>(A)</sup>**  
8-Pin WSON With Exposed Thermal Pad  
Top View

**Table 5-3. Pin Functions: OPA2990**

| PIN  |     | I/O | DESCRIPTION                     |
|------|-----|-----|---------------------------------|
| NAME | NO. |     |                                 |
| IN1+ | 3   | I   | Noninverting input, channel 1   |
| IN1- | 2   | I   | Inverting input, channel 1      |
| IN2+ | 5   | I   | Noninverting input, channel 2   |
| IN2- | 6   | I   | Inverting input, channel 2      |
| OUT1 | 1   | O   | Output, channel 1               |
| OUT2 | 7   | O   | Output, channel 2               |
| V+   | 8   | —   | Positive (highest) power supply |
| V-   | 4   | —   | Negative (lowest) power supply  |



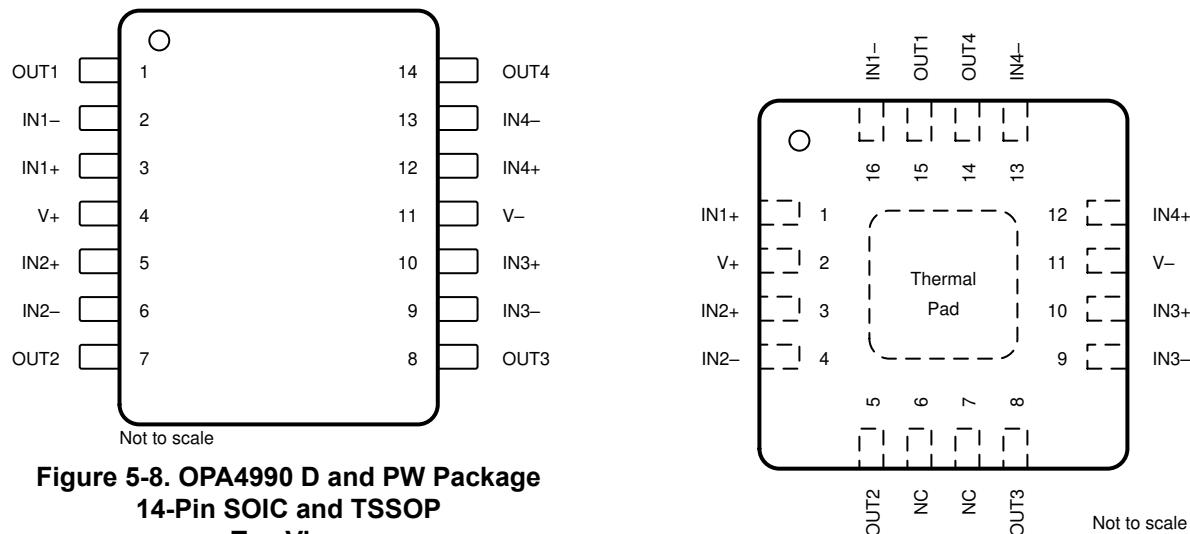
**Figure 5-6. OPA2990S DGS Package  
10-Pin VSSOP  
Top View**



**Figure 5-7. OPA2990S RUG Package  
10-Pin X2QFN  
Top View**

**Table 5-4. Pin Functions: OPA2990S**

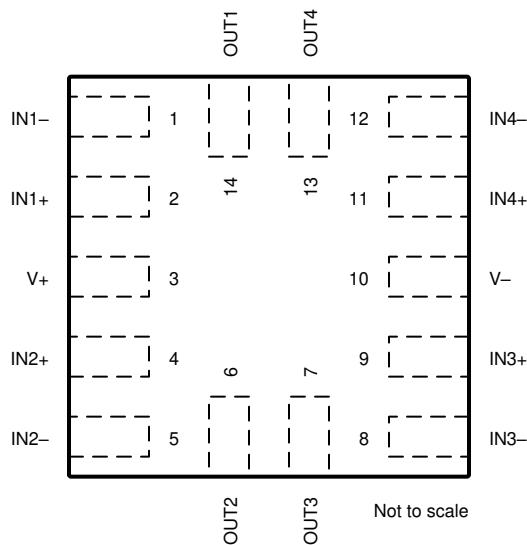
| PIN   |       | I/O | DESCRIPTION |   |
|-------|-------|-----|-------------|---|
| NAME  | VSSOP |     | X2QFN       |   |
| IN1+  | 3     | 10  | I           | Noninverting input, channel 1   |
| IN1-  | 2     | 9   | I           | Inverting input, channel 1  |
| IN2+  | 7     | 4   | I           | Noninverting input, channel 2   |
| IN2-  | 8     | 5   | I           | Inverting input, channel 2  |
| OUT1  | 1     | 8   | O           | Output, channel 1   |
| OUT2  | 9     | 6   | O           | Output, channel 2   |
| SHDN1 | 5     | 2   | I           | Shutdown, channel 1: low = amplifier enabled, high = amplifier disabled. See <a href="#">Shutdown</a> section for more information. |
| SHDN2 | 6     | 3   | I           | Shutdown, channel 2: low = amplifier enabled, high = amplifier disabled. See <a href="#">Shutdown</a> section for more information. |
| V+    | 10    | 7   | —           | Positive (highest) power supply   |
| V-    | 4     | 1   | —           | Negative (lowest) power supply  |



**Figure 5-8. OPA4990 D and PW Package  
14-Pin SOIC and TSSOP  
Top View**

A. Connect thermal pad to V-. See [Packages with an Exposed Thermal Pad](#) section for more information.

**Figure 5-9. OPA4990 RTE Package(A)  
16-Pin WQFN With Exposed Thermal Pad  
Top View**



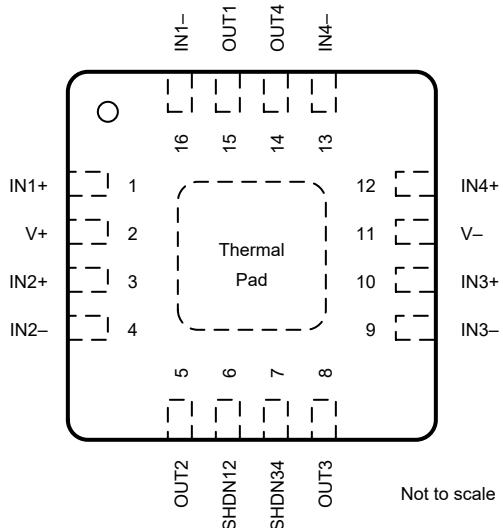
**Figure 5-10. OPA4990 RUC Package  
14-Pin X2QFN With Exposed Thermal Pad  
Top View**

**Table 5-5. Pin Functions: OPA4990**

| NAME | PIN               |      |       | I/O | DESCRIPTION                   |
|------|-------------------|------|-------|-----|-------------------------------|
|      | SOIC and<br>TSSOP | WQFN | X2QFN |     |                               |
| IN1+ | 3                 | 1    | 2     | I   | Noninverting input, channel 1 |
| IN1- | 2                 | 16   | 1     | I   | Inverting input, channel 1    |
| IN2+ | 5                 | 3    | 4     | I   | Noninverting input, channel 2 |

**Table 5-5. Pin Functions: OPA4990 (continued)**

| NAME | PIN            |      |       | I/O | DESCRIPTION                     |
|------|----------------|------|-------|-----|---------------------------------|
|      | SOIC and TSSOP | WQFN | X2QFN |     |                                 |
| IN2– | 6              | 4    | 5     | I   | Inverting input, channel 2      |
| IN3+ | 10             | 10   | 9     | I   | Noninverting input, channel 3   |
| IN3– | 9              | 9    | 8     | I   | Inverting input, channel 3      |
| IN4+ | 12             | 12   | 11    | I   | Noninverting input, channel 4   |
| IN4– | 13             | 13   | 12    | I   | Inverting input, channel 4      |
| NC   | —              | 6, 7 | —     | —   | Do not connect                  |
| OUT1 | 1              | 15   | 14    | O   | Output, channel 1               |
| OUT2 | 7              | 5    | 6     | O   | Output, channel 2               |
| OUT3 | 8              | 8    | 7     | O   | Output, channel 3               |
| OUT4 | 14             | 14   | 13    | O   | Output, channel 4               |
| V+   | 4              | 2    | 3     | —   | Positive (highest) power supply |
| V–   | 11             | 11   | 10    | —   | Negative (lowest) power supply  |



A. Connect thermal pad to V-. See *Packages with an Exposed Thermal Pad* section for more information.

**Figure 5-11. OPA4990S RTE Package<sup>(A)</sup>  
16-Pin WQFN With Exposed Thermal Pad  
Top View**

**Table 5-6. Pin Functions: OPA4990S**

| PIN    |     | I/O | DESCRIPTION  |
|--------|-----|-----|--|
| NAME   | NO. |     |  |
| IN1+   | 1   | I   | Noninverting input, channel 1  |
| IN1-   | 16  | I   | Inverting input, channel 1   |
| IN2+   | 3   | I   | Noninverting input, channel 2  |
| IN2-   | 4   | I   | Inverting input, channel 2   |
| IN3+   | 10  | I   | Noninverting input, channel 3  |
| IN3-   | 9   | I   | Inverting input, channel 3   |
| IN4+   | 12  | I   | Noninverting input, channel 4  |
| IN4-   | 13  | I   | Inverting input, channel 4   |
| OUT1   | 15  | O   | Output, channel 1  |
| OUT2   | 5   | O   | Output, channel 2  |
| OUT3   | 8   | O   | Output, channel 3  |
| OUT4   | 14  | O   | Output, channel 4  |
| SHDN12 | 6   | I   | Shutdown, channels 1 and 2: low = amplifiers enabled, high = amplifiers disabled. See <a href="#">Shutdown</a> section for more information. |
| SHDN34 | 7   | I   | Shutdown, channels 3 and 4: low = amplifiers enabled, high = amplifiers disabled. See <a href="#">Shutdown</a> section for more information. |
| VCC+   | 2   | —   | Positive (highest) power supply  |
| VCC-   | 11  | —   | Negative (lowest) power supply   |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)<sup>(1)</sup>

|                                      |                                     | MIN          | MAX          | UNIT |
|--------------------------------------|-------------------------------------|--------------|--------------|------|
| Supply voltage, $V_S = (V+) - (V-)$  |                                     | 0            | 42           | V    |
| Signal input pins                    | Common-mode voltage <sup>(3)</sup>  | $(V-) - 0.5$ | $(V+) + 0.5$ | V    |
|                                      | Differential voltage <sup>(3)</sup> |              | $V_S + 0.2$  | V    |
|                                      | Current <sup>(3)</sup>              | -10          | 10           | mA   |
| Shutdown pin voltage <sup>(4)</sup>  |                                     | $V_-$        | $(V-) + 20$  | V    |
| Output short-circuit <sup>(2)</sup>  |                                     | Continuous   |              |      |
| Operating ambient temperature, $T_A$ |                                     | -55          | 150          | °C   |
| Junction temperature, $T_J$          |                                     |              | 150          | °C   |
| Storage temperature, $T_{stg}$       |                                     | -65          | 150          | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to ground, one amplifier per package. Extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual destruction. See the [Thermal Protection](#) section for more information.
- (3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
- (4) Cannot exceed  $V_+$ .

### 6.2 ESD Ratings

|             |                         | VALUE  | UNIT       |
|-------------|-------------------------|--|------------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | $\pm 2000$ |
|             |                         | Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | $\pm 1000$ |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

|          |   | MIN          | MAX                          | UNIT |
|----------|---|--------------|------------------------------|------|
| $V_S$    | Supply voltage, $(V+) - (V-)$                                 | 2.7          | 40                           | V    |
| $V_I$    | Input voltage range   | $(V-) - 0.2$ | $(V+) + 0.2$                 | V    |
| $V_{IH}$ | High level input voltage at shutdown pin (amplifier disabled) | $(V-) + 1.1$ | $(V-) + 20 V$ <sup>(1)</sup> | V    |
| $V_{IL}$ | Low level input voltage at shutdown pin (amplifier enabled)   | $(V-)$       | $(V-) + 0.2$                 | V    |
| $T_A$    | Specified temperature   | -40          | 125                          | °C   |

- (1) Cannot exceed  $V_+$ .

## 6.4 Thermal Information for Single Channel

| THERMAL METRIC <sup>(1)</sup> |  | OPA990, OPA990S |        |               |                                 |        | UNIT |  |
|-------------------------------|--|-----------------|--------|---------------|---------------------------------|--------|------|--|
|                               |  | DBV<br>(SOT-23) |        | DCK<br>(SC70) | DRL <sup>(2)</sup><br>(SOT-553) |        |      |  |
|                               |  | 5 PINS          | 6 PINS | 5 PINS        | 5 PINS                          | 6 PINS |      |  |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 192.1           | 174.5  | 204.6         | TBD                             | TBD    | °C/W |  |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 113.6           | 113.4  | 116.5         | TBD                             | TBD    | °C/W |  |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 60.5            | 55.8   | 51.8          | TBD                             | TBD    | °C/W |  |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 37.2            | 39.6   | 24.9          | TBD                             | TBD    | °C/W |  |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 60.3            | 55.6   | 51.5          | TBD                             | TBD    | °C/W |  |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | N/A             | N/A    | N/A           | TBD                             | TBD    | °C/W |  |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

(2) This package option is preview for OPA990.

## 6.5 Thermal Information for Dual Channel

| THERMAL METRIC <sup>(1)</sup> |  | OPA2990, OPA2990S |                   |                |                |               |               | UNIT  |      |
|-------------------------------|--|-------------------|-------------------|----------------|----------------|---------------|---------------|-------|------|
|                               |  | D<br>(SOIC)       | DDF<br>(SOT-23-8) | DGK<br>(VSSOP) | DGS<br>(VSSOP) | DSG<br>(WSON) | PW<br>(TSSOP) |       |      |
|                               |  | 8 PINS            | 8 PINS            | 8 PINS         | 10 PINS        | 8 PINS        | 8 PINS        |       |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 138.7             | 150.4             | 189.3          | 152.2          | 81.6          | 188.4         | 149.6 | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 78.7              | 85.6              | 75.8           | 67.3           | 101.6         | 77.1          | 58.3  | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 82.2              | 70.0              | 111.0          | 95.5           | 48.3          | 119.1         | 77.7  | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 27.8              | 8.1               | 15.4           | 67.9           | 6.0           | 14.2          | 1.3   | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 81.4              | 69.6              | 109.3          | 94.3           | 48.3          | 117.4         | 77.5  | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | N/A               | N/A               | N/A            | N/A            | 22.8          | N/A           | N/A   | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.6 Thermal Information for Quad Channel

| THERMAL METRIC <sup>(1)</sup> |  | OPA4990, OPA4990S |               |                              |               | UNIT |
|-------------------------------|--|-------------------|---------------|------------------------------|---------------|------|
|                               |  | D<br>(SOIC)       | PW<br>(TSSOP) | RTE <sup>(2)</sup><br>(WQFN) | RUC<br>(WQFN) |      |
|                               |  | 14 PINS           | 14 PINS       | 16 PINS                      | 14 PINS       |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 105.2             | 134.7         | 53.5                         | 143.0         | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 61.2              | 55.0          | 58.3                         | 46.4          | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 61.1              | 79.0          | 28.6                         | 81.8          | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 21.4              | 9.2           | 2.1                          | 1.0           | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 60.7              | 78.1          | 28.6                         | 81.5          | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | N/A               | N/A           | 12.6                         | N/A           | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

(2) This package option is preview for OPA4990.

## 6.7 Electrical Characteristics

For  $V_S = (V+) - (V-) = 2.7 \text{ V}$  to  $40 \text{ V}$  ( $\pm 1.35 \text{ V}$  to  $\pm 20 \text{ V}$ ) at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10 \text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

| PARAMETER                  |  | TEST CONDITIONS   |  | MIN  | TYP               | MAX                          | UNIT                                 |  |
|----------------------------|--|---|--|--|-------------------|------------------------------|--------------------------------------|--|
| <b>OFFSET VOLTAGE</b>      |  |   |  |  |                   |                              |                                      |  |
| $V_{OS}$                   | Input offset voltage                     | $V_{CM} = V_-$  | $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ | $\pm 0.3$  | $\pm 1.5$         | $\mu\text{V}$                | $\mu\text{V}$                        |  |
|                            |  |   |  |  | $\pm 1.75$        |                              |                                      |  |
| $dV_{OS}/dT$               | Input offset voltage drift               |   | $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ |  | $\pm 0.6$         |                              | $\mu\text{V}/^\circ\text{C}$         |  |
| PSRR                       | Input offset voltage versus power supply | $V_{CM} = V_-$ , $V_S = 4 \text{ V}$ to $40 \text{ V}$  | $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ | $\pm 0.1$  | $\pm 1.3$         | $\mu\text{V}/\text{V}$       | $\mu\text{V}/\text{V}$               |  |
|                            |  | $V_{CM} = V_-$ , $V_S = 2.7 \text{ V}$ to $40 \text{ V}$ <sup>(2)</sup>                                 |  | $\pm 0.75$   | $\pm 6.6$         |                              |                                      |  |
|                            | Channel separation                       | $f = 0 \text{ Hz}$  |  |  | 5                 |                              | $\mu\text{V}/\text{V}$               |  |
| <b>INPUT BIAS CURRENT</b>  |  |   |  |  |                   |                              |                                      |  |
| $I_B$                      | Input bias current                       |   |  |  | $\pm 10$          |                              | $\text{pA}$                          |  |
| $I_{os}$                   | Input offset current                     |   |  |  | $\pm 5$           |                              | $\text{pA}$                          |  |
| <b>NOISE</b>               |  |   |  |  |                   |                              |                                      |  |
| $E_N$                      | Input voltage noise                      | $f = 0.1 \text{ Hz}$ to $10 \text{ Hz}$   | $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ | 6  |                   | $\mu\text{V}_{PP}$           | $\mu\text{V}_{RMS}$                  |  |
|                            |  |   |  | 1  |                   |                              |                                      |  |
| $e_N$                      | Input voltage noise density              | $f = 1 \text{ kHz}$   | $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ | 30   |                   | $\text{nV}/\sqrt{\text{Hz}}$ | $\text{nV}/\sqrt{\text{Hz}}$         |  |
|                            |  | $f = 10 \text{ kHz}$  |  | 28   |                   |                              |                                      |  |
| $i_N$                      | Input current noise                      | $f = 1 \text{ kHz}$   |  |  | 2                 |                              | $\text{fA}/\sqrt{\text{Hz}}$         |  |
| <b>INPUT VOLTAGE RANGE</b> |  |   |  |  |                   |                              |                                      |  |
| $V_{CM}$                   | Common-mode voltage range                |   |  | $(V-) - 0.2$   | $(V+) + 0.2$      | $\text{V}$                   |                                      |  |
| CMRR                       | Common-mode rejection ratio              | $V_S = 40 \text{ V}$ , $(V-) - 0.1 \text{ V} < V_{CM} < (V+) - 2 \text{ V}$ (PMOS pair)                 | $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ | 100  | 115               | $\text{dB}$                  | $\text{dB}$                          |  |
|                            |  | $V_S = 4 \text{ V}$ , $(V-) - 0.1 \text{ V} < V_{CM} < (V+) - 2 \text{ V}$ (PMOS pair)                  |  | 75   | 90                |                              |                                      |  |
|                            |  | $V_S = 2.7 \text{ V}$ , $(V-) - 0.1 \text{ V} < V_{CM} < (V+) - 2 \text{ V}$ (PMOS pair) <sup>(2)</sup> |  | 70   | 90                |                              |                                      |  |
|                            |  | $V_S = 2.7 - 40 \text{ V}$ , $(V+) - 1 \text{ V} < V_{CM} < (V+) + 0.1 \text{ V}$ (NMOS pair)           |  |  | 80                |                              |                                      |  |
|                            |  | $(V+) - 2 \text{ V} < V_{CM} < (V+) - 1 \text{ V}$  |  | See <a href="#">Offset Voltage (Transition Region)</a> in the <i>Typical Characteristics</i> section |                   |                              |                                      |  |
| <b>INPUT CAPACITANCE</b>   |  |   |  |  |                   |                              |                                      |  |
| $Z_{ID}$                   | Differential                             |   |  |  | $540 \parallel 3$ |                              | $\text{G}\Omega \parallel \text{pF}$ |  |
| $Z_{ICM}$                  | Common-mode                              |   |  |  | 6 $\parallel$ 1   |                              | $\text{T}\Omega \parallel \text{pF}$ |  |

## 6.7 Electrical Characteristics (continued)

For  $V_S = (V+) - (V-) = 2.7 \text{ V to } 40 \text{ V}$  ( $\pm 1.35 \text{ V to } \pm 20 \text{ V}$ ) at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10 \text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

| PARAMETER                 | TEST CONDITIONS                   | MIN   | TYP  | MAX | UNIT       |
|---------------------------|-----------------------------------|---|--|-----|------------|
| <b>OPEN-LOOP GAIN</b>     |                                   |   |  |     |            |
| A <sub>OL</sub>           | Open-loop voltage gain            | $V_S = 40 \text{ V, } V_{CM} = V_S / 2, (V-) + 0.1 \text{ V} < V_O < (V+) - 0.1 \text{ V}$  | 120  | 145 | dB         |
|                           |                                   | $T_A = -40^\circ\text{C to } 125^\circ\text{C}$   |  | 142 |            |
|                           |                                   | $V_S = 4 \text{ V, } V_{CM} = V_S / 2, (V-) + 0.1 \text{ V} < V_O < (V+) - 0.1 \text{ V}$   | 104  | 130 |            |
|                           |                                   | $T_A = -40^\circ\text{C to } 125^\circ\text{C}$   |  | 125 |            |
| A <sub>OL</sub>           |                                   | $V_S = 2.7 \text{ V, } V_{CM} = V_S / 2, (V-) + 0.1 \text{ V} < V_O < (V+) - 0.1 \text{ V}$ | 101  | 118 | dB         |
|                           |                                   | $V^{(2)}$   |  | 117 |            |
| <b>FREQUENCY RESPONSE</b> |                                   |   |  |     |            |
| GBW                       | Gain-bandwidth product            |   | 1.1  |     | MHz        |
| SR                        | Slew rate                         | $V_S = 40 \text{ V, } G = +1, C_L = 20 \text{ pF}$  | 4.5  |     | V/ $\mu$ s |
| t <sub>S</sub>            | Settling time                     | To 0.1%, $V_S = 40 \text{ V, } V_{STEP} = 10 \text{ V, } G = +1, CL = 20 \text{ pF}$        | 4  |     | $\mu$ s    |
|                           |                                   | To 0.1%, $V_S = 40 \text{ V, } V_{STEP} = 2 \text{ V, } G = +1, CL = 20 \text{ pF}$         | 2  |     |            |
|                           |                                   | To 0.01%, $V_S = 40 \text{ V, } V_{STEP} = 10 \text{ V, } G = +1, CL = 20 \text{ pF}$       | 5  |     |            |
|                           |                                   | To 0.01%, $V_S = 40 \text{ V, } V_{STEP} = 2 \text{ V, } G = +1, CL = 20 \text{ pF}$        | 3  |     |            |
|                           | Phase margin                      | $G = +1, R_L = 10 \text{ k}\Omega, C_L = 20 \text{ pF}$                                     | 60   |     | °          |
|                           | Overload recovery time            | $V_{IN} \times \text{gain} > V_S$   | 600  |     | ns         |
| THD+N                     | Total harmonic distortion + noise | $V_S = 40 \text{ V, } V_O = 1 \text{ V}_{RMS}, G = 1, f = 1 \text{ kHz}$                    | 0.00162%   |     |            |
| <b>OUTPUT</b>             |                                   |   |  |     |            |
|                           | Voltage output swing from rail    | Positive and negative rail headroom   | $V_S = 40 \text{ V, } R_L = \text{no load}$  | 2   | mV         |
|                           |                                   |   | $V_S = 40 \text{ V, } R_L = 10 \text{ k}\Omega$  | 45  |            |
|                           |                                   |   | $V_S = 40 \text{ V, } R_L = 2 \text{ k}\Omega$   | 200 |            |
|                           |                                   |   | $V_S = 2.7 \text{ V, } R_L = \text{no load}$   | 1   |            |
|                           |                                   |   | $V_S = 2.7 \text{ V, } R_L = 10 \text{ k}\Omega$   | 5   |            |
|                           |                                   |   | $V_S = 2.7 \text{ V, } R_L = 2 \text{ k}\Omega$  | 25  |            |
| I <sub>SC</sub>           | Short-circuit current             |   | ±80  |     | mA         |
| C <sub>LOAD</sub>         | Capacitive load drive             |   | See <a href="#">Small-Signal Overshoot vs Capacitive Load</a> in the <a href="#">Typical Characteristics</a> section |     |            |
| Z <sub>O</sub>            | Open-loop output impedance        | $f = 1 \text{ MHz, } I_O = 0 \text{ A}$   | 575  |     | Ω          |

## 6.7 Electrical Characteristics (continued)

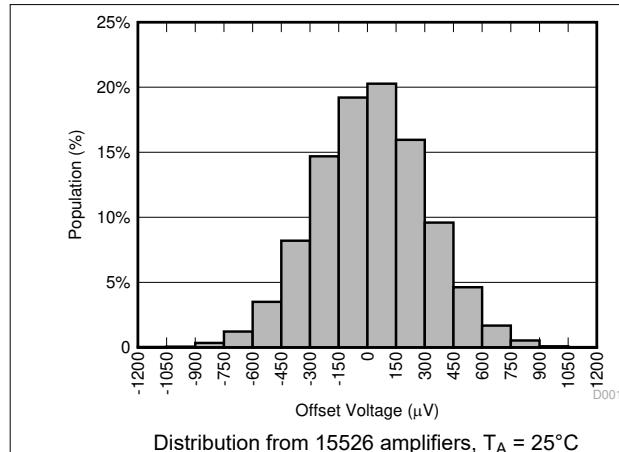
For  $V_S = (V+) - (V-) = 2.7 \text{ V to } 40 \text{ V} (\pm 1.35 \text{ V to } \pm 20 \text{ V})$  at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10 \text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

| PARAMETER           | TEST CONDITIONS  |  | MIN   | TYP           | MAX           | UNIT                          |
|---------------------|--|--|---|---------------|---------------|-------------------------------|
| <b>POWER SUPPLY</b> |  |  |   |               |               |                               |
| $I_Q$               | Quiescent current per amplifier  | OPA2990, OPA4990, $I_O = 0 \text{ A}$  |   | 120           | 150           | $\mu\text{A}$                 |
|                     |  |  | $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ |               | 160           |                               |
|                     | OPA990, $I_O = 0 \text{ A}$  |  |   | 130           | 170           |                               |
|                     |  |  | $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ |               | 175           |                               |
| Turn-on time        | At $T_A = 25^\circ\text{C}$ , $V_S = 40 \text{ V}$ , $V_S$ ramp rate $> 0.3 \text{ V}/\mu\text{s}$ |  |   | 40            |               | $\mu\text{s}$                 |
| <b>SHUTDOWN</b>     |  |  |   |               |               |                               |
| $I_{QSD}$           | Quiescent current per amplifier  | $V_S = 2.7 \text{ V to } 40 \text{ V}$ , all amplifiers disabled, $SHDN = V_- + 2 \text{ V}$   |   | 20            | 30            | $\mu\text{A}$                 |
| $Z_{SHDN}$          | Output impedance during shutdown   | $V_S = 2.7 \text{ V to } 40 \text{ V}$ , amplifier disabled, $SHDN = V_- + 2 \text{ V}$  |   | 10    12      |               | $\text{G}\Omega    \text{pF}$ |
| $V_{IH}$            | Logic high threshold voltage (amplifier disabled)  | For valid input high, the SHDN pin voltage should be greater than the maximum threshold but less than or equal to $(V_-) + 20 \text{ V}$ |   | $(V_-) + 0.8$ | $(V_-) + 1.1$ | $\text{V}$                    |
| $V_{IL}$            | Logic low threshold voltage (amplifier enabled)  | For valid input low, the SHDN pin voltage should be less than the minimum threshold but greater than or equal to $V_-$                   |   | $(V_-) + 0.2$ | $(V_-) + 0.8$ | $\text{V}$                    |
| $t_{ON}$            | Amplifier enable time <sup>(1)</sup>   | $G = +1$ , $V_{CM} = V_-$ , $V_O = 0.1 \times V_S / 2$   |   | 11            |               | $\mu\text{s}$                 |
| $t_{OFF}$           | Amplifier disable time <sup>(1)</sup>  | $V_{CM} = V_-$ , $V_O = V_S / 2$   |   | 2.5           |               | $\mu\text{s}$                 |
|                     | SHDN pin input bias current (per pin)  | $V_S = 2.7 \text{ V to } 40 \text{ V}$ , $(V_-) + 20 \text{ V} \geq SHDN \geq (V_-) + 0.9 \text{ V}$                                     |   | 500           |               | $\text{nA}$                   |
|                     |  | $V_S = 2.7 \text{ V to } 40 \text{ V}$ , $(V_-) \leq SHDN \leq (V_-) + 0.7 \text{ V}$  |   | 150           |               |                               |

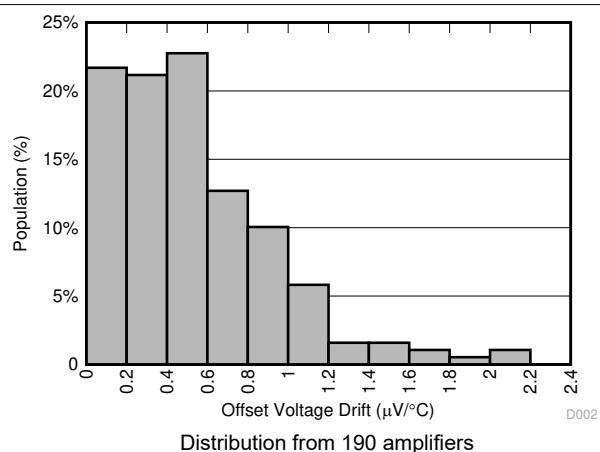
(1) Disable time ( $t_{OFF}$ ) and enable time ( $t_{ON}$ ) are defined as the time interval between the 50% point of the signal applied to the SHDN pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.  
 (2) Specified by characterization only.

## 6.8 Typical Characteristics

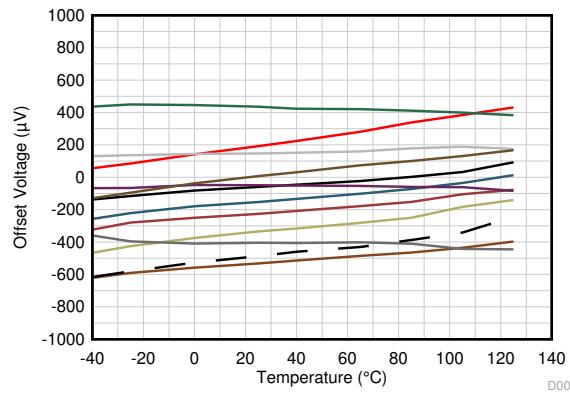
at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 20\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 10\text{ pF}$  (unless otherwise noted)



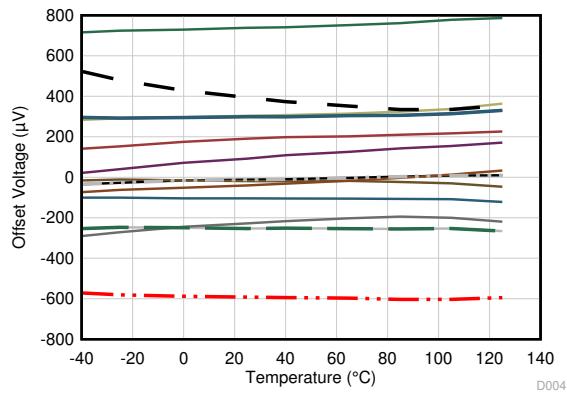
**Figure 6-1. Offset Voltage Production Distribution**



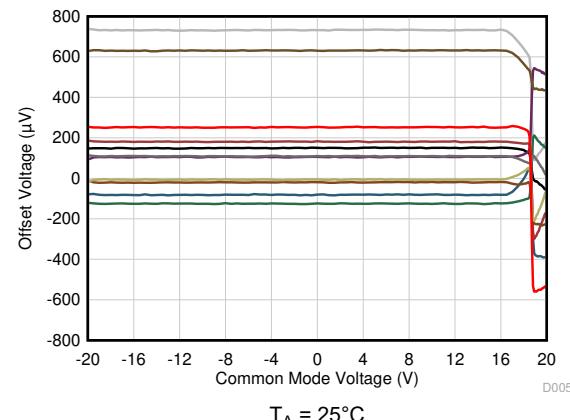
**Figure 6-2. Offset Voltage Drift Distribution**



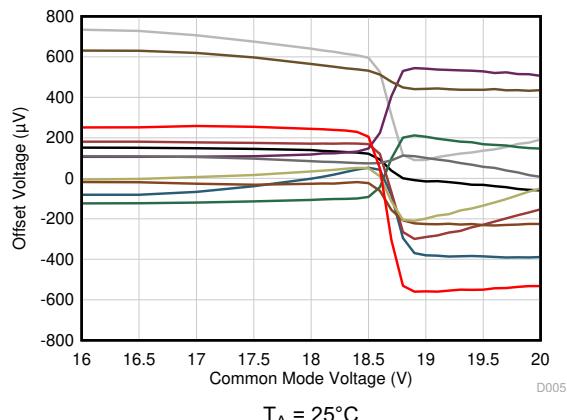
**Figure 6-3. Offset Voltage vs Temperature**



**Figure 6-4. Offset Voltage vs Temperature**



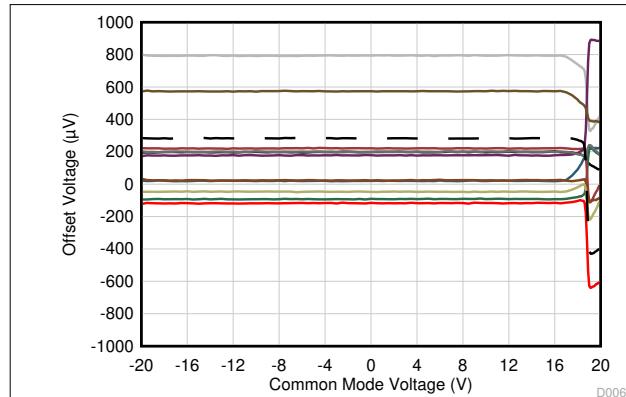
**Figure 6-5. Offset Voltage vs Common-Mode Voltage**



**Figure 6-6. Offset Voltage vs Common-Mode Voltage (Transition Region)**

## 6.8 Typical Characteristics (continued)

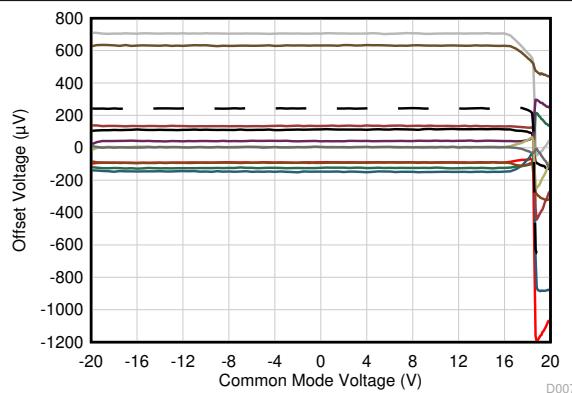
at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 20\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 10\text{ pF}$  (unless otherwise noted)



$T_A = 125^\circ\text{C}$

Each color represents one sample device.

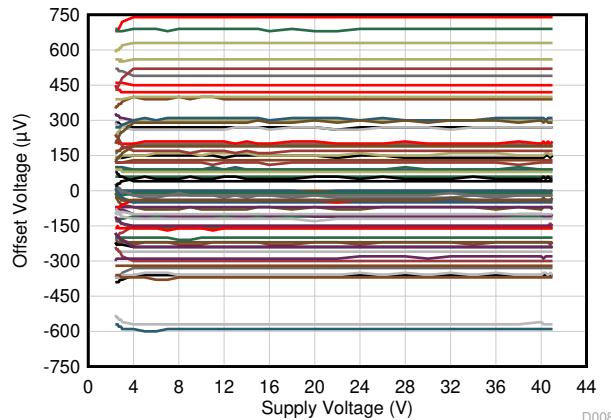
Figure 6-7. Offset Voltage vs Common-Mode Voltage



$T_A = -40^\circ\text{C}$

Each color represents one sample device.

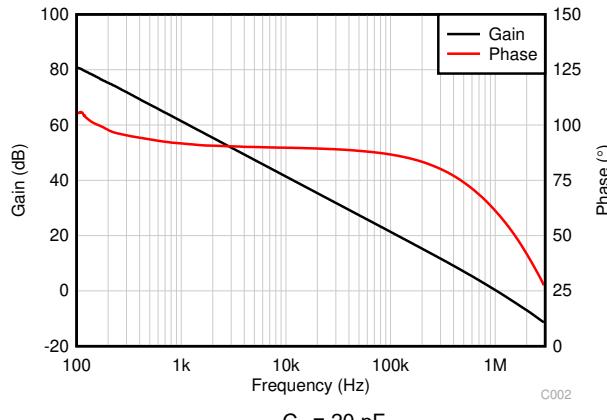
Figure 6-8. Offset Voltage vs Common-Mode Voltage



$V_{CM} = V_-$

Each color represents one sample device.

Figure 6-9. Offset Voltage vs Power Supply



$C_L = 20\text{ pF}$

Figure 6-10. Open-Loop Gain and Phase vs Frequency

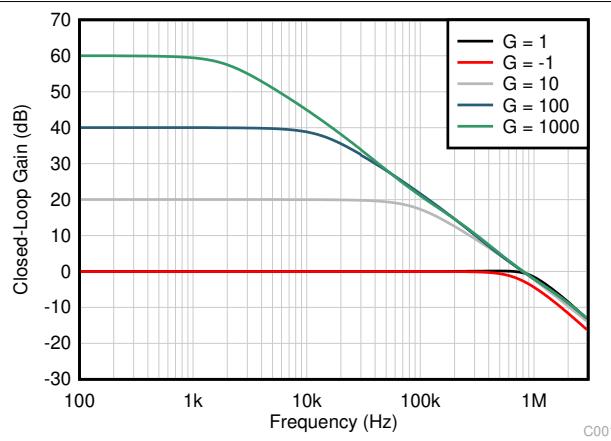


Figure 6-11. Closed-Loop Gain vs Frequency

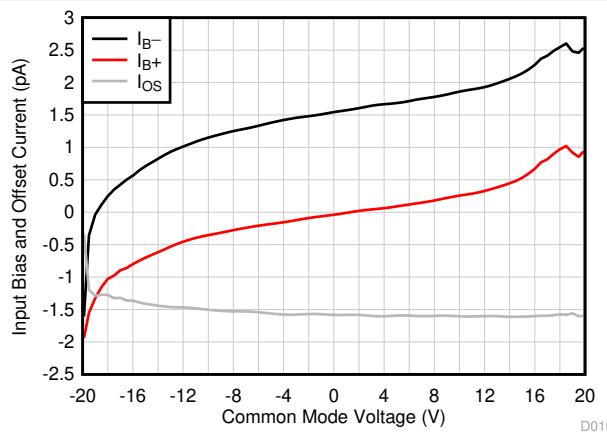


Figure 6-12. Input Bias Current vs Common-Mode Voltage

## 6.8 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 20\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 10\text{ pF}$  (unless otherwise noted)

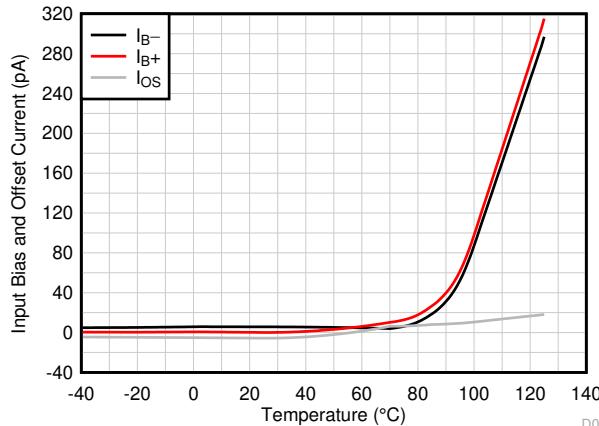


Figure 6-13. Input Bias Current vs Temperature

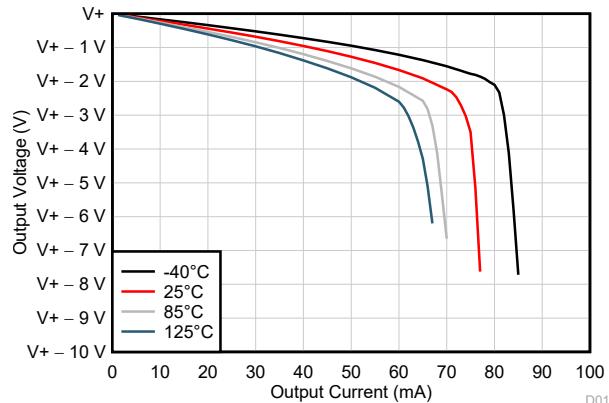


Figure 6-14. Output Voltage Swing vs Output Current (Sourcing)

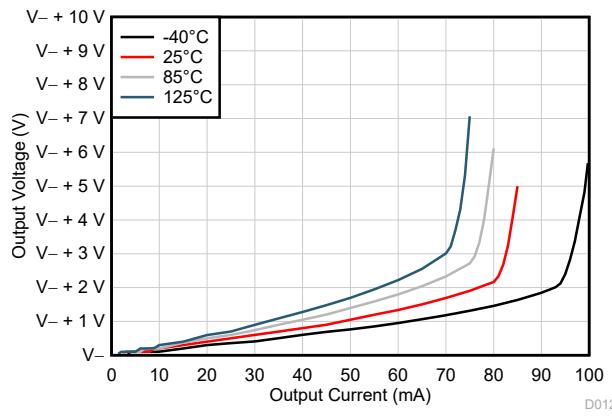


Figure 6-15. Output Voltage Swing vs Output Current (Sinking)

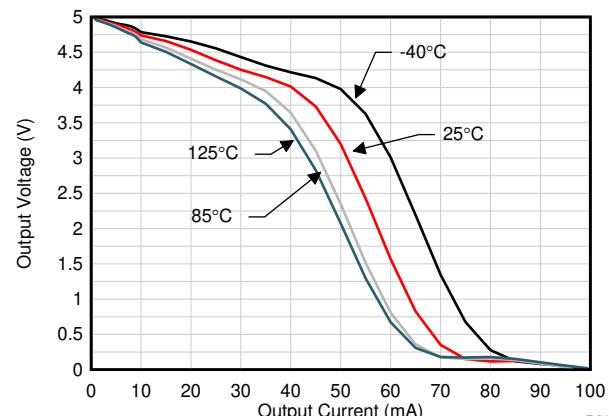


Figure 6-16. Output Voltage Swing vs Output Current (Sourcing)

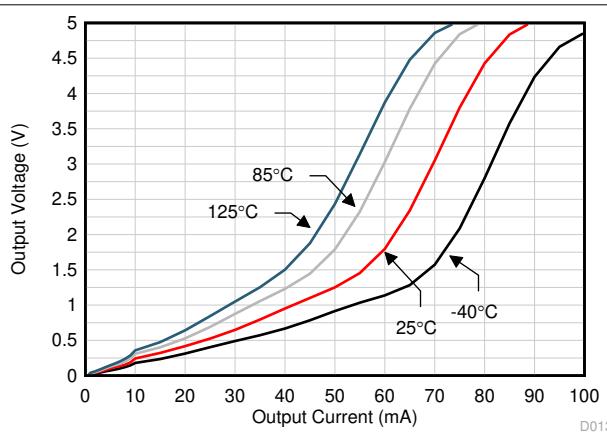


Figure 6-17. Output Voltage Swing vs Output Current (Sinking)

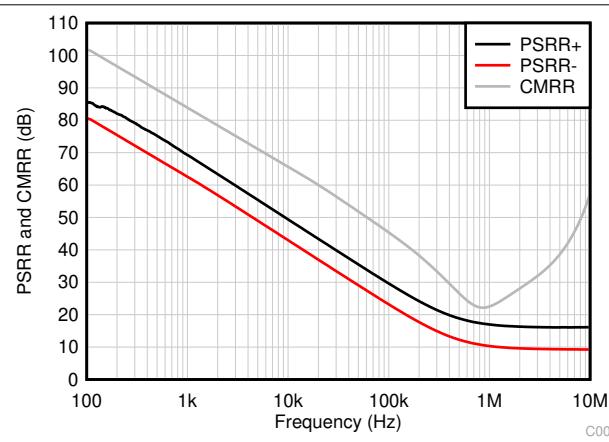
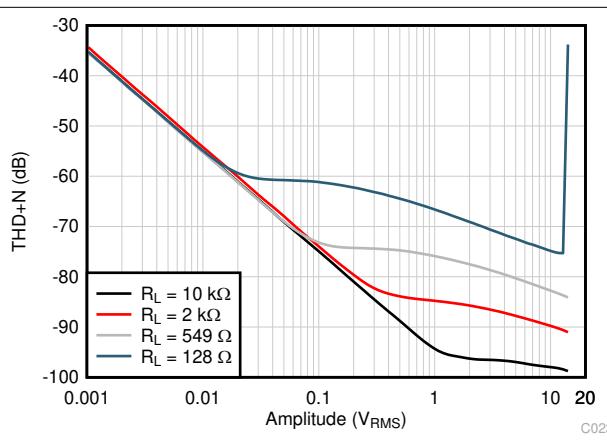
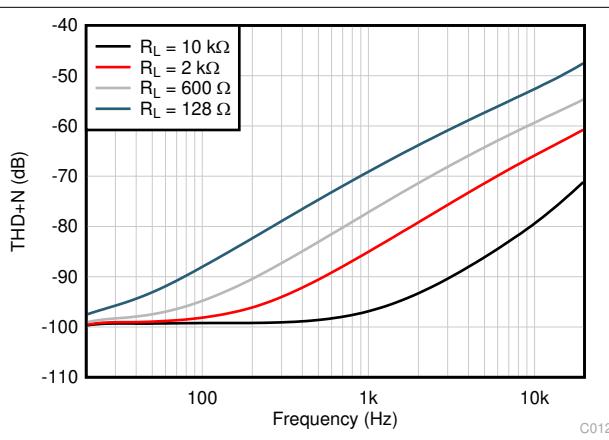
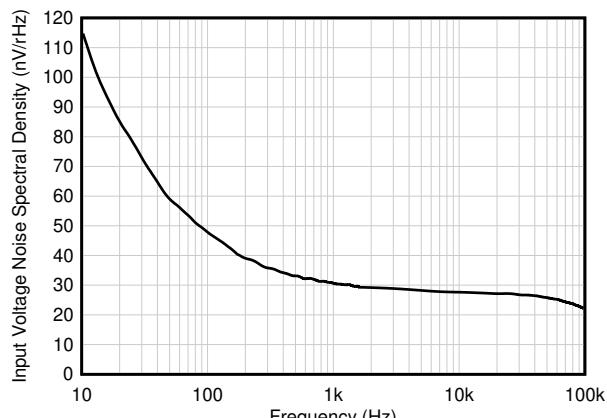
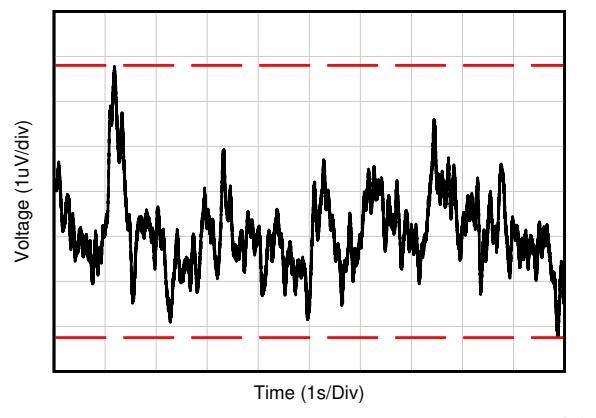
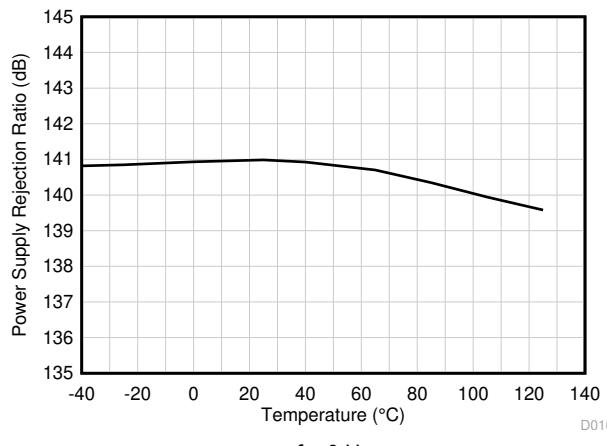
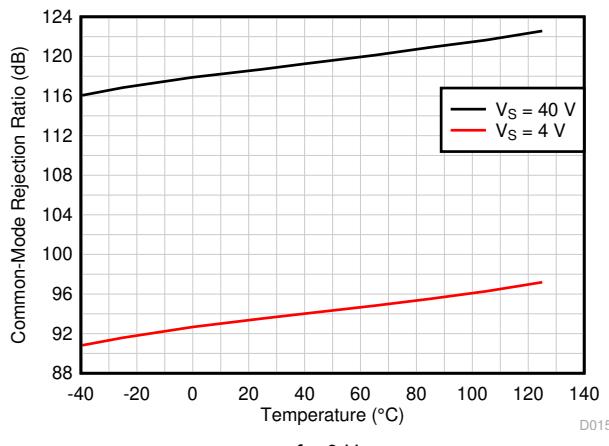


Figure 6-18. CMRR and PSRR vs Frequency

## 6.8 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 20\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 10\text{ pF}$  (unless otherwise noted)



## 6.8 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 20\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 10\text{ pF}$  (unless otherwise noted)

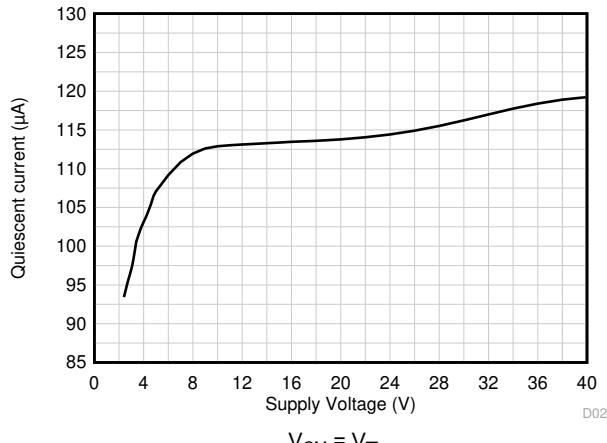


Figure 6-25. Quiescent Current vs Supply Voltage

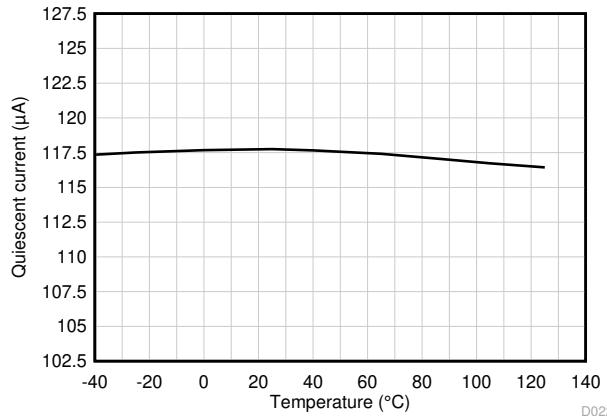


Figure 6-26. Quiescent Current vs Temperature

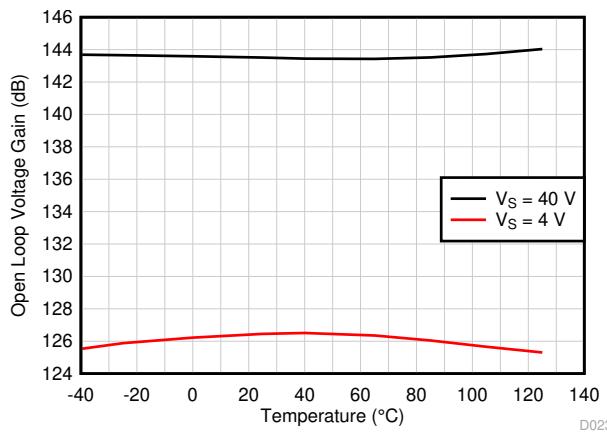


Figure 6-27. Open-Loop Voltage Gain vs Temperature (dB)

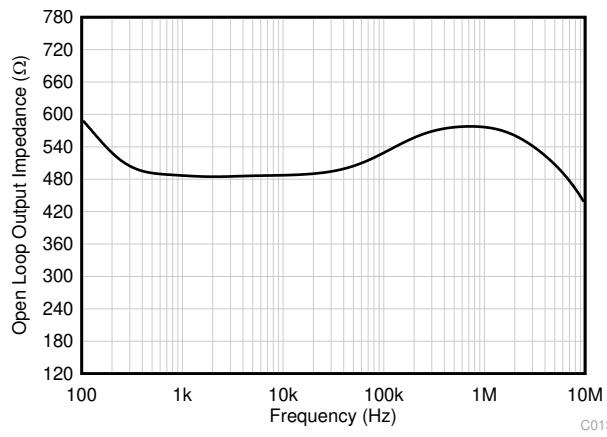


Figure 6-28. Open-Loop Output Impedance vs Frequency

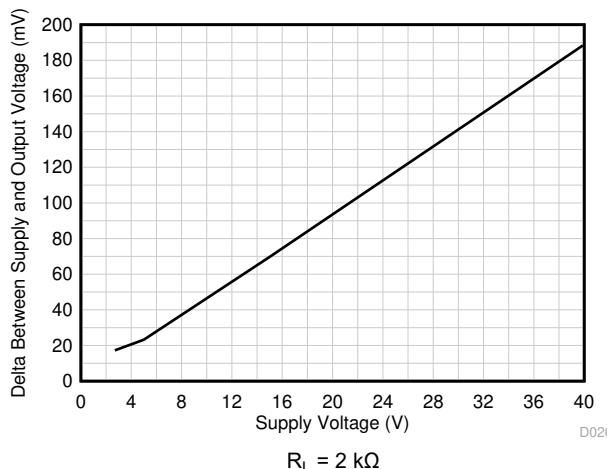


Figure 6-29. Output Swing vs Supply Voltage, Positive Swing

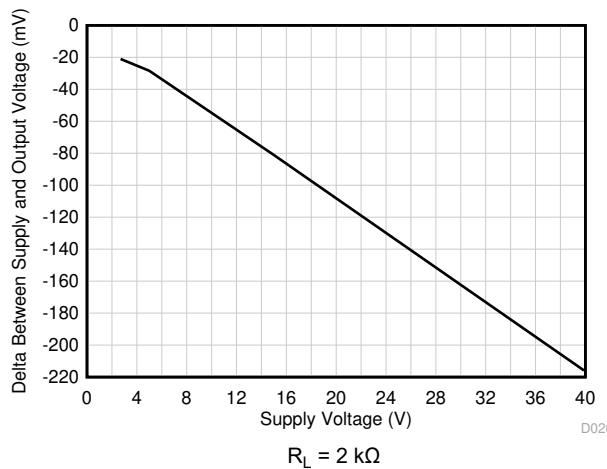


Figure 6-30. Output Swing vs Supply Voltage, Negative Swing

## 6.8 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 20\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 10\text{ pF}$  (unless otherwise noted)

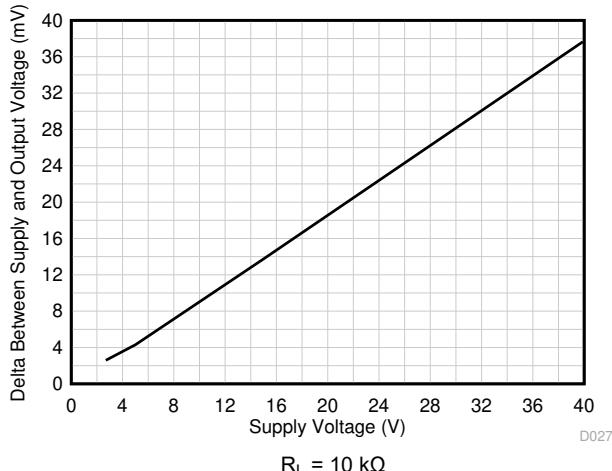


Figure 6-31. Output Swing vs Supply Voltage, Positive Swing

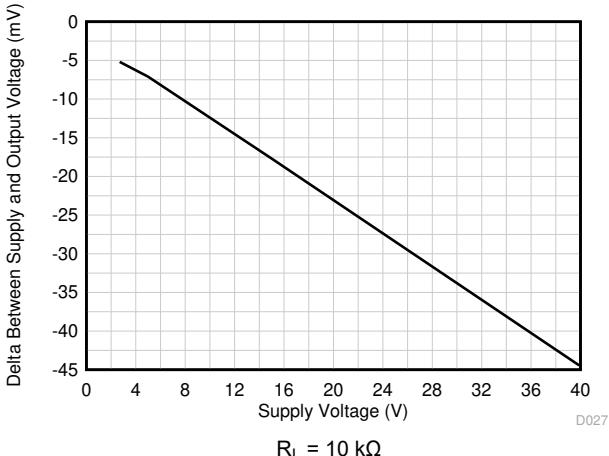


Figure 6-32. Output Swing vs Supply Voltage, Negative Swing

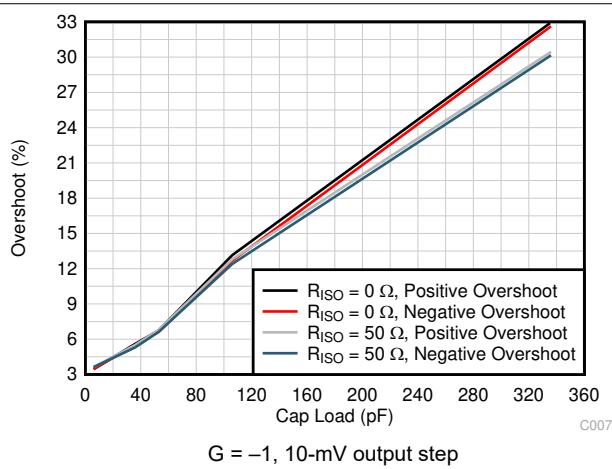


Figure 6-33. Small-Signal Overshoot vs Capacitive Load

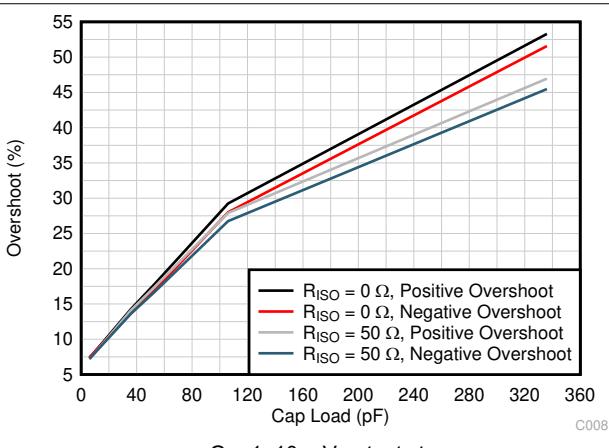


Figure 6-34. Small-Signal Overshoot vs Capacitive Load

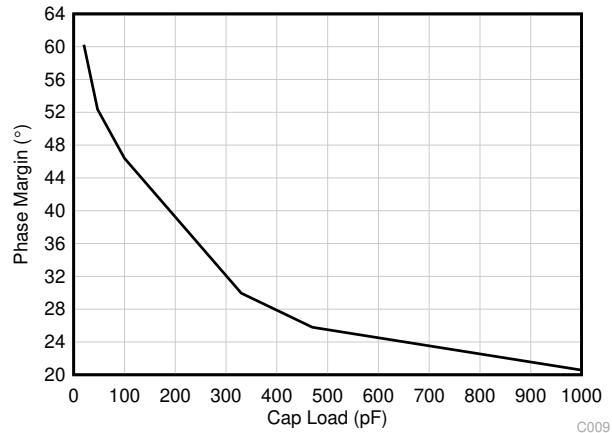
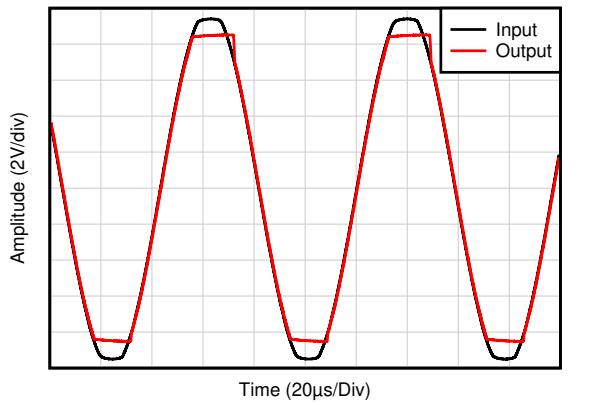


Figure 6-35. Phase Margin vs Capacitive Load



$V_{IN} = \pm 20\text{ V}$ ;  $V_S = V_{OUT} = \pm 17\text{ V}$

Figure 6-36. No Phase Reversal

## 6.8 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 20\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 10\text{ pF}$  (unless otherwise noted)

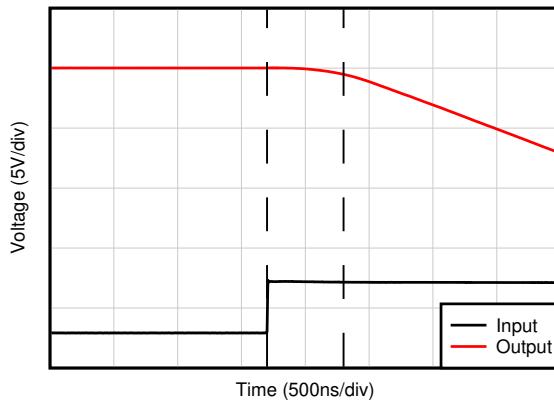


Figure 6-37. Positive Overload Recovery

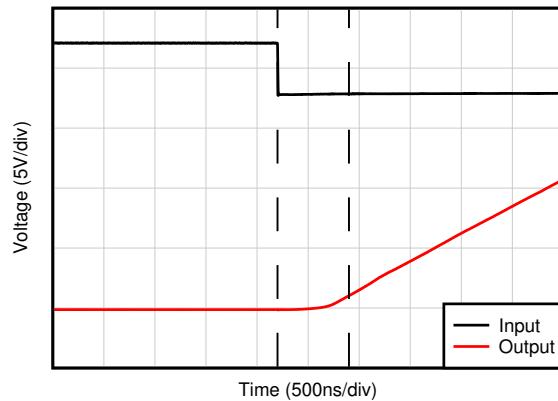
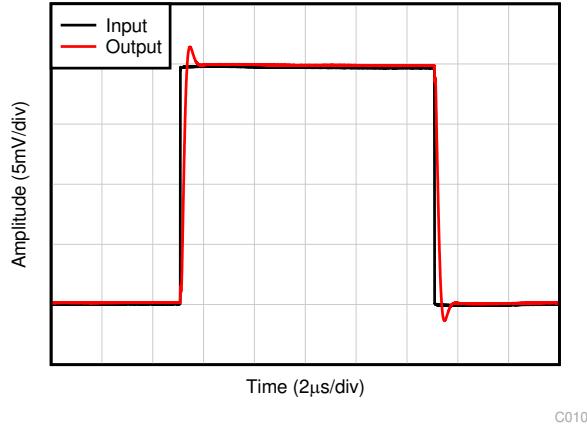
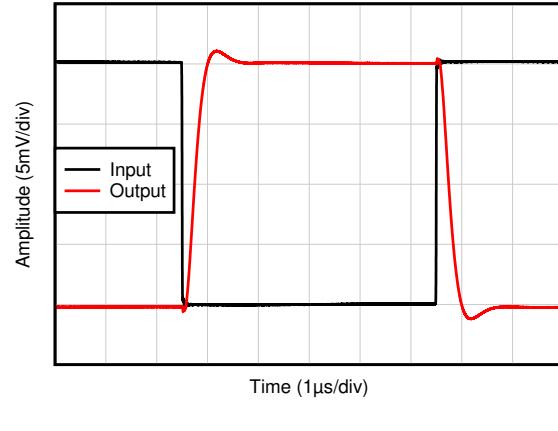


Figure 6-38. Negative Overload Recovery



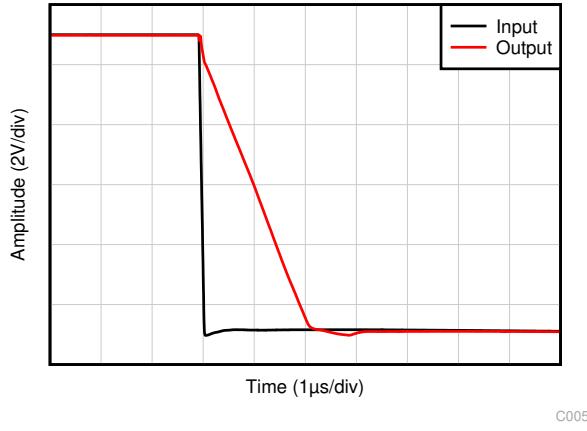
$C_L = 20\text{ pF}$ ,  $G = 1$ , 20-mV step response

Figure 6-39. Small-Signal Step Response



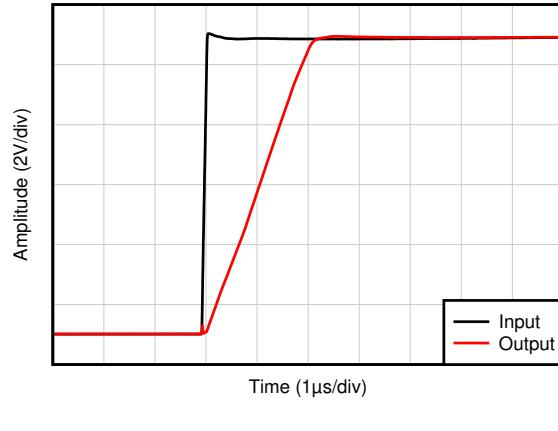
$C_L = 20\text{ pF}$ ,  $G = -1$ , 20-mV step response

Figure 6-40. Small-Signal Step Response



$C_L = 20\text{ pF}$ ,  $G = 1$

Figure 6-41. Large-Signal Step Response (Falling)



$C_L = 20\text{ pF}$ ,  $G = 1$

Figure 6-42. Large-Signal Step Response (Rising)

## 6.8 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 20\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 10\text{ pF}$  (unless otherwise noted)

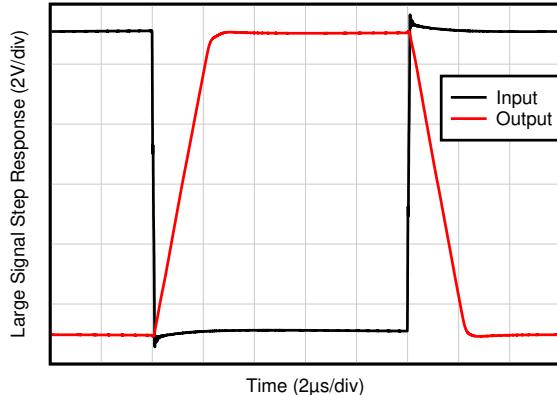


Figure 6-43. Large-Signal Step Response

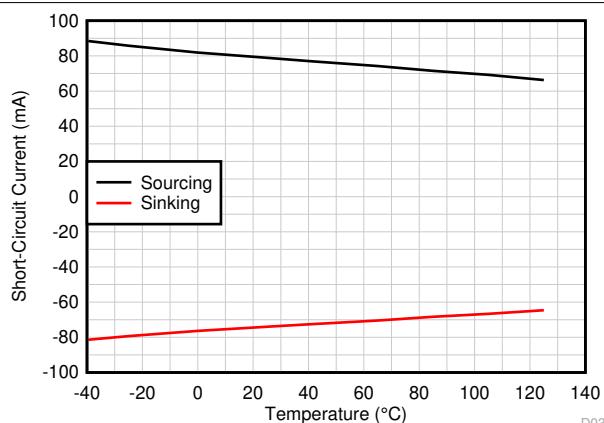


Figure 6-44. Short-Circuit Current vs Temperature

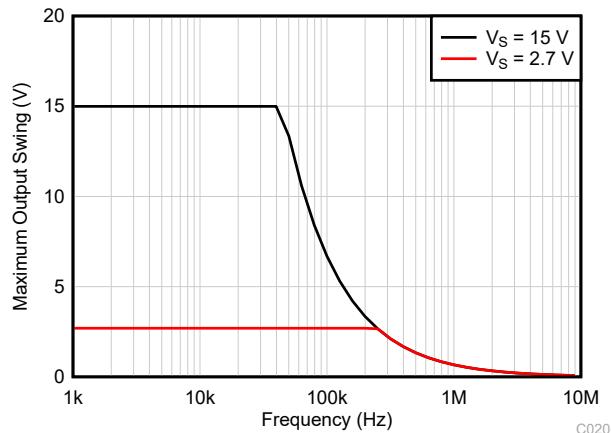


Figure 6-45. Maximum Output Voltage vs Frequency

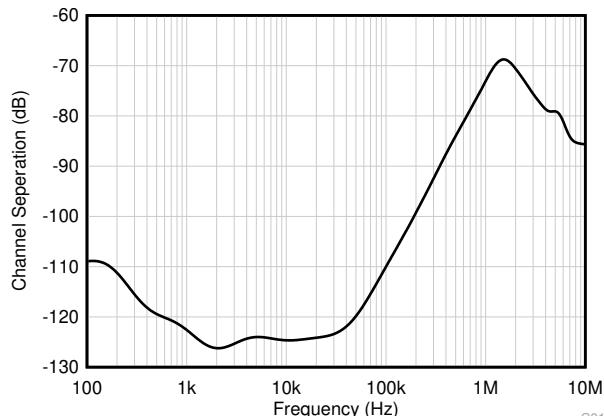


Figure 6-46. Channel Separation vs Frequency

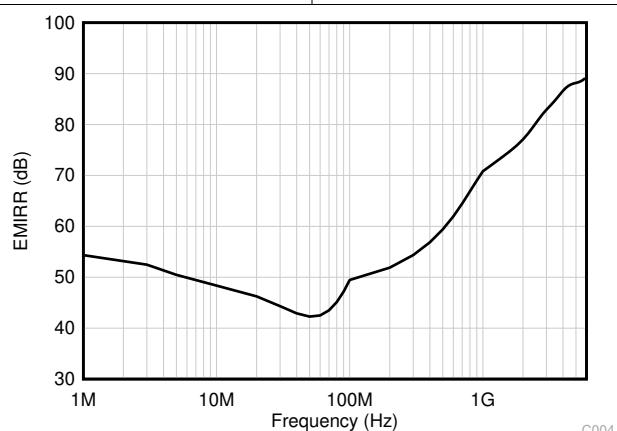


Figure 6-47. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

## 7 Detailed Description

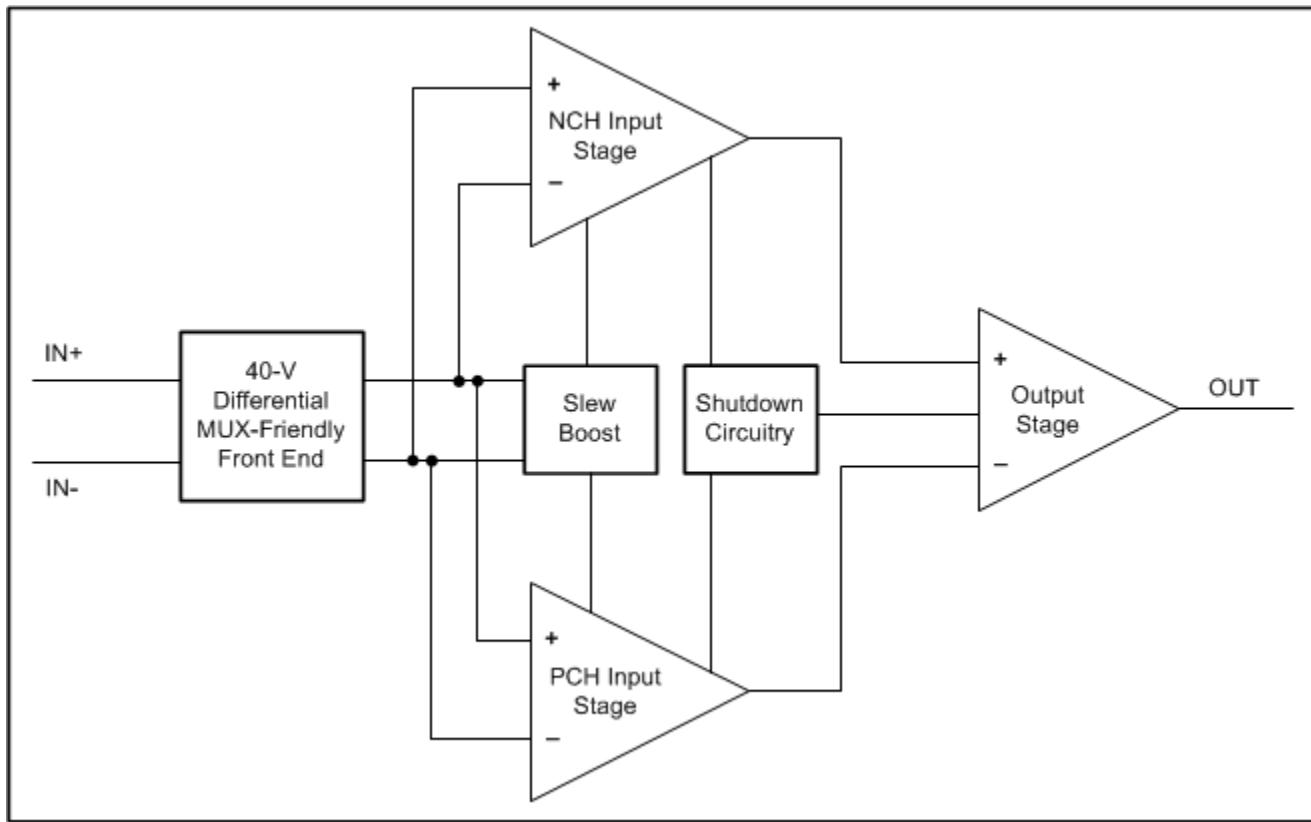
### 7.1 Overview

The OPAX990 family (OPA990, OPA2990, and OPA4990) is a family of high voltage (40-V) general purpose operational amplifiers.

These devices offer excellent DC precision and AC performance, including rail-to-rail input/output, low offset ( $\pm 300 \mu\text{V}$ , typ), and low offset drift ( $\pm 0.6 \mu\text{V}/^\circ\text{C}$ , typ).

Unique features such as differential and common-mode input voltage range to the supply rail, high short-circuit current ( $\pm 80 \text{ mA}$ ), high slew rate (4.5 V/ $\mu\text{s}$ ), and shutdown make the OPAX990 an extremely flexible, robust, and high-performance operational amplifier for high-voltage industrial applications.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Input Protection Circuitry

The OPAX990 uses a unique input architecture to eliminate the requirement for input protection diodes but still provides robust input protection under transient conditions. Figure 7-1 shows conventional input diode protection schemes that are activated by fast transient step responses and introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 7-2. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current and resulting in extended settling time.

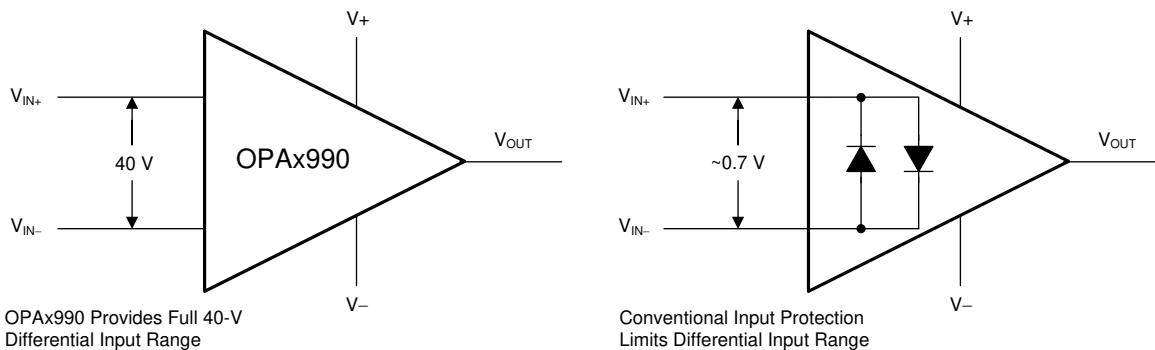


Figure 7-1. OPAX990 Input Protection Does Not Limit Differential Input Capability

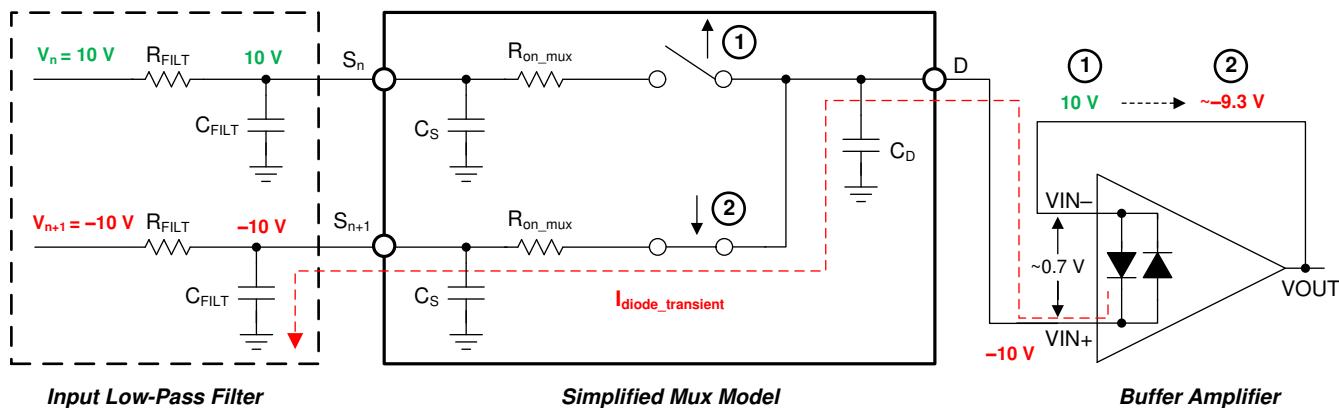


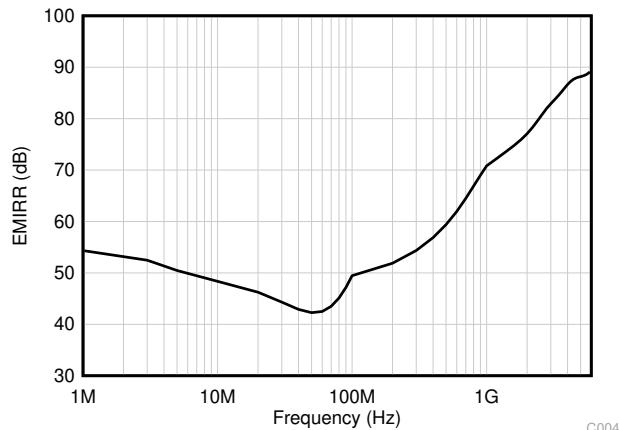
Figure 7-2. Back-to-Back Diodes Create Settling Issues

The OPAX990 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications using a patented input protection architecture that does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The OPAX990 tolerates a maximum differential swing (voltage between inverting and non-inverting pins of the op amp) of up to 40 V, making the device suitable for use as a comparator or in applications with fast-ramping input signals such as data-acquisition systems; see the TI TechNote [MUX-Friendly Precision Operational Amplifiers](#) for more information.

### 7.3.2 EMI Rejection

The OPAX990 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAX990 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 7-3 shows the results of this testing on the OPAX990. Table 7-1 shows the EMIRR IN+ values for the OPAX990 at particular frequencies commonly encountered in real-world applications. The [EMI Rejection Ratio of Operational](#)

*Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from [www.ti.com](http://www.ti.com).



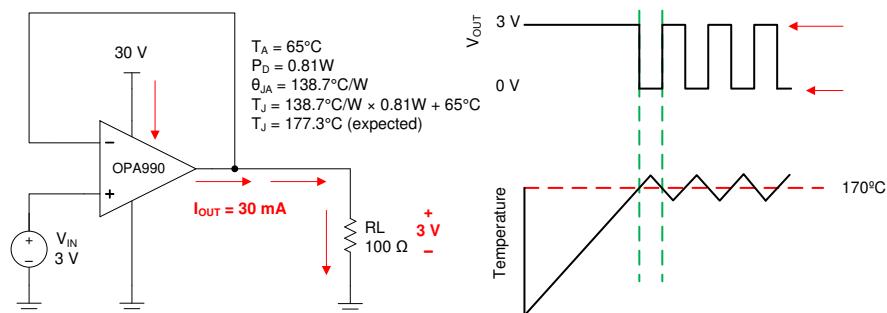
**Figure 7-3. EMIRR Testing**

**Table 7-1. OPA990 EMIRR IN+ For Frequencies of Interest**

| FREQUENCY | APPLICATION OR ALLOCATION  | EMIRR IN+ |
|-----------|--|-----------|
| 400 MHz   | Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications   | 59.5 dB   |
| 900 MHz   | Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications                        | 68.9 dB   |
| 1.8 GHz   | GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)  | 77.8 dB   |
| 2.4 GHz   | 802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz) | 78.0 dB   |
| 3.6 GHz   | Radiolocation, aero communication and navigation, satellite, mobile, S-band  | 88.8 dB   |
| 5 GHz     | 802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)  | 87.6 dB   |

### 7.3.3 Thermal Protection

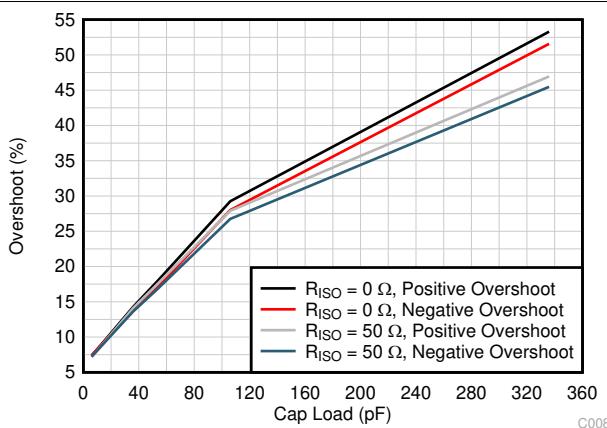
The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the OPAx990 is 150°C. Exceeding this temperature causes damage to the device. The OPAx990 has a thermal protection feature that reduces damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 170°C. Figure 7-4 shows an application example for the OPA990 that has significant self heating because of its power dissipation (0.81 W). Thermal calculations indicate that for an ambient temperature of 65°C, the device junction temperature must reach 177°C. The actual device, however, turns off the output drive to recover towards a safe junction temperature. Figure 7-4 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3 V. When self heating causes the device junction temperature to increase above the internal limit, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor  $R_L$ . If the condition that caused excessive power dissipation is not removed, the amplifier will oscillate between a shutdown and enabled state until the output fault is corrected.



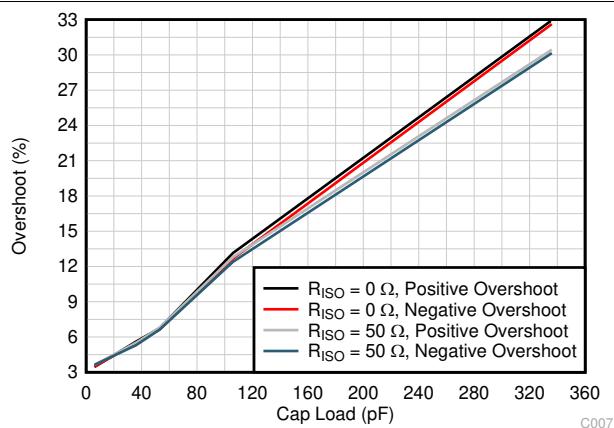
**Figure 7-4. Thermal Protection**

### 7.3.4 Capacitive Load and Stability

The OPAx990 features a resistive output stage capable of driving moderate capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive large capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see Figure 7-5 and Figure 7-6. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.



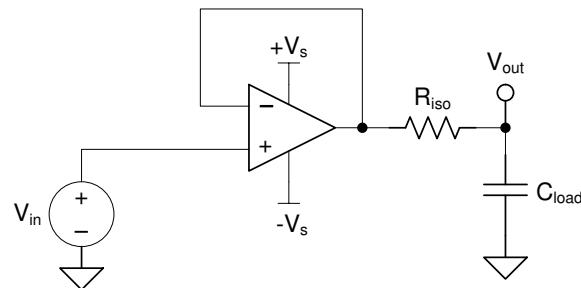
**Figure 7-5. Small-Signal Overshoot vs Capacitive Load (10-mV Output Step, G = 1)**



**Figure 7-6. Small-Signal Overshoot vs Capacitive Load (10-mV Output Step, G = -1)**

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small resistor,  $R_{ISO}$ , in series with the output, as shown in Figure 7-7. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the

capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio  $R_{ISO} / R_L$ , and is generally negligible at low output levels. A high capacitive load drive makes the OPAX990 well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in [Figure 7-7](#) uses an isolation resistor,  $R_{ISO}$ , to stabilize the output of an op amp.  $R_{ISO}$  modifies the open-loop gain of the system for increased phase margin.



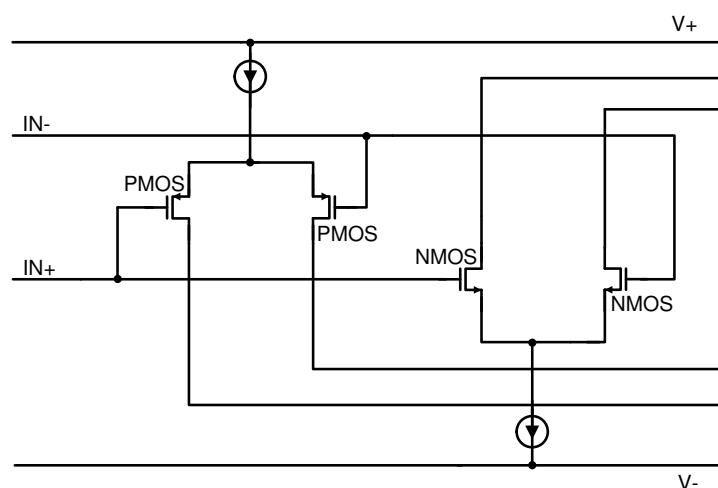
**Figure 7-7. Extending Capacitive Load Drive With the OPA990**

### 7.3.5 Common-Mode Voltage Range

The OPAx990 is a 40-V, true rail-to-rail input operational amplifier with an input common-mode range that extends 200 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in [Figure 7-8](#). The N-channel pair is active for input voltages close to the positive rail, typically  $(V_+) - 1$  V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately  $(V_+) - 2$  V. There is a small transition region, typically  $(V_+) - 2$  V to  $(V_+) - 1$  V in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

[Figure 6-5](#) shows this transition region for a typical device in terms of input voltage offset in more detail.

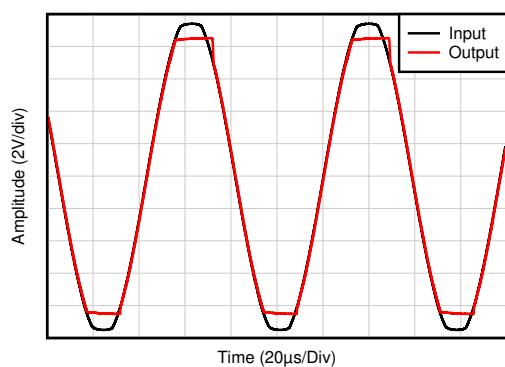
For more information on common-mode voltage range and PMOS/NMOS pair interaction, see [Op Amps With Complementary-Pair Input Stages](#) application note.



**Figure 7-8. Rail-to-Rail Input Stage**

### 7.3.6 Phase Reversal Protection

The OPAx990 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx990 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in [Figure 7-9](#). For more information on phase reversal, see [Op Amps With Complementary-Pair Input Stages](#) application note.



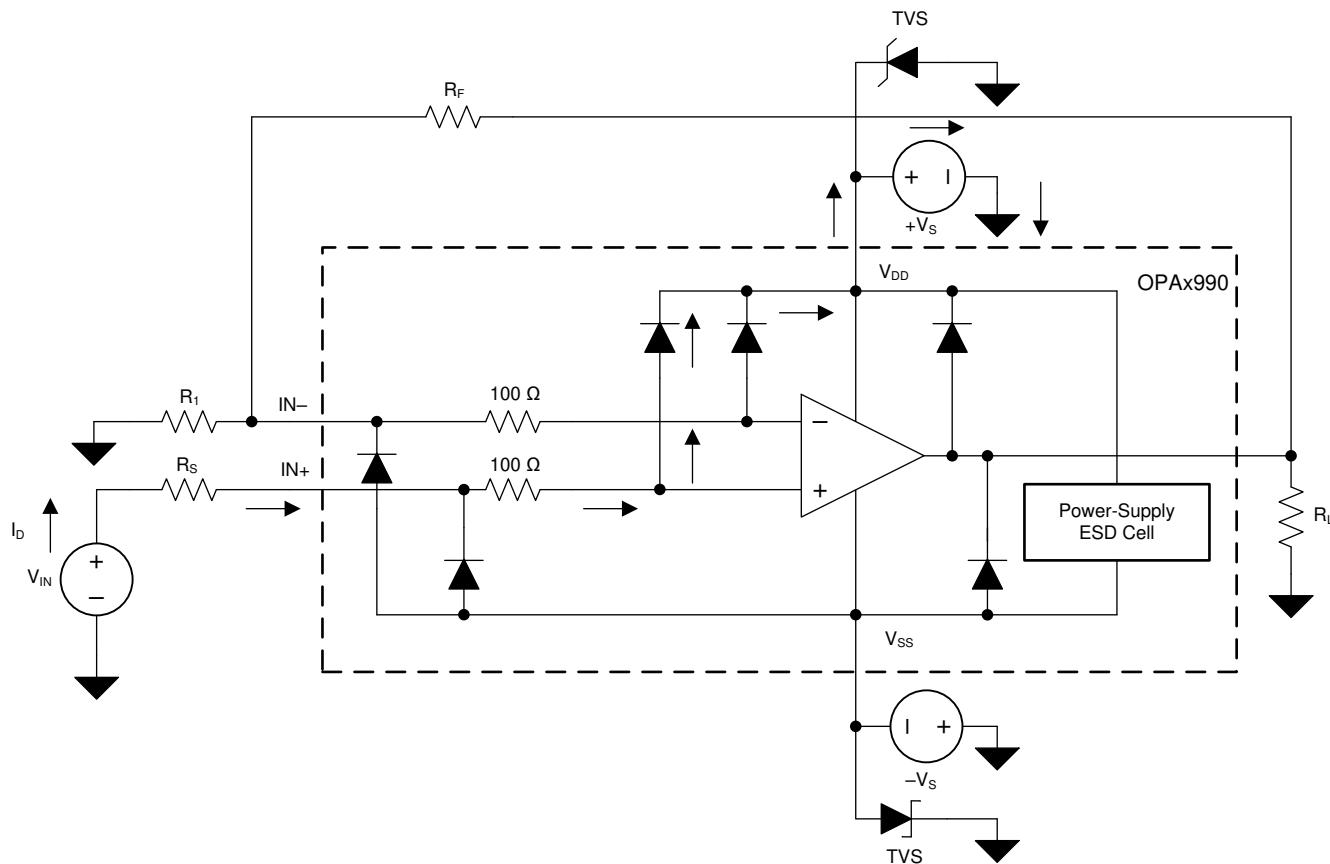
C016

**Figure 7-9. No Phase Reversal**

### 7.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 7-10 shows an illustration of the ESD circuits contained in the OPAX990 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.



**Figure 7-10. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application**

An ESD event is very short in duration and very high voltage (for example; 1 kV, 100 ns), whereas an EOS event is long duration and lower voltage (for example; 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

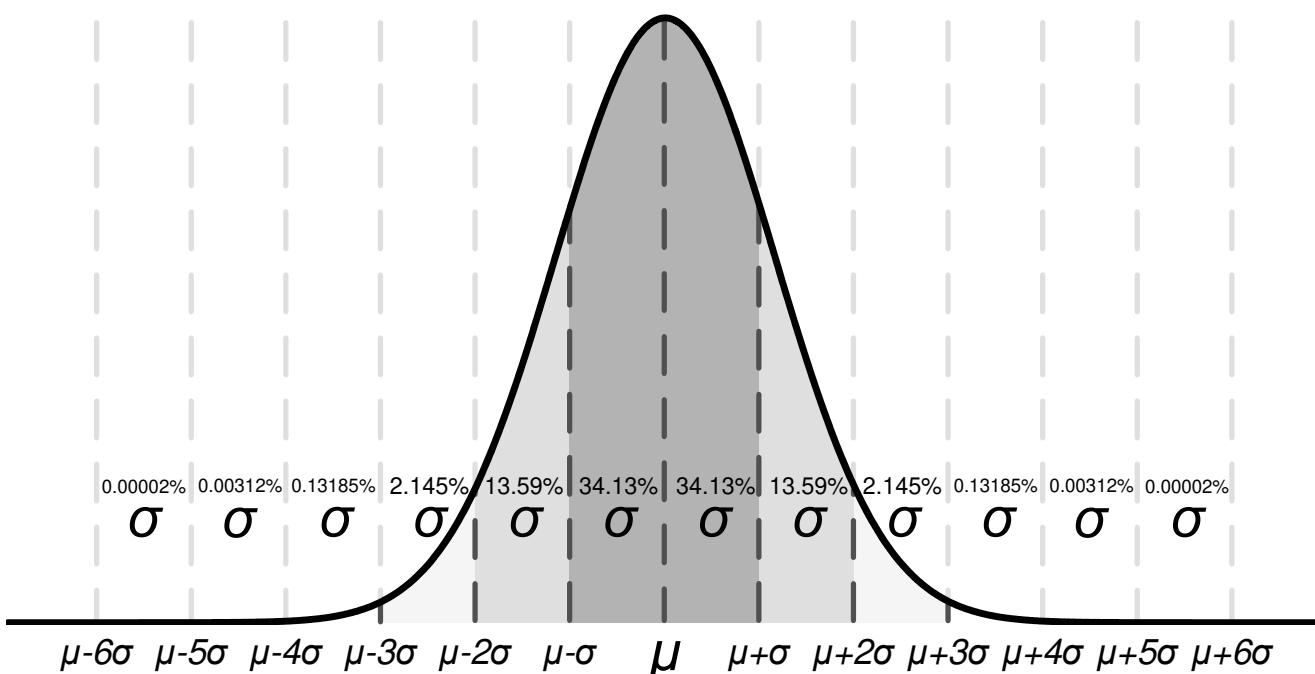
Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

### 7.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAX990 is approximately 600 ns.

### 7.3.9 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier in order to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier will exhibit some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian* ("bell curve"), or *normal* distributions, and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in the *Electrical Characteristics* table.



**Figure 7-11. Ideal Gaussian Distribution**

Figure 7-11 shows an example distribution, where  $\mu$ , or *mu*, is the mean of the distribution, and where  $\sigma$ , or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from  $\mu-\sigma$  to  $\mu+\sigma$ ).

Depending on the specification, values listed in the *typical* column of the *Electrical Characteristics* table are represented in different ways. As a general rule of thumb, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean ( $\mu$ ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation ( $\mu + \sigma$ ) in order to most accurately represent the typical value.

You can use this chart to calculate approximate probability of a specification in a unit; for example, for OPAX990, the typical input voltage offset is 300  $\mu$ V, so 68.2% of all OPAX990 devices are expected to have an offset from

–300  $\mu$ V to +300  $\mu$ V. At 4  $\sigma$  ( $\pm 1200 \mu$ V), 99.9937% of the distribution has an offset voltage less than  $\pm 1200 \mu$ V, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are assured by TI, and units outside these limits will be removed from production material. For example, the OPAX990 family has a maximum offset voltage of 1.5 mV at 25°C, and even though this corresponds to 5  $\sigma$  ( $\approx 1$  in 1.7 million units), which is extremely unlikely, TI assures that any unit with larger offset than 1.5 mV will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for your application, and design worst-case conditions using this value. For example, the 6 $\sigma$  value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and could be an option as a wide guardband to design a system around. In this case, the OPAX990 family does not have a maximum or minimum for offset voltage drift, but based on [Figure 6-2](#) and the typical value of 0.6  $\mu$ V/°C in the [Electrical Characteristics](#) table, it can be calculated that the 6- $\sigma$  value for offset voltage drift is about 3.6  $\mu$ V/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should be used only to estimate the performance of a device.

### 7.3.10 Packages With an Exposed Thermal Pad

The OPAX990 family is available in packages such as the WSON-8 (DSG) and WQFN-16 (RTE) which feature an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must either be connected to V– or left floating. Attaching the thermal pad to a potential other than V– is not allowed, and performance of the device is not assured when doing so.

### 7.3.11 Shutdown

The OPAX990S devices feature one or more shutdown pins (SHDN) that disable the op amp, placing it into a low-power standby mode. In this mode, the op amp typically consumes about 20  $\mu$ A. The SHDN pins are active high, meaning that shutdown mode is enabled when the input to the SHDN pin is a valid logic high. The amplifier is enabled when the input to the SHDN pin is a valid logic low.

The SHDN pins are referenced to the negative supply rail of the op amp. The threshold of the shutdown feature lies around 800 mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure optimal shutdown behavior, the SHDN pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V– and V– + 0.2 V. A valid logic high is defined as a voltage between V– + 1.1 V and V– + 20 V. The shutdown pin circuitry includes a pull-down resistor, which will inherently pull the voltage of the pin to the negative supply rail if not driven. Thus, to enable the amplifier, the SHDN pins should either be left floating or driven to a valid logic low. To disable the amplifier, the SHDN pins must be driven to a valid logic high. The maximum voltage allowed at the SHDN pins is V– + 20 V or V+, whichever is lower. Exceeding V– + 20V or V+, whichever is lower, will damage the device.

The SHDN pins are high-impedance CMOS inputs. Channels of single and dual op amp packages are independently controlled, and channels of quad op amp packages are controlled in pairs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The typical enable time out of shutdown is 11  $\mu$ s; disable time is 2.5  $\mu$ s. When disabled, the output assumes a high-impedance state. This architecture allows the OPAX990S family to operate as a gated amplifier, multiplexer, or programmable-gain amplifier. Shutdown time ( $t_{OFF}$ ) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 10-k $\Omega$  load to midsupply (VS / 2) is required. If using the OPAX990S without a load, the resulting turnoff time significantly increases.

## 7.4 Device Functional Modes

The OPAX990 has a single functional mode and is operational when the power-supply voltage is greater than or equal to 2.7 V ( $\pm 1.35$  V). The maximum power supply voltage for the OPAX990 is 40 V ( $\pm 20$  V).

The OPAX990S devices feature a shutdown pin, which can be used to place the op amp into a low-power mode. See [Shutdown](#) section for more information.

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The OPAx990 family offers excellent DC precision and AC performance. These devices operate up to 40-V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 1.1-MHz bandwidth and high output drive. These features make the OPAx990 a robust, high-performance operational amplifier for high-voltage industrial applications.

### 8.2 Typical Applications

#### 8.2.1 High Voltage Buffered Multiplexer

The OPAx990S shutdown devices can be configured to create a high voltage, buffered multiplexer. Outputs can be connected together on a common bus and the shutdown pins can be used to select the desired channel to pass through. Since the amplifier circuitry has been designed such that disable transitions occur significantly faster than enable transitions, the amplifier naturally exhibits a "break before make" switch topology. Amplifier outputs enter a high impedance state when placed in shutdown, so there is no risk of bus contention when connecting multiple channel outputs together. Additionally, because outputs are isolated from inputs, there is no concern about the impedance at the input of each channel interacting undesirably with the impedance at the output, like an amplifier gain stage or ADC driver circuit. Also, because this topology uses amplifiers instead of MOSFET switches, other common issues with multiplexers such as charge injection or signal error due to  $R_{ON}$  effects are eliminated.

Figure 8-1 shows an example topology for a basic 2:1 multiplexer. When SEL is low, channel 1 is selected and active; when SEL is high, channel 2 is selected and active. For more information on how to use the OPAx990S shutdown function, see the shutdown section in the [Electrical Characteristics](#) table.

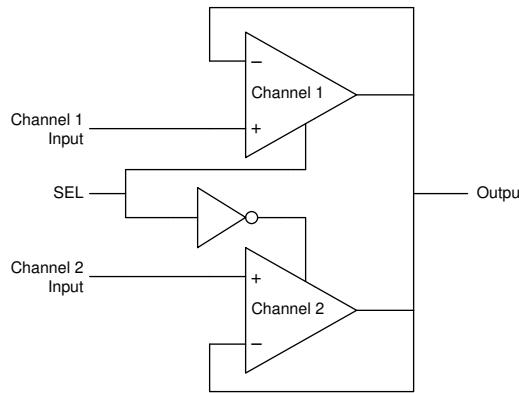


Figure 8-1. High Voltage Buffered Multiplexer

#### 8.2.2 Slew Rate Limit for Input Protection

In control systems for valves or motors, abrupt changes in voltages or currents can cause mechanical damages. By controlling the slew rate of the command voltages into the drive circuits, the load voltages ramps up and down at a safe rate. For symmetrical slew-rate applications (positive slew rate equals negative slew rate), one additional op amp provides slew-rate control for a given analog gain stage. The unique input protection and high output current and slew rate of the OPAx990 make the device an optimal amplifier to achieve slew rate control for both dual- and single-supply systems. Figure 8-2 shows the OPA990 in a slew-rate limit design.

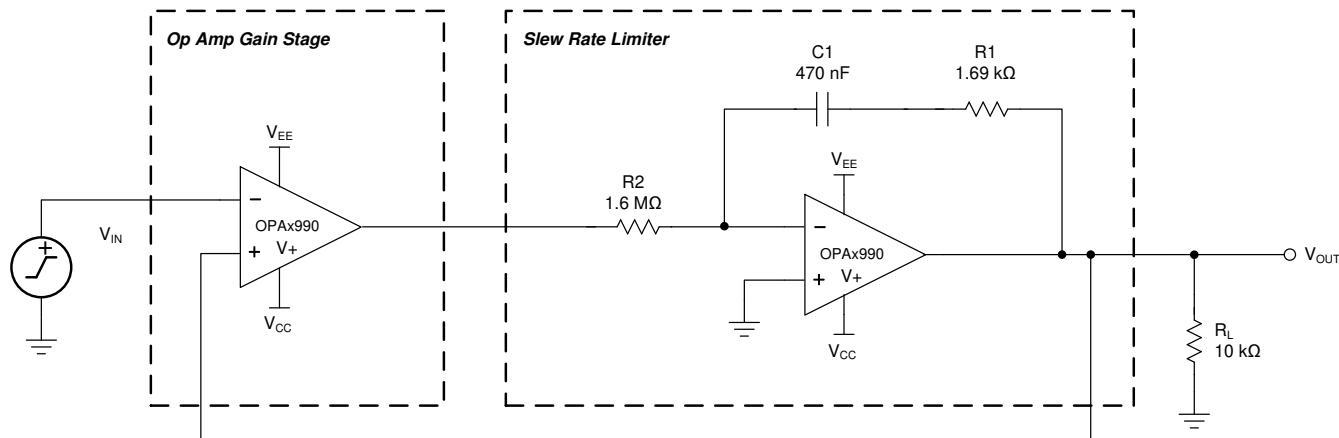


Figure 8-2. Slew Rate Limiter Uses One Op Amp

## 9 Power Supply Recommendations

The OPAx990 is specified for operation from 2.7 V to 40 V ( $\pm 1.35$  V to  $\pm 20$  V); many specifications apply from  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  or with specific supply voltages and test conditions. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

### CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout* section.

## 10 Layout

### 10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu\text{F}$  ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in [Figure 10-2](#), keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at  $85^\circ\text{C}$  for 30 minutes is sufficient for most circumstances.

### 10.2 Layout Example

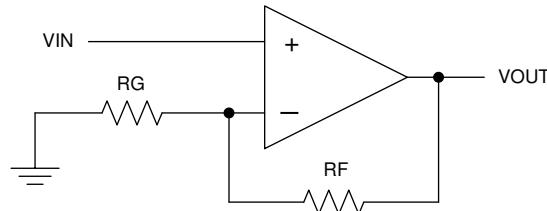
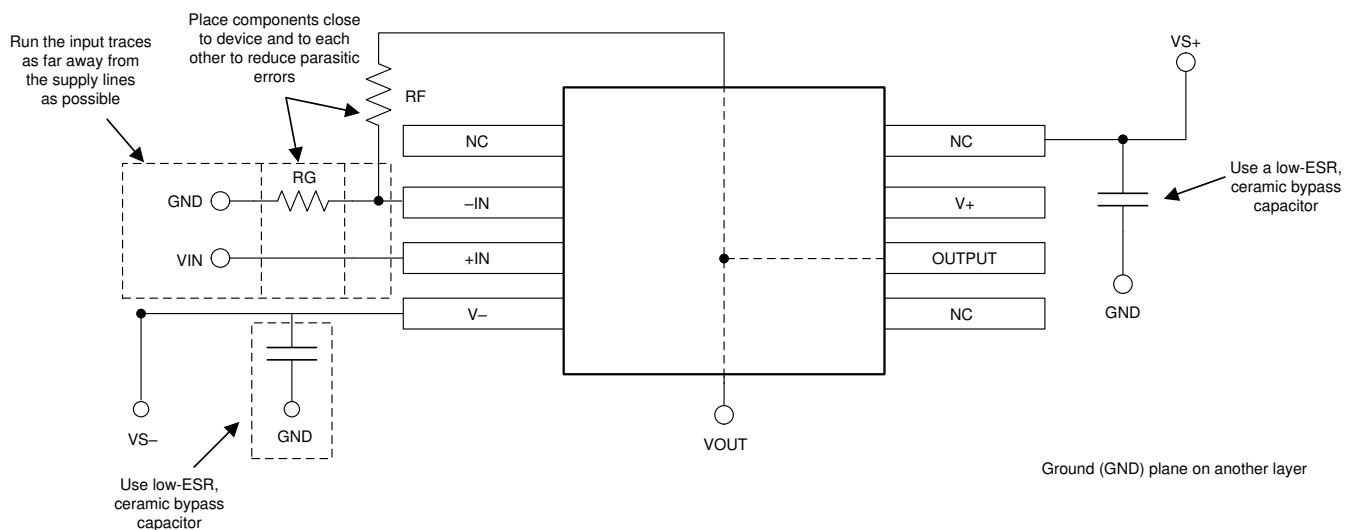
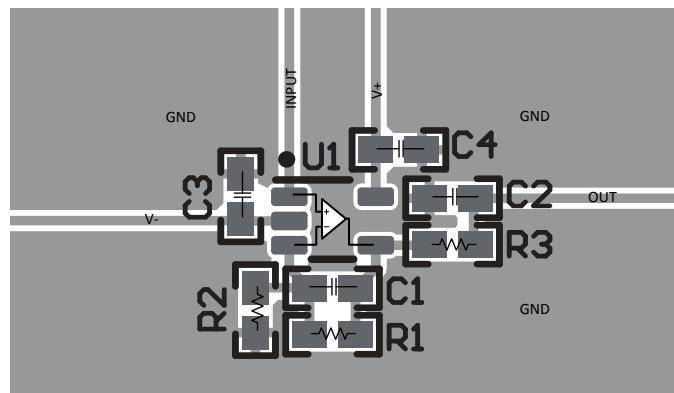


Figure 10-1. Schematic Representation



**Figure 10-2. Operational Amplifier Board Layout for Noninverting Configuration**



**Figure 10-3. Example Layout for SC70 (DCK) Package**

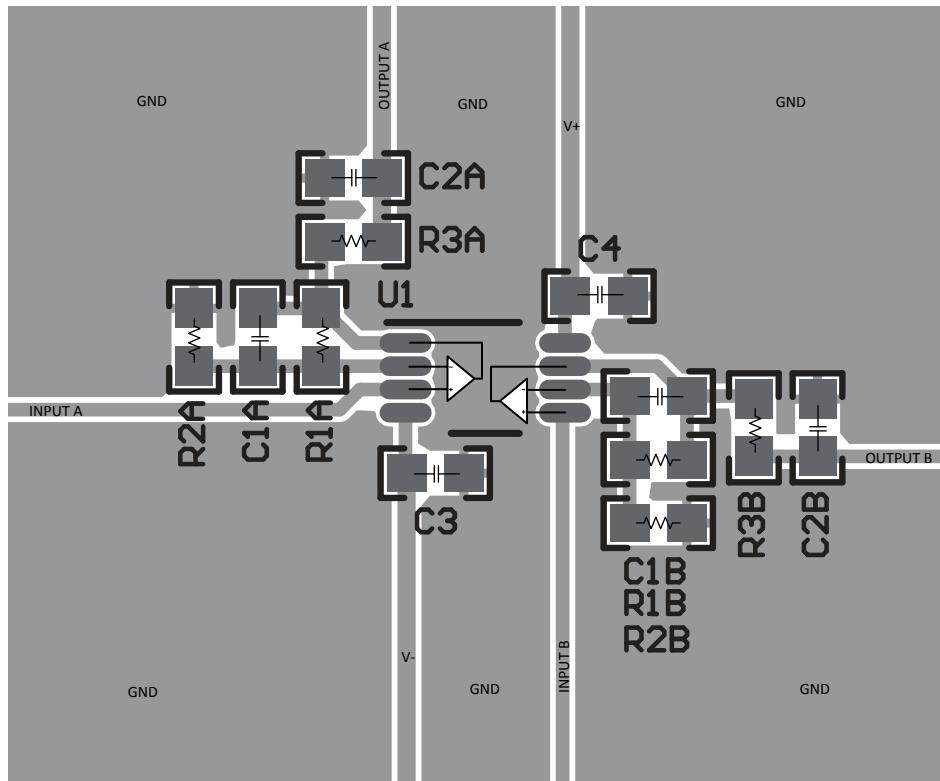


Figure 10-4. Example Layout for VSSOP-8 (DGK) Package

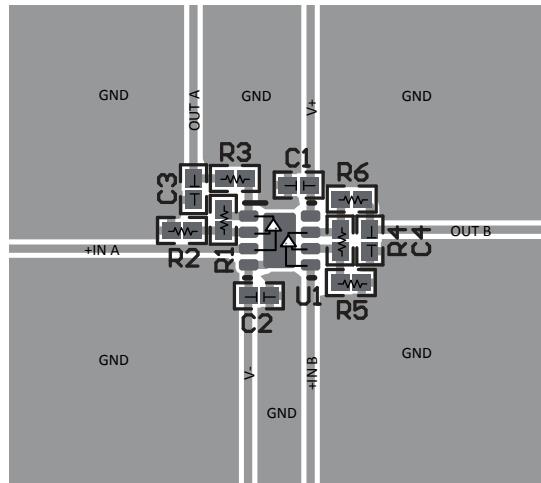


Figure 10-5. Example Layout for WSON-8 (DSG) Package

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

##### 11.1.1.1 *TINA-TI™ (Free Software Download)*

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

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#### Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

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### 11.2 Documentation Support

#### 11.2.1 Related Documentation

Texas Instruments, [MUX-Friendly, Precision Operational Amplifiers](#) application brief

Texas Instruments, [EMI Rejection Ratio of Operational Amplifiers](#) application report

Texas Instruments, [Op Amps With Complementary-Pair Input Stages](#) application note

### 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 11.5 Trademarks

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### 11.6 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins        | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|-----------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">OPA2990IDDFR</a>  | Active        | Production           | SOT-23-THIN (DDF)   8 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O90F                |
| OPA2990IDDFR.A                | Active        | Production           | SOT-23-THIN (DDF)   8 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O90F                |
| <a href="#">OPA2990IDGKR</a>  | Active        | Production           | VSSOP (DGK)   8       | 2500   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 125   | 2H9T                |
| OPA2990IDGKR.A                | Active        | Production           | VSSOP (DGK)   8       | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | 2H9T                |
| <a href="#">OPA2990IDR</a>    | Active        | Production           | SOIC (D)   8          | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | OP2990              |
| OPA2990IDR.A                  | Active        | Production           | SOIC (D)   8          | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | OP2990              |
| OPA2990IDRG4                  | Active        | Production           | SOIC (D)   8          | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | OP2990              |
| OPA2990IDRG4.A                | Active        | Production           | SOIC (D)   8          | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | OP2990              |
| <a href="#">OPA2990IDSGR</a>  | Active        | Production           | WSON (DSG)   8        | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O29G                |
| OPA2990IDSGR.A                | Active        | Production           | WSON (DSG)   8        | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O29G                |
| OPA2990IDSGRG4                | Active        | Production           | WSON (DSG)   8        | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O29G                |
| OPA2990IDSGRG4.A              | Active        | Production           | WSON (DSG)   8        | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O29G                |
| <a href="#">OPA2990IPWR</a>   | Active        | Production           | TSSOP (PW)   8        | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O2990P              |
| OPA2990IPWR.A                 | Active        | Production           | TSSOP (PW)   8        | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O2990P              |
| OPA2990IPWRG4                 | Active        | Production           | TSSOP (PW)   8        | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O2990P              |
| OPA2990IPWRG4.A               | Active        | Production           | TSSOP (PW)   8        | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O2990P              |
| <a href="#">OPA2990SIDGSR</a> | Active        | Production           | VSSOP (DGS)   10      | 2500   LARGE T&R      | Yes         | NIPDAUAG                             | Level-2-260C-1 YEAR               | -40 to 125   | OP29                |
| OPA2990SIDGSR.A               | Active        | Production           | VSSOP (DGS)   10      | 2500   LARGE T&R      | Yes         | NIPDAUAG                             | Level-2-260C-1 YEAR               | -40 to 125   | OP29                |
| <a href="#">OPA2990SIRUGR</a> | Active        | Production           | X2QFN (RUG)   10      | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-2-260C-1 YEAR               | -40 to 125   | H9F                 |
| OPA2990SIRUGR.A               | Active        | Production           | X2QFN (RUG)   10      | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-2-260C-1 YEAR               | -40 to 125   | H9F                 |
| <a href="#">OPA2990TIDDFR</a> | Active        | Production           | SOT-23-THIN (DDF)   8 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O90F                |
| OPA2990TIDDFR.A               | Active        | Production           | SOT-23-THIN (DDF)   8 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O90F                |
| <a href="#">OPA4990IDR</a>    | Active        | Production           | SOIC (D)   14         | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | OPA4990D            |
| OPA4990IDR.A                  | Active        | Production           | SOIC (D)   14         | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | OPA4990D            |
| <a href="#">OPA4990IPWR</a>   | Active        | Production           | TSSOP (PW)   14       | 2000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-2-260C-1 YEAR               | -40 to 125   | OPA49PW             |
| OPA4990IPWR.A                 | Active        | Production           | TSSOP (PW)   14       | 2000   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 125   | OPA49PW             |
| <a href="#">OPA4990IRTER</a>  | Active        | Production           | WQFN (RTE)   16       | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O49RT               |
| OPA4990IRTER.A                | Active        | Production           | WQFN (RTE)   16       | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O49RT               |
| OPA4990IRTERG4                | Active        | Production           | WQFN (RTE)   16       | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O49RT               |

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| OPA4990IRTERG4.A              | Active        | Production           | WQFN (RTE)   16  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O49RT               |
| <a href="#">OPA4990IRUCR</a>  | Active        | Production           | QFN (RUC)   14   | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | FMF                 |
| OPA4990IRUCR.A                | Active        | Production           | QFN (RUC)   14   | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | FMF                 |
| <a href="#">OPA4990SIRTER</a> | Active        | Production           | WQFN (RTE)   16  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O4990S              |
| OPA4990SIRTER.A               | Active        | Production           | WQFN (RTE)   16  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O4990S              |
| <a href="#">OPA990IDBVR</a>   | Active        | Production           | SOT-23 (DBV)   5 | 3000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 125   | O90V                |
| OPA990IDBVR.A                 | Active        | Production           | SOT-23 (DBV)   5 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O90V                |
| OPA990IDBVRG4                 | Active        | Production           | SOT-23 (DBV)   5 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O90V                |
| OPA990IDBVRG4.A               | Active        | Production           | SOT-23 (DBV)   5 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O90V                |
| <a href="#">OPA990IDCKR</a>   | Active        | Production           | SC70 (DCK)   5   | 3000   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 125   | 1FL                 |
| OPA990IDCKR.A                 | Active        | Production           | SC70 (DCK)   5   | 3000   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 125   | 1FL                 |
| <a href="#">OPA990SIDBVR</a>  | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 125   | O90S                |
| OPA990SIDBVR.A                | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O90S                |
| OPA990SIDBVRG4                | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O90S                |
| OPA990SIDBVRG4.A              | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | O90S                |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

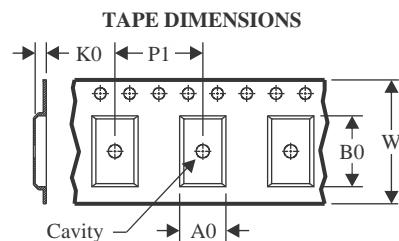
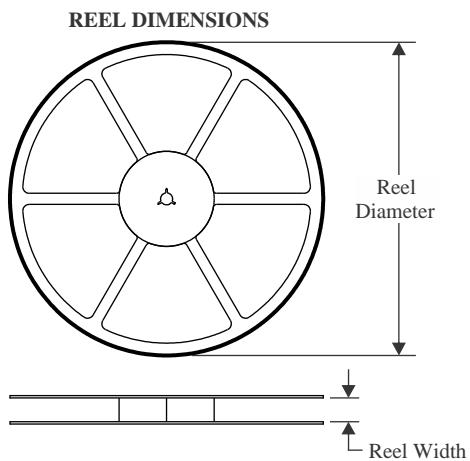
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF OPA4990 :**

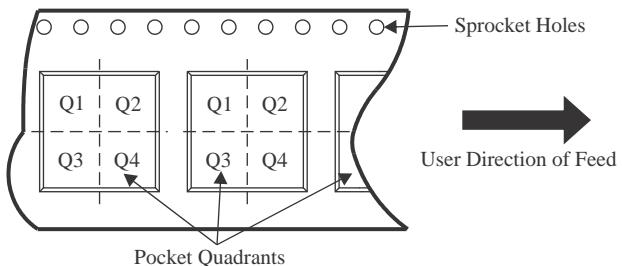
- Automotive : [OPA4990-Q1](#)

**NOTE: Qualified Version Definitions:**

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**


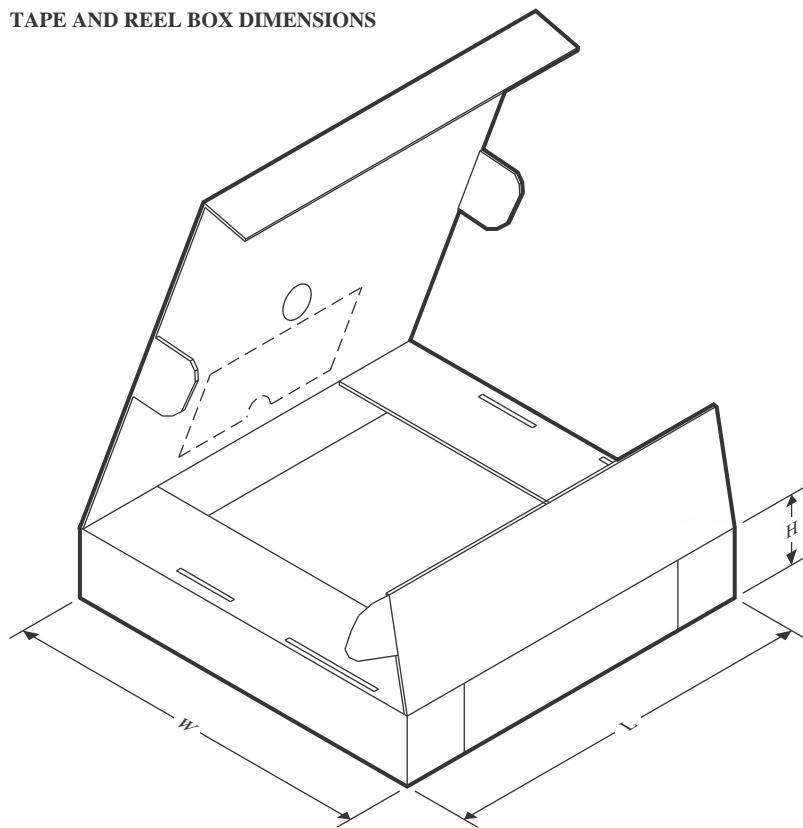
|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| OPA2990IDDFR   | SOT-23-THIN  | DDF             | 8    | 3000 | 180.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| OPA2990IDGKR   | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| OPA2990IDR     | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| OPA2990IDRG4   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| OPA2990IDSGR   | WSON         | DSG             | 8    | 3000 | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| OPA2990IDSGRG4 | WSON         | DSG             | 8    | 3000 | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| OPA2990IPWR    | TSSOP        | PW              | 8    | 2000 | 330.0              | 12.4               | 7.0     | 3.6     | 1.6     | 8.0     | 12.0   | Q1            |
| OPA2990IPWRG4  | TSSOP        | PW              | 8    | 2000 | 330.0              | 12.4               | 7.0     | 3.6     | 1.6     | 8.0     | 12.0   | Q1            |
| OPA2990SIDGSR  | VSSOP        | DGS             | 10   | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| OPA2990SIRUGR  | X2QFN        | RUG             | 10   | 3000 | 178.0              | 8.4                | 1.75    | 2.25    | 0.56    | 4.0     | 8.0    | Q1            |
| OPA2990TIDDFR  | SOT-23-THIN  | DDF             | 8    | 3000 | 180.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q2            |
| OPA4990IDR     | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| OPA4990IPWR    | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| OPA4990IRTER   | WQFN         | RTE             | 16   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| OPA4990IRTERG4 | WQFN         | RTE             | 16   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| OPA4990IRUCR   | QFN          | RUC             | 14   | 3000 | 180.0              | 9.5                | 2.16    | 2.16    | 0.5     | 4.0     | 8.0    | Q2            |
| OPA4990SIRTER  | WQFN         | RTE             | 16   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| OPA990IDBVR    | SOT-23       | DBV             | 5    | 3000 | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| OPA990IDBVRG4  | SOT-23       | DBV             | 5    | 3000 | 180.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| OPA990IDCKR    | SC70         | DCK             | 5    | 3000 | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| OPA990SIDBVR   | SOT-23       | DBV             | 6    | 3000 | 180.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| OPA990SIDBVRG4 | SOT-23       | DBV             | 6    | 3000 | 180.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| OPA2990IDDFR   | SOT-23-THIN  | DDF             | 8    | 3000 | 210.0       | 185.0      | 35.0        |
| OPA2990IDGKR   | VSSOP        | DGK             | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| OPA2990IDR     | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| OPA2990IDRG4   | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| OPA2990IDSGR   | WSON         | DSG             | 8    | 3000 | 210.0       | 185.0      | 35.0        |
| OPA2990IDSGRG4 | WSON         | DSG             | 8    | 3000 | 210.0       | 185.0      | 35.0        |
| OPA2990IPWR    | TSSOP        | PW              | 8    | 2000 | 353.0       | 353.0      | 32.0        |
| OPA2990IPWRG4  | TSSOP        | PW              | 8    | 2000 | 353.0       | 353.0      | 32.0        |
| OPA2990SIDGSR  | VSSOP        | DGS             | 10   | 2500 | 366.0       | 364.0      | 50.0        |
| OPA2990SIRUGR  | X2QFN        | RUG             | 10   | 3000 | 205.0       | 200.0      | 33.0        |
| OPA2990TIDDFR  | SOT-23-THIN  | DDF             | 8    | 3000 | 210.0       | 185.0      | 35.0        |
| OPA4990IDR     | SOIC         | D               | 14   | 2500 | 353.0       | 353.0      | 32.0        |
| OPA4990IPWR    | TSSOP        | PW              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| OPA4990IRTER   | WQFN         | RTE             | 16   | 3000 | 367.0       | 367.0      | 35.0        |
| OPA4990IRTERG4 | WQFN         | RTE             | 16   | 3000 | 367.0       | 367.0      | 35.0        |
| OPA4990IRUCR   | QFN          | RUC             | 14   | 3000 | 205.0       | 200.0      | 30.0        |
| OPA4990SIRTER  | WQFN         | RTE             | 16   | 3000 | 367.0       | 367.0      | 35.0        |
| OPA4990IDBVR   | SOT-23       | DBV             | 5    | 3000 | 208.0       | 191.0      | 35.0        |

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| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| OPA990IDBVRG4  | SOT-23       | DBV             | 5    | 3000 | 210.0       | 185.0      | 35.0        |
| OPA990IDCKR    | SC70         | DCK             | 5    | 3000 | 190.0       | 190.0      | 30.0        |
| OPA990SIDBVR   | SOT-23       | DBV             | 6    | 3000 | 210.0       | 185.0      | 35.0        |
| OPA990SIDBVRG4 | SOT-23       | DBV             | 6    | 3000 | 210.0       | 185.0      | 35.0        |

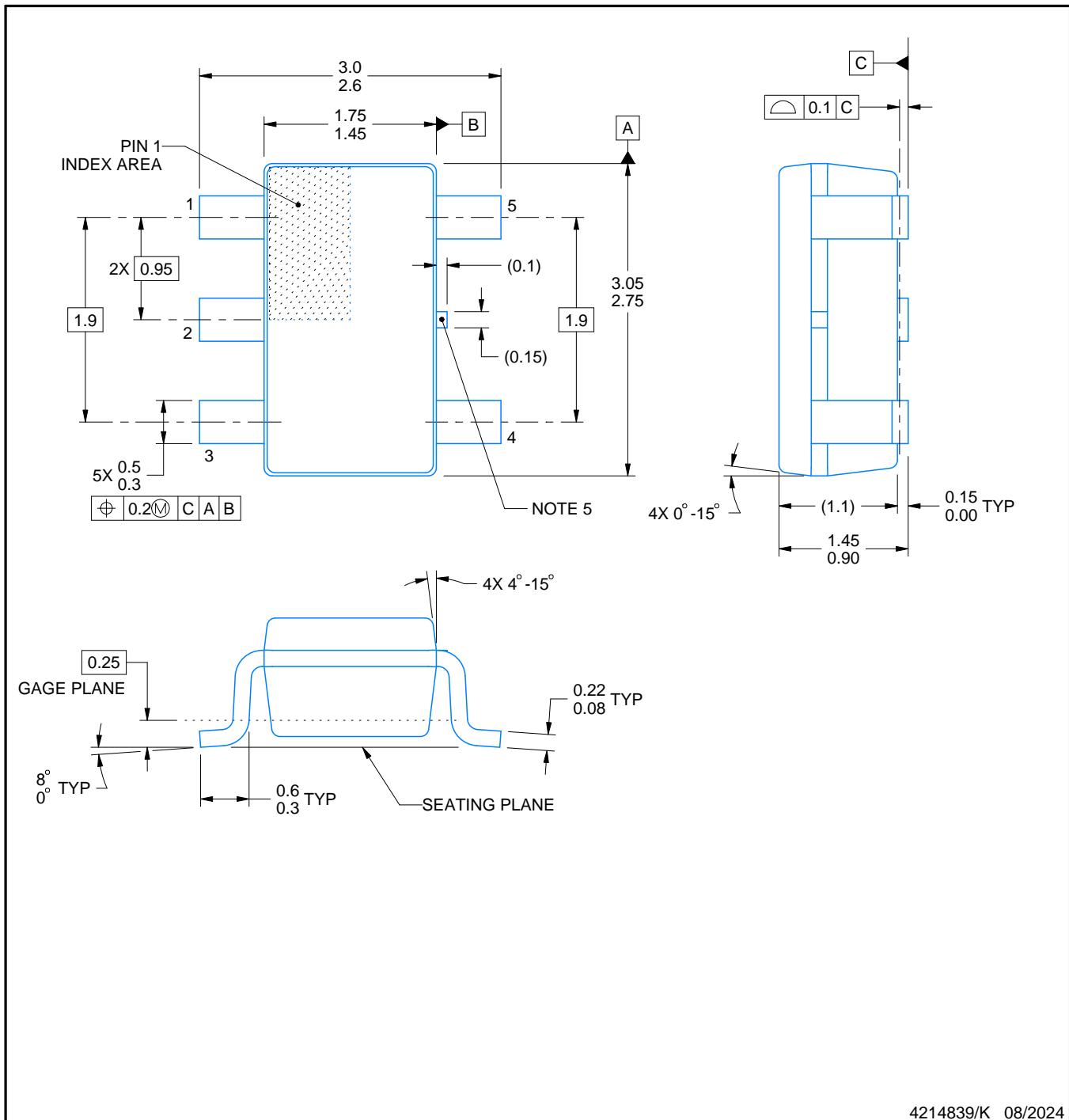
## PACKAGE OUTLINE

**DBV0005A**



## **SOT-23 - 1.45 mm max height**

## SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

## NOTES:

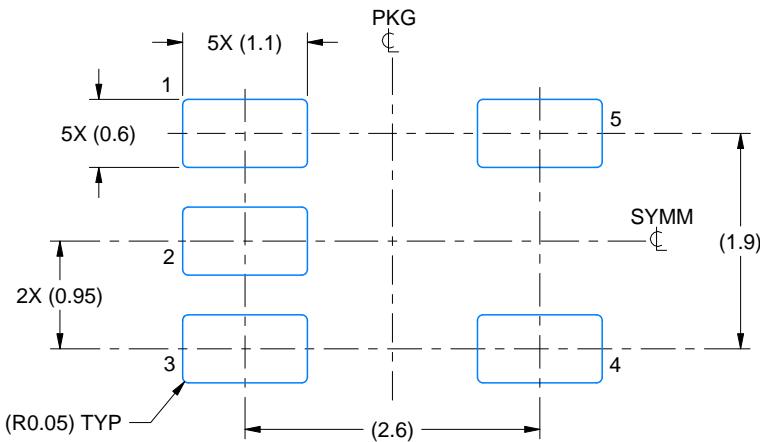
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

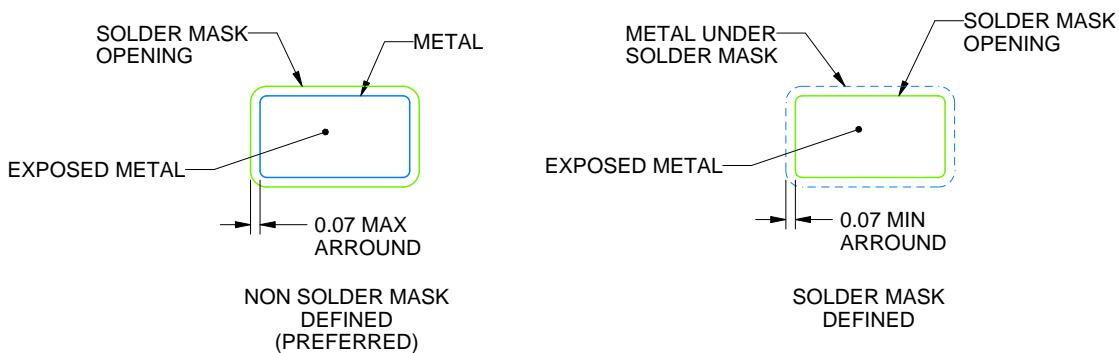
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

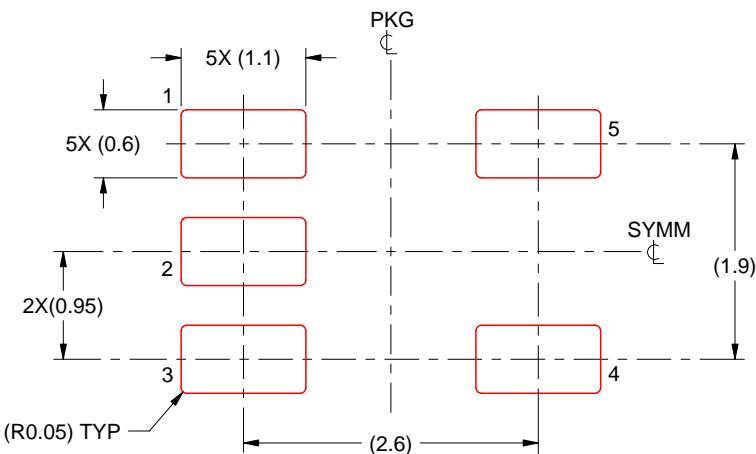
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

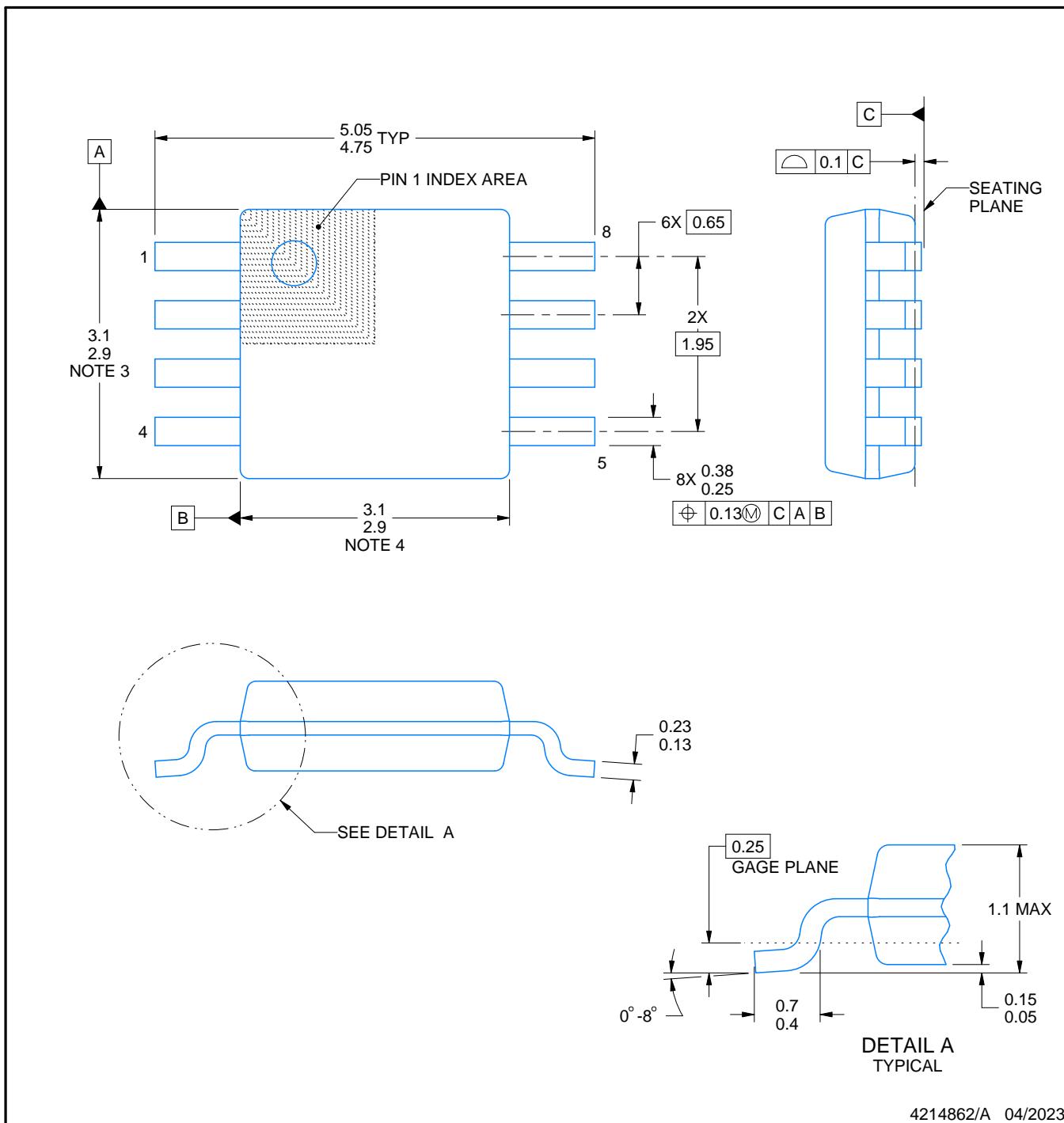
# PACKAGE OUTLINE

DGK0008A



VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

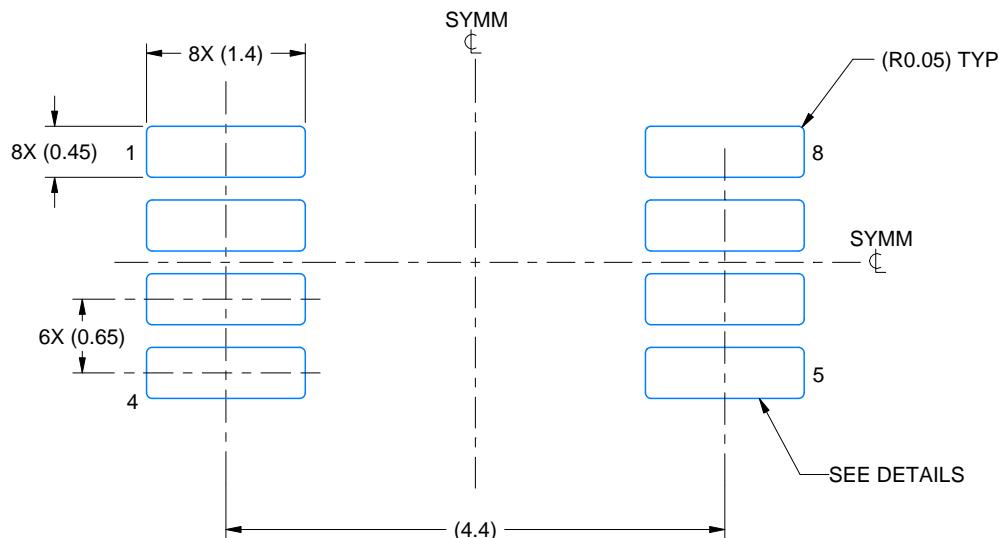
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

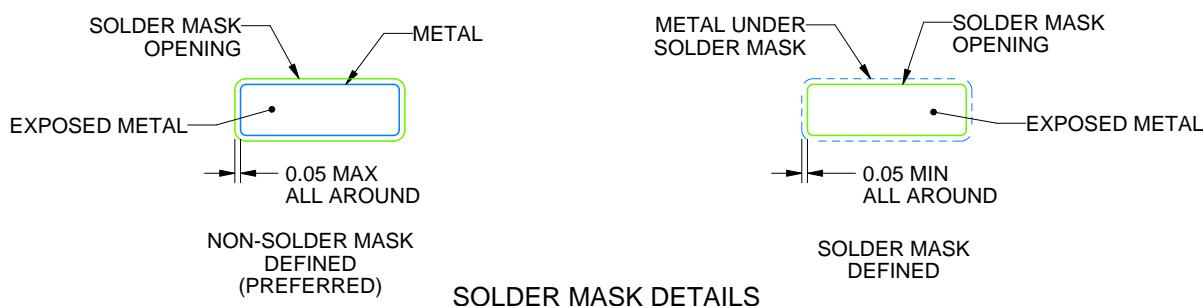
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

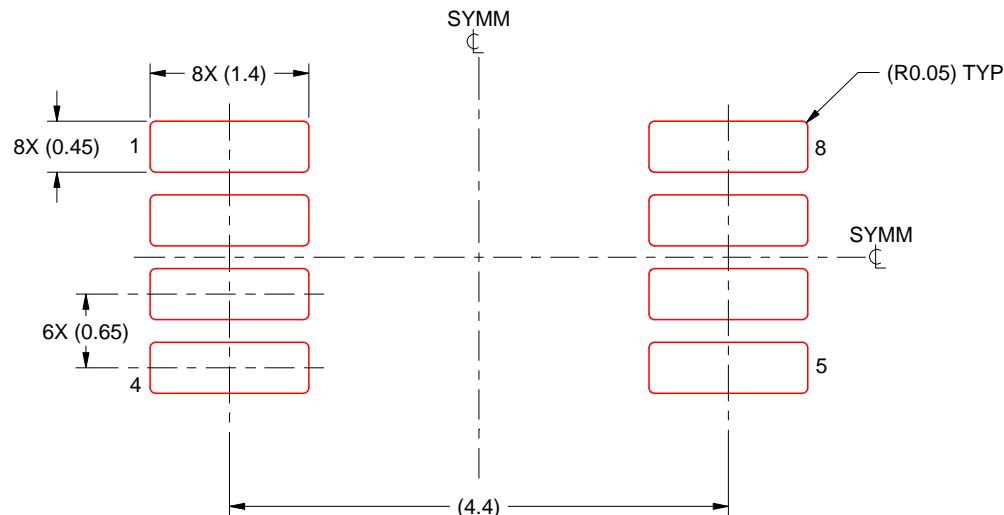
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

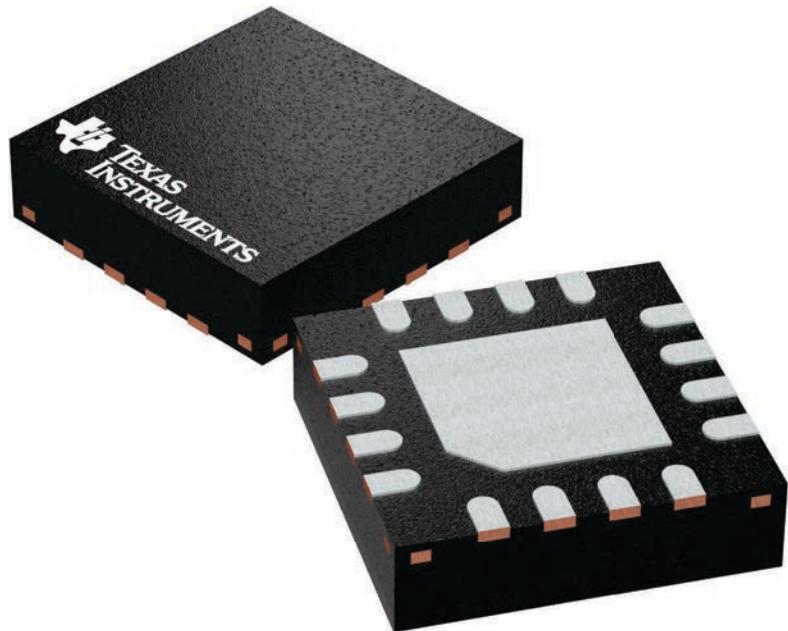
### RTE 16

### WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225944/A

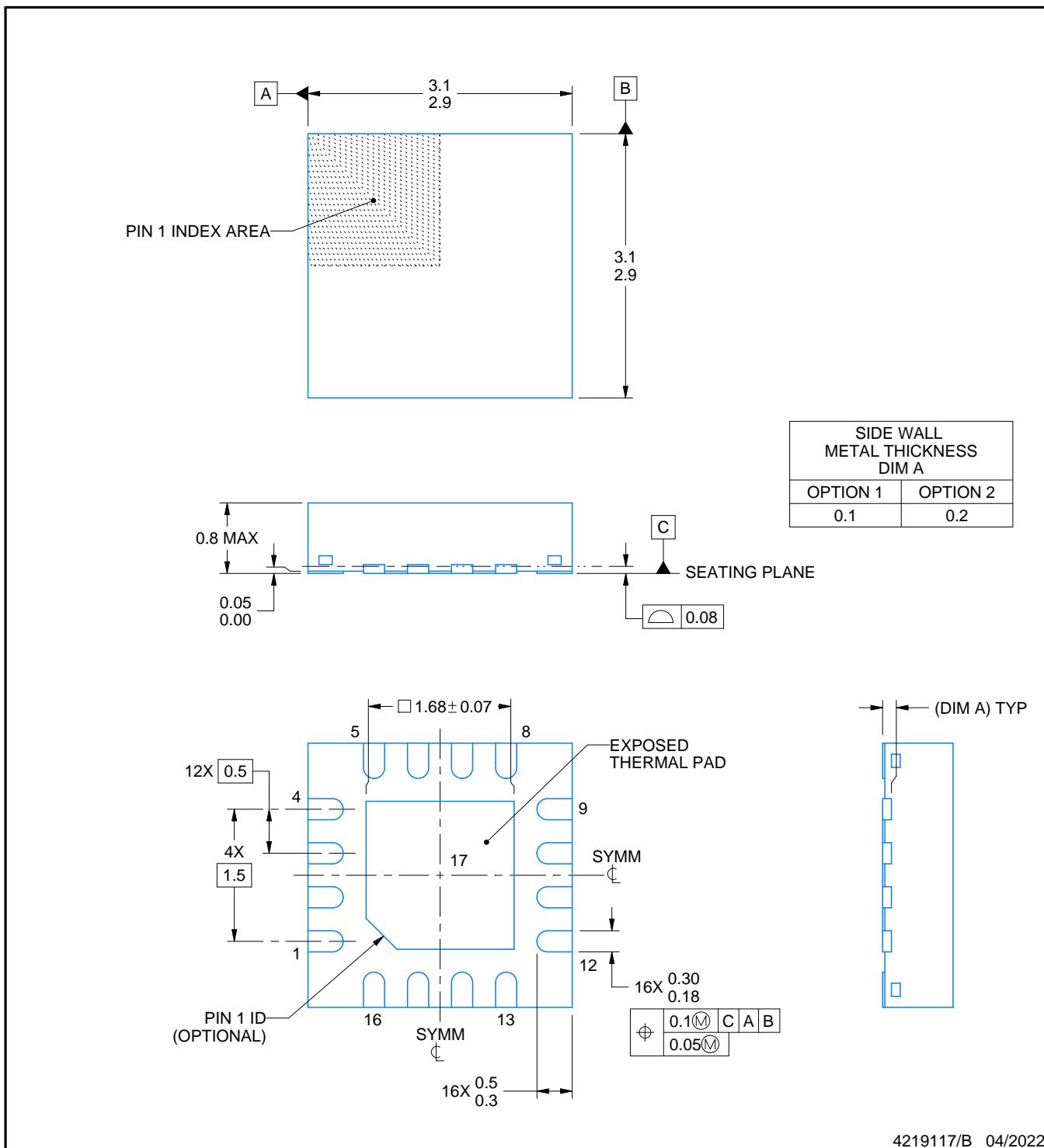
# PACKAGE OUTLINE

RTE0016C



WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



## NOTES:

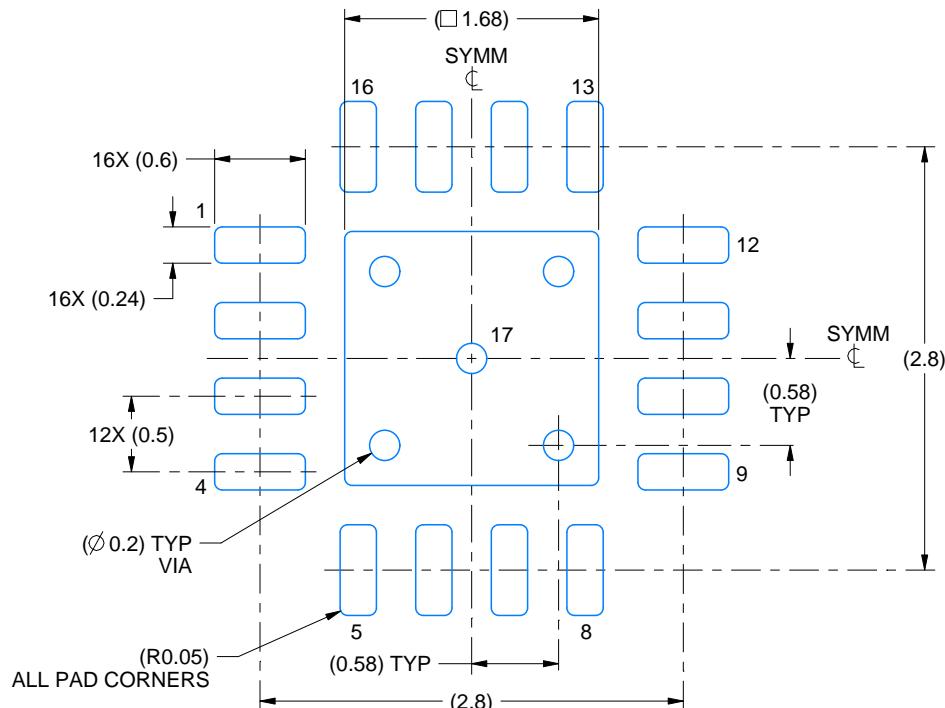
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

## EXAMPLE BOARD LAYOUT

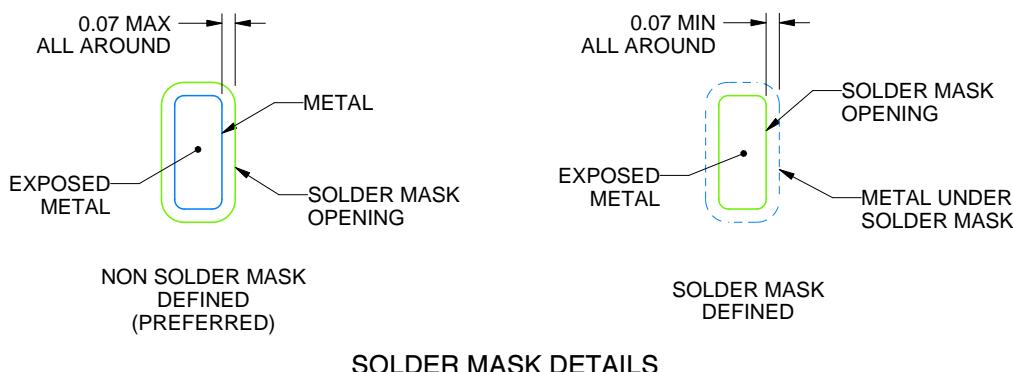
**RTE0016C**

## **WQFN - 0.8 mm max height**

#### PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



4219117/B 04/2022

#### NOTES: (continued)

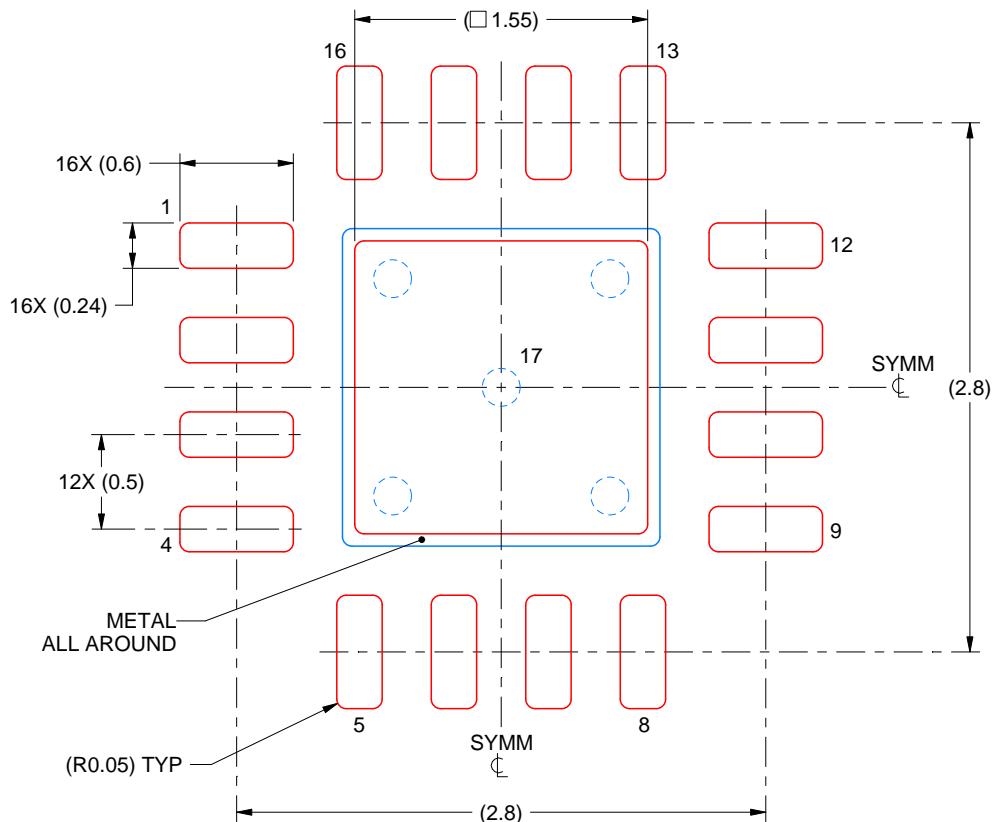
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219117/B 04/2022

NOTES: (continued)

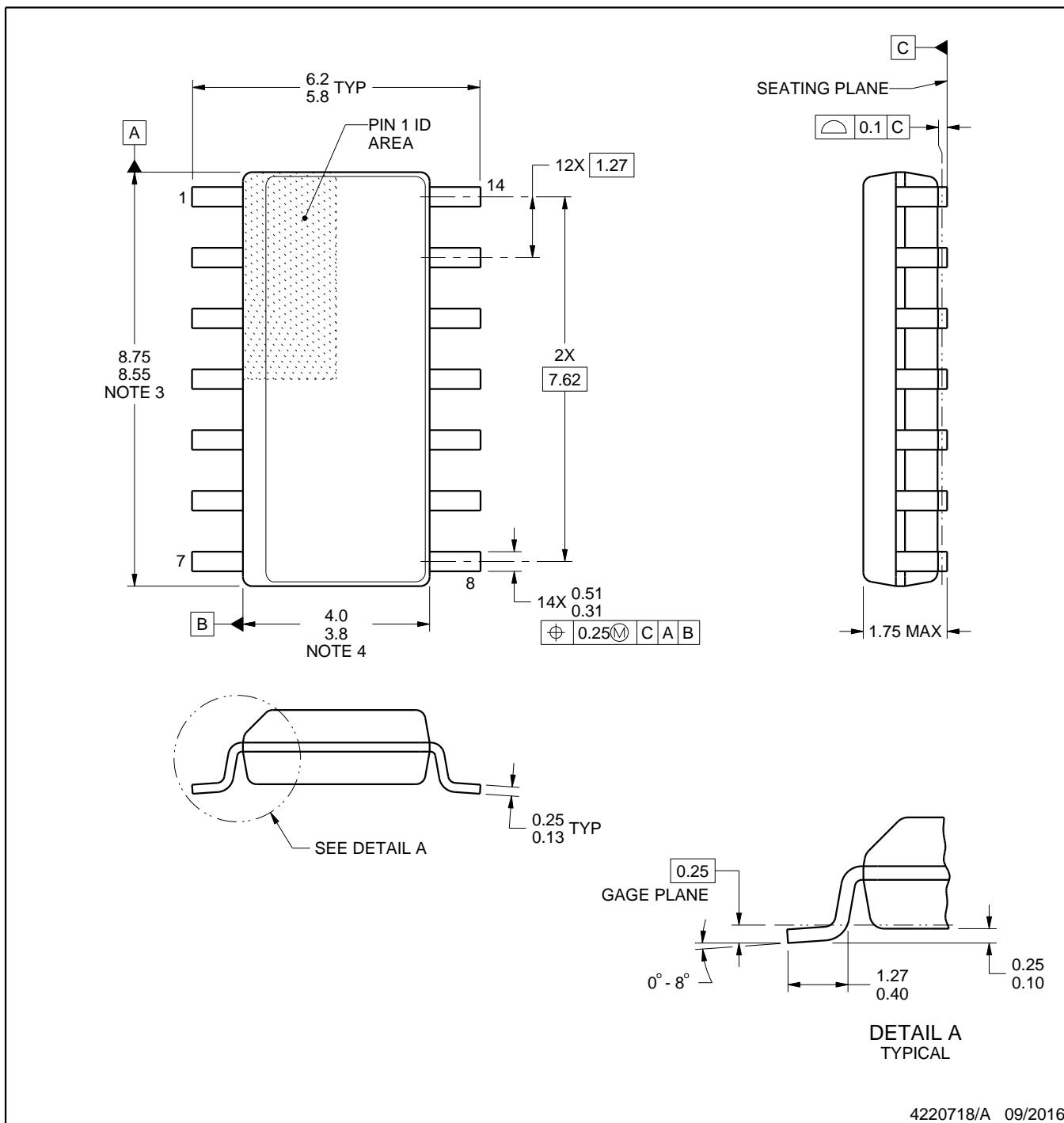
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



## NOTES:

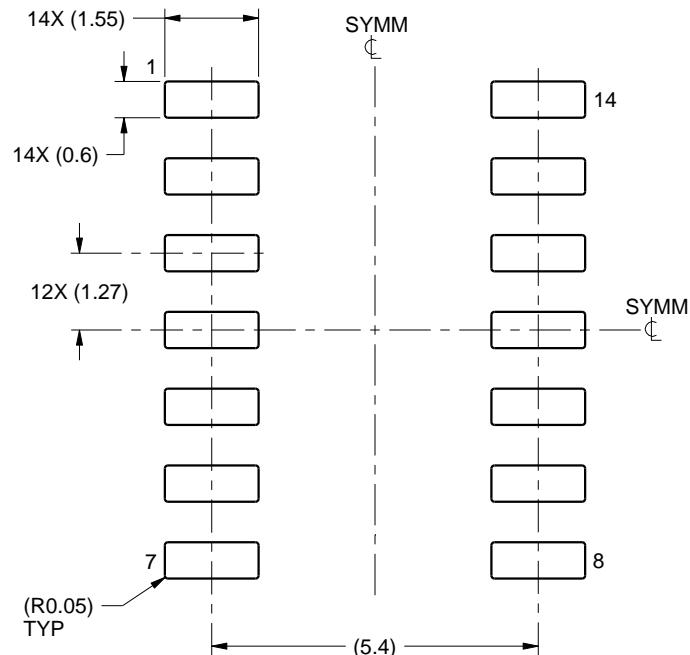
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

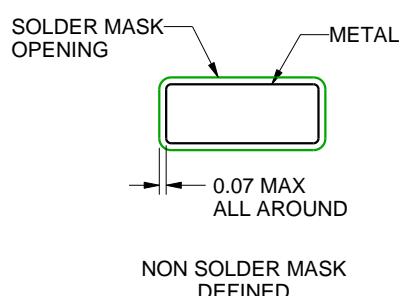
D0014A

SOIC - 1.75 mm max height

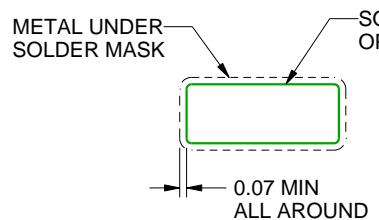
SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

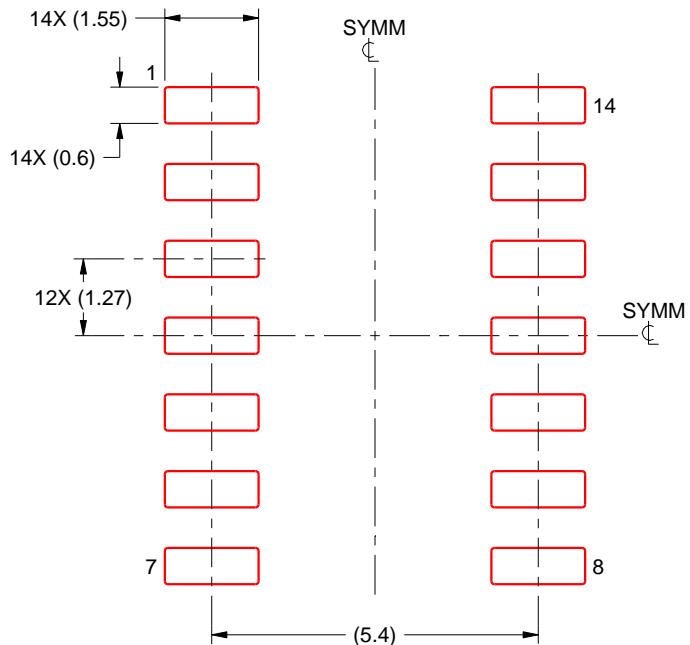
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

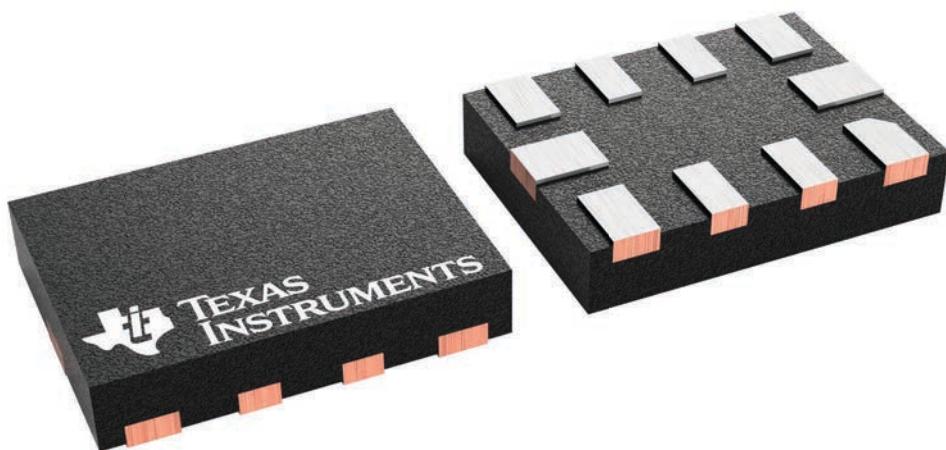
### RUG 10

### X2QFN - 0.4 mm max height

1.5 x 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

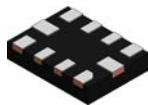
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4231768/A

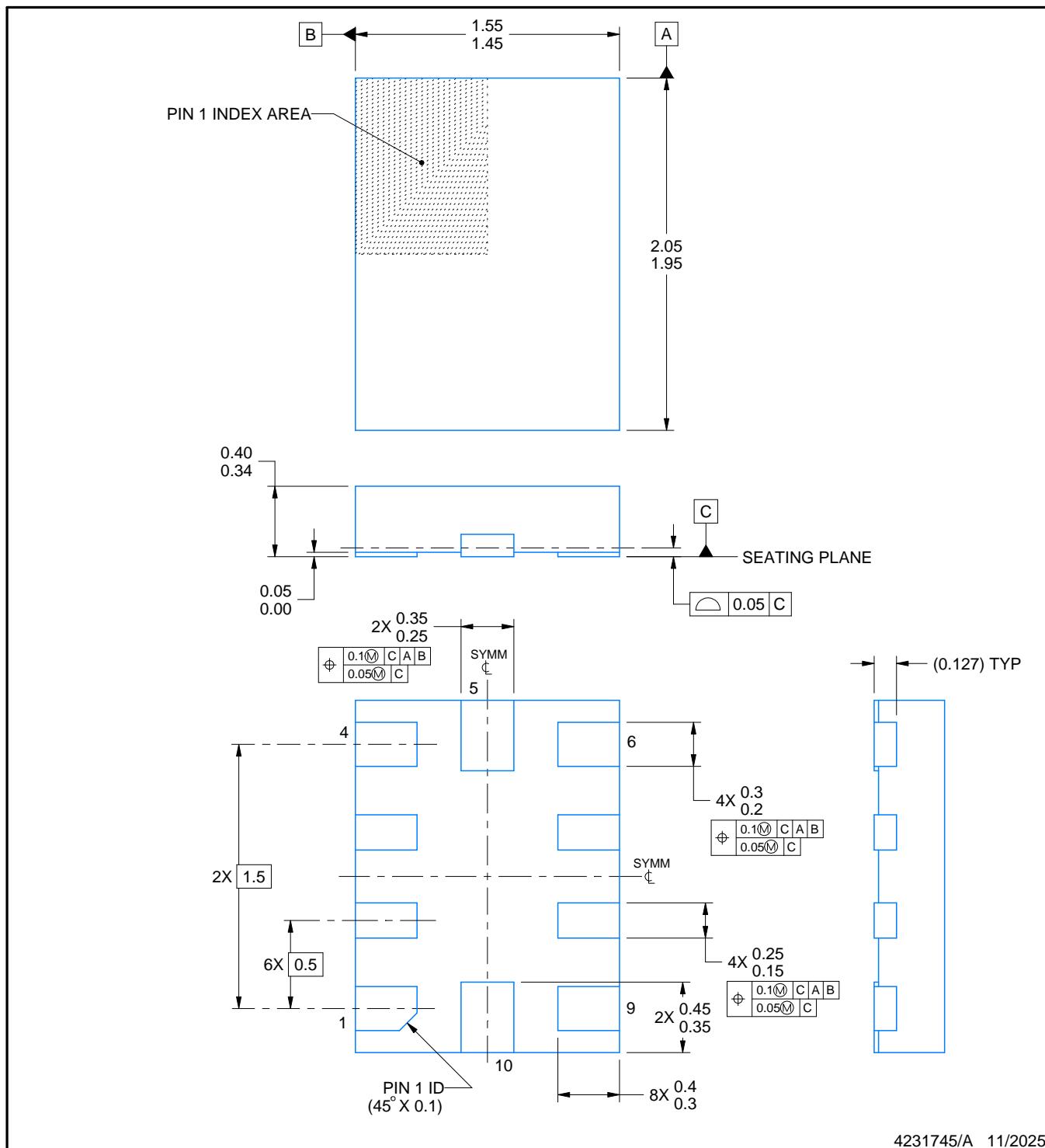
# PACKAGE OUTLINE

RUG0010A



X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4231745/A 11/2025

## NOTES:

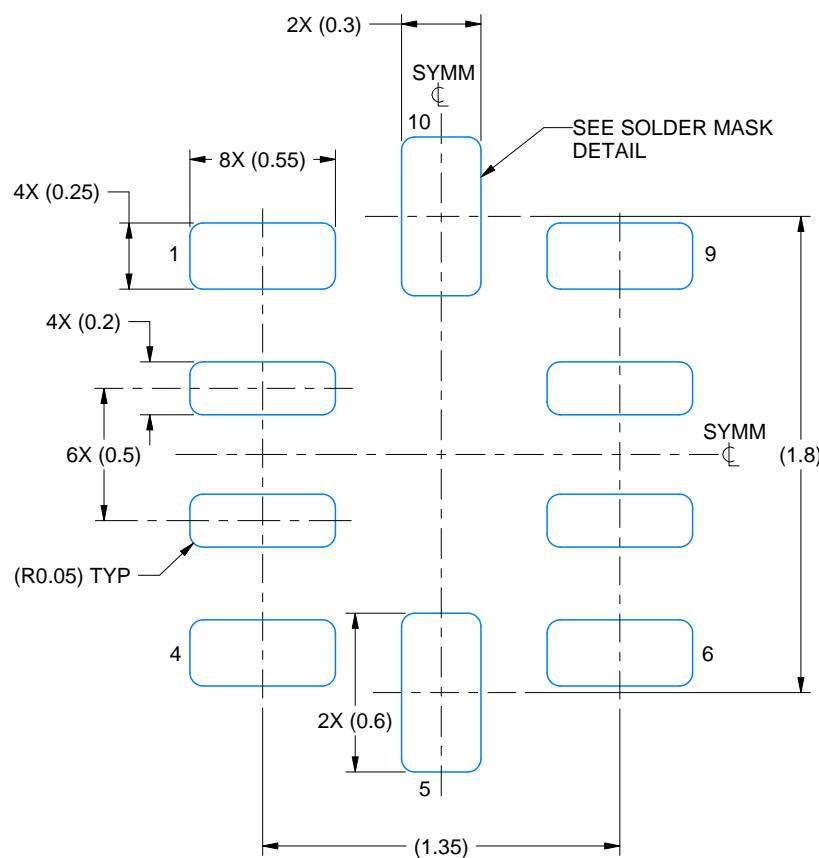
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

RUG0010A

X2QFN - 0.4 mm max height

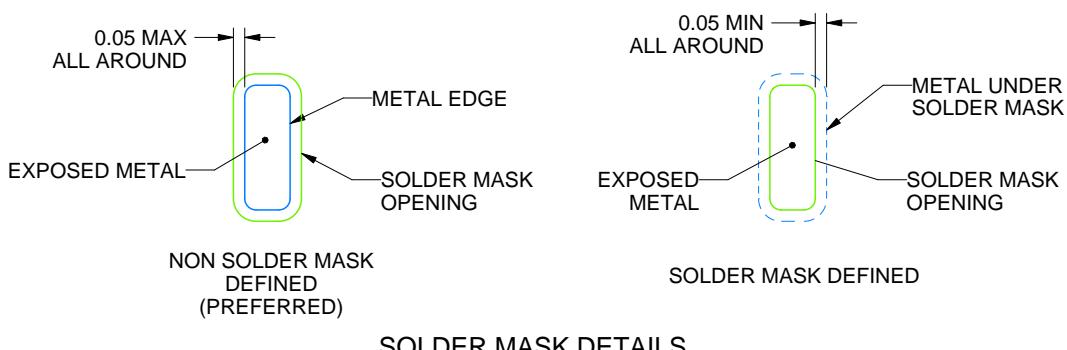
PLASTIC QUAD FLATPACK - NO LEAD



## LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 35X



4231745/A 11/2025

NOTES: (continued)

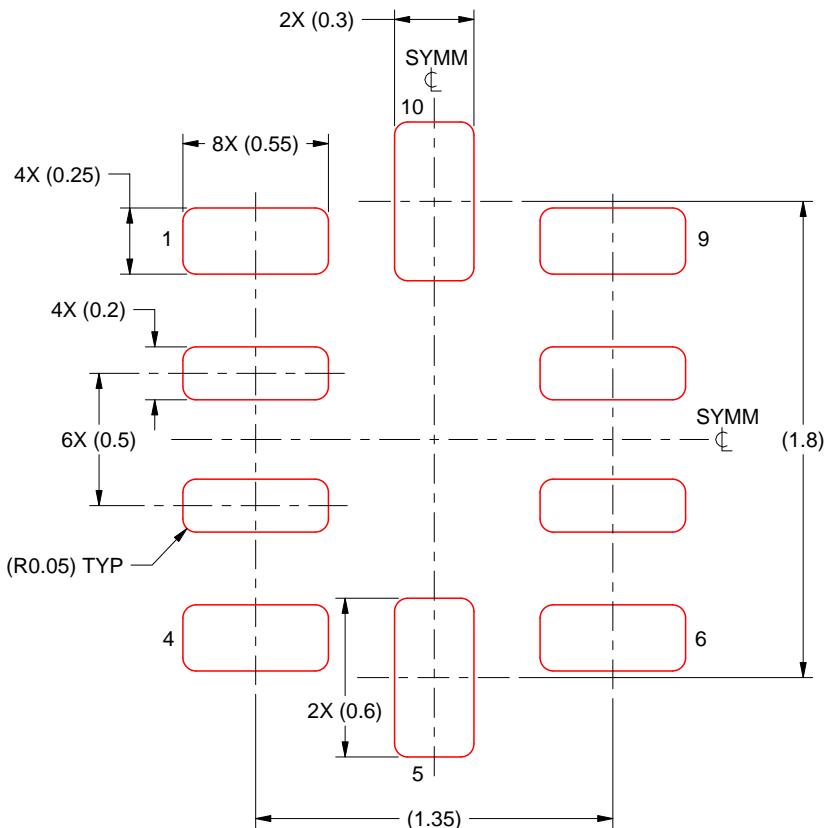
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

RUG0010A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 35X

4231745/A 11/2025

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

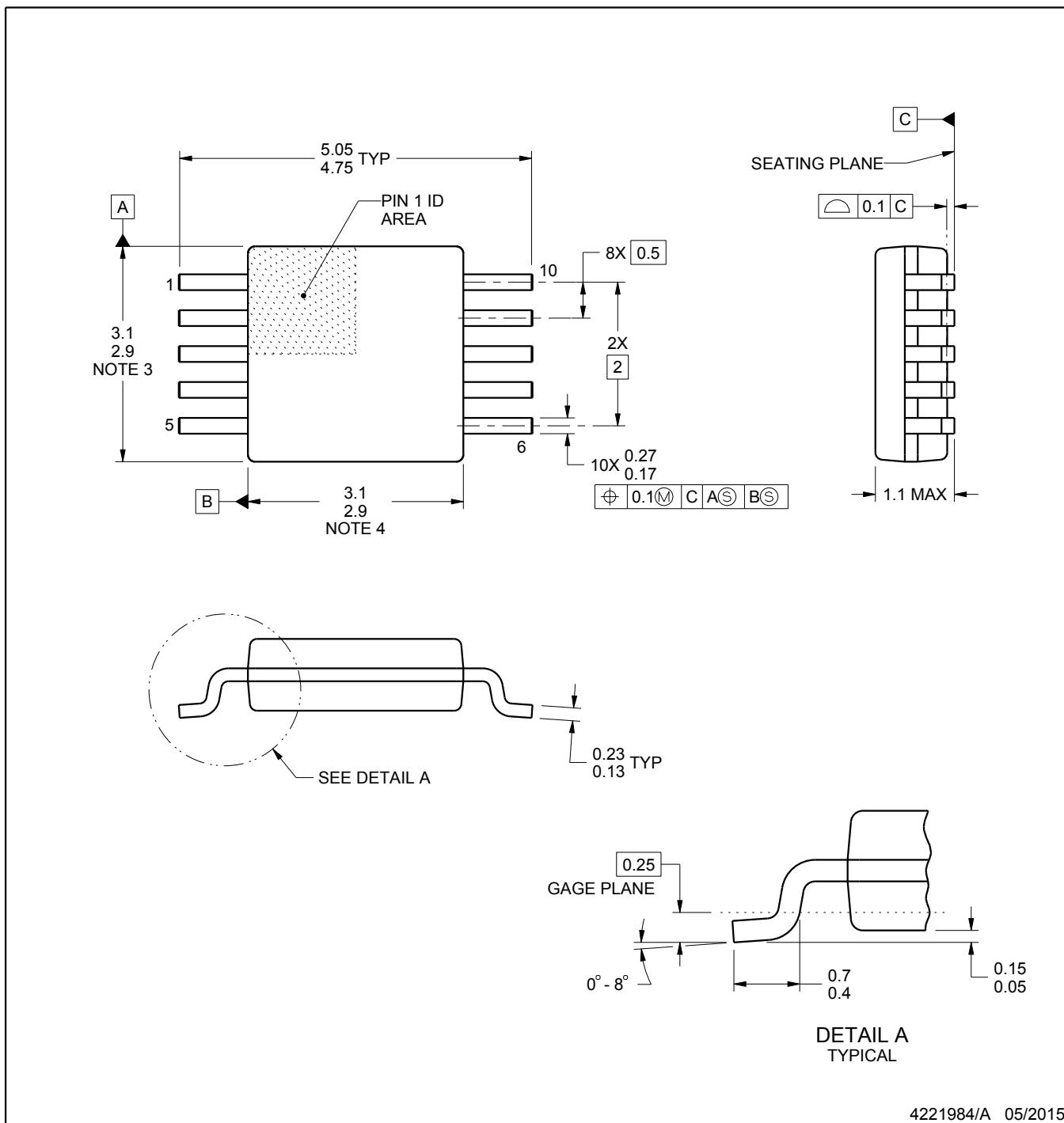
# PACKAGE OUTLINE

DGS0010A



VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

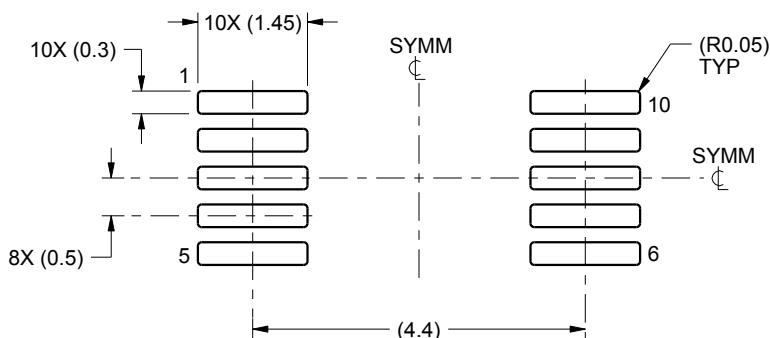
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

# EXAMPLE BOARD LAYOUT

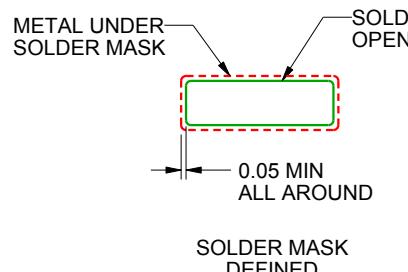
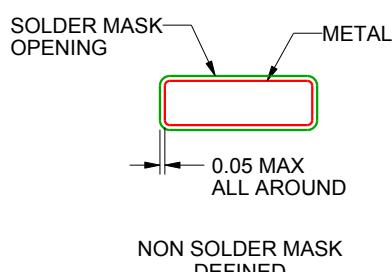
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

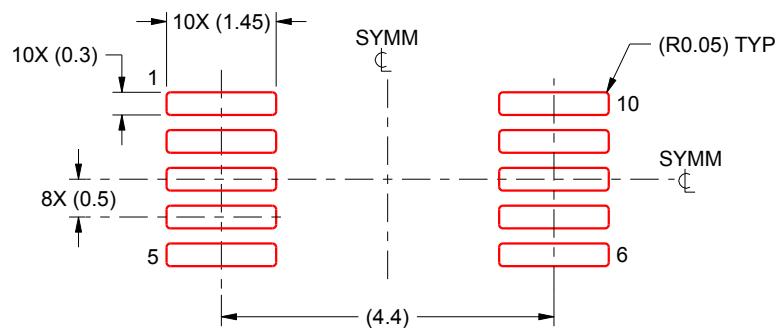
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

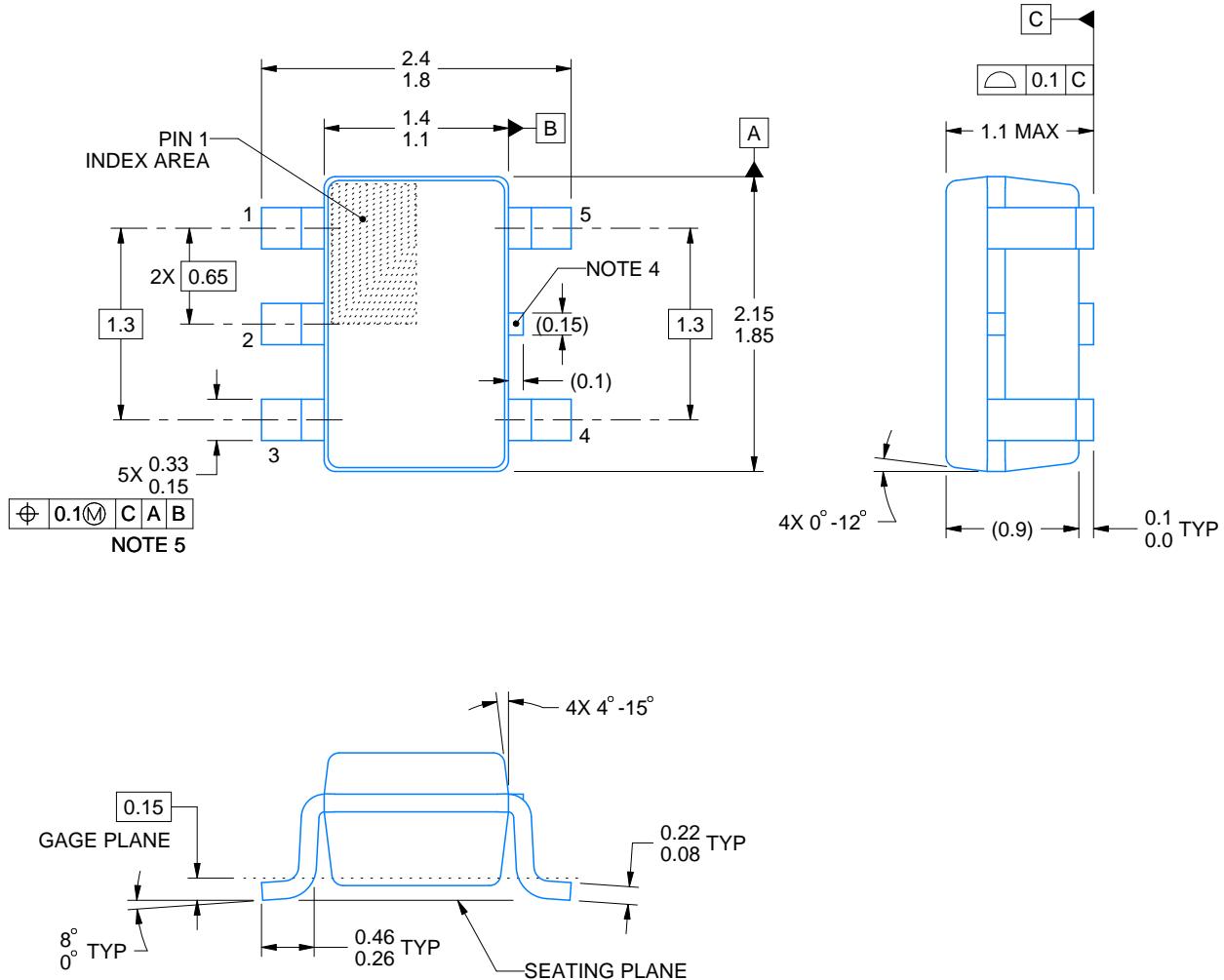
## PACKAGE OUTLINE

**DCK0005A**



## SOT - 1.1 max height

## SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

## NOTES:

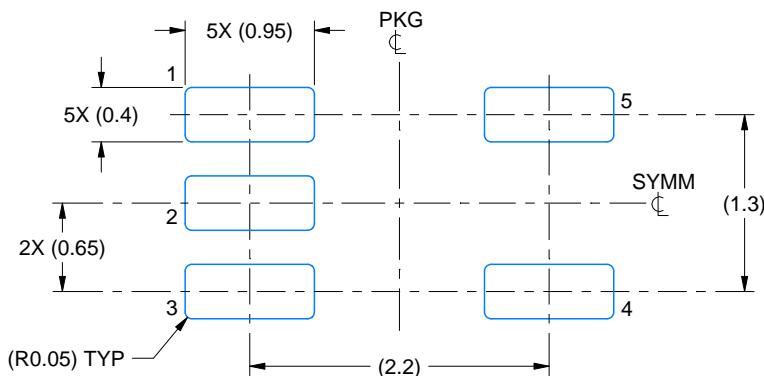
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

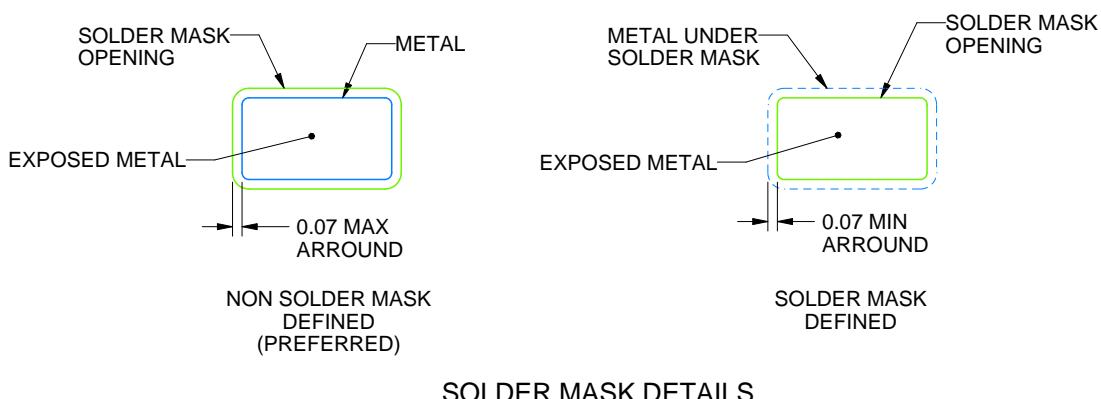
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



4214834/G 11/2024

NOTES: (continued)

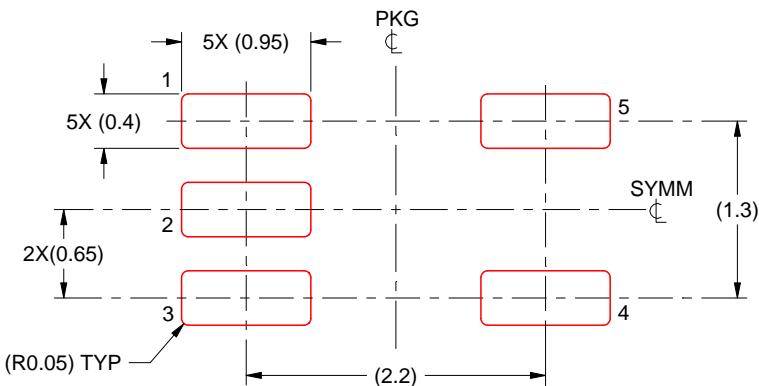
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

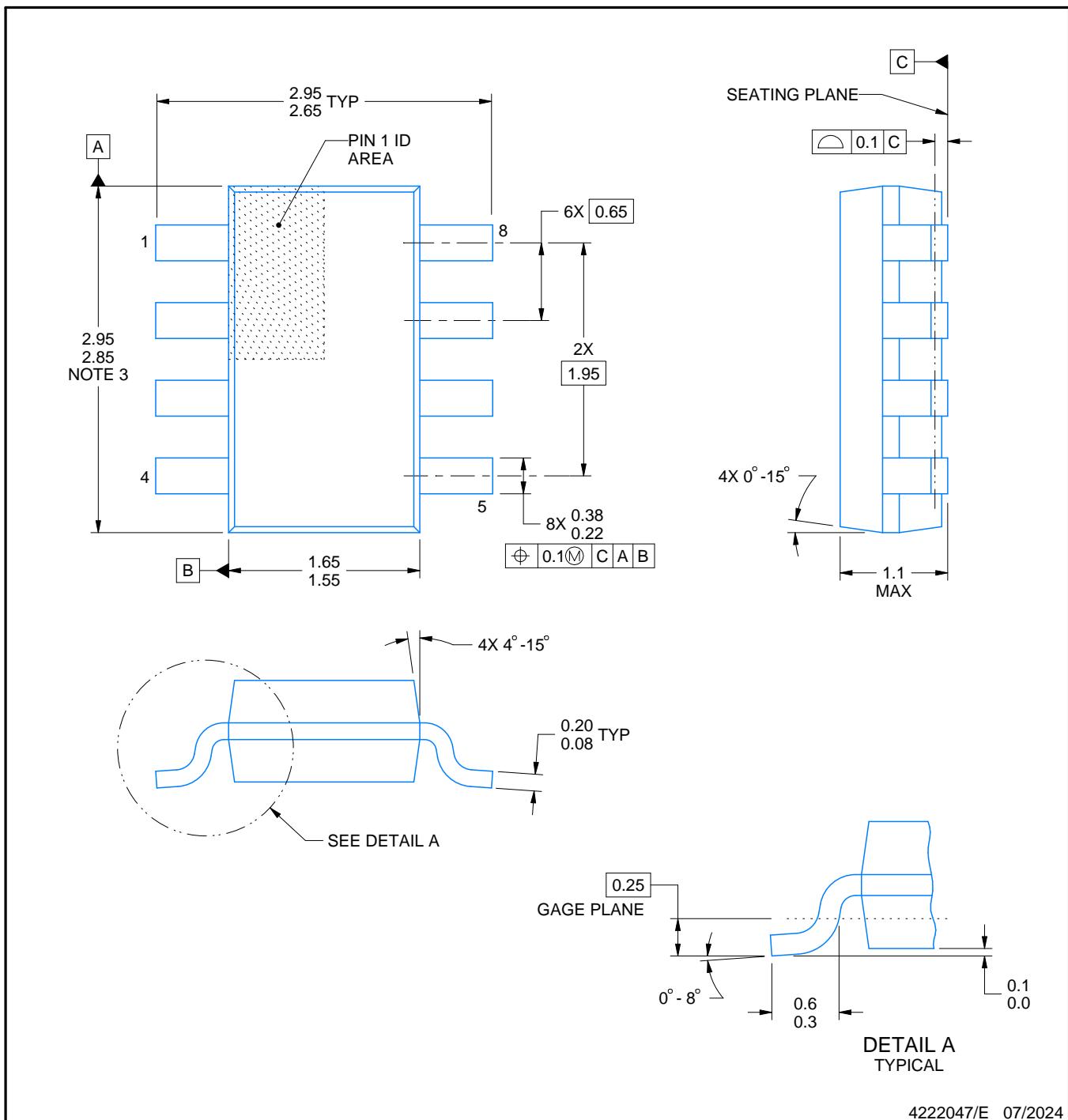
# PACKAGE OUTLINE

DDF0008A



SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



## NOTES:

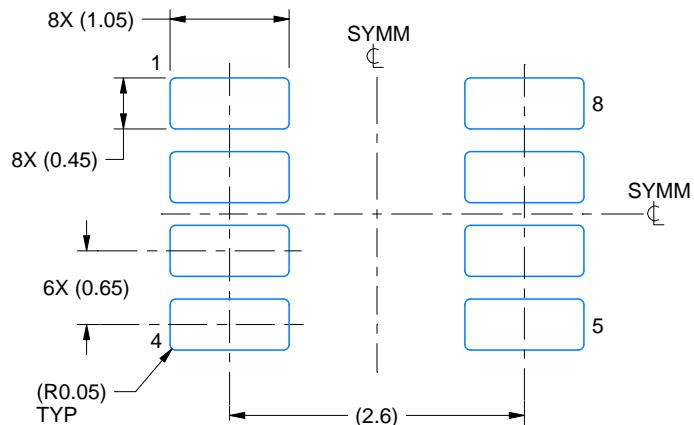
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

## EXAMPLE BOARD LAYOUT

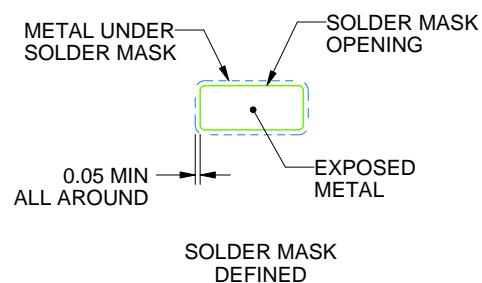
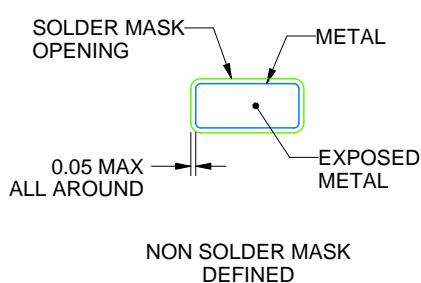
**DDF0008A**

## **SOT-23-THIN - 1.1 mm max height**

## PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



## SOLDER MASK DETAILS

4222047/E 07/2024

#### NOTES: (continued)

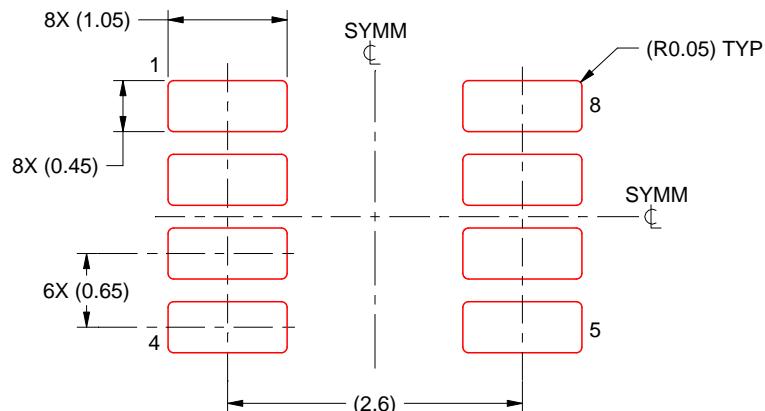
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

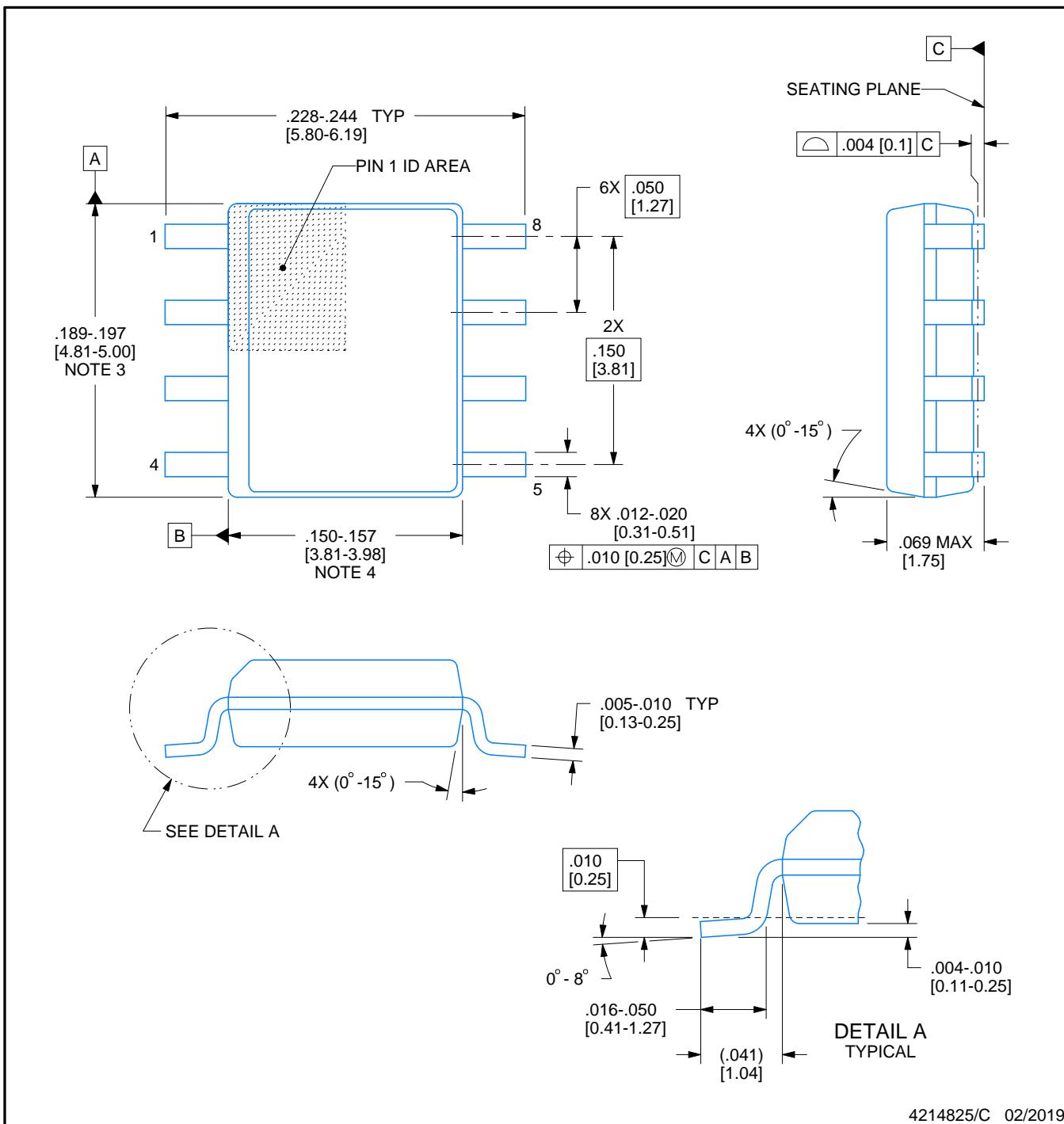
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



### NOTES:

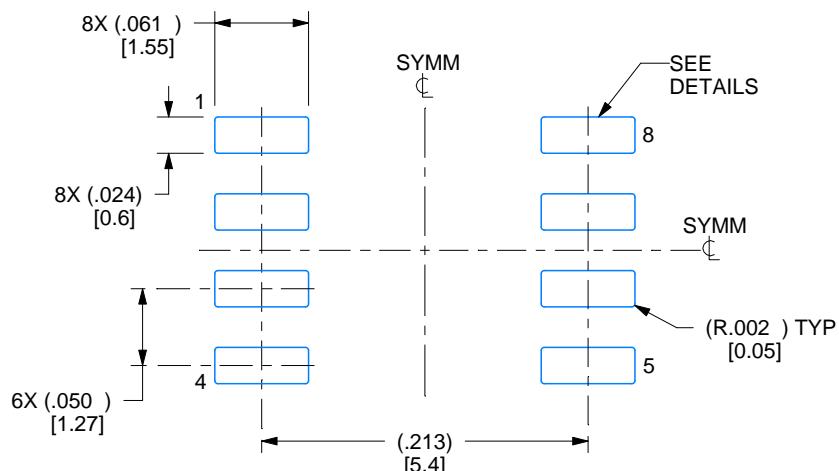
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

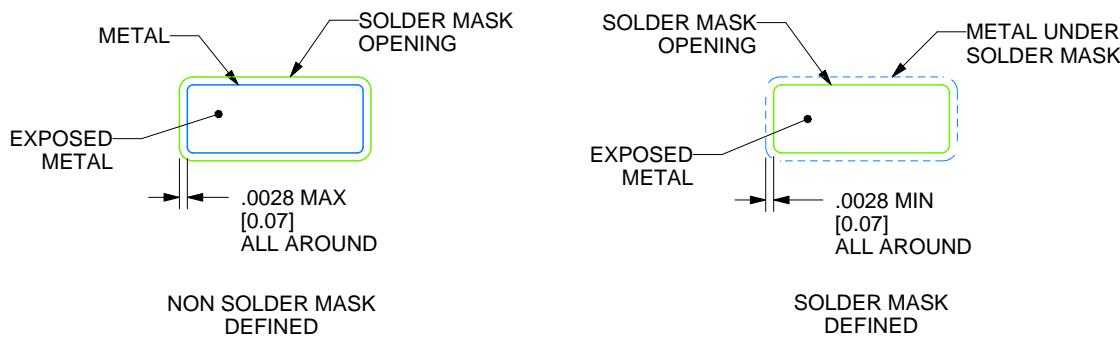
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

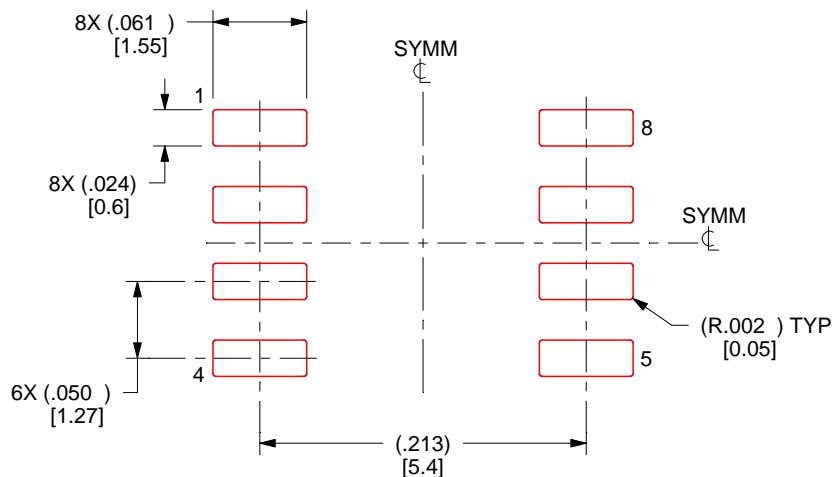
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

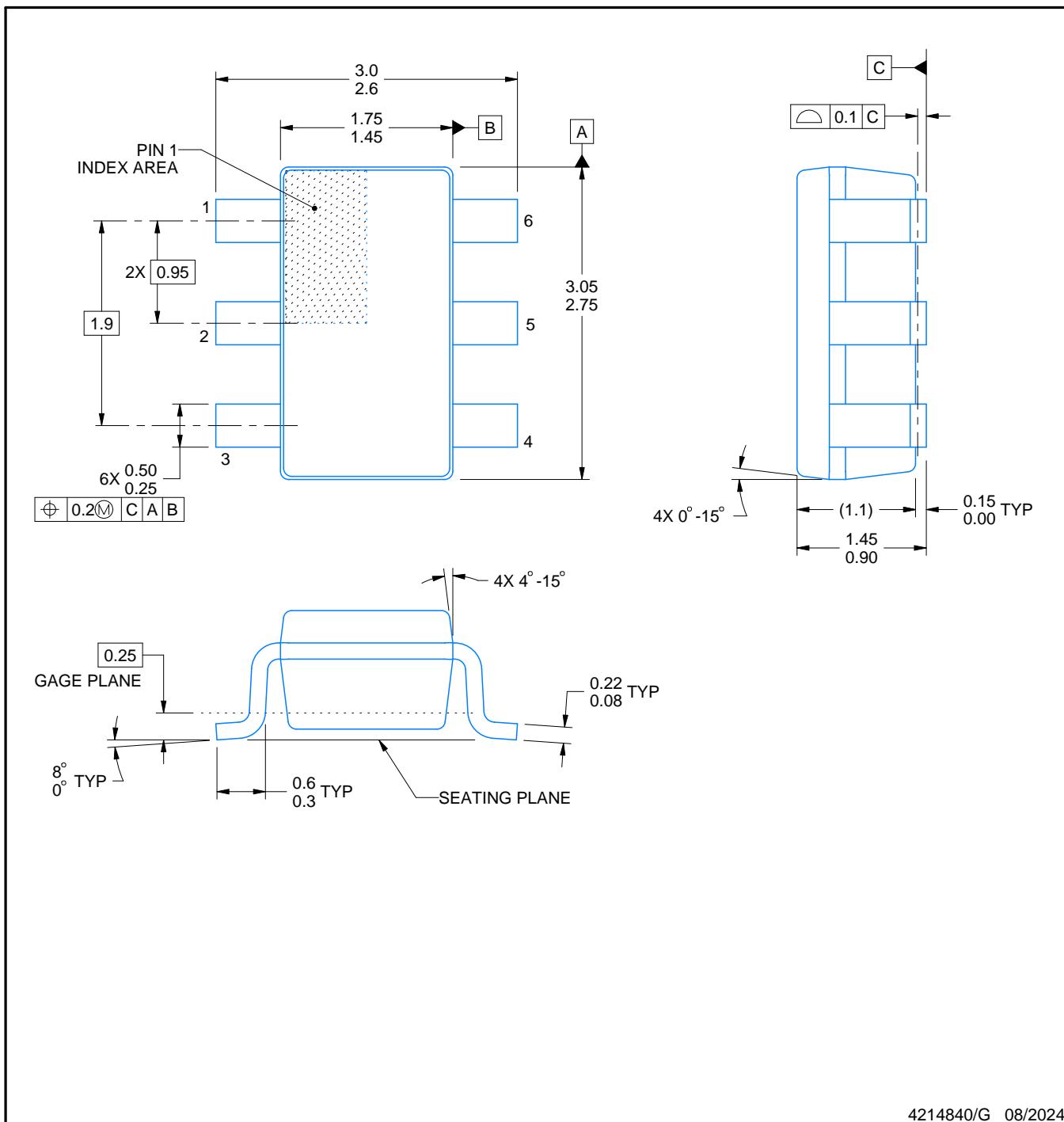
# PACKAGE OUTLINE

DBV0006A



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



## NOTES:

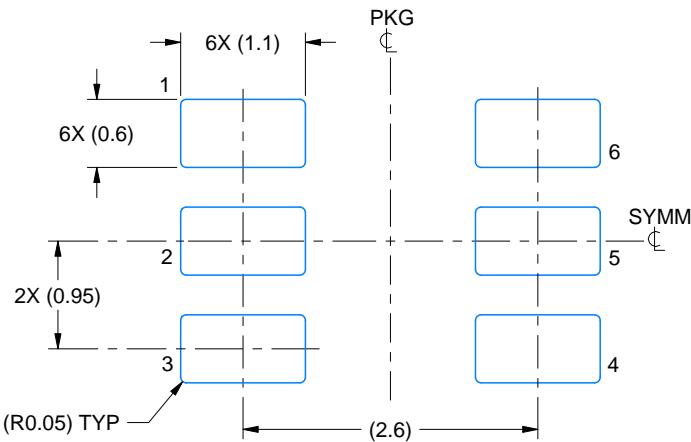
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

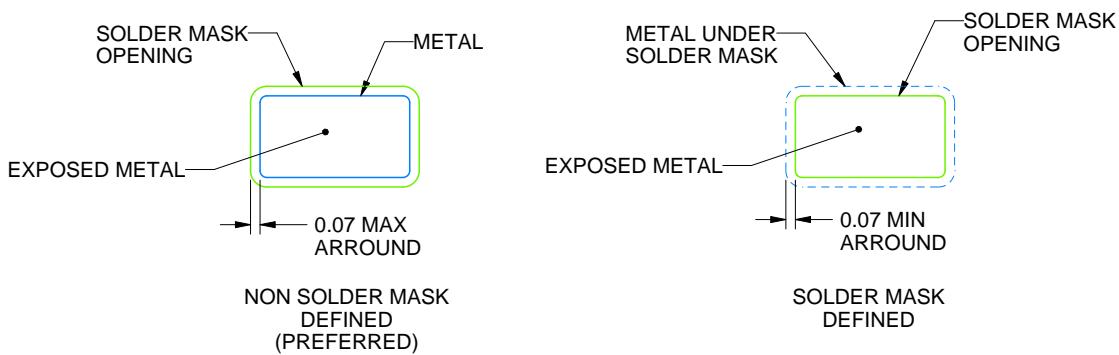
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

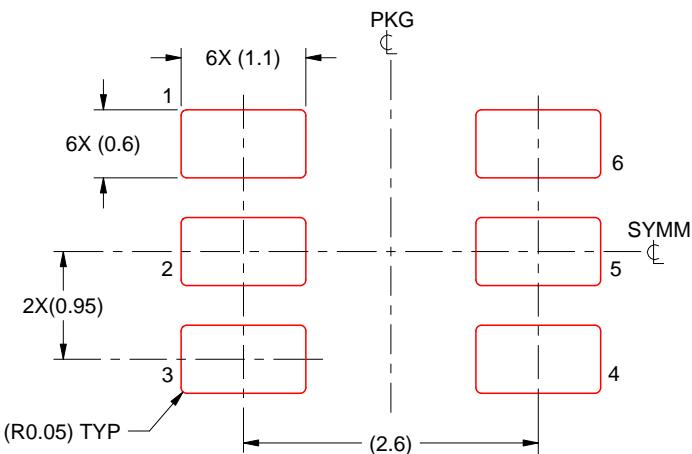
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

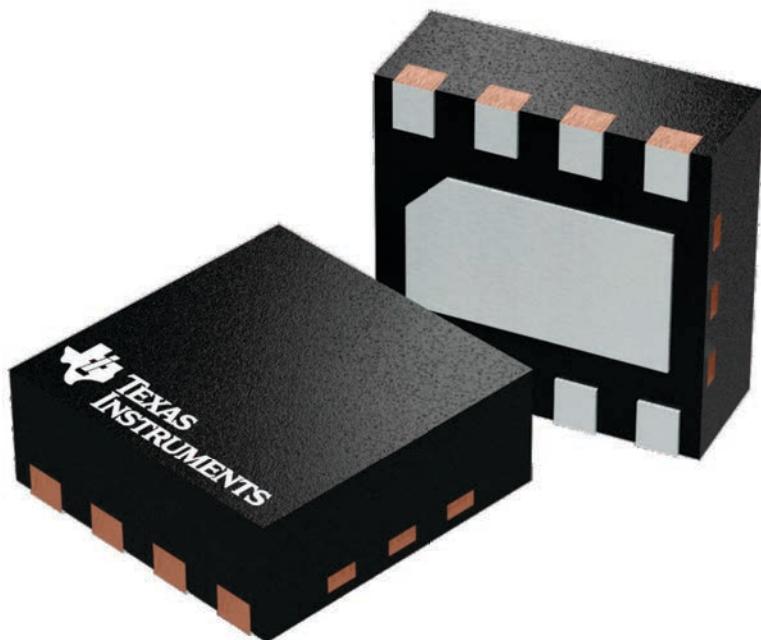
## DSG 8

## WSON - 0.8 mm max height

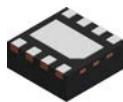
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224783/A

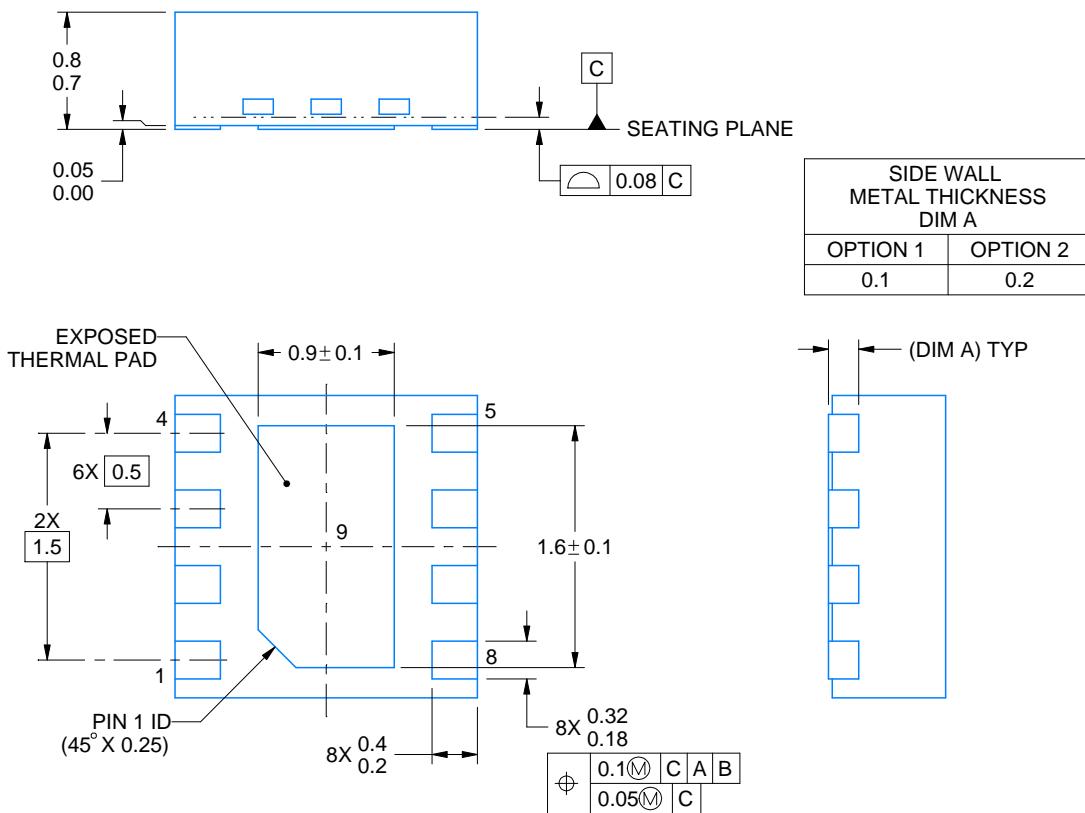
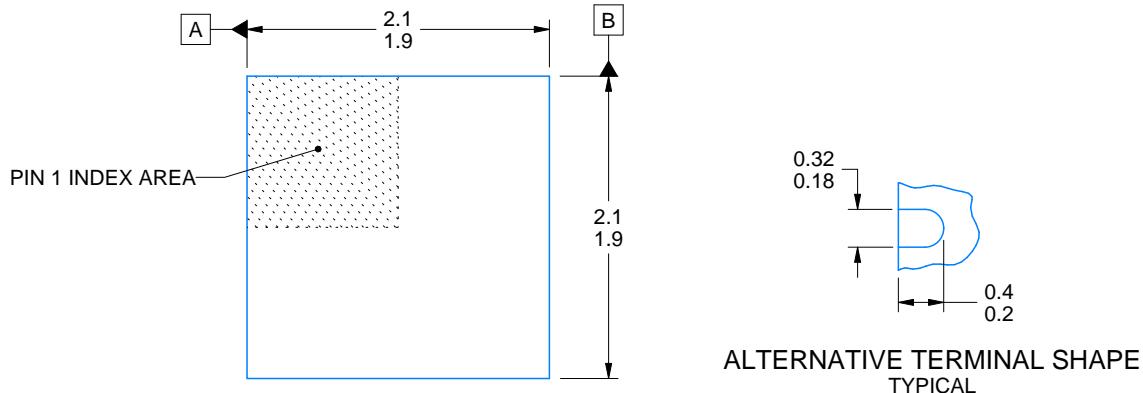


# PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4218900/E 08/2022

## NOTES:

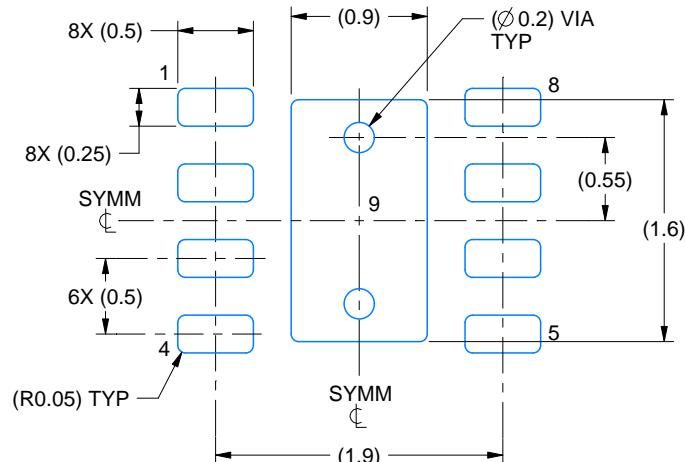
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

## EXAMPLE BOARD LAYOUT

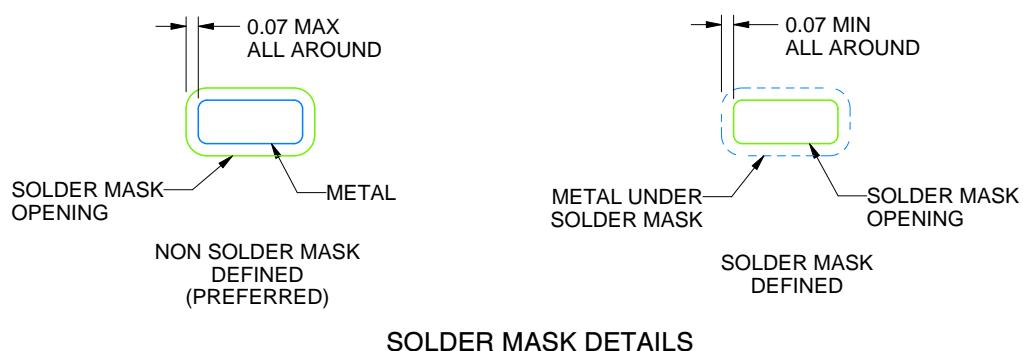
**DSG0008A**

## WSON - 0.8 mm max height

## PLASTIC SMALL OUTLINE - NO LEAD



## LAND PATTERN EXAMPLE



4218900/E 08/2022

#### NOTES: (continued)

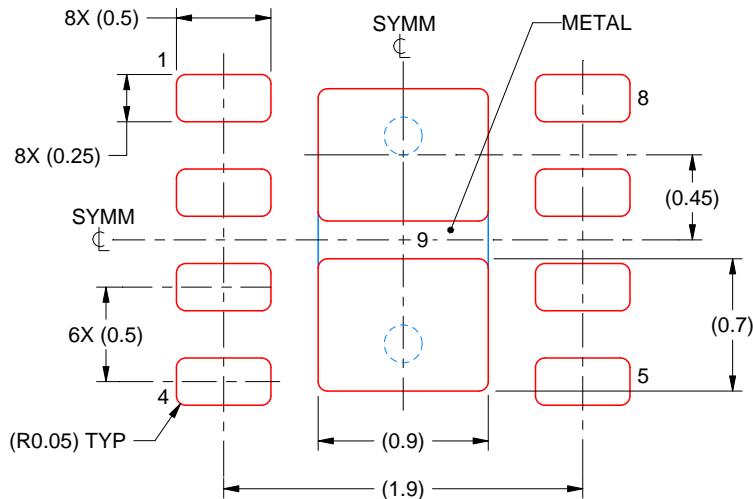
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:  
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

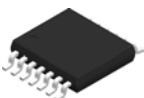
4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

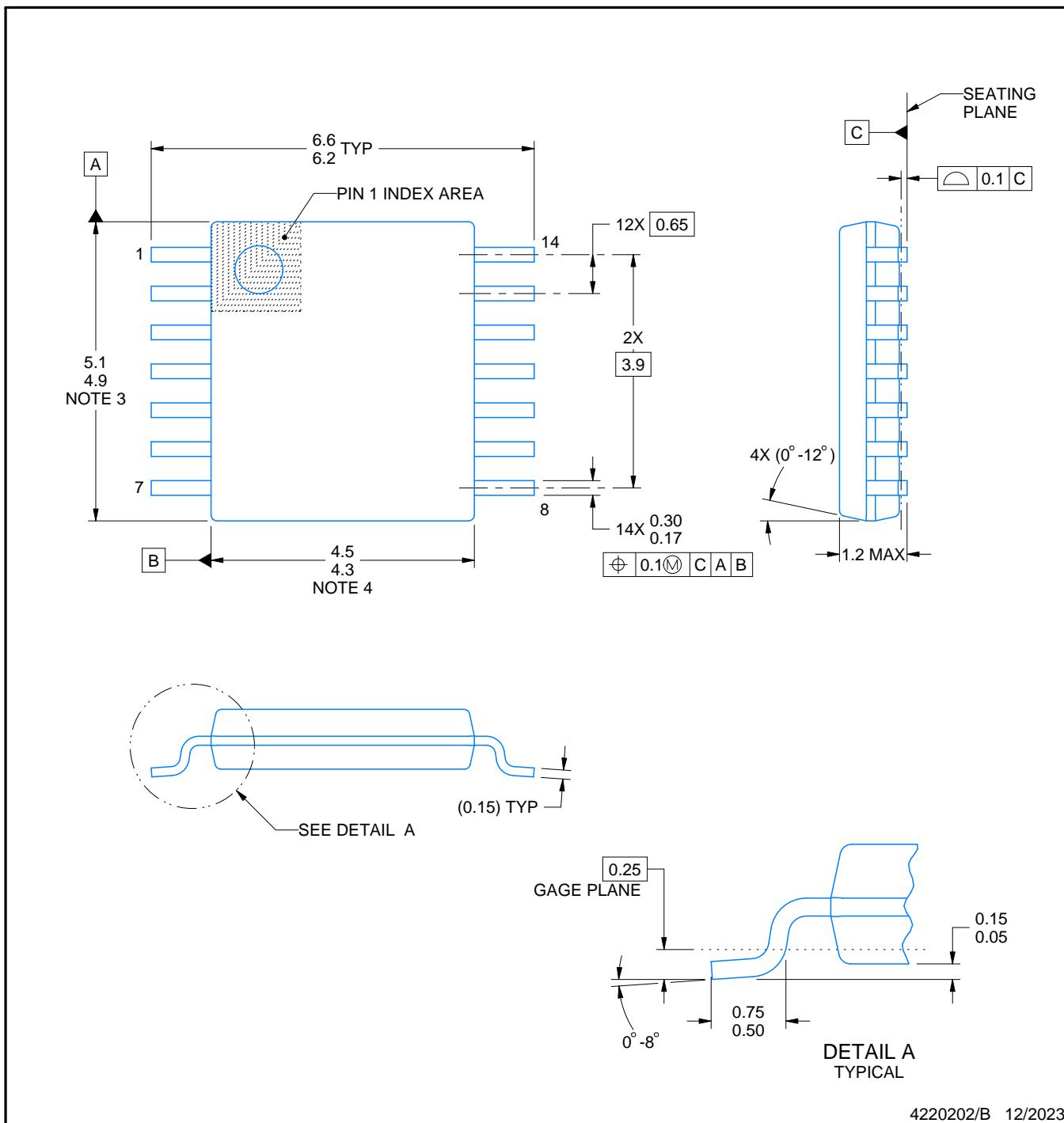
# PACKAGE OUTLINE

PW0014A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

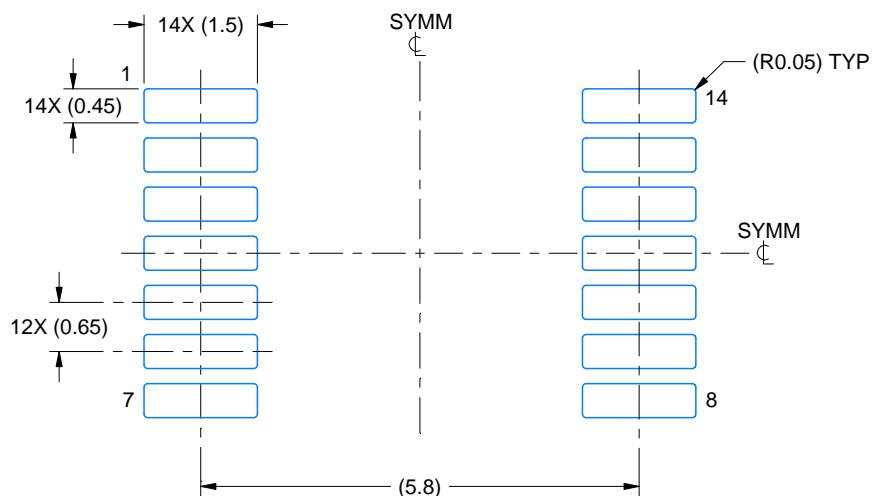
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

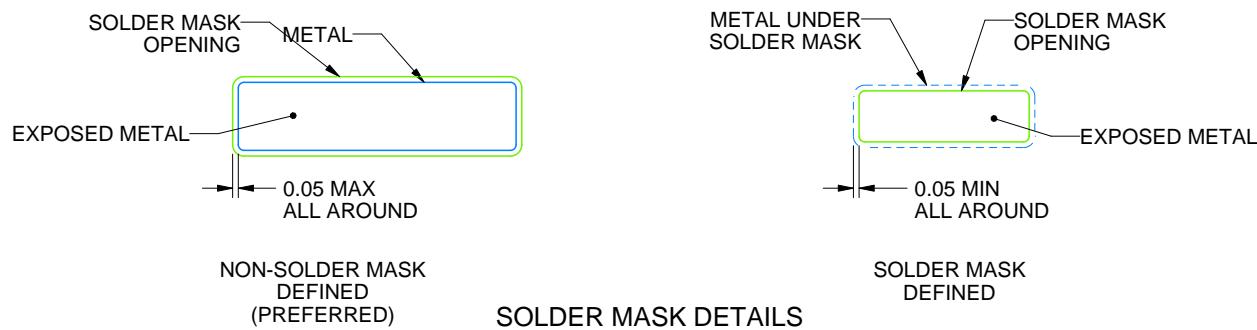
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

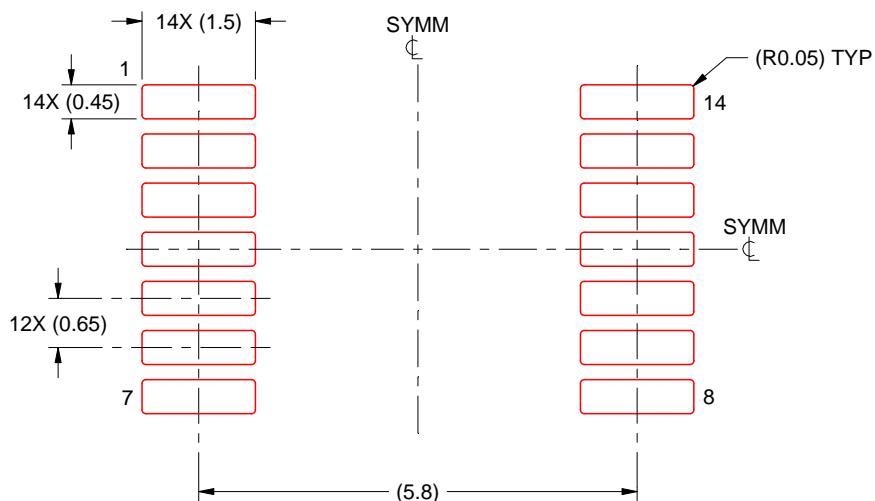
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

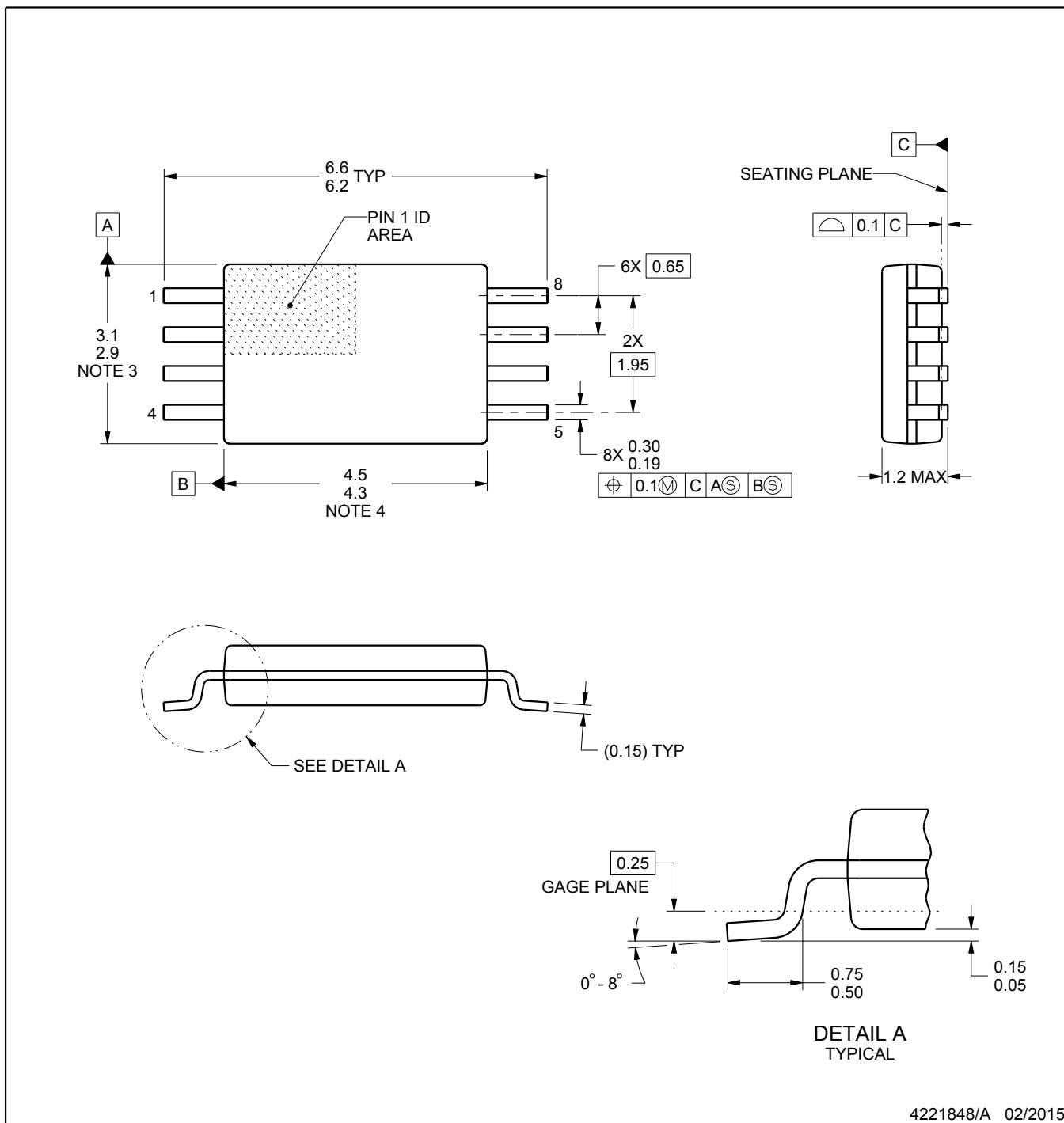
# PACKAGE OUTLINE

PW0008A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

## NOTES:

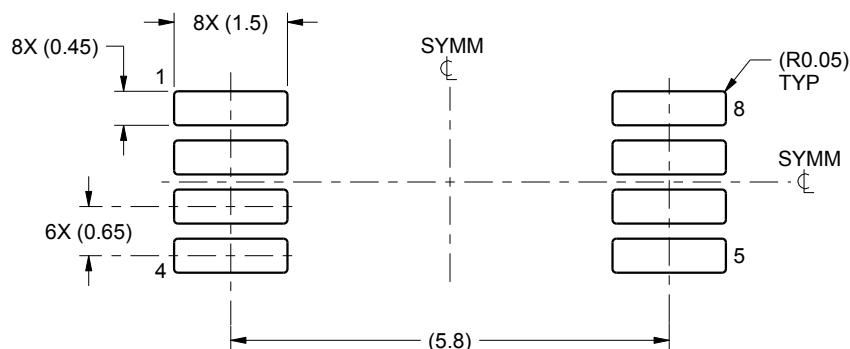
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

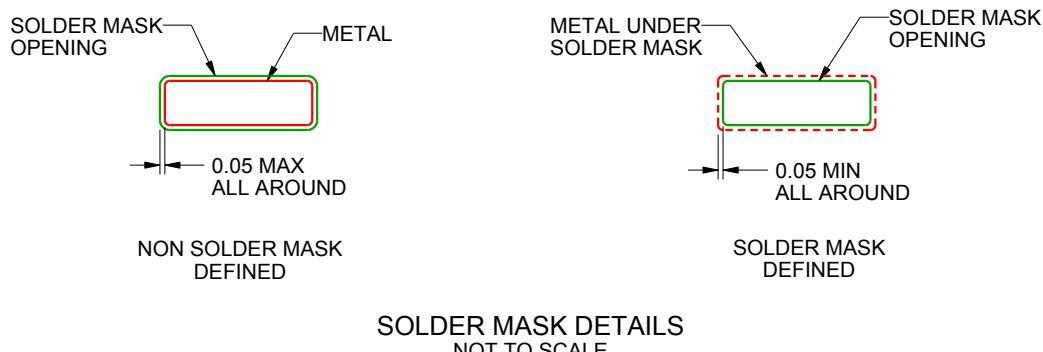
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



4221848/A 02/2015

NOTES: (continued)

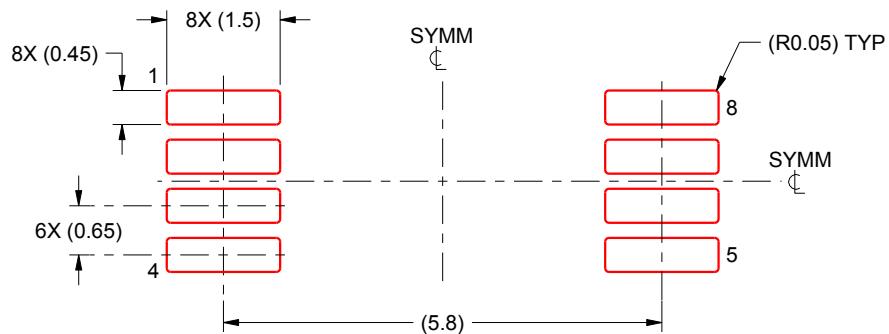
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

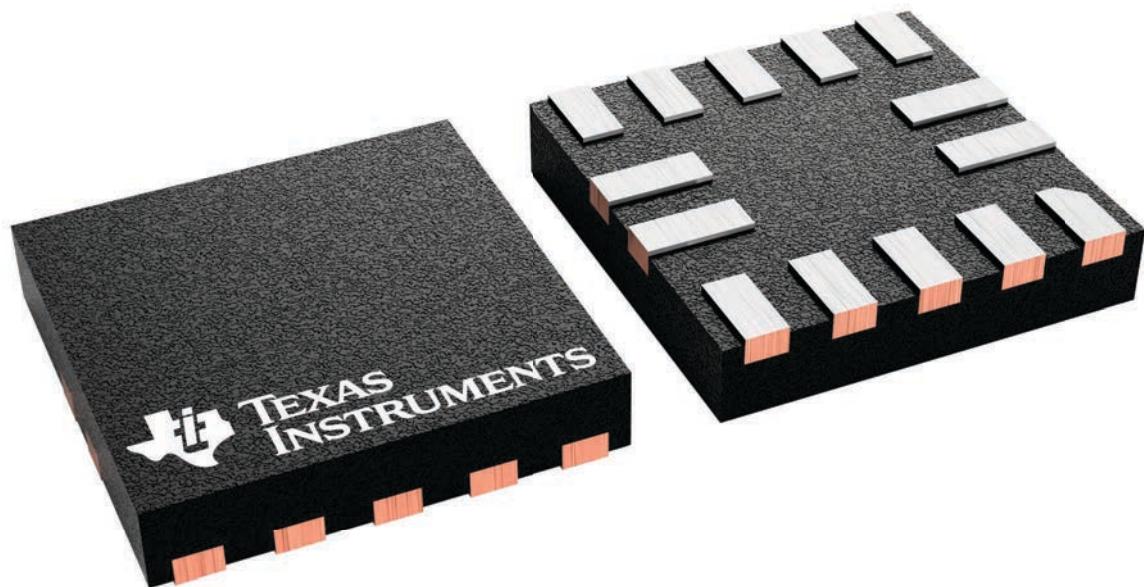
## RUC 14

## X2QFN - 0.4 mm max height

2 x 2, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



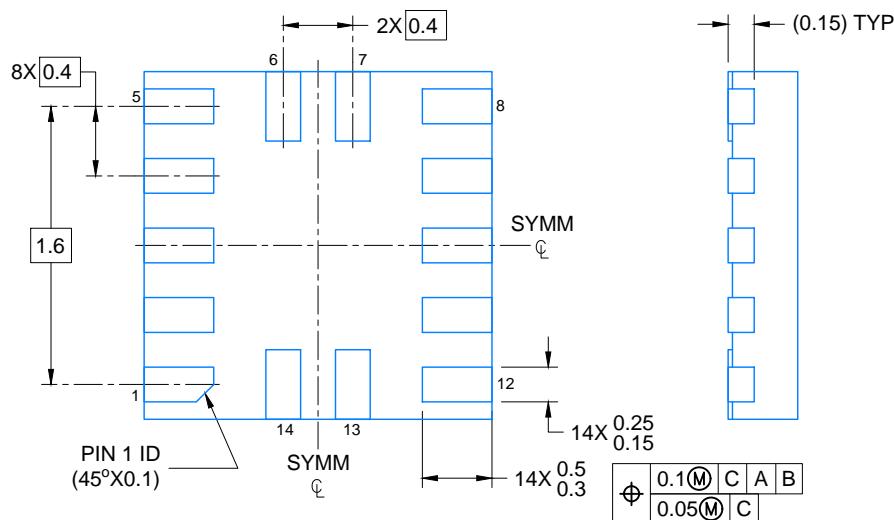
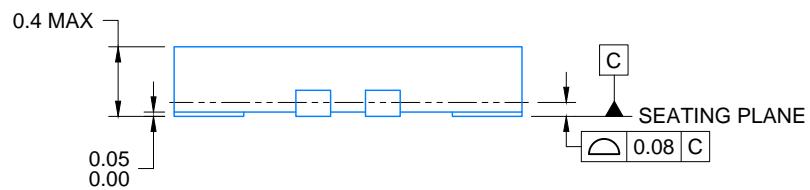
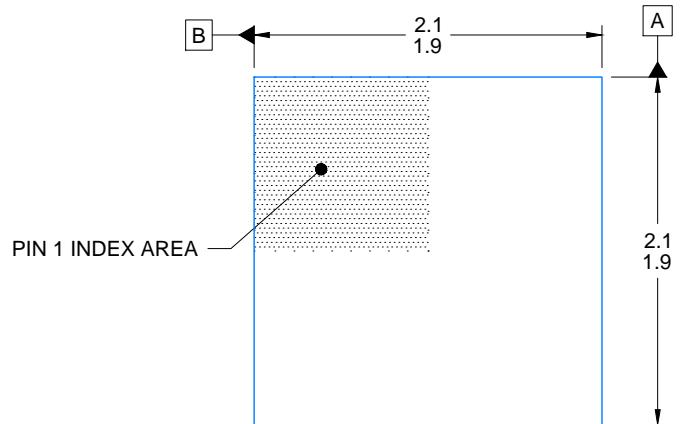
4229871/A

RUC0014A

# PACKAGE OUTLINE

X2QFN - 0.4 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



4220584/A 05/2019

NOTES:

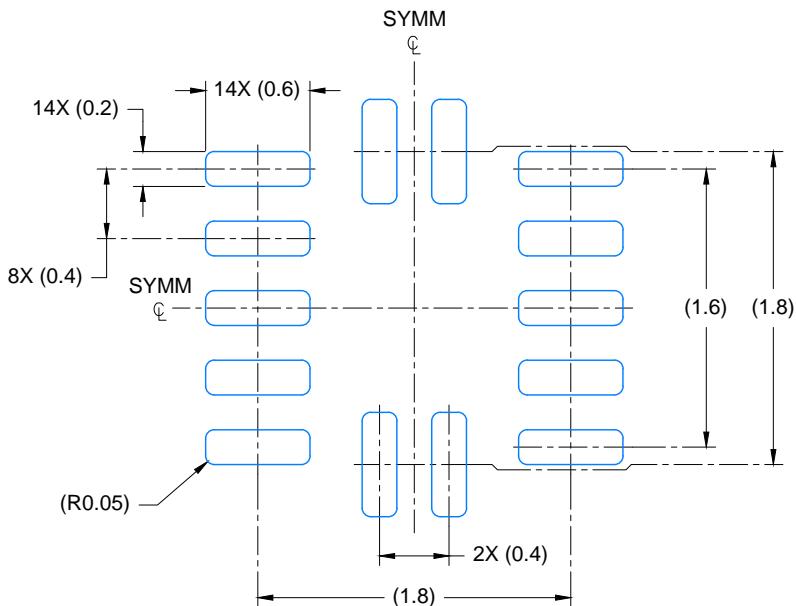
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

X2QFN - 0.4 mm max height

RUC0014A

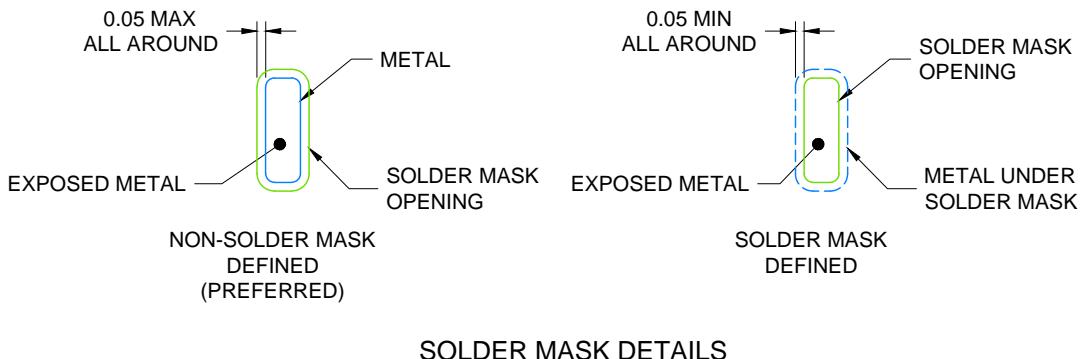
PLASTIC QUAD FLAT PACK- NO LEAD



## LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 23X



## SOLDER MASK DETAILS

4220584/A 05/2019

NOTES: (continued)

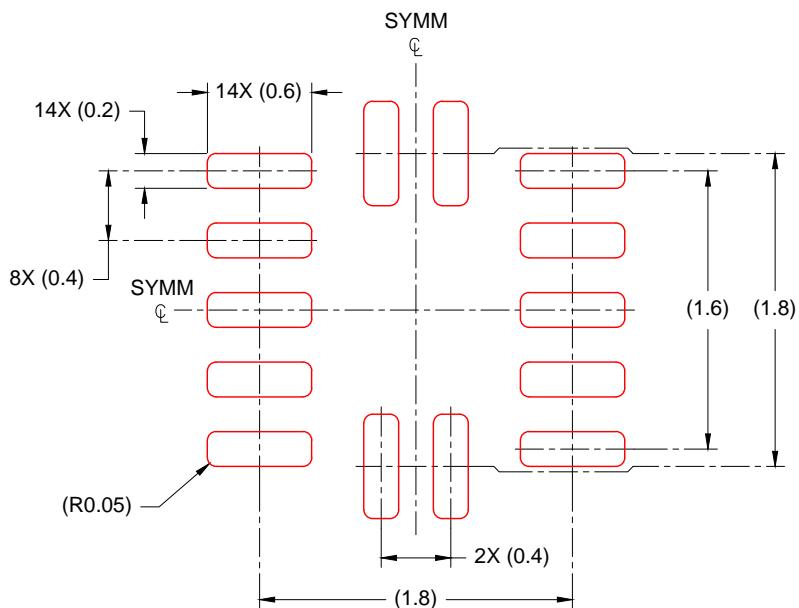
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

X2QFN - 0.4 mm max height

RUC0014A

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.100mm THICK STENCIL  
SCALE: 23X

4220584/A 05/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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