OPAx371D 125kHz, 650nA NanoPower, 1.5V Low Voltage, Decompensated Amplifier for Power Conscious Applications

1 Features

- Wide gain bandwidth product: 125kHz
- Low quiescent current: 650nA/ch
- Operational from supply voltage as low as 1.5V
- Low integrated noise (0.1Hz - 10Hz): 3.9μV_{p-p}
- Low input offset voltage: ±0.3mV
- Low input bias current: 500fA
- Rail-to-rail input and output
- Decompensated, gain ≥ 10V/V (stable)
- Integrated RFI and EMI filters
- Extended industrial temperature range: –40°C to 125°C

2 Applications

- Portable electronics
- Medical sensor patch
- CO Detector
- Active filters
- Audio microphone preamplifier
- Low-side current sensing
- Motion detector (PIR, uWave, and so forth)
- Pulse oximeter

3 Description

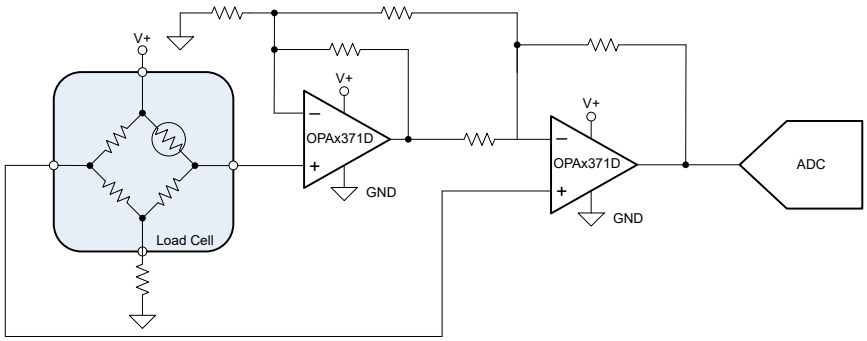
The OPAx371D family includes single (OPA371D), dual (OPA2371D), and quad (OPA4317D) decompensated operational amplifiers optimized for high efficiency in ultra-low-voltage applications. Operating from 1.5V to 5.5V with rail-to-rail input and output swing, this family of amplifiers deliver an exceptional gain bandwidth of 125kHz with only 650nA of quiescent current. The OPAx371D enables high gain circuit configurations and longevity in battery powered systems. The availability of miniature packages also allow this amplifier family to be used effectively in high density board applications.

The OPAx371D high gain bandwidth eliminates the need for cascaded amplifier stages in signal conditioning and filtering applications such as ECG patches, motion detectors, and personal electronics, simplifying design while reducing both board space and overall system power consumption.

Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE(2)	PACKAGE SIZE(3)
OPA371D	Single	DBV (SOT-23, 5)	2.9mm × 2.8mm
		DCK (SC70, 5)	2mm × 2.1mm
		DQN (SOT-5X3, 5)(1)	1mm × 1mm
OPA2371D	Dual	D (SOIC, 8)(1)	4.9mm × 6mm
		DSG (WSON, 8)(1)	2mm × 2mm
		DGK (VSSOP, 8)(1)	3mm × 4.9mm
OPA4371D	Quad	PW (TSSOP, 14)(1)	5mm × 6.4mm

(1) Product preview (not Production Data).
(2) For more information, see Section 10.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Bridge Amplifier Circuit

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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4 Pin Configuration and Functions

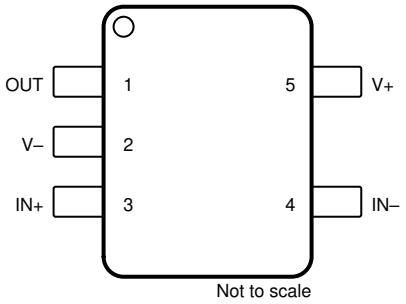


Figure 4-1. OPA371D DBV Package
5-Pin SOT-23
Top View

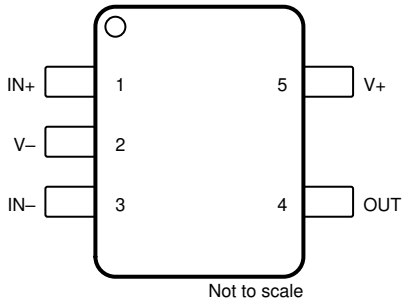


Figure 4-2. OPA371D DCK Package
5-Pin SC70
Top View

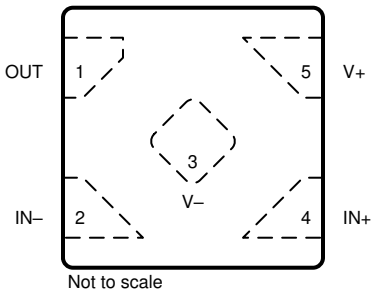


Figure 4-3. OPA371D DQN Package
5-Pin SOT-5X3
Top View

Table 4-1. Pin Functions: OPA371D

PIN				TYPE (1)	DESCRIPTION
NAME	NO.				
	SOT-23	SC70	SOT-5X3		
IN–	4	3	2	I	Inverting input
IN+	3	1	2	I	Noninverting input
OUT	1	4	1	O	Output
V–	2	2	3	I	Negative (low) supply or ground (for single-supply operation)
V+	5	5	5	I	Positive (high) supply

(1) I = input, O = output

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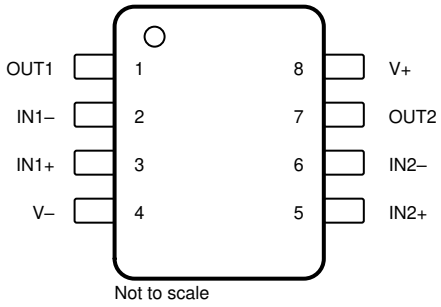
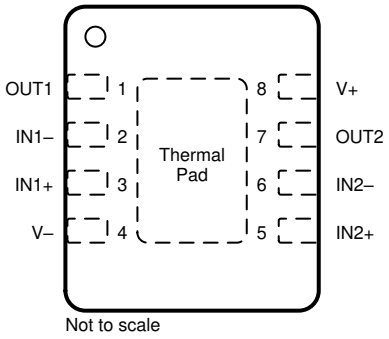


Figure 4-4. OPA2371D D and DGK Packages 8-Pin SOIC and VSSOP Top View



Connect exposed thermal pad to V–. See Figure 4-5 for more information.

Figure 4-5. OPA2371D DSG Package 8-Pin WSON With Exposed Thermal Pad Top View

Table 4-2. Pin Functions: OPA2371D

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	I	Negative (low) supply or ground (for single-supply operation)
V+	8	I	Positive (high) supply

(1) I = input, O = output

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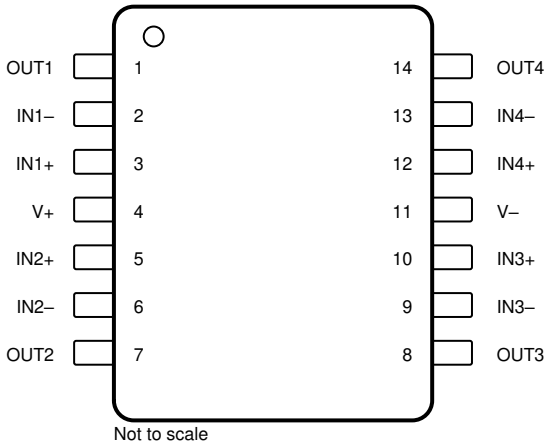


Figure 4-6. OPA4371D PW Package
14-Pin TSSOP
Top View

Table 4-3. Pin Functions: OPA4371D

PIN		TYPE[1]	DESCRIPTION
NAME	TSSOP		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
IN3–	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4–	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
NC	—	—	No internal connection
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V–	11	I or —	Negative (low) supply or ground (for single-supply operation)
V+	4	I	Positive (high) supply

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	Supply voltage, V_S = (V+) – (V–)	0	6.0	V
Signal input pins	Common-mode voltage(1) (2)	(V-) - 0.5	(V+) + 0.5	V
	Differential voltage(1) (2)		(V+) + 0.2	V
	Current (2)	–10	10	mA
Output short-circuit (3)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	1.5	5.5	V
C_{BYP}	Bypass capacitor on the power supply pins (1)	0.1		µF
T_A	Specified temperature	–40	125	°C

(1) For C_{BYP}, use low-ESR ceramic capacitors between each supply pin and ground. Only one C_{BYP} is sufficient for single supply operation. Ensure that C_{BYP} is placed as close to the device as possible and the supply trace routes through C_{BYP} before reaching the supply pin.

5.4 Thermal Information for Single Channel

THERMAL METRIC (1)		OPA371x			UNIT
		DBV (2) (SOT-23)	DCK (2) (SC70)	DQN(2) (SOT-5X3)	
		5 PINS	5 PINS	5 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	211.9	272.7	–	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	103.4	123.6	–	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	79.4	95.3	–	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	38	36.6	–	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	78.5	94.8	–	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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(2) This package option is preview.

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5.5 Electrical Characteristics: OPAx371D

For V_S = 1.5 V to 5.5 V (±0.75 V to ±2.75 V) at T_A = 25°C, G = 10V/V, R_F = 1.8MΩ, R_L = 1 MΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±0.3	±1.75	mV
			T_A = 0°C to 85°C			±1.8	
dV_{OS}/dT	Input offset voltage drift (1)		T_A = 0°C to 85°C		±0.58		µV/°C
PSRR	Input offset voltage versus power supply			79	95		dB
			T_A = –40°C to 125°C	79			
INPUT BIAS CURRENT							
I_B	Input bias current (1)				±0.5	±2	pA
			T_A = 0°C to 85°C			±80	
			T_A = –40°C to 125°C			±560	
I_{OS}	Input offset current (1)				±0.3	±1.5	pA
			T_A = 0°C to 85°C			±30	
			T_A = –40°C to 125°C			±150	
NOISE							
E_N	Input voltage noise	V_S = 5.5V, f = 0.1 to 10Hz			3.9		μV_{PP}
e_N	Input voltage noise density	V_S = 5.5V, f = 1kHz	V_S = 5.5V, f = 1kHz		155		$nV/\sqrt{Hz}$
i_N	Input current noise density (2)	f = 1 kHz			5		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE							
V_I	Input voltage range(2)			(V–) – 0.1		(V+) + 0.2	V
			T_A = –40°C to 125°C	(V–)		(V+)	
CMRR	Common-mode rejection ratio	V_S = 5.5 V, (V–) ≤ V_{CM} ≤ (V+) – 0.7 V		78	94		dB
		V_S = 5.5 V, (V–) ≤ V_{CM} ≤ (V+) – 0.7 V (1)	T_A = 0°C to 85°C	76			
		V_S = 5.5 V, (V–) ≤ V_{CM} ≤ (V+) – 0.7 V (1)	T_A = –40°C to 125°C	74			
		V_S = 1.5 V, (V–) ≤ V_{CM} ≤ (V+) – 0.7 V (1)		68	90		
		V_S = 1.5 V, (V–) ≤ V_{CM} ≤ (V+) – 0.7 V (1)	T_A = 0°C to 85°C	68			
		V_S = 1.5 V, (V–) ≤ V_{CM} ≤ (V+) – 0.7 V (1)	T_A = –40°C to 125°C	67			
		V_S = 5.5 V, (V–) ≤ V_{CM} ≤ (V+)		65	83		
		V_S = 5.5 V, (V–) ≤ V_{CM} ≤ (V+)	T_A = 0°C to 85°C	63			
		V_S = 5.5 V, (V–) ≤ V_{CM} ≤ (V+)	T_A = –40°C to 125°C	63			
INPUT IMPEDANCE							
Z_{ID}	Differential				80 || 0.3		GΩ || pF
Z_{ICM}	Common-mode				100 || 2.2		
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 5.5 V, (V–) + 0.10 V < V_O < (V+) – 0.10 V, R_L = 100kΩ to V_S / 2		110	133		dB
		V_S = 5.5 V, (V–) + 0.10 V < V_O < (V+) – 0.10 V, R_L = 100kΩ to V_S / 2	T_A = 0°C to 85°C	108			
		V_S = 5.5 V, (V–) + 0.10 V < V_O < (V+) – 0.10 V, R_L = 100kΩ to V_S / 2	T_A = –40°C to 125°C	96			
		V_S = 1.5 V, (V–) + 0.10 V < V_O < (V+) – 0.10 V, R_L = 100kΩ to V_S / 2		94	122		
		V_S = 5.5 V, (V–) + 0.25 V < V_O < (V+) – 0.25 V, R_L = 10kΩ to V_S / 2 (1)		116	130		
		V_S = 1.5 V, (V–) + 0.25 V < V_O < (V+) – 0.25 V, R_L = 10kΩ to V_S / 2 (1)		103	118		
FREQUENCY RESPONSE							

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5.5 Electrical Characteristics: OPAx371D (continued)

For V_S = 1.5 V to 5.5 V (±0.75 V to ±2.75 V) at T_A = 25°C, G = 10V/V, R_F = 1.8MΩ, R_L = 1 MΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

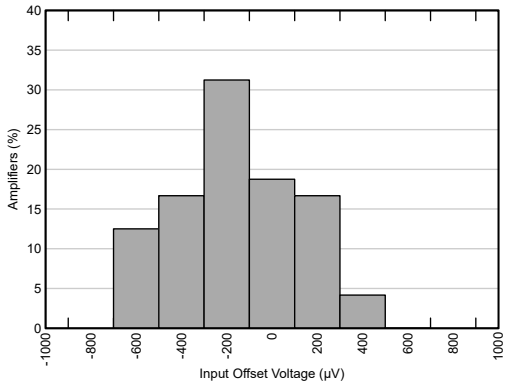
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GBW	Gain-bandwidth product	V_S = 5.5 V, G = 100 V/V, C_L= 10pF			125		kHz
SR	Slew rate	V_S = 5.5 V, G = +1, V_{STEP} = 4V_{PP}, C_L= 10pF			70		mV/µs
t_S	Settling time	To 0.1%, V_S = 5.5 V, V_{STEP} = 2 V, C_L= 20pF	To 0.1%, V_S = 5.5 V, V_{STEP} = 2 V		330		µs
PM	Phase Margin	V_S = 5.5 V, C_L = 30 pF			63		°
C_L Drive	Cap Load Drive	Phase Margin = 45°			80		pF
$t_{overload}$	Overload recovery time	V_{IN} × gain > V_S			50		µs
EMIRR	Electro-magnetic interference rejection ratio	f = 1.8 GHz, V_{IN_EMIRR} = 100 mV			91		dB
OUTPUT							
V_o	Voltage output swing from rail	V_S = 5.5V, R_L = 100kΩ to V_S / 2	V_S = 5.5V, R_L = 100kΩ to V_S / 2		2.5	10	mV
		V_S = 5.5V, R_L = 100kΩ to V_S / 2	T_A = –40°C to 125°C			15	
		V_S = 1.5V, R_L = 100kΩ to V_S / 2	V_S = 1.5V, R_L = 100kΩ to V_S / 2		1	12	
		V_S = 1.5V, R_L = 100kΩ to V_S / 2	T_A = –40°C to 125°C			17	
I_{SC}	Short-circuit current (3)	V_S = 5.5 V		±11.5	±18		mA
			T_A = –40°C to 125°C	±5.5			
Z_O	Open-loop output impedance	f = 100 Hz	f = 100 Hz		93		kΩ
	Power-on time	V_S = 0 to 5.5 V, 1% settling			0.7		ms
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = 1.5 V, I_O = 0 A, OPA371D			665	900	nA
			T_A = –40°C to 125°C			1000	
		V_S = 1.5 V, I_O = 0 A, OPA2371D/OPA4371D			630	900	
			T_A = –40°C to 125°C			1000	
		V_S = 5.5 V, I_O = 0 A, OPA371D			680	905	
			T_A = –40°C to 125°C			1030	
		V_S = 5.5 V, I_O = 0 A, OPA2371D/OPA4371D			650	905	
			T_A = –40°C to 125°C			1030	
SHUTDOWN							

(1) Max / Min limit is specified based on characterization results.
(2) Specified based on design simulation results
(3) Short circuit current specified here is average of sourcing and sinking short circuit currents

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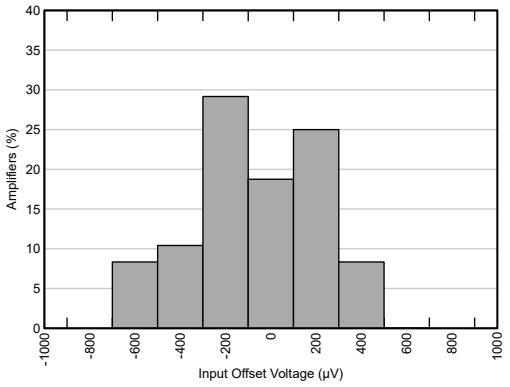
5.6 Typical Characteristics

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, G = 10V/V, R_F= 1.8MΩ, R_L = 1MΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



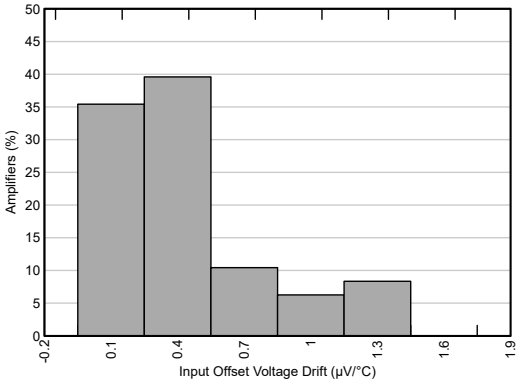
48 units Mean = -3.5µV Sigma = 290µV

Figure 5-1. Offset Voltage Histogram



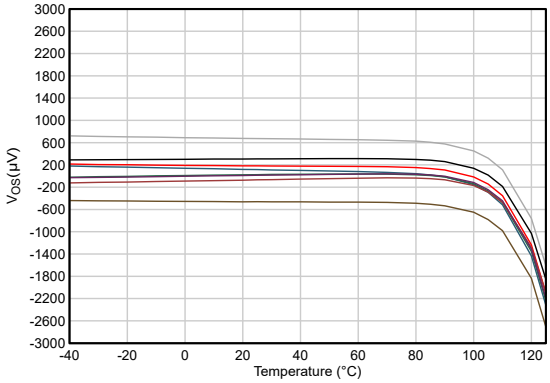
48 units Mean = -0.4µV Sigma = 275µV

Figure 5-2. Offset Voltage Histogram (VS = 1.5V)



48 units Mean = 0.5µV/°C Sigma = 0.33µV/°C

Figure 5-3. Offset Voltage Drift Histogram (0°C to 85°C)



V_{CM} = V–

Figure 5-4. Input Offset Voltage vs Temperature

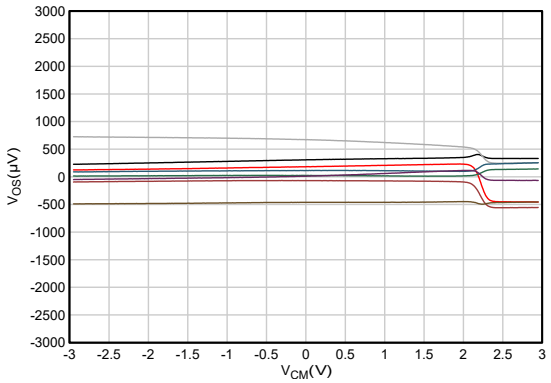


Figure 5-5. Offset Voltage vs Common-Mode

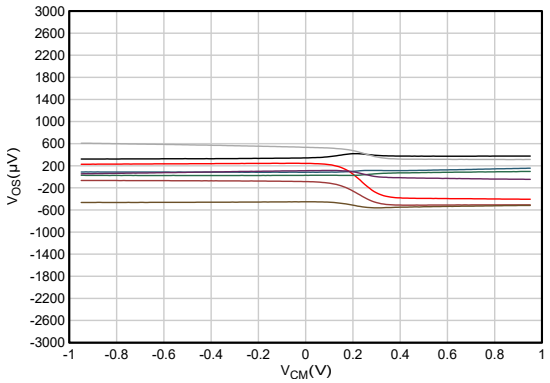
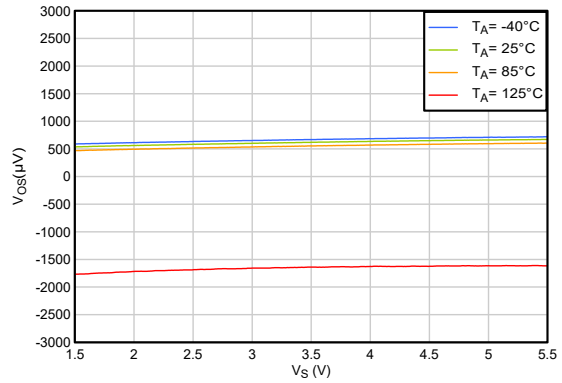


Figure 5-6. Offset Voltage vs Common-Mode (V_S = 1.5V)

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5.6 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, G = 10V/V, R_F= 1.8MΩ, R_L = 1MΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_{CM} = (V–)

Figure 5-7. Offset Voltage vs Supply Voltage

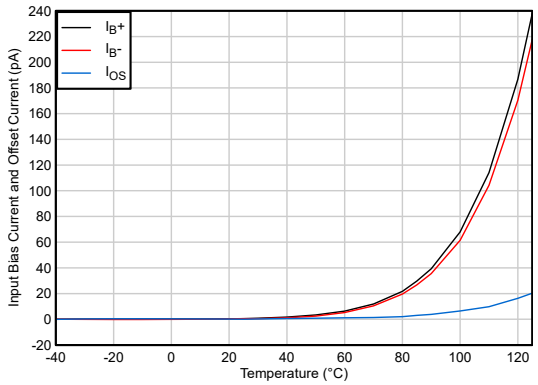


Figure 5-8. I_B and I_{OS} vs Temperature

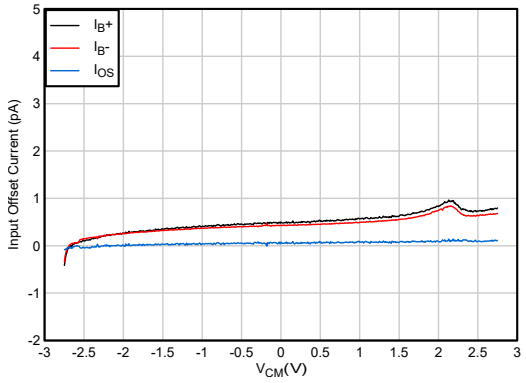
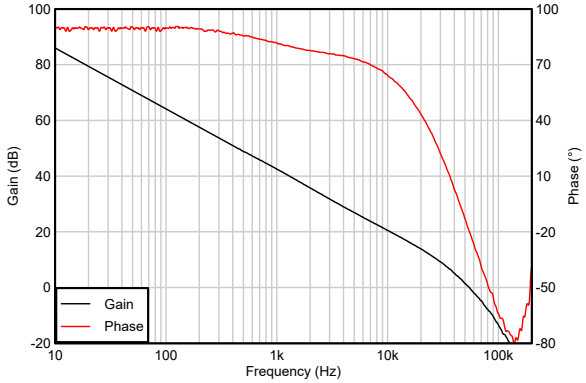


Figure 5-9. I_B and I_{OS} vs Common-Mode Voltage



R_L = 1MΩ, C_L = 20pF

Figure 5-10. Open-Loop Gain and Phase vs Frequency

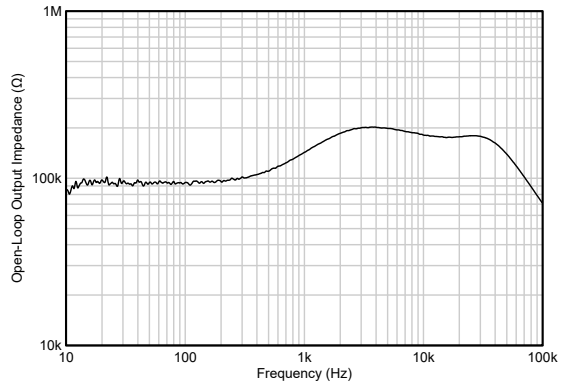
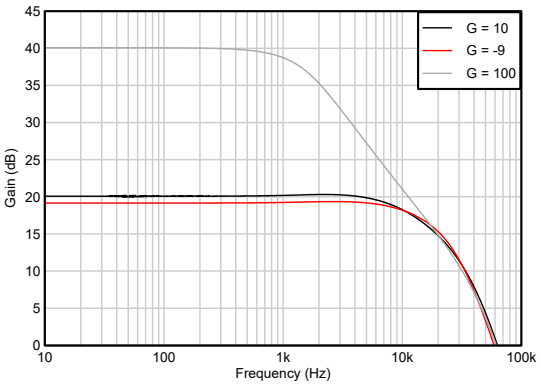


Figure 5-11. Open-Loop Output Impedance vs Frequency



C_L = 20pF

Figure 5-12. Closed-Loop Gain vs Frequency

5.6 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, G = 10V/V, R_F= 1.8MΩ, R_L = 1MΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

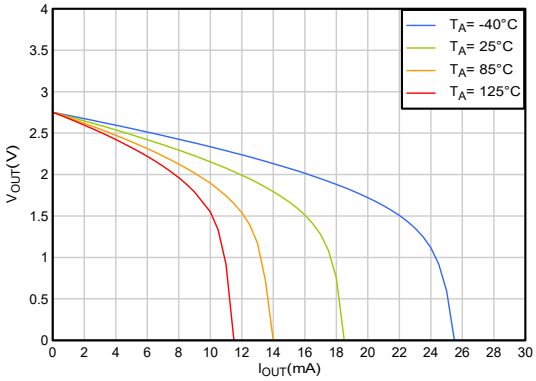


Figure 5-13. Output Voltage vs Output Current (Sourcing)

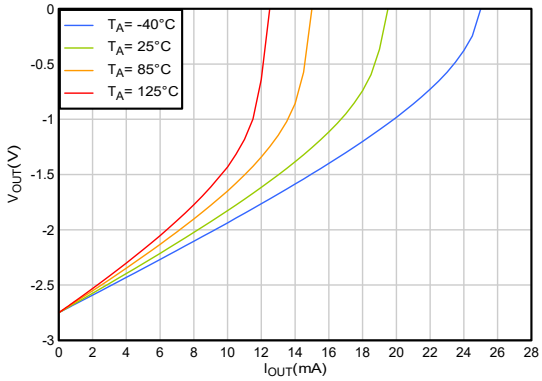


Figure 5-14. Output Voltage vs Output Current (Sinking)

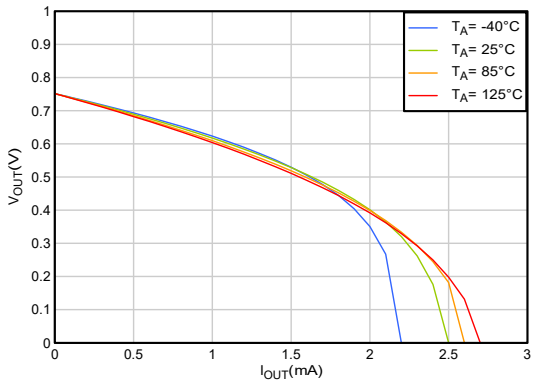


Figure 5-15. Output Voltage vs Output Current (V_S=1.5V)

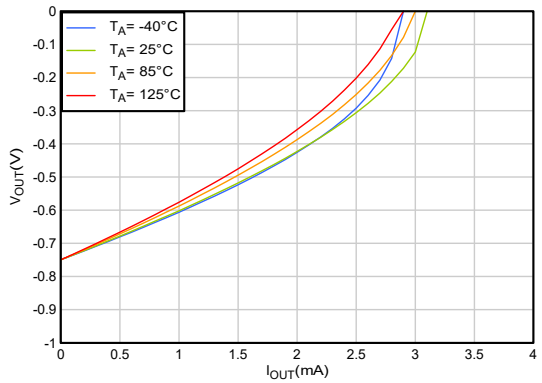


Figure 5-16. Output Voltage vs Output Current (V_S=1.5V)

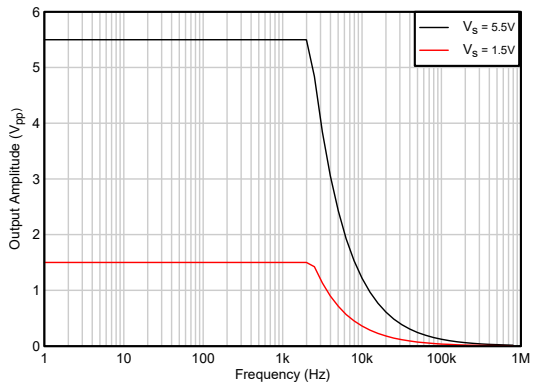


Figure 5-17. Max Output Voltage vs Frequency

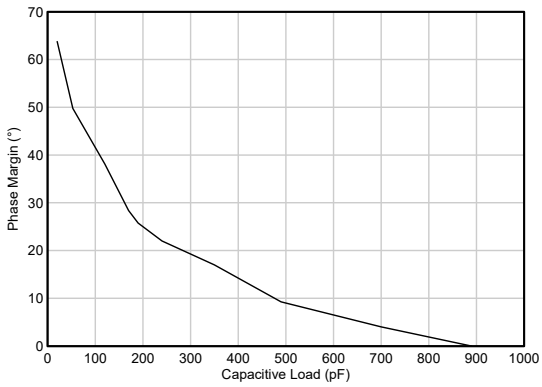


Figure 5-18. Phase Margin vs Capacitive Load

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5.6 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, G = 10V/V, R_F= 1.8MΩ, R_L = 1MΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

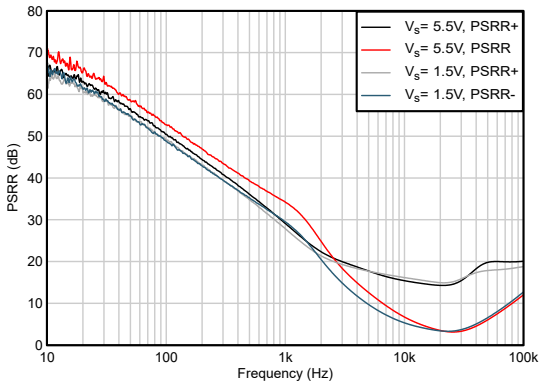


Figure 5-19. PSRR vs Frequency

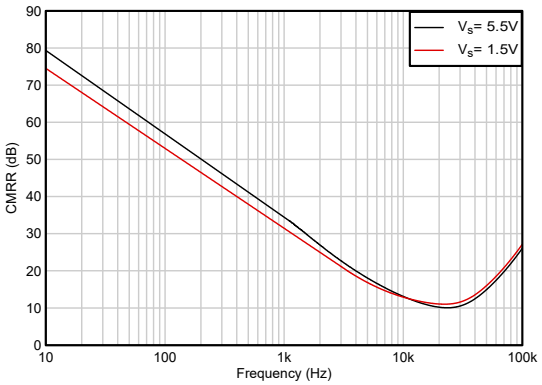
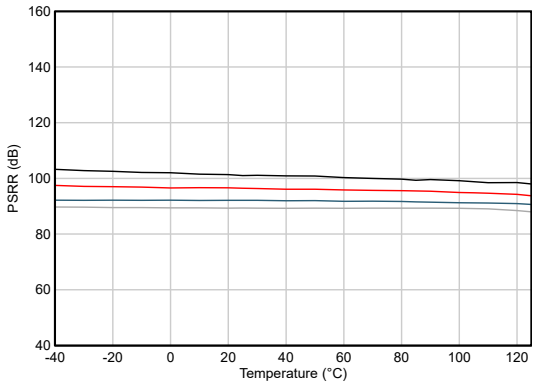


Figure 5-20. CMRR vs Frequency



3 units, V_S = 1.5V to 5.5V

Figure 5-21. DC PSRR vs Temperature

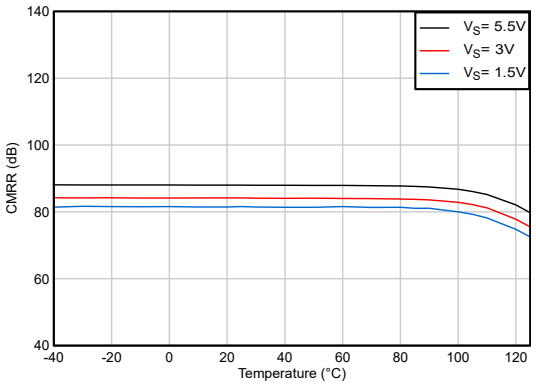


Figure 5-22. DC CMRR vs Temp ((V–) ≥ VCM ≥ (V+) - 0.7V)

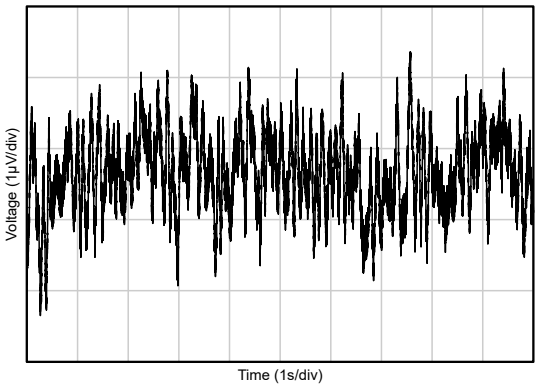


Figure 5-23. 0.1Hz to 10Hz Voltage Noise in Time Domain

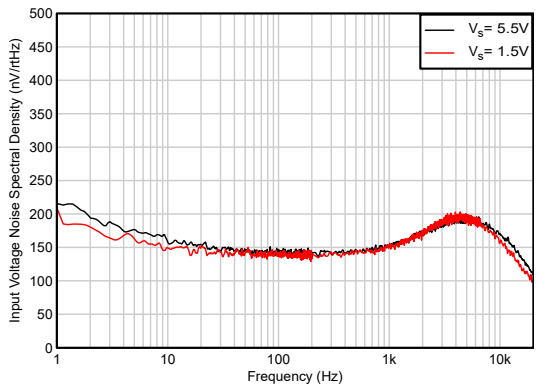
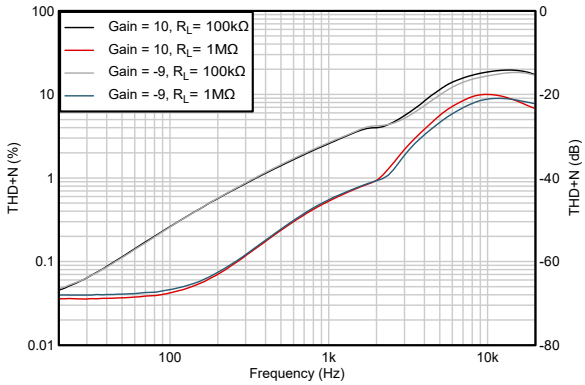


Figure 5-24. Input Voltage Noise Spectral Density

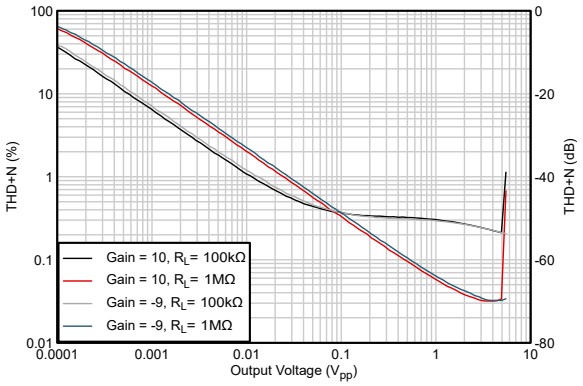
5.6 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, G = 10V/V, R_F= 1.8MΩ, R_L = 1MΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



BW = 80kHz V_{OUT} = 1V_{RMS}

Figure 5-25. THD + N vs Frequency



BW = 80kHz f = 1kHz

Figure 5-26. THD + N vs Amplitude

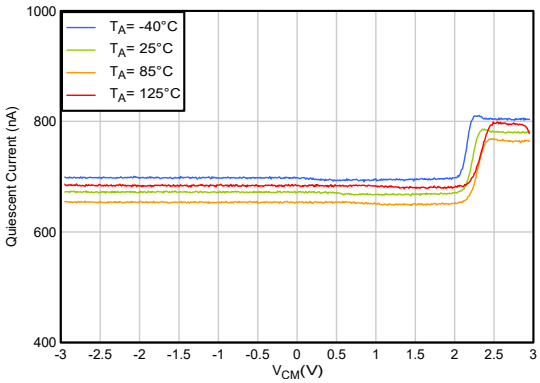


Figure 5-27. Quiescent Current vs Common-Mode

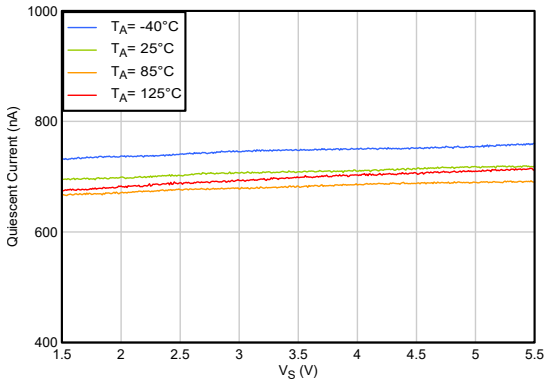


Figure 5-28. Quiescent Current vs Supply Voltage

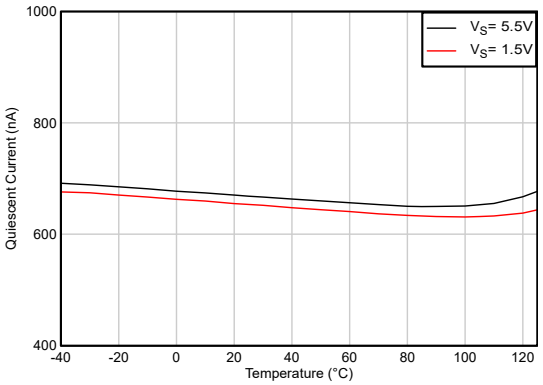
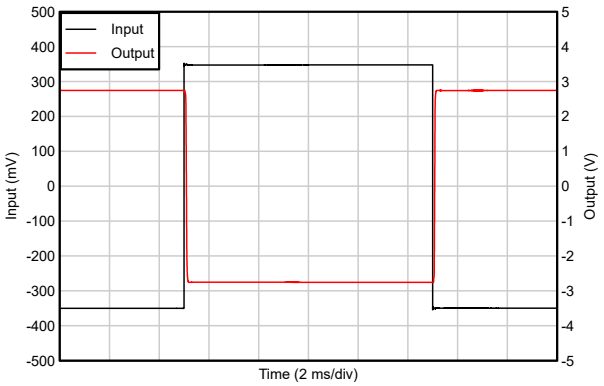


Figure 5-29. Quiescent Current vs Temperature



G = –9 V_{IN} = 700mV_{PP}

Figure 5-30. Overload Recovery

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5.6 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, G = 10V/V, R_F= 1.8MΩ, R_L = 1MΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

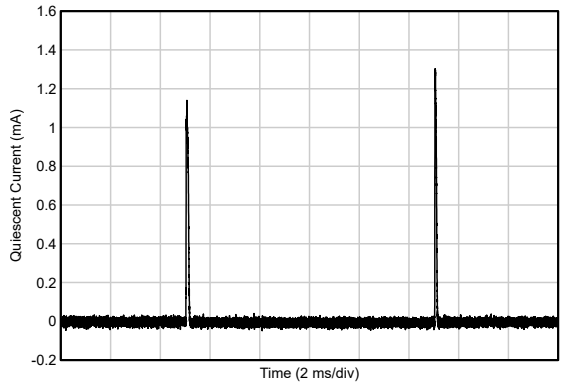
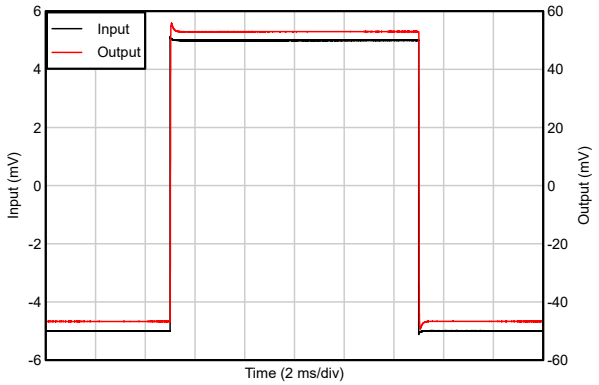
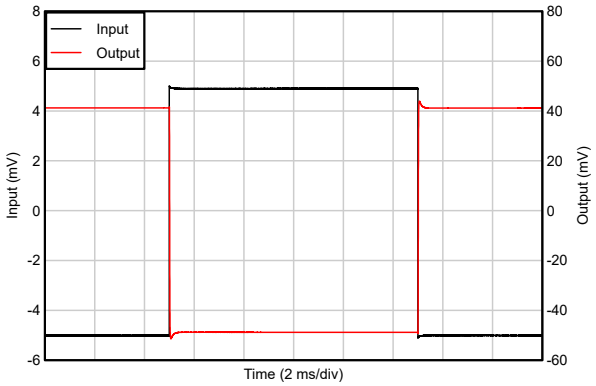


Figure 5-31. Quiescent Current During Overload



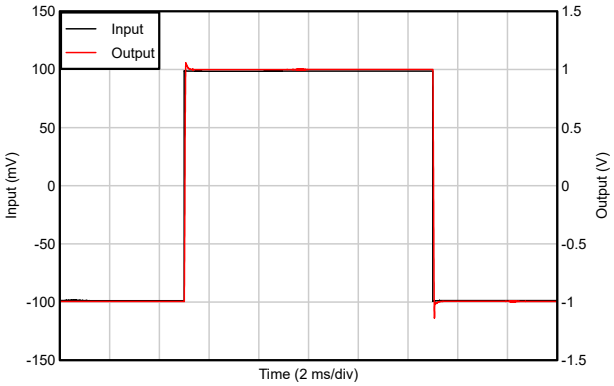
G = 10, V_{IN} = 10mV_{PP}, C_L = 20pF

Figure 5-32. Small-Signal Step Response



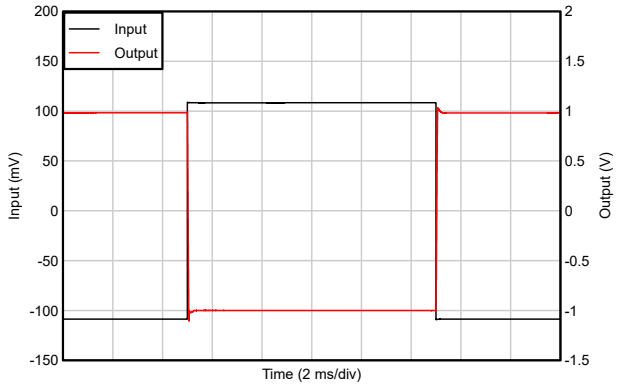
G = -9, V_{IN} = 10mV_{PP}, C_L = 20pF

Figure 5-33. Small-Signal Step Response



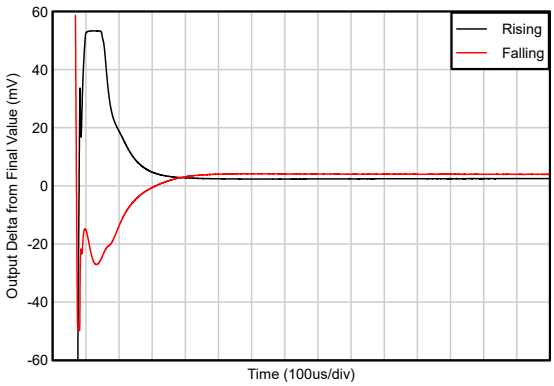
G = 10, V_{OUT} = 2V_{PP}, C_L = 20pF

Figure 5-34. Large-Signal Step Response



G = -9, V_{OUT} = 2V_{PP}, C_L = 20pF

Figure 5-35. Large-Signal Step Response



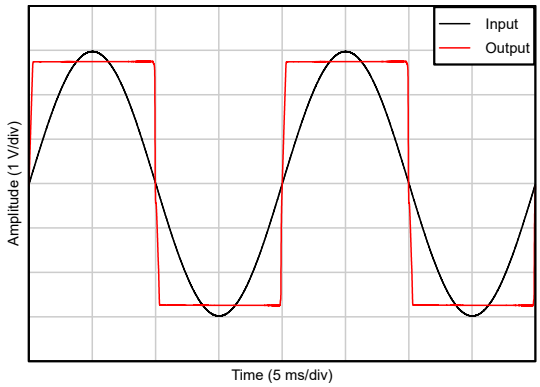
G = 10V_{IN} = 2V_{PP}

Figure 5-36. Settling Time

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5.6 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, G = 10V/V, R_F= 1.8MΩ, R_L = 1MΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



G = 10V_{IN} = 6V_{PP}

Figure 5-37. No Phase Reversal

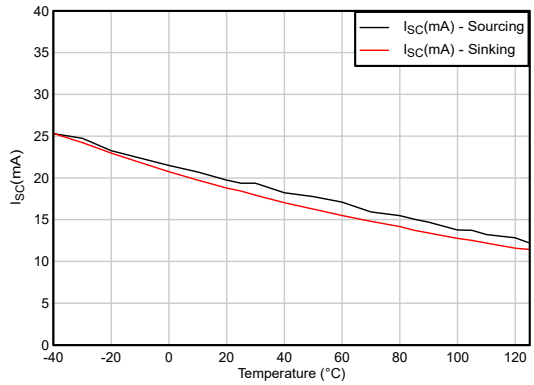


Figure 5-38. Short-Circuit Current vs Temperature (VS = 5.5V)

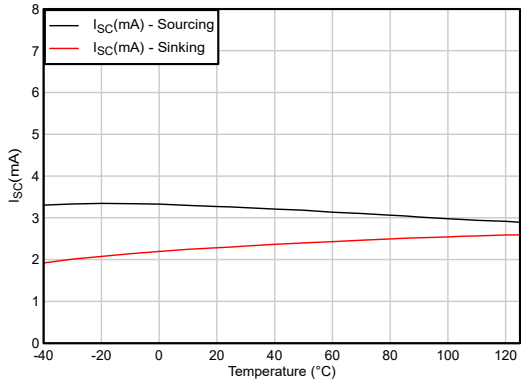


Figure 5-39. Short-Circuit Current vs Temperature (VS = 1.5V)

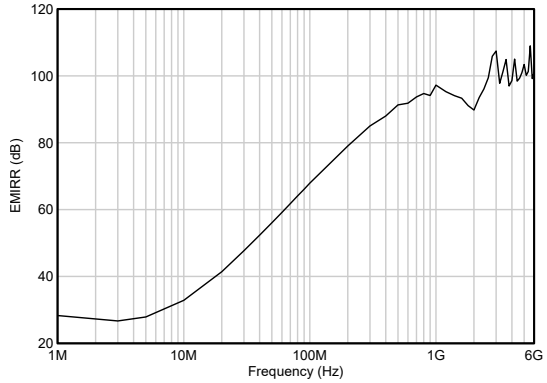


Figure 5-40. EMIRR vs Frequency

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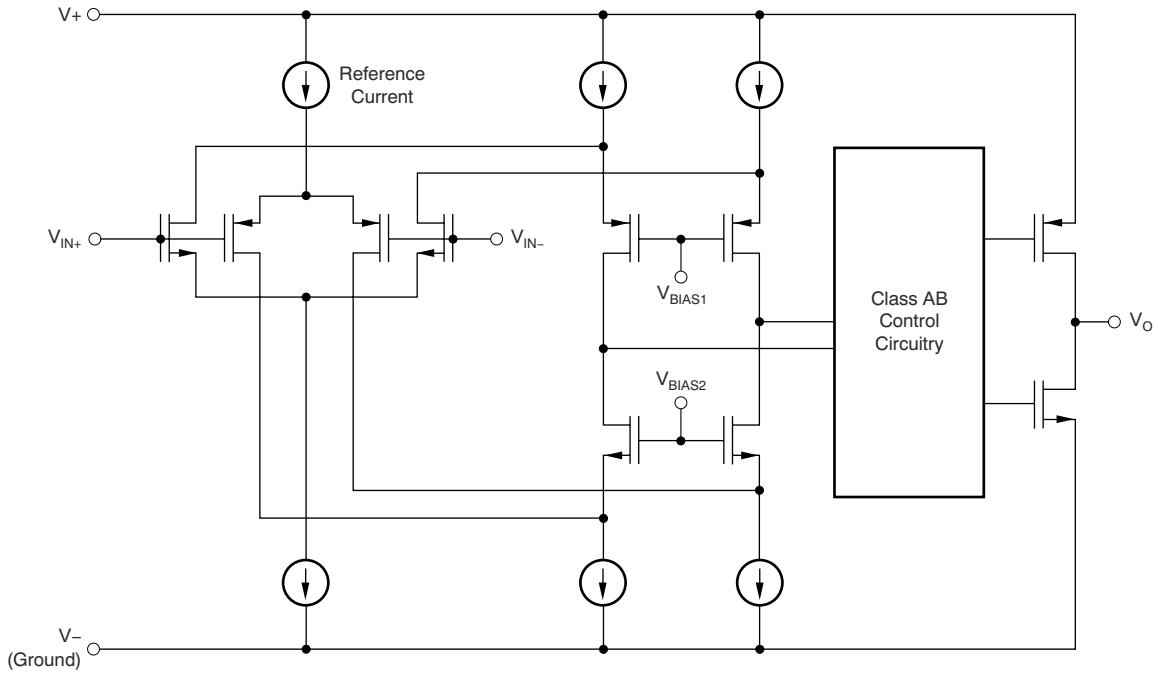
6 Detailed Description

6.1 Overview

The OPAx371D family of low-power, rail-to-rail input and output operational amplifiers is specifically designed for high-gain, battery-powered applications. This family of amplifiers utilizes a decompensated architecture that enables operation from an ultra-low supply voltage of 1.5V to a standard supply voltage of 5.5V and are optimized for use in noise gains of 10V/V or higher. The decompensated architecture provides 125kHz of gain-bandwidth product and up to 70mV/µs of slew rate with around 650nA of quiescent current per channel, delivering AC performance better than unity-gain stable architectures with similar power consumption. This eliminates the need for multiple cascaded amplifier stages in sensor signal conditioning and filtering applications, reducing both component count and total system power consumption.

The input common-mode voltage range includes both rails, allowing the OPAx371D series to be used in many single-supply or dual-supply configurations. The OPAx371D can drive capacitive loads up to 100pF at a gain of 10V/V and features 3.9µVp-p integrated noise (0.1Hz to 10Hz), enabling designers to achieve both improved AC performance and lower power consumption. The design also delivers good DC performance with 0.3mV input offset voltage (typical) and 500fA of input bias current (typical), along with good PSRR, CMRR, and AOL and features an integrated RFI and EMI rejection filter for reliable operation in electrically noisy environments.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Operating Voltage

The OPAx371D series of operational amplifiers is fully specified and ensured for operation from 1.5V to 5.5V. In addition, many specifications apply from –40°C to 125°C. Bypass power-supply pins to ground with at least 0.1µF ceramic capacitors.

6.3.2 Rail-to-Rail Input and Output

The input common-mode voltage range of the OPAx371D extends to either supply rail, even when operating at ultra-low supply voltages as low as 1.5V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. Refer to Section 6.2 for more details.

For most amplifiers with a complementary input stage, the P-channel input pair is designed to deliver better performance in terms of input offset voltage and offset drift over the N-channel pair. Within the transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region. The OPAx371D specifies P-channel pair operation until 0.7V from the positive rail, providing a much wider P-channel input range compared to most complementary input amplifiers. This extended range is particularly useful when operating at lower supply voltages (1.5V, 1.8V, and so forth), allowing wide common-mode swing of input signals to be accommodated within the P-channel input pair while avoiding the transition region and maintaining linearity.

Designed as a nano-power, low-noise operational amplifier, the OPAx371D also delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability for resistive loads up to 100kΩ. Different load conditions change the ability of the amplifier to swing close to the rails.

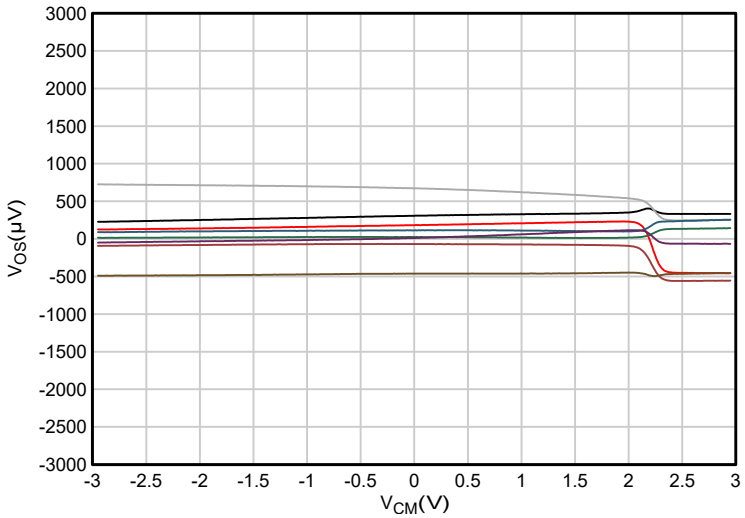


Figure 6-1. Offset Voltage vs Common-Mode

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6.3.3 Decompensated Architecture with Wide Gain-Bandwidth Product

Amplifiers such as the OPAx371D family are not unity-gain stable and are referred to as *decompensated amplifiers*. The decompensated architecture typically allows for higher GBW, higher slew rate, and lower noise compared to a unity-gain stable amplifier with similar quiescent currents. The increased available bandwidth reduces the rise time and settling time of the op amp, allowing for sampling at faster rates in an ADC-based signal chain.

As shown in Figure 6-2, the dominant pole of a unity-gain stable amplifier, f_d, is moved to the frequency f_1 in the case of a decompensated op amp. The solid A_{OL} plot is the open-loop gain plot of a traditional unity-gain stable op amp. The change in internal compensation in a decompensated amp such as the OPAx371D increases the bandwidth for the same amount of power. Besides the advantages in the above mentioned parameters, an increased slew rate and a better distortion value is achieved because of the higher available loop-gain, compared to the unity-gain counterpart. The most important factor to consider is verifying that the op amp is in a noise gain (NG) greater than G_{min}. A value of NG lower than G_{min} results in instability, as shown in Figure 6-2, because the 1/ß curve intersects the A_{OL} curve at 40dB/decade. This method of analyzing stability is called the *rate of closure method*. See TI precision labs for a better understanding on device stability and for different techniques of providing stability.

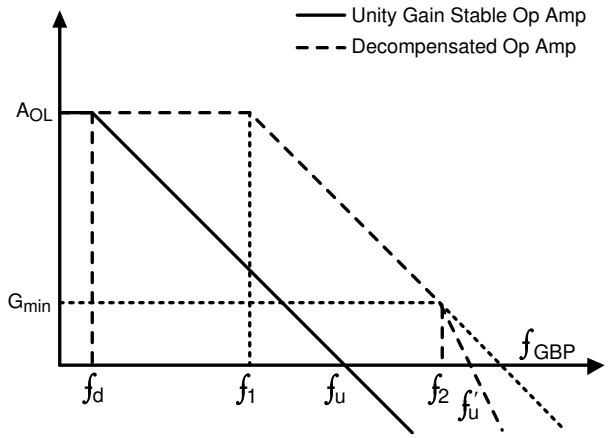


Figure 6-2. Gain vs Frequency Characteristics for a Unity-Gain Stable Op Amp and a Decompensated Op Amp

The OPAx371D family is stable in a noise gain of 10V/V (20dB) or higher in conventional gain circuits. The device has 120kHz of small-signal bandwidth (SSBW) in this gain configuration with approximately 65° of phase margin. The high GBW and low power consumption of the OPAx371D devices make these devices appropriate for power sensitive, high-gain applications.

6.3.4 Capacitive Load and Stability

The OPAx371D is designed to be used in applications where driving a capacitive load is required. As with all operational amplifiers, there can be specific instances where the OPAx371D can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. The capacitive load, in conjunction with the operational amplifier open-loop output impedance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases when capacitive loading increases. When operating in a gain of 10V/V, the OPAx371D remains stable with a pure capacitive load up to approximately 100pF with a good phase margin of 42° typical. The equivalent series resistance (ESR) of some very large capacitors (C_L greater than 1µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when measuring the overshoot response of the amplifier at higher voltage gains.

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One technique for increasing the capacitive load drive capability of the amplifier is to insert a small resistor (typically 10Ω to 20Ω) in series with the output, as shown in Figure 6-3. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistive load connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

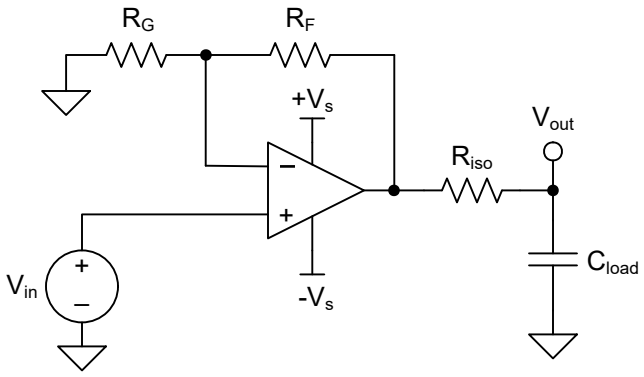


Figure 6-3. Improving Capacitive Load Drive

6.3.5 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or high gain. Once one of the output devices enters the saturation region, the output stage requires additional time to return to the linear operating state which is referred to as overload recovery time. After the output stage returns to the linear operating state, the amplifier begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time of the OPAx371D is approximately 50µs.

6.3.6 EMI Rejection

The OPAx371D uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx371D benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. Figure 6-4 shows the results of this testing on the OPAx371D. Table 6-1 shows the EMIRR IN+ values for the OPAx371D at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application note contains detailed information on the topic of EMIRR performance as relating to op amps and is available for download from www.ti.com.

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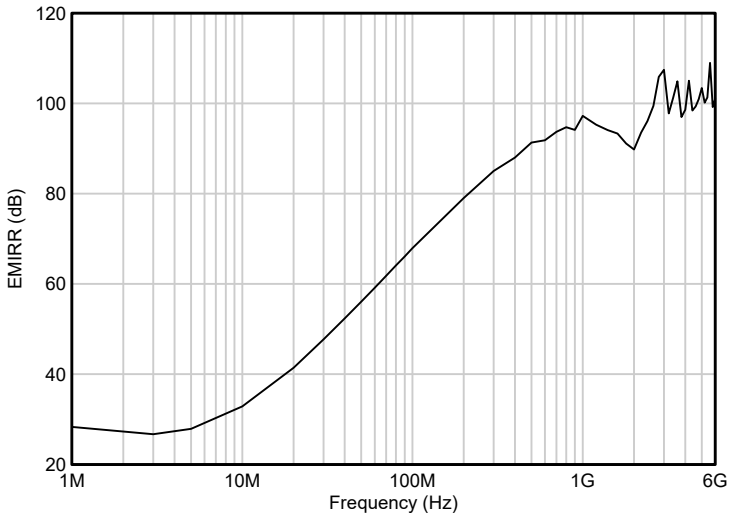


Figure 6-4. EMIRR Testing

Table 6-1. TLV904xD EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	88dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	95dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	90dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	95dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	98dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	100dB

6.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect the circuits from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 6-5 shows the ESD circuits contained in the OPAx371D devices. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

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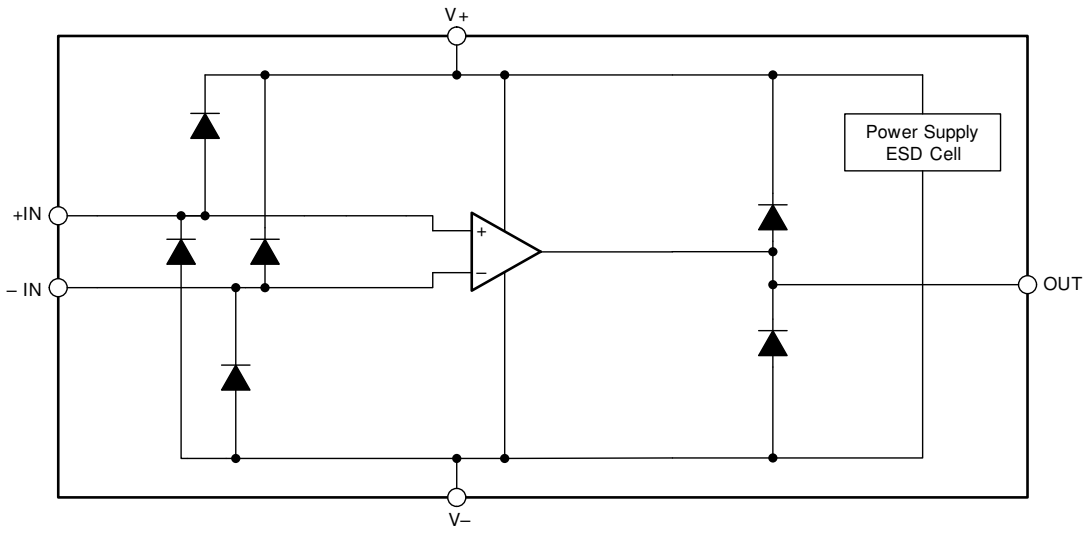


Figure 6-5. Equivalent Internal ESD Circuitry

6.3.8 Input and ESD Protection

The OPAx371D family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10mA. Figure 6-6 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

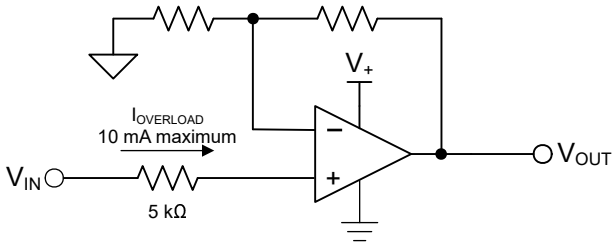


Figure 6-6. Input Current Protection

6.4 Device Functional Modes

The OPAx371D family haa a single functional mode. These devices are powered on as long as the power-supply voltage is between 1.5V (±0.75V) and 5.5V (±2.75V).

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPAx371D family of low-power, rail-to-rail input and output operational amplifiers is specifically designed for portable, high gain applications. The devices operate from 1.5V to 5.5V, are stable above 10V/V and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving resistive loads greater than 100kΩ connected to any point between V+ and V–. The input common-mode voltage range includes both rails and allows the OPAx371D series to be used in many single-supply or dual supply configurations.

7.2 Typical Application

7.2.1 Low-Side, Current Sensing Application

Figure 7-1 shows the OPAx371D configured in a low-side current sensing application.

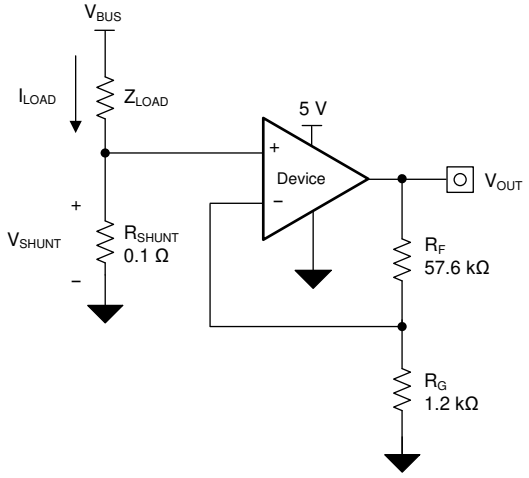


Figure 7-1. Low-Side, Current-Sensing Application

7.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0A to 1A
- Maximum output voltage: 4.9V
- Maximum shunt voltage: 100mV

7.2.1.2 Detailed Design Procedure

The transfer function of the circuit in Figure 7-1 is given in Equation 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is shown using Equation 2.

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100mV}{1A} = 100m\Omega \quad (2)$$

Using Equation 2, R_{SHUNT} is calculated to be 100mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the OPAx371D to produce an output voltage of approximately 0V to 4.9V. The gain needed by the OPAx371D to produce the necessary output voltage is calculated using Equation 3.

$$Gain = \frac{V_{OUT_MAX} - V_{OUT_MIN}}{V_{IN_MAX} - V_{IN_MIN}} \quad (3)$$

Using Equation 3, the required gain is calculated to be 49V/V, which is set with resistors R_F and R_G. Equation 4 sizes the resistors R_F and R_G, to set the gain of the OPAx371D to 49V/V.

$$Gain = 1 + \frac{R_F}{R_G} \quad (4)$$

Selecting R_F as 57.6kΩ and R_G as 1.2kΩ provides a combination that equals 49V/V. Figure 7-2 shows the measured transfer function of the circuit shown in Figure 7-1. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistors values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system; you must choose an impedance that is optimized for your system parameters.

7.2.1.3 Application Curve

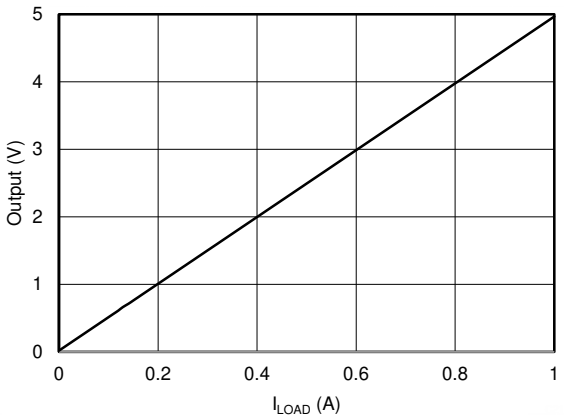


Figure 7-2. Low-Side, Current-Sense Transfer Function

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7.3 Power Supply Recommendations

The OPAx371D family is specified for operation from 1.5V to 5.5V (±0.75V to ±2.75V); many specifications apply from –40°C to 125°C. *Section 5.5* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6V can permanently damage the device; see the *Section 5.1* table.

Place 0.1µF bypass capacitors close to the power-supply pins to reduce coupling errors from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Section 7.4.1*.

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7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power connections of the board and propagate to the power pins of the op amp. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in Figure 7-4. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example

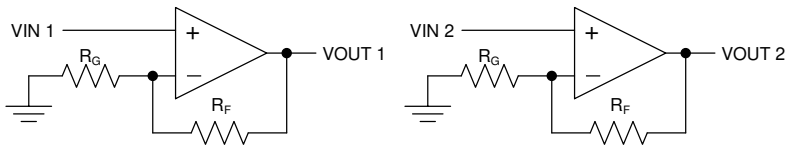


Figure 7-3. Schematic Representation

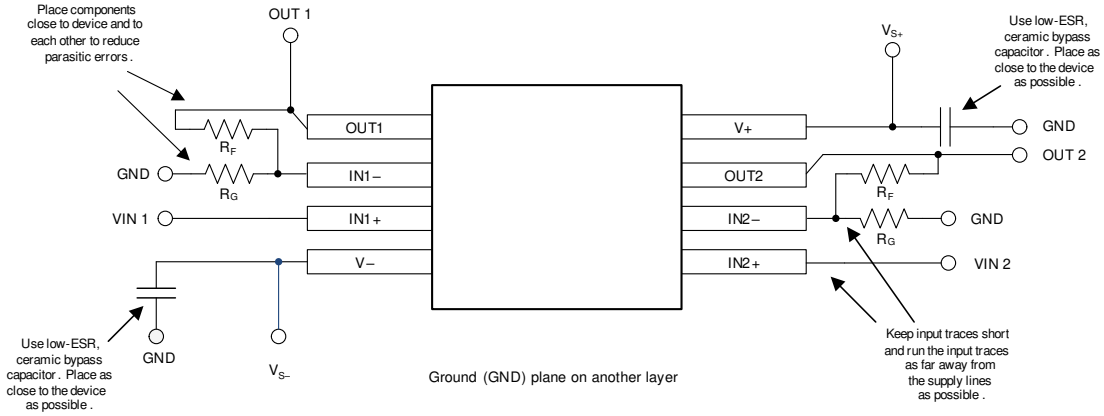


Figure 7-4. Layout Example

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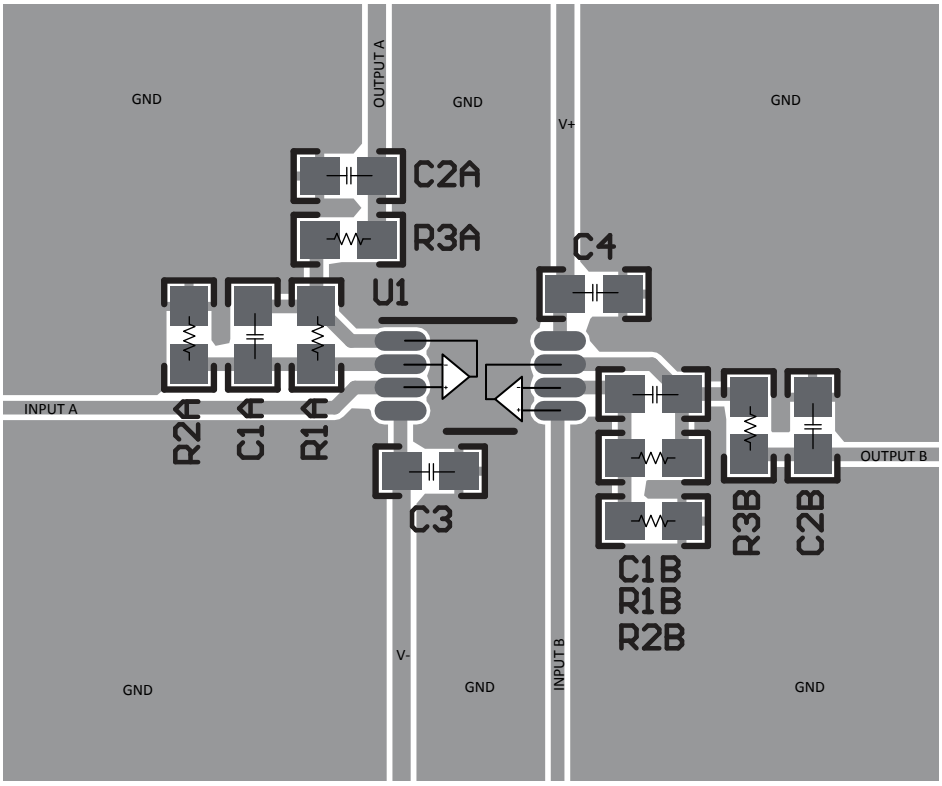


Figure 7-5. Example Layout for VSSOP-8 (DGK) Package

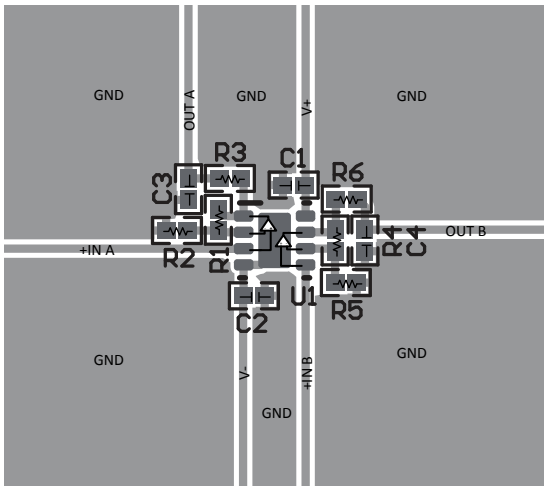


Figure 7-6. Example Layout for WSON-8 (DSG) Package

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *EMI rejection ratio of operational amplifiers* application note
- Texas Instruments, *QFN/SON PCB attachment* application note
- Texas Instruments, *Quad flatpack no-lead logic packages* application note

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2026) to Revision A (August 2026)	Page
• Changed the document status from *Advanced Mixed* to *Production Data*	1
• Updated the *Application* section	1
• Updated ESD HBM Rating from 2000V to 4000V	6
• Updated ESD CDM Rating from 1000V to 1500V	6
• Updated *Thermal Information for Single Channel* table	6
• Updated maximum Input Bias Current at TA = 0°C to 85°C from 100 pA to 80 pA	8
• Updated maximum Input Bias Current at TA = -40°C to 125°C from 600 pA to 560 pA	8
• Updated maximum Input Offset Current at TA = 0°C to 85°C from 45 pA to 30 pA	8

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA371DDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	48CH
OPA371DDCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	POST-PLAT AG SPOT	Level-1-260C-UNLIM	-40 to 125	48BH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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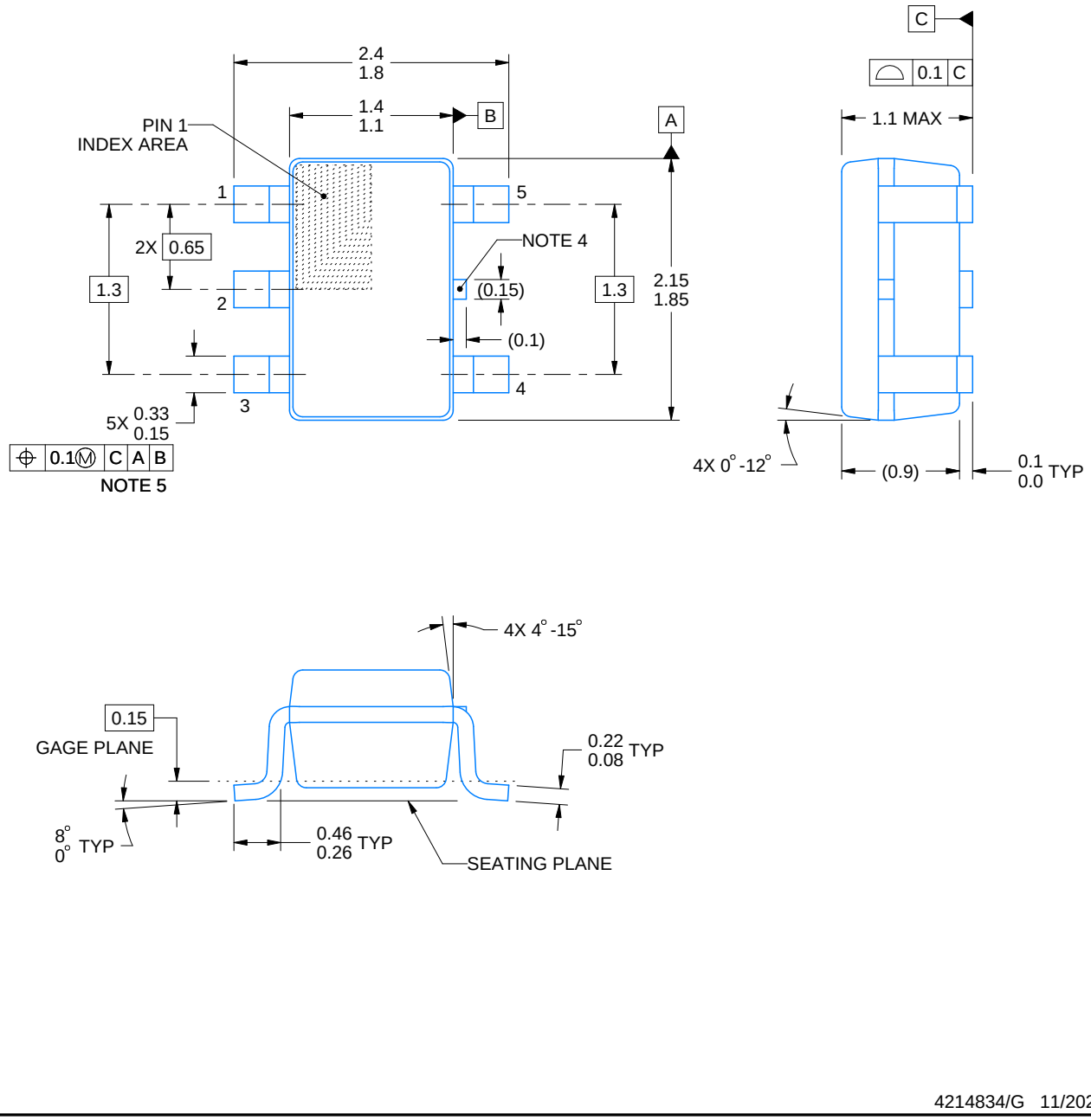
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

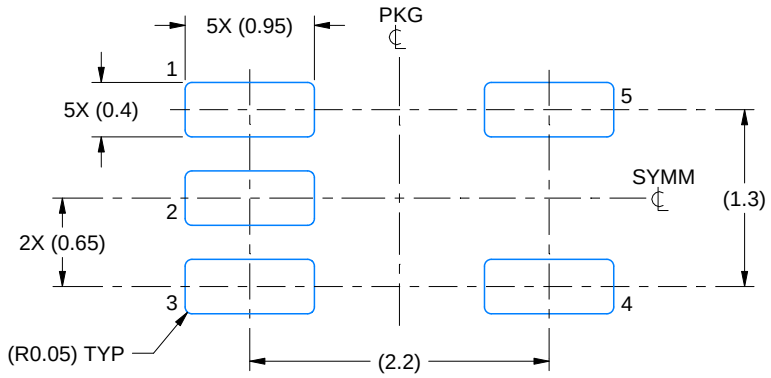
SMALL OUTLINE TRANSISTOR



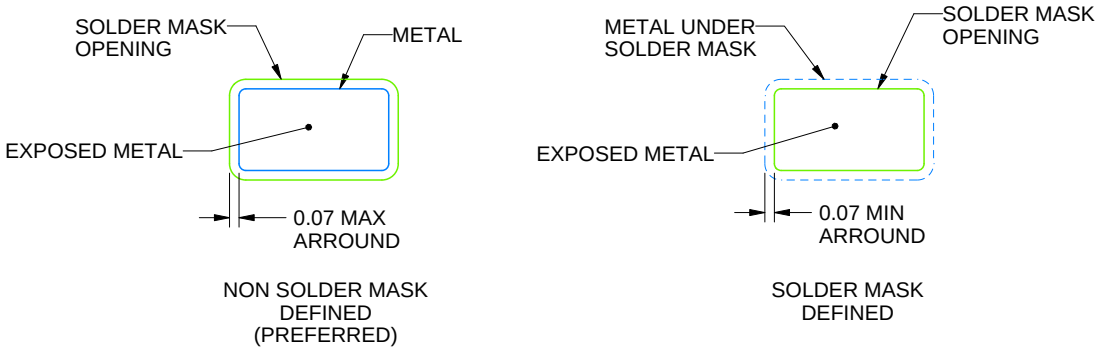
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

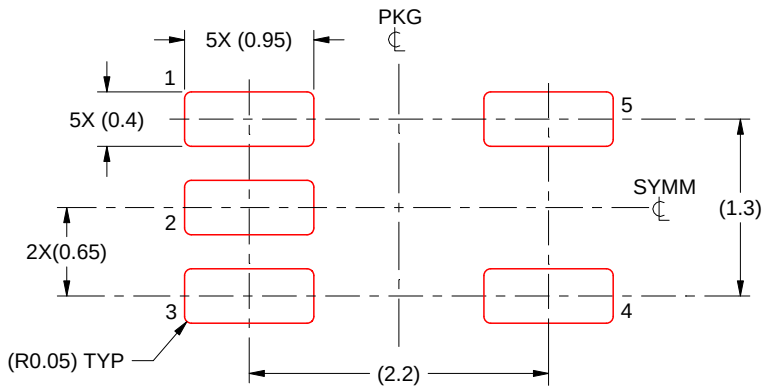


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

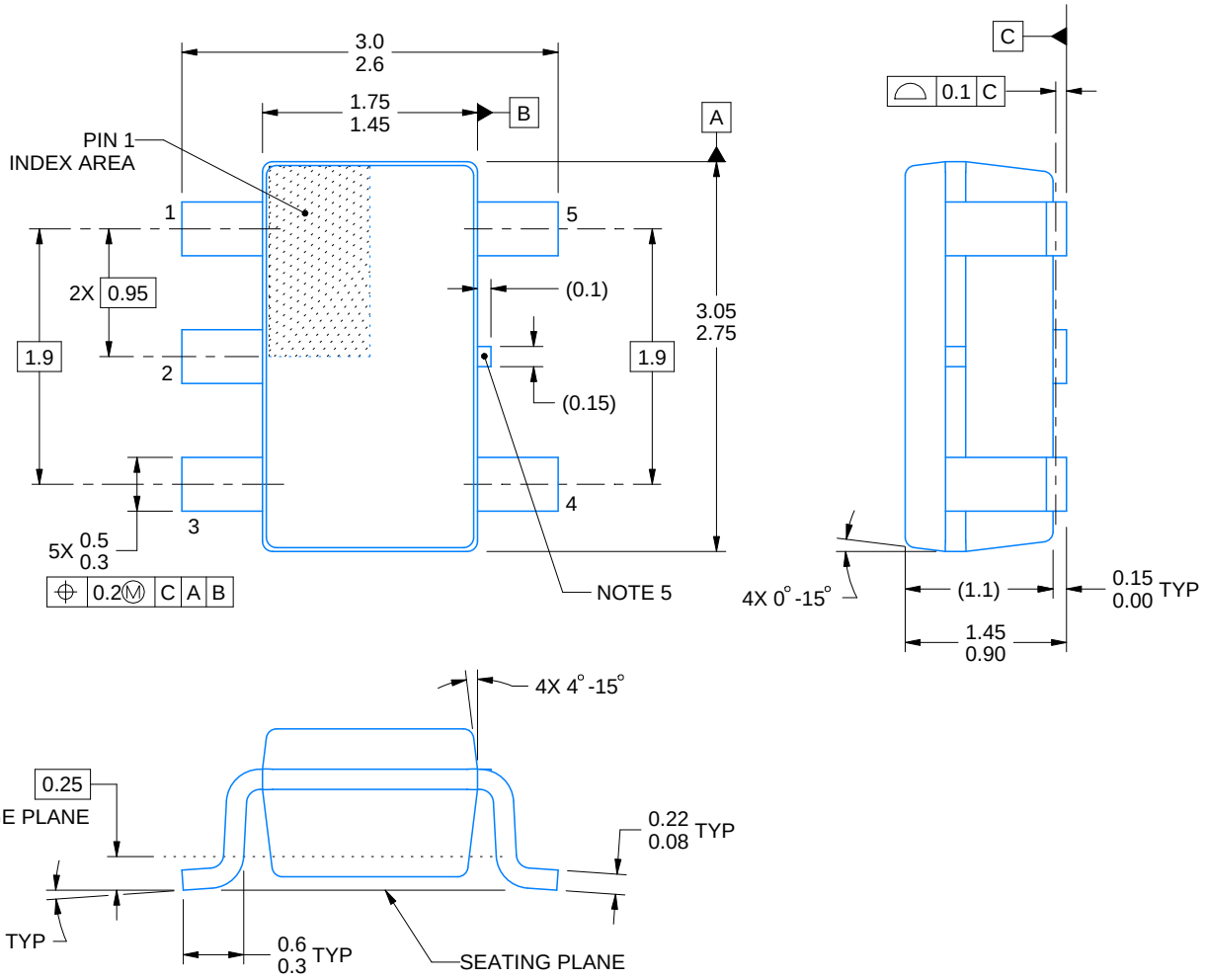
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

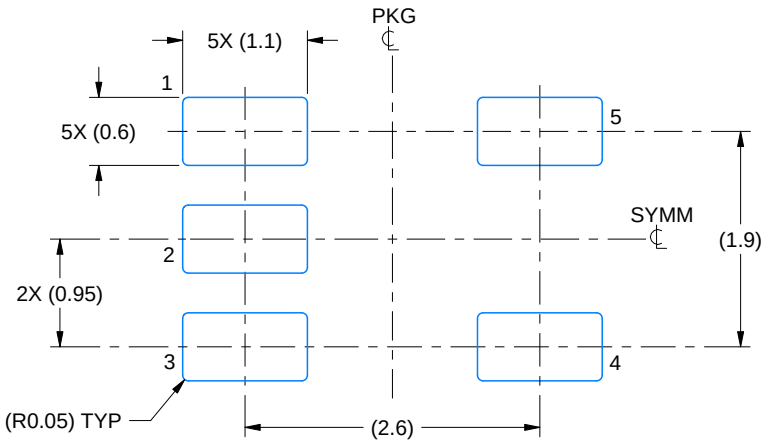
SMALL OUTLINE TRANSISTOR



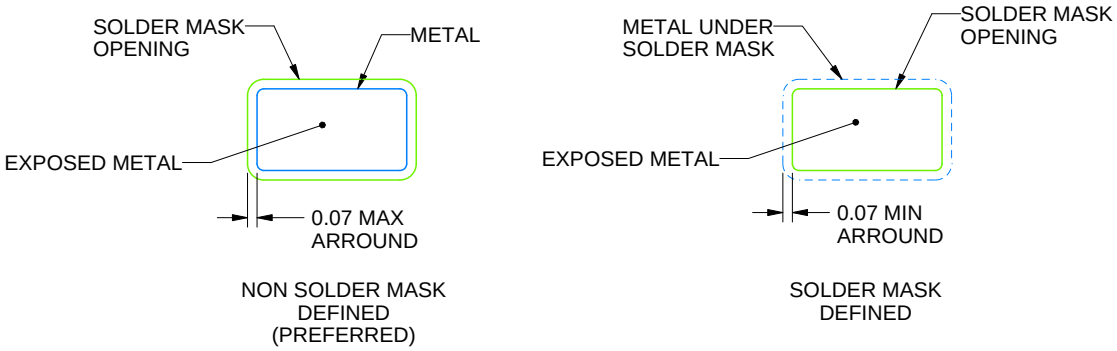
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5. Support pin may differ or may not be present.



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EXPOSED METAL SHOWN
SCALE:15X

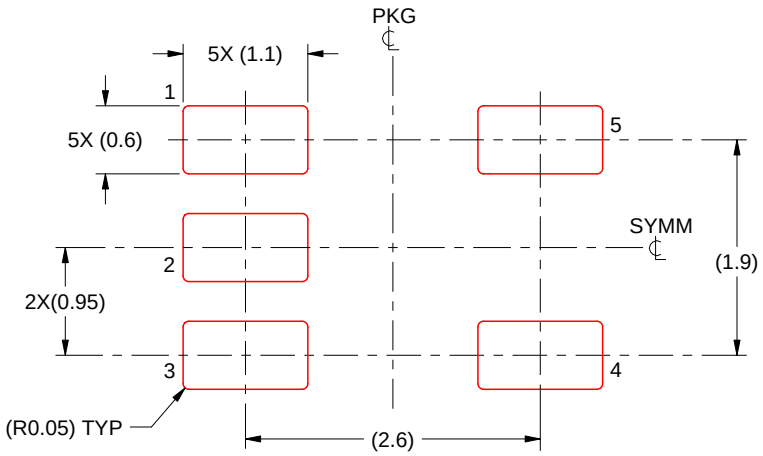


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

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9. Board assembly site may have different recommendations for stencil design.

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