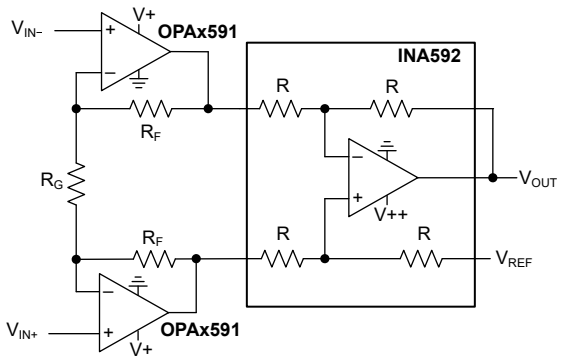
OPAx591 85V, Precision (1µV/°C), Low-Power (450µA), High-Slew Rate (100V/µs) Op Amps With MUX-Friendly Inputs

1 Features

- Wide supply voltage range: 8V to 85V
- Low offset voltage: 225µV, max
- Low offset drift: 1µV/°C, max
- High CMRR: 125dB, min
- High PSRR: 120dB, min
- Low input bias current: 15pA, max
- Low noise: 12.9nV/√Hz at 1kHz
- Wide bandwidth: 3.75MHz at 40dB
- High slew rate: 100V/µs
- Low quiescent current: 450µA
- Rail-to-rail output
- Unity gain stable
- Mux-friendly inputs
- Thermal shutdown protection
- Small package options:
  - Single: SOT-23
  - Dual: VSSOP, SOIC

2 Applications

- Semiconductor test
- CT and PET scanner
- Programmable DC power supply
- Source measurement unit (SMU)
- Analytical lab instrumentation
- Power analyzer
- Optical module



OPA591 Buffer With INA592

3 Description

The OPAx591 and OPA2591 (OPAx591) are a family of high precision, 85V CMOS power amplifiers available in small, industry standard packages.

These devices are laser trimmed to provide excellent dc performance, including 225µV max offset, 1µV/°C max offset drift. The high power supply and common-mode rejection help these op amps maintain high dc performance across different operating conditions. Degradation of precision is minimal because of the very low input bias current across the entire operating voltage range.

The OPAx591 also excels in ac performance despite the low quiescent current consumption. Proprietary design techniques provide 100V/µs slew rate and MUX-friendly inputs to enable fast settling of large signals. The low broadband noise help maintain signal fidelity across a wide frequency spectrum.

The combination of high precision, low noise, low power, and small packages make the OPAx591 a great choice for high voltage, space constrained systems where power consumption and, or thermal management is critical. Such systems include automated test equipment requiring high voltage and precision, power supplies requiring current or voltage sensing, and piezo actuator driving for haptic feedback systems.

This family of amplifiers operates over the extended industrial temperature range of –40°C to +125°C.

Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE (1)
OPA591	Single	DBV (SOT-23, 5)
OPA2591	Dual	D (SOIC, 8)(2)
		DGK (VSSOP, 8)

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) This package is preview only.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....3
5 Specifications....4
5.1 Absolute Maximum Ratings....4
5.2 ESD Ratings....4
5.3 Recommended Operating Conditions....4
5.4 Thermal Information for OPA591....5
5.5 Thermal Information OPA2591....5
5.6 Electrical Characteristics....6
5.7 Typical Characteristics....8
6 Detailed Description....16
6.1 Overview....16
6.2 Functional Block Diagram....16
6.3 Feature Description....17
6.4 Device Functional Modes....20
7 Application and Implementation....21
7.1 Application Information....21
7.2 Typical Applications....21
7.3 Power Supply Recommendations....25
7.4 Layout....25
8 Device and Documentation Support....29
8.1 Receiving Notification of Documentation Updates....29
8.2 Support Resources....29
8.3 Trademarks....29
8.4 Electrostatic Discharge Caution....29
8.5 Glossary....29
9 Revision History....29
10 Mechanical, Packaging, and Orderable Information....29

Copyright © 2026 Texas Instruments Incorporated

4 Pin Configuration and Functions

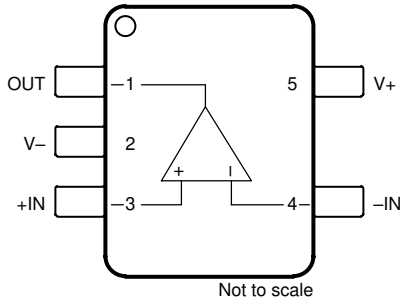


Figure 4-1. OPA591 DBV Package, 5-Pin SOT-23 (Top View)

Table 4-1. Pin Functions: OPA591

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN	3	Input	Noninverting input
–IN	4	Input	Inverting input
OUT	1	Output	Output
V+	5	Power	Positive (highest) power supply
V–	2	Power	Negative (lowest) power supply

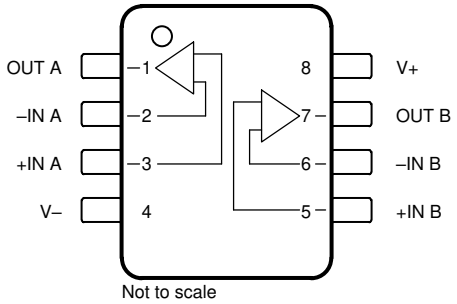


Figure 4-2. OPA2591 D Package, 8-Pin SOIC and DGK Package, 8-Pin VSSOP (Top View)

Table 4-2. Pin Functions: OPA2591

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V+	8	Power	Positive (highest) power supply
V–	4	Power	Negative (lowest) power supply

Copyright © 2026 Texas Instruments Incorporated

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)			93	V
	Signal input pin voltage[2]	Common-mode	(V–) – 0.3	(V+) + 0.3	V
		Differential		(V+) – (V–)	
	Input current, all input pins[2]			±10	mA
I_{SC}	Output short circuit[3]			Continuous	
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails must be current-limited to 10mA or less.
(3) Short-circuit to ground.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Dual supply	±4		±42.5	V
		Single supply	8		85	
T_A	Ambient temperature		–40		125	°C

Copyright © 2026 Texas Instruments Incorporated

5.4 Thermal Information for OPA591

THERMAL METRIC[1]		OPA591 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	99.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	42.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	64.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information OPA2591

THERMAL METRIC[1]		OPA2591 D (SOIC) 8 PINS	OPA2591 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.3	143.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.2	50.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.0	78.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.8	3.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	58.1	77.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Copyright © 2026 Texas Instruments Incorporated

5.6 Electrical Characteristics

at V_S = 85V (±42.5V), T_A = 25°C, R_L = 10kΩ to mid-supply, and V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±50	±225	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C(1)			±0.2	±1	µV/°C
PSRR	Power supply rejection ratio	8V ≤ V_S ≤ 85V			±0.2	±1	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current(1)				±5	±15	pA
		T_A = –40°C to +85°C				±50	
		T_A = –40°C to +125°C				±1	nA
I_{OS}	Input offset current(1)				±5	±15	pA
		T_A = –40°C to +85°C				±55	
		T_A = –40°C to +125°C				±1	nA
NOISE							
	Input voltage noise	f = 0.1Hz to 10Hz			1.4		$µV_{PP}$
e_n	Input voltage noise density	f = 100Hz			17.8		nV/√Hz
		f = 1kHz			12.9		
		f = 10kHz			12.8		
i_n	Current noise density	f = 1kHz			10		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage	Linear operation		(V–) – 0.1		(V+) – 3.5	V
CMRR	Common-mode rejection	(V–) ≤ V_{CM} ≤ (V+) – 3.5V		125	140		dB
			T_A = –40°C to +125°C(1)	120	140		
INPUT IMPEDANCE							
	Differential				100 || 2.5		MΩ || pF
	Common-mode				10 || 5.5		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 1V < V_O < (V+) – 1.5V, R_L = 10kΩ to mid-supply(1)		134	140		dB
			T_A = –40°C to +125°C	120	140		
		(V–) + 3V < V_O < (V+) – 3.5V, R_L = 2kΩ to mid-supply		116	126		
			T_A = –40°C to +125°C(1)	112	126		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	G = 1			2.25		MHz
		G = 10			2.8		
		G = 100			3.25		
SR	Slew rate	G = ±1, V_O = 70V step			100		V/µs
t_S	Settling time	To ±0.01%, G = 1, V_O = 70V step, C_L = 20pF			4.25		µs
	Overload recovery	G = –10			1.1		µs
THD+N	Total harmonic distortion + noise	G = +1, V_O = $70V_{PP}$, f = 1kHz	R_L = 10kΩ		–102		dB
			R_L = 2kΩ		–95		

Copyright © 2026 Texas Instruments Incorporated

5.6 Electrical Characteristics (continued)

at V_S = 85V (±42.5V), T_A = 25°C, R_L = 10kΩ to mid-supply, and V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_O	Voltage output swing from rail(1)	No load				25	mV
		R_L = 10kΩ to mid-supply				500	
		R_L = 2kΩ to mid-supply				2.25	V
I_{SC}	Output current				±30		mA
C_{LOAD}	Capacitive load drive				1		nF
Z_O	Open-loop output impedance	f = 1MHz			550		Ω
POWER SUPPLY							
I_Q	Quiescent current	I_O = 0mA			450	550	µA
			T_A = –40°C to +125°C(1)			550	
TEMPERATURE							
	Overtemperature shutdown	Shutdown temperature, T_J			170		°C
		Thermal hysteresis			20		

(1) Specification established from device population bench system measurements across multiple lots.

Copyright © 2026 Texas Instruments Incorporated

5.7 Typical Characteristics

at T_A = 25°C, V_S = 85V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ (unless otherwise noted)

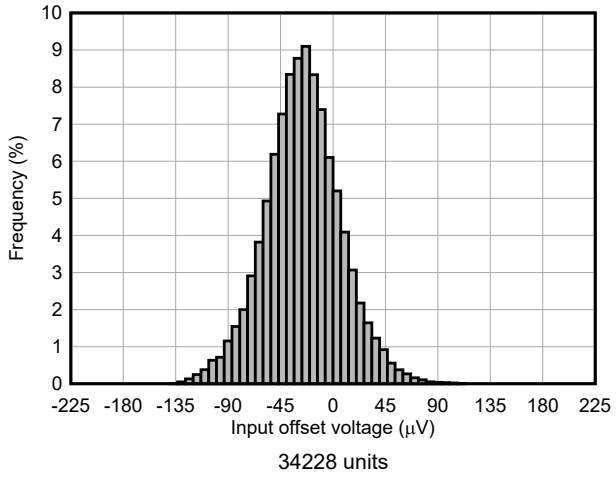


Figure 5-1. Offset Voltage Production Distribution at 25°C

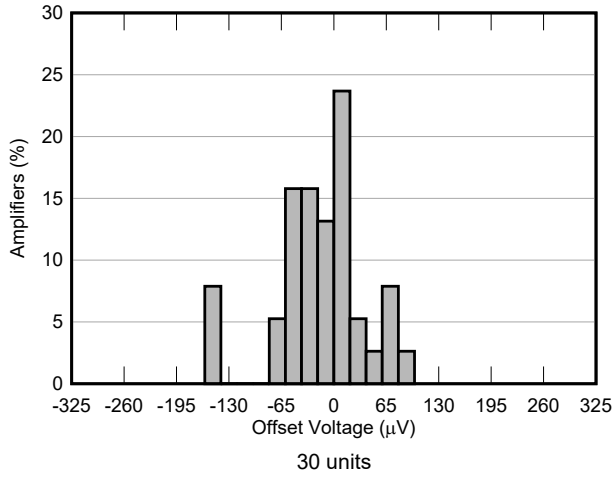


Figure 5-2. Offset Voltage Production Distribution at 125°C

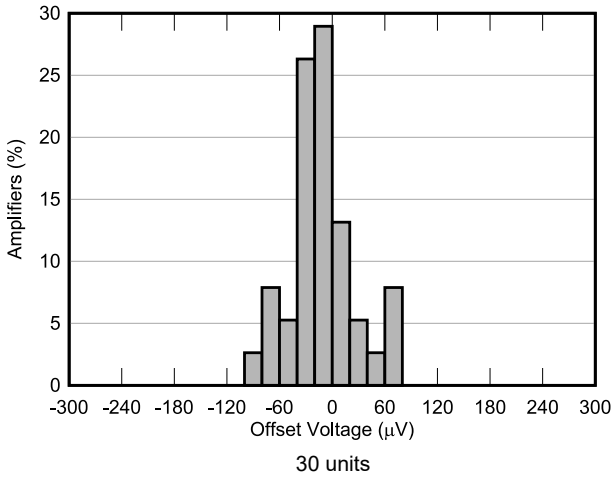


Figure 5-3. Offset Voltage Production Distribution at −40°C

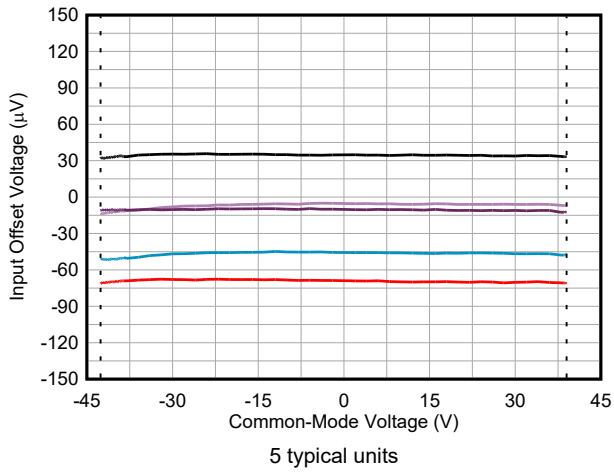


Figure 5-4. Input Offset Voltage vs Common-Mode Voltage

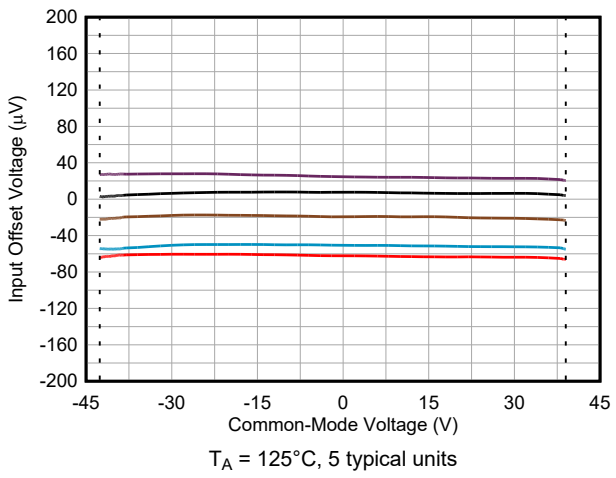


Figure 5-5. Input Offset Voltage vs Common-Mode Voltage

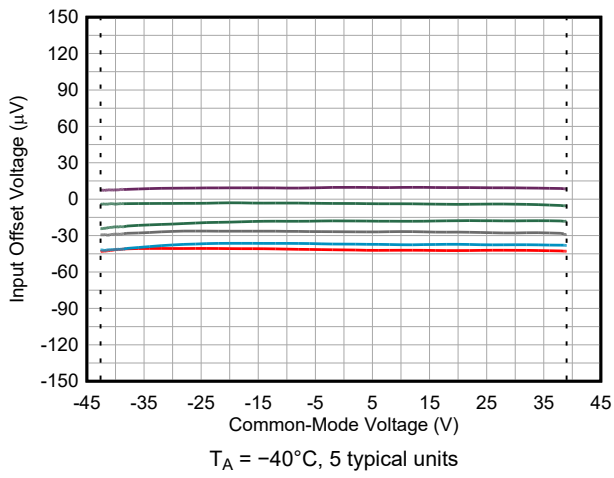


Figure 5-6. Input Offset Voltage vs Common-Mode Voltage

Copyright © 2026 Texas Instruments Incorporated

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 85V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ (unless otherwise noted)

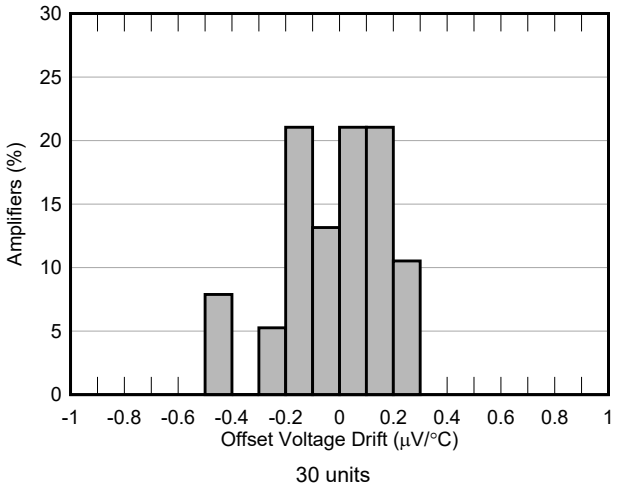


Figure 5-7. Offset Voltage Drift Distribution

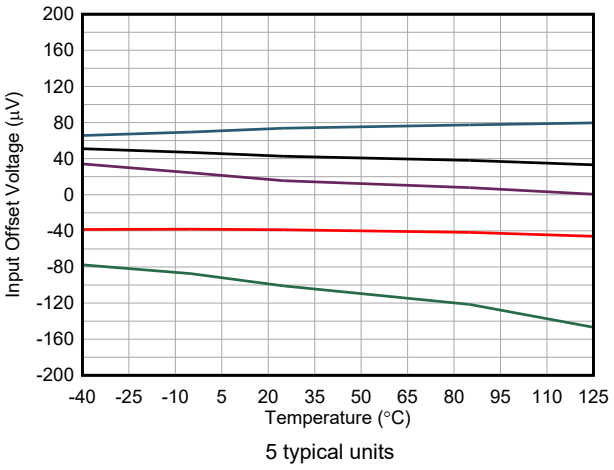


Figure 5-8. Input Offset Voltage vs Temperature

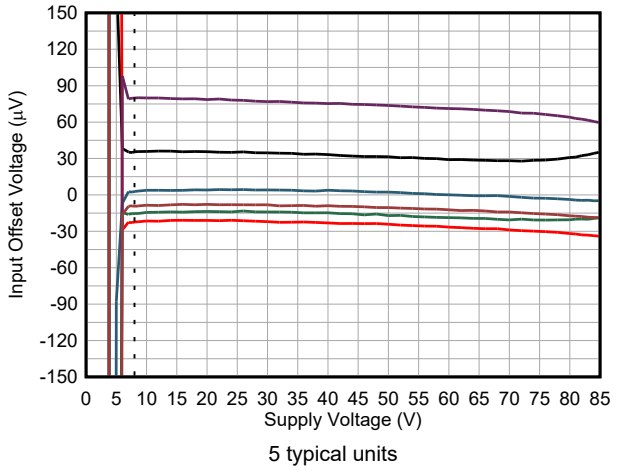


Figure 5-9. Offset Voltage vs Power Supply Voltage

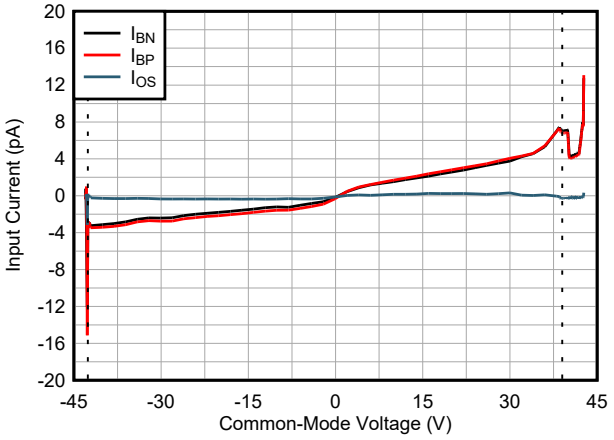


Figure 5-10. Input Bias vs Common-Mode Voltage

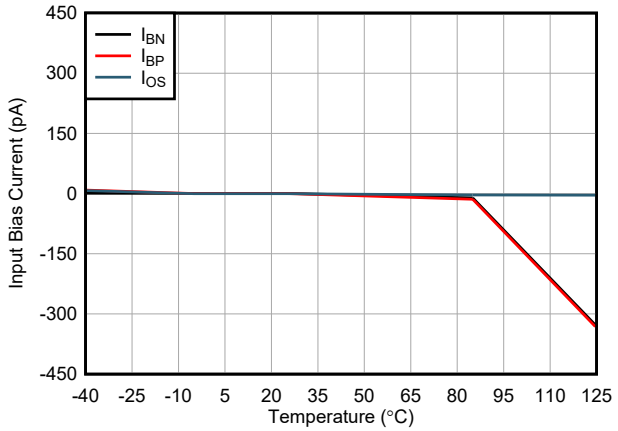


Figure 5-11. Input Bias and Input Offset Current vs Temperature

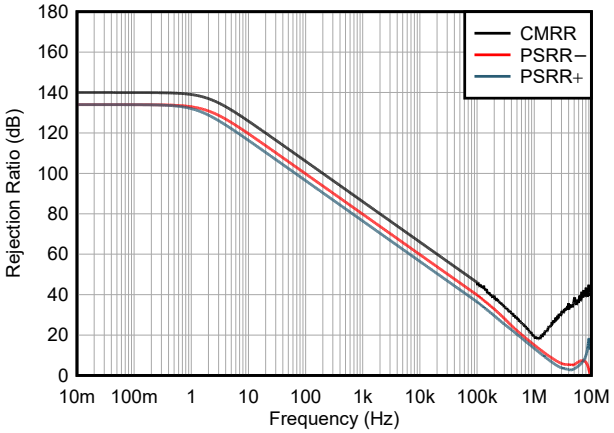


Figure 5-12. Power-Supply and Common-Mode Rejection Ratio vs Frequency

Copyright © 2026 Texas Instruments Incorporated

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 85V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ (unless otherwise noted)

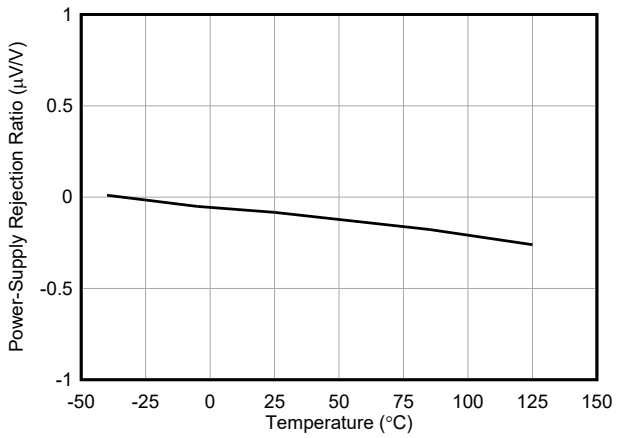


Figure 5-13. Power-Supply Rejection Ratio vs Temperature

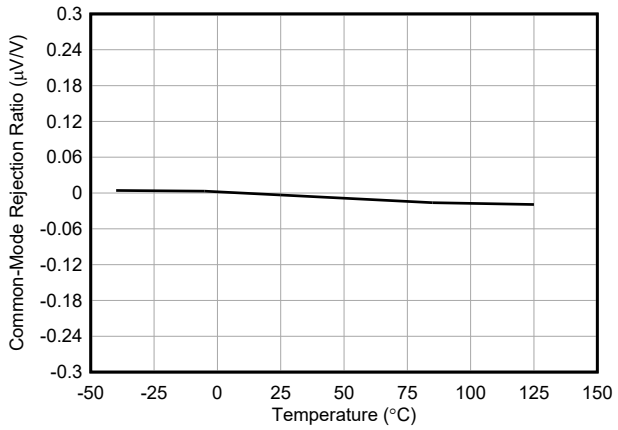


Figure 5-14. Common-Mode Rejection Ratio vs Temperature

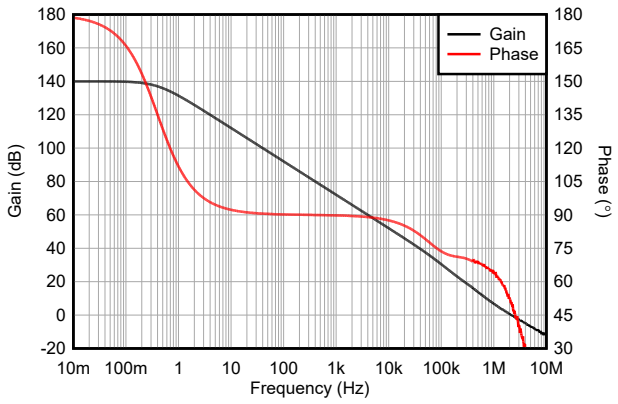


Figure 5-15. Open-Loop Gain and Phase vs Frequency

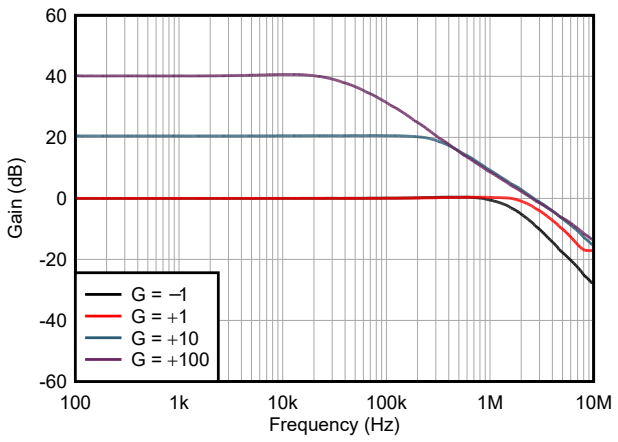


Figure 5-16. Closed-Loop Gain vs Frequency

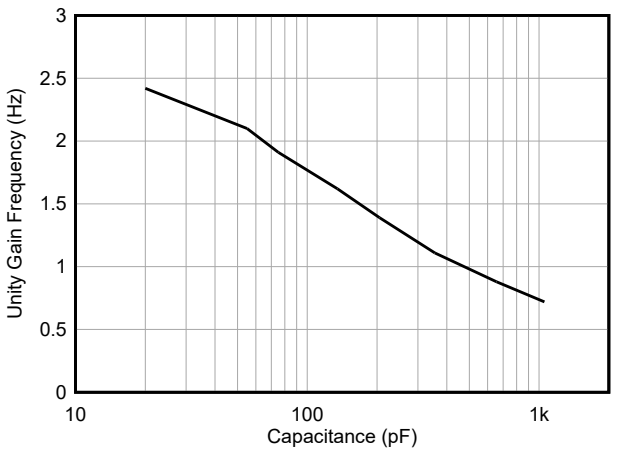


Figure 5-17. Unity-Gain Bandwidth vs Capacitive Load

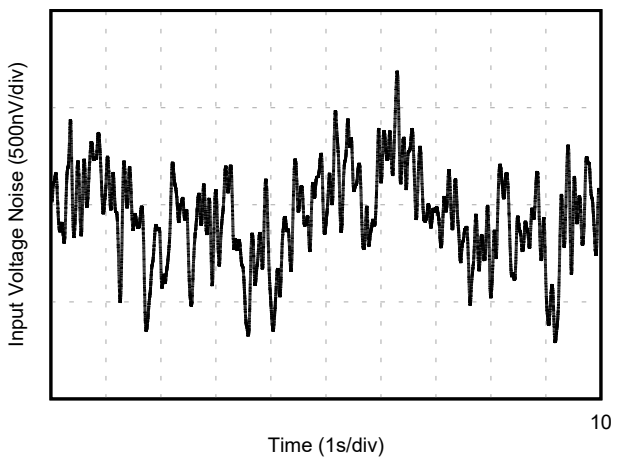


Figure 5-18. Voltage Noise Density vs Frequency

Copyright © 2026 Texas Instruments Incorporated

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 85V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ (unless otherwise noted)

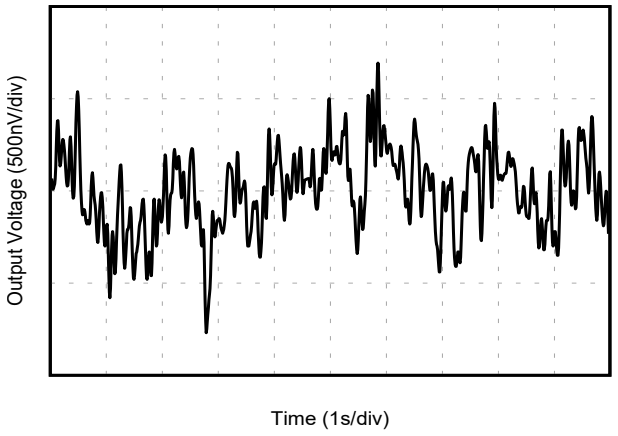


Figure 5-19. 0.1Hz to 10Hz Noise

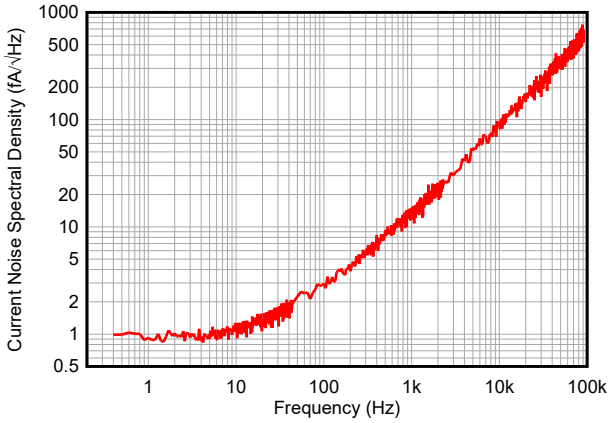


Figure 5-20. Current Noise Density vs Frequency

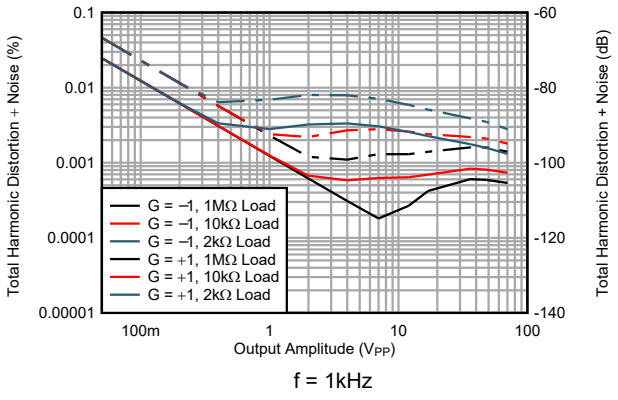


Figure 5-21. Total Harmonic Distortion + Noise Ratio vs Output Amplitude

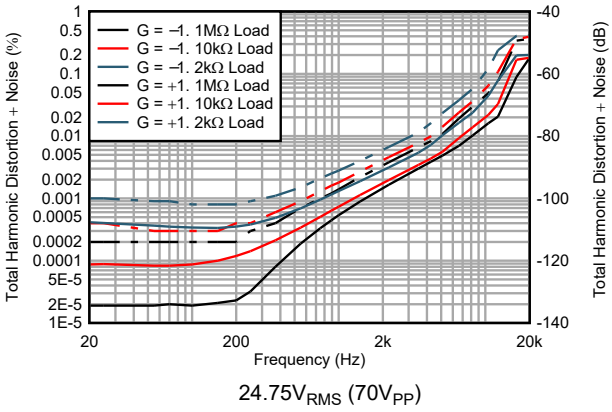


Figure 5-22. Total Harmonic Distortion + Noise Ratio vs Frequency

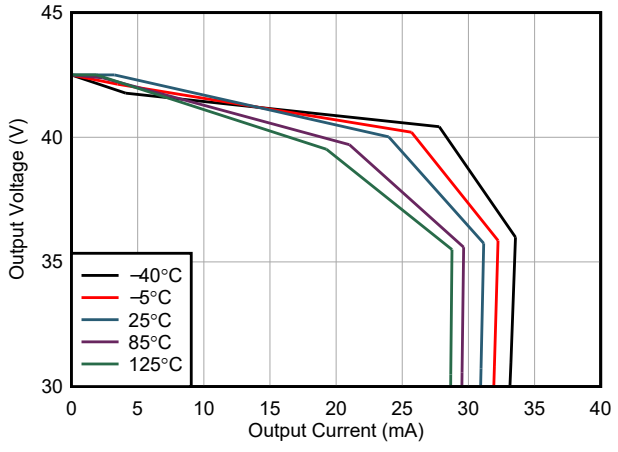


Figure 5-23. Output Voltage Swing vs Output Sourcing Current

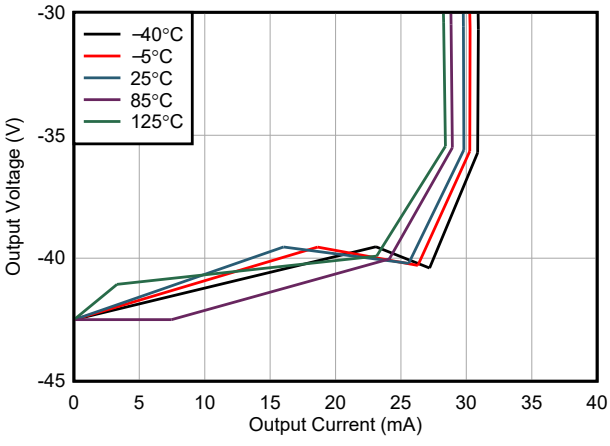


Figure 5-24. Output Voltage Swing vs Output Sinking Current

Copyright © 2026 Texas Instruments Incorporated

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 85V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ (unless otherwise noted)

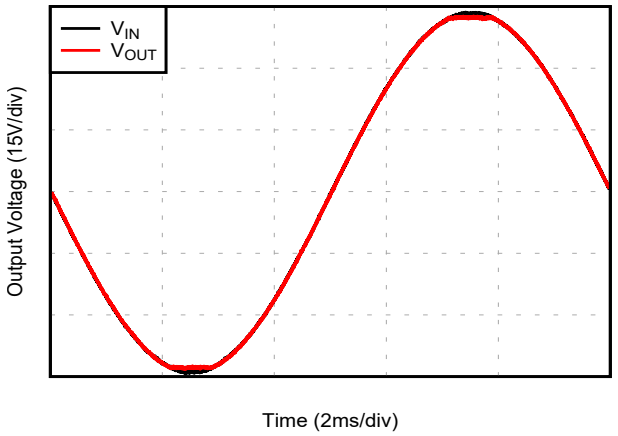


Figure 5-25. No Phase Reversal

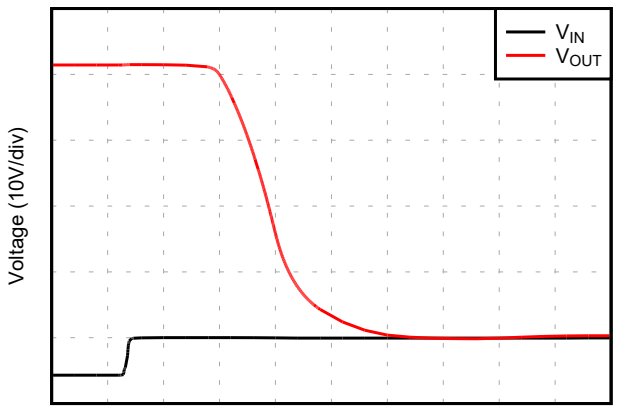


Figure 5-26. Positive Overload Recovery

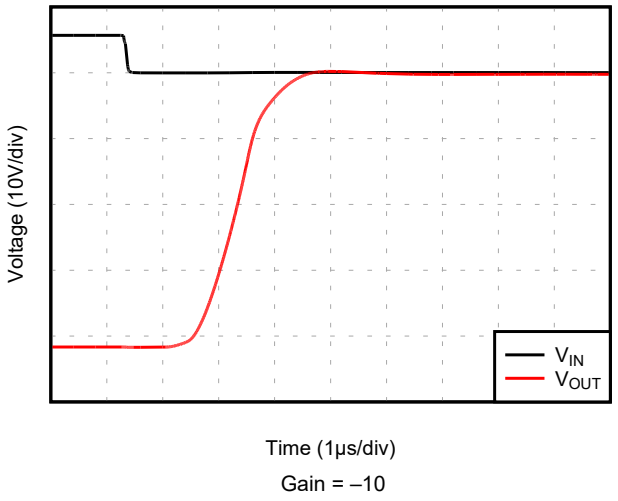


Figure 5-27. Negative Overload Recovery

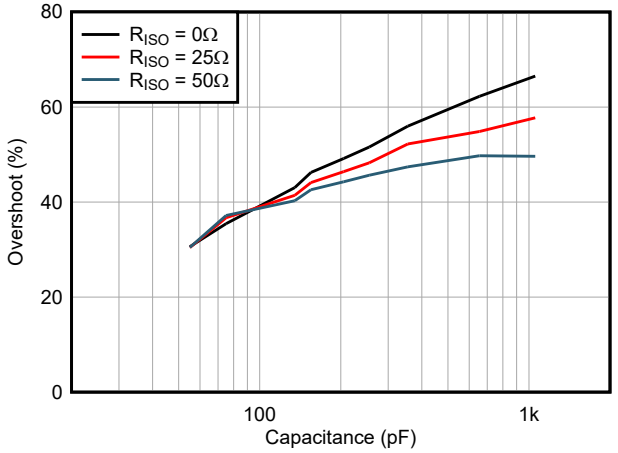


Figure 5-28. Open-Loop Output Impedance vs Frequency

Copyright © 2026 Texas Instruments Incorporated

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 85V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ (unless otherwise noted)

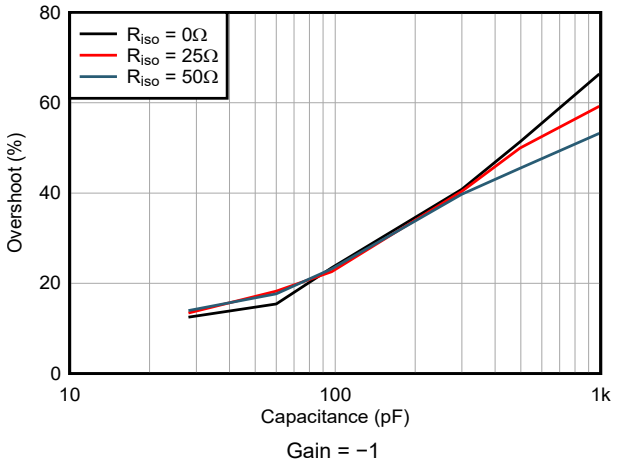


Figure 5-29. Small-Signal Overshoot vs Capacitive Load

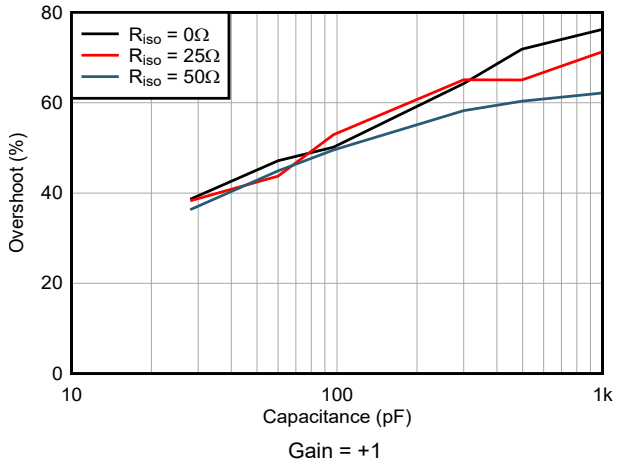


Figure 5-30. Small-Signal Overshoot vs Capacitive Load

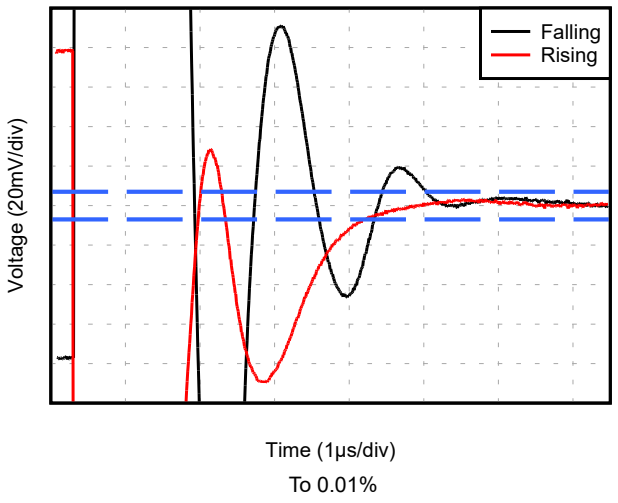


Figure 5-31. Settling Time

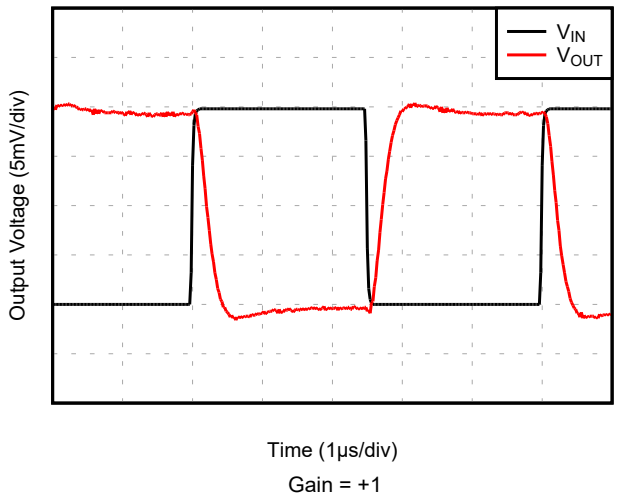


Figure 5-32. Small-Signal Step Response

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 85V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ (unless otherwise noted)

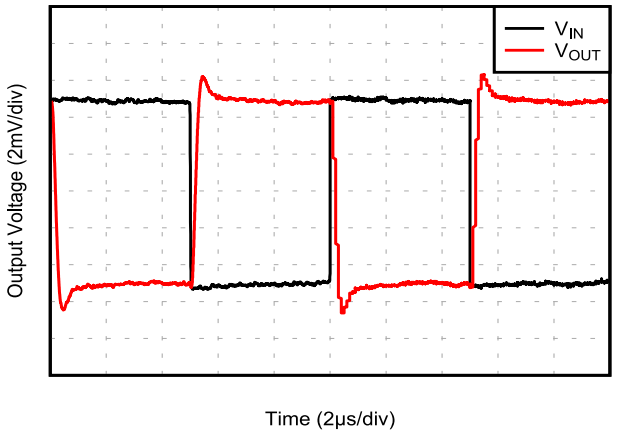


Figure 5-33. Small-Signal Step Response

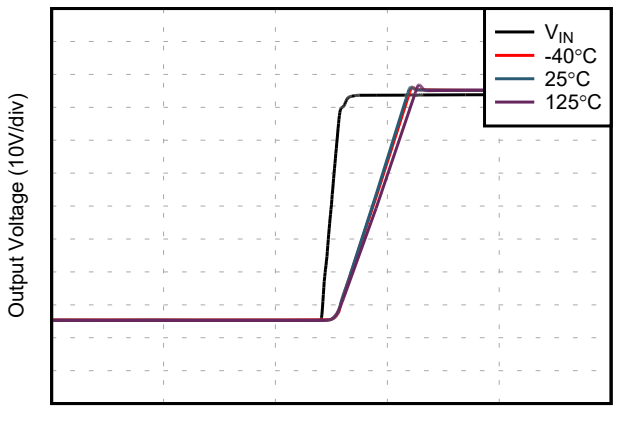


Figure 5-34. Large-Signal Step Response (Rising)

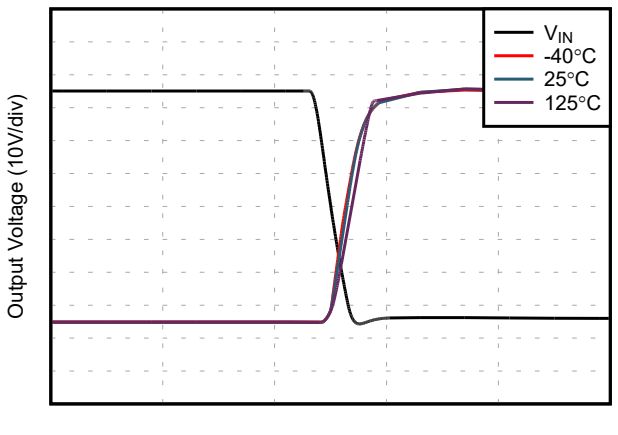


Figure 5-35. Large-Signal Step Response (Rising)

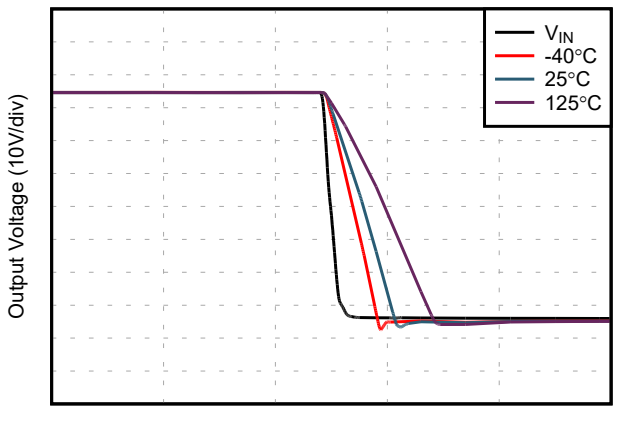


Figure 5-36. Large-Signal Step Response (Falling)

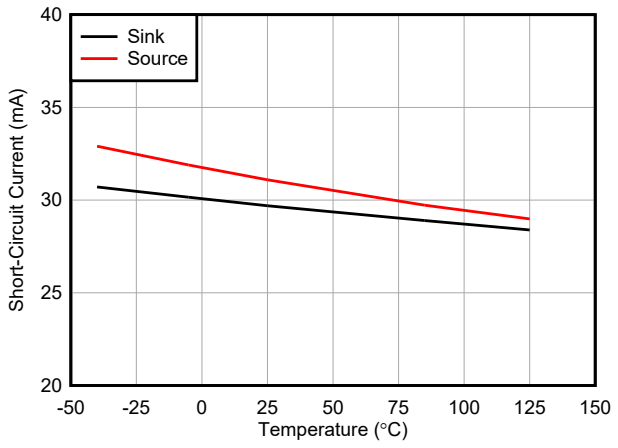


Figure 5-37. Short-Circuit Current vs Temperature

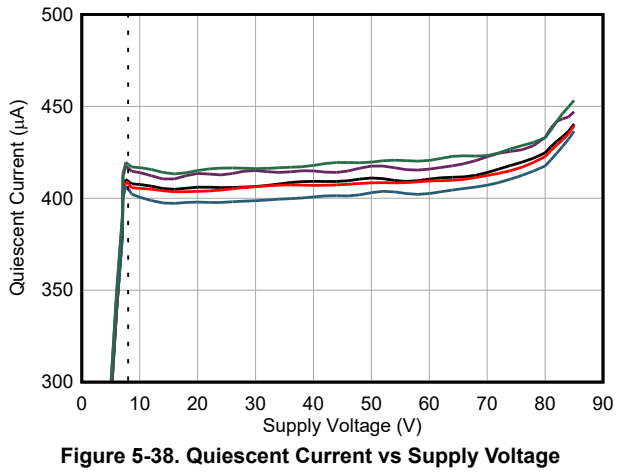


Figure 5-38. Quiescent Current vs Supply Voltage

Copyright © 2026 Texas Instruments Incorporated

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 85V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ (unless otherwise noted)

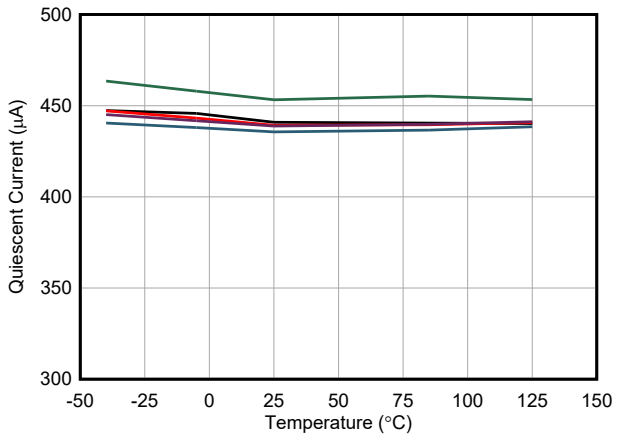


Figure 5-39. Quiescent Current vs Temperature

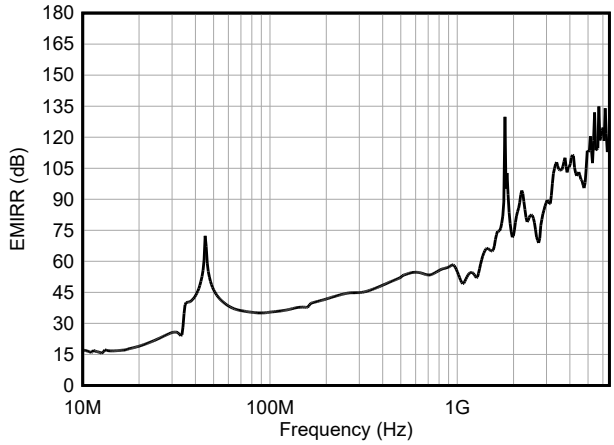


Figure 5-40. Electromagnetic Interference Rejection

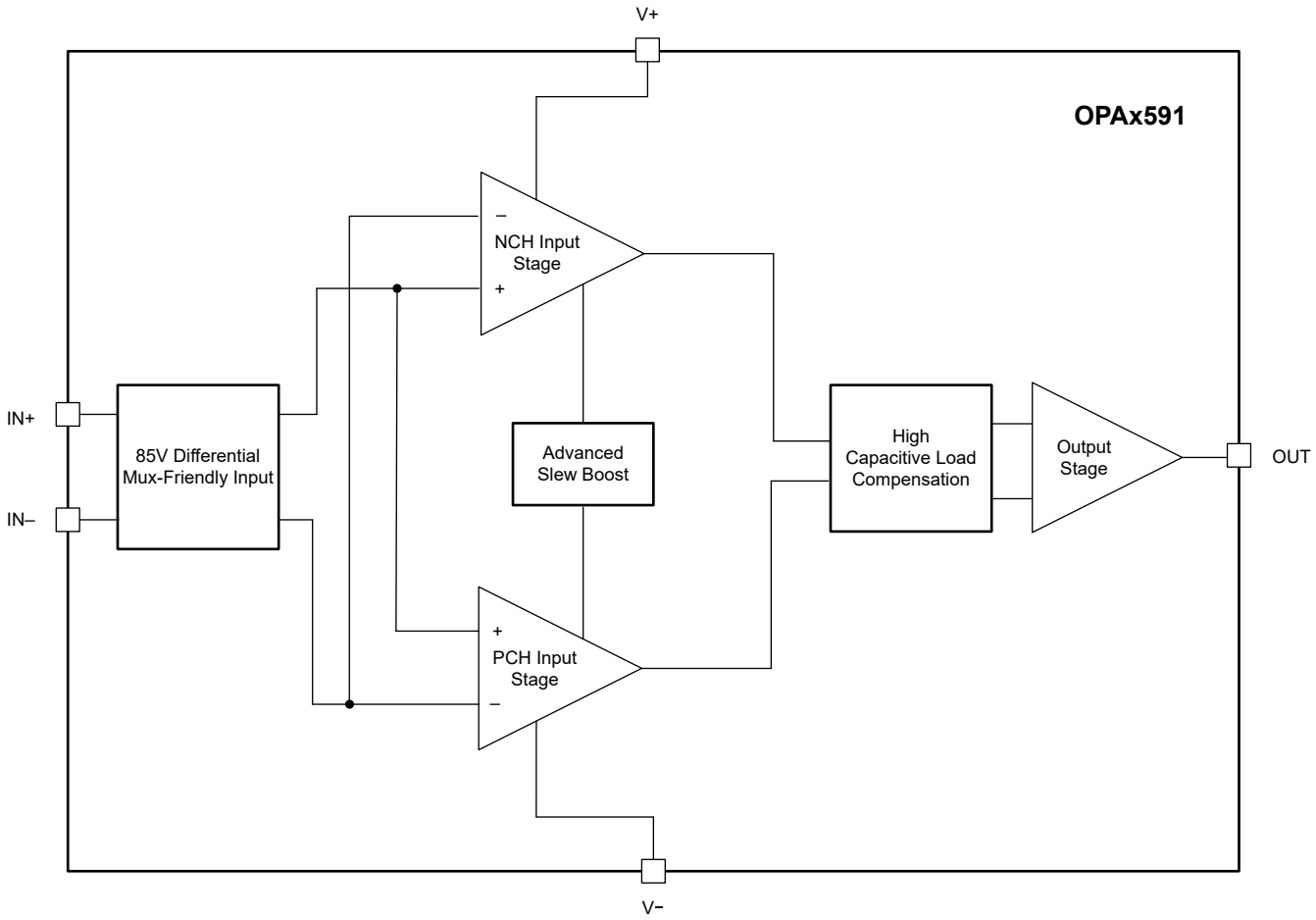
6 Detailed Description

6.1 Overview

The OPAx591 are high precision, low power (450µA), high-slew rate (100V/µs), 85V operational amplifiers (op amps). These op amps uses a proprietary design technique to achieve a very high slew capability with minimal power consumption. The OPAx591 is capable of driving ±30mA of output current and can swing to within 100mV of either power supply rail.

The amplifiers feature state-of-the-art CMOS technology and advanced design features that help achieve outstanding ac performance and enable small package options. The OPAx591 strengths also include 3.75MHz bandwidth, 12.8nV/√Hz noise spectral density, and low input bias current. These features make the OPAx591 an exceptional choice to gain or buffer the output of a digital-to-analog converter (DAC) and precision high-side current sense applications.

6.2 Functional Block Diagram



Copyright © 2026 Texas Instruments Incorporated

6.3 Feature Description

6.3.1 Offset Correction

The input offset voltage of an op amp is a major source of error in many applications. Input offset is caused by small mismatches in the input transistors and can vary significantly across operating temperature. The mismatch can be corrected for at the wafer level by measuring the offset voltage and simultaneously adjusting, or trimming, the current through the input transistors until the offset is near zero.

Each unit of OPAx591 is laser trimmed at production to correct for input offset voltage and input offset voltage variation across temperature known as offset voltage drift. Offset voltage drift describes the slope of the input offset versus temperature curve. In devices that exhibit non-linear and non-monotonic input offset over temperature characteristics, as is common with trimmed field-effect transistor (FET) input amplifiers, special care must be taken to calculate drift. The the box method, described by Equation 1, is the most common way to calculate drift.

$$dV_{OS}/dT = \frac{|V_{OS(Max)} - V_{OS(Min)}|}{T_{Max} - T_{Min}} \quad (1)$$

Unfortunately, the box method yields a one sided distribution that makes the use statistical analysis inappropriate. The OPAx591 uses a different method to properly represent drift performance. The OPAx591 is specified by computing the slopes of the input offset voltage versus temperature curve at various points along the temperature axis. The generated slopes yield normal distributions which are then used to perform statistical analysis. This method is consistent with other high precision, FET input amplifiers like the OPAx192, and provides a sufficiently conservative representation of the input offset voltage drift.

A useful curve can be generated to demonstrate how the OPAx591 drift performance varies across different temperature ranges. Designers can use Figure 6-1 in error analysis for the temperature most applicable to the application. When performing an error analysis over the full specified temperature range, use the typical and maximum values for input offset voltage drift as described in *Electrical Characteristics*.

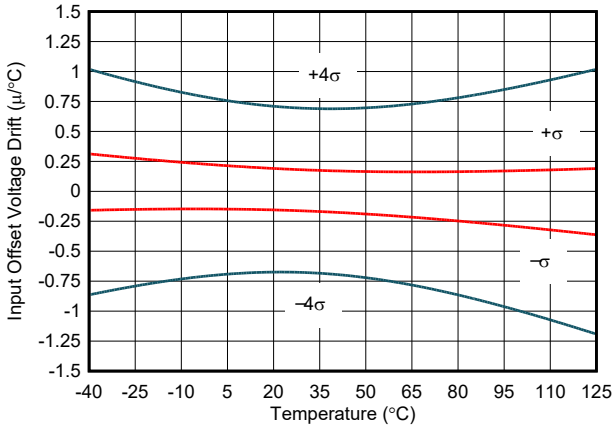


Figure 6-1. Input Offset Voltage Drift Versus Temperature

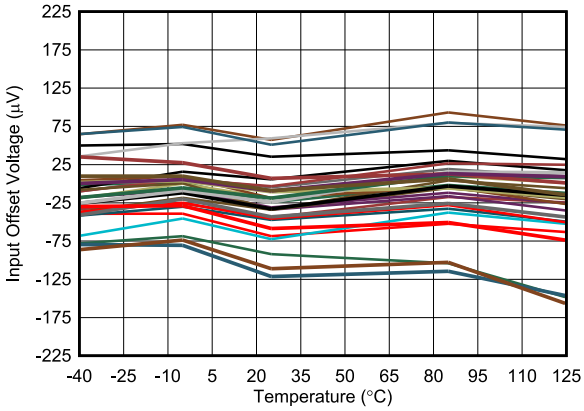


Figure 6-2. Input Offset Voltage Versus Temperature

The OPAx591 is carefully trimmed to achieve a maximum input offset voltage drift of 1µV/°C. This number is specified with robust statistical methods on device population bench system measurements. The low drift enables the amplifiers to be used in very high precision, high voltage applications. The input offset voltage versus temperature is for the OPA591 is illustrated in Figure 6-2.

Copyright © 2026 Texas Instruments Incorporated

6.3.2 MUX-Friendly Inputs

The OPAx591 use a unique input architecture to eliminate the need for input protection diodes but still provide robust input protection under transient conditions. The conventional input diode protection schemes in Figure 6-3are activated by fast transient step responses, and potentially introduce signal distortion and settling time delays because of alternate current paths; see also Figure 6-4. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes that cause an increase in input current and result in extended settling time.

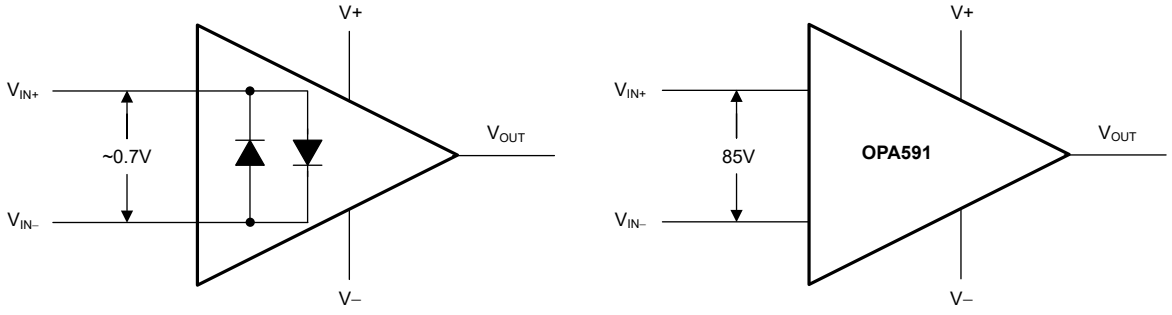


Figure 6-3. OPA591 Input Protection Does Not Limit Differential Input Capability

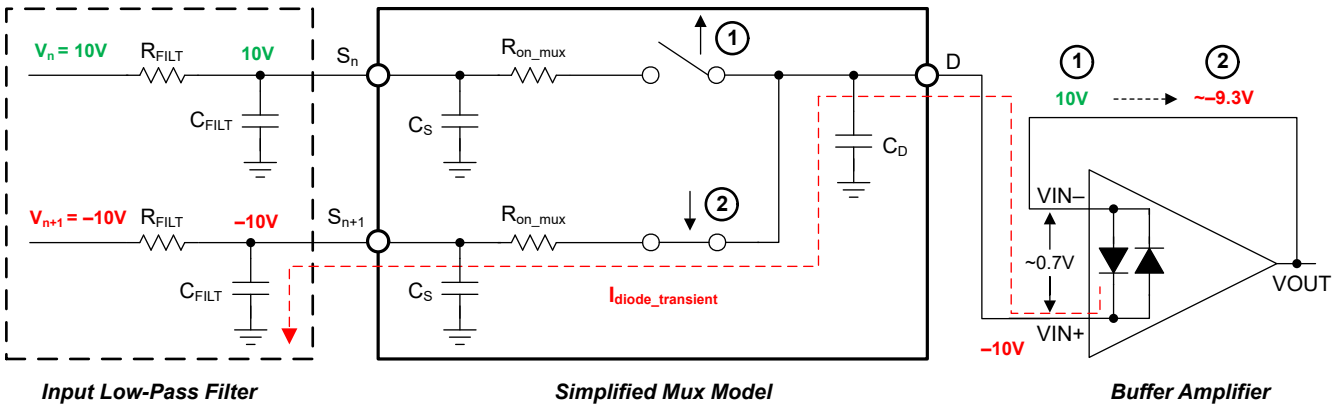


Figure 6-4. Back-to-Back Diodes Create Settling Issues

The OPAx591 feature a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making these devices an excellent choice for multichannel, high-switched, input applications. The OPAx591 tolerate a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 85V, making these devices a great choice for use as a comparator or in applications with fast-ramping or switched input signals.

Copyright © 2026 Texas Instruments Incorporated

6.3.3 Thermal Protection

The OPAx591 has a thermal protection feature that prevents damage from self heating. When the junction temperature (T_J) reaches approximately 170ºC, the op amp output stage disables. This thermal protection works by monitoring the temperature of the output stage and turning off the op amp output drive. Thermal protection forces the output to a high-impedance state. The OPAx591 is designed with approximately 20°C of thermal hysteresis and returns to normal operation when the output stage temperature becomes less than approximately 150°C.

This thermal protection is not designed to prevent this device from exceeding absolute maximum ratings, but rather from excessive thermal overload.

6.3.4 Advanced Slew Boost

Slew rate is the maximum rate of change of output voltage change with respect to time and is typically specified in units of volts per microsecond, V/µs. Op amps can enter a slew condition when a large, rapid moving signal is applied at the input. While slewing, the op amp enters an open loop condition and significant slew induced distortion can be seen on the output signal.

Equation 2 shows that the slew rate, SR, of an op amp is typically determined by the saturation current of the input stage, I_{TAIL}, and the compensation capacitor, C_C.

$$SR = \frac{I_{TAIL}}{C_C} \tag{2}$$

Slew rate typically scales with the quiescent current, I_Q, of the op amp. There are several ways that designers have overcome slew rate limitation. For example, lowering C_C, commonly known as decompensation, improves slew rate at the expense of stability. Decompensated op amps require a minimum gain and are not stable at unity gain. More commonly, modern op amps are equipped with slew boost technology that increases I_{SAT} to improve slew rate. Slew boost circuits can vary in implementation, but typically, expect about a four-fold improvement over comparable unboosted op amps.

The OPAx591 uses a proprietary design to achieve an unprecedented slew rate to I_Q ratio. The novel slew boost technology in OPAx591 provides a nearly 100 × slew rate improvement over comparable unboosted op amps. The op amp is unity gain stable and can be used configured as a buffer if desired.

Table 6-1 shows a comparison of slew rates and quiescent currents of different op amps.

Table 6-1. Op Amp Slew Rates and Quiescent Current

PART NUMBER	SLEW RATE	QUIESCENT CURRENT
OPAx591	100V/µs	450µA
OPAx188	0.8V/µs	425µA
OPAx202	0.35V/µs	580µA
OPAx192	20V/µs	1mA
OPA454	13V/µs	3.2mA

Copyright © 2026 Texas Instruments Incorporated

6.3.5 Full-Power Bandwidth Improved

The full-power bandwidth curve has been a staple in datasheets for decades. The full-power bandwidth of an op amp provides some indication about where designers can expect slew-induced distortion on a signal of a given amplitude and frequency. The full-power bandwidth curve is generated using Equation 3.

$$\text{FPBW} = \frac{\text{SR}}{2\pi V_{\text{OUT_MAX}}} \tag{3}$$

Figure 6-5 shows the full-power bandwidth of the OPAx591. The curve is a good reference for designers that need to achieve high-voltage, high-frequency output swings with little concern for distortion performance. Unfortunately, the curve provides little indication of the true distortion at any given point on the curve. The full-power bandwidth curve is, after all, only a theoretical value and slew-induced distortion appears gradually as the output nears the maximum rate of change. Furthermore, slew-induced distortion is only one of several sources of op-amp distortion. Therefore, the curve is a decent starting point, but not a reliable source for distortion performance.

Figure 6-6 shows the full power bandwidth in terms of total harmonic distortion (THD) performance for the OPAx591. This curve provides a better indication of the level of distortion that a designer can expect for a signal of a given amplitude and frequency. For example, the OPAx591 can achieve approximately −100dB or better of THD at $70V_{PP}$ up to approximately 1kHz. As a second example, the OPAx591 can achieve approximately −130dB or better of THD at $10V_{PP}$ up to about 1kHz. As a result of limitations in measurement bandwidth, only 20kHz data are recorded.

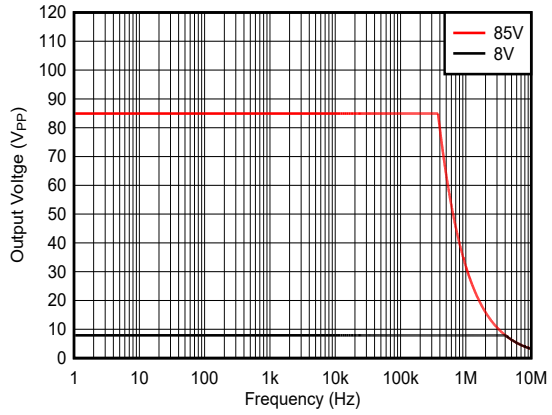


Figure 6-5. Full-Power Bandwidth

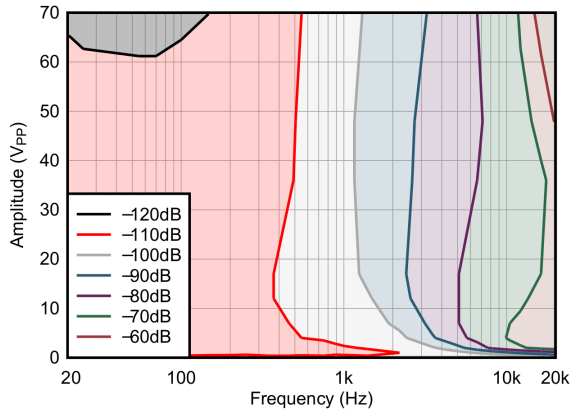


Figure 6-6. Full-Power Bandwidth Improved

6.3.6 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time.

6.4 Device Functional Modes

The OPAx591 has a single functional mode and is operational when the power-supply voltage is between 8V (±4V) and 85V (±42.5V).

Copyright © 2026 Texas Instruments Incorporated

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPAx591 are high precision, low power (450µA), high-slew rate (100V/µs), 85V power operational amplifiers (op amps). These op amps use a proprietary design technique to achieve a very high slewing capability while consuming minimal power. The low power consumption helps reduce heat generation on the board while the output swings near the supply rail. The high slew reduces slew related distortion at the output when dealing with large peak, high frequency signals.

7.2 Typical Applications

7.2.1 High Voltage Instrumentation Amplifier

Current monitoring is a critical function in a wide range of applications. While several current sensing methods exist, a shunt resistor provides a highly accurate, and robust approach. Designers need to choose between high-side and low-side current measurements. High-side measurement is often preferred where accuracy and load protection are critical.

High-side current sense circuits require special consideration of the input and output common-mode limitations of the amplifier. The biggest challenge in high-side current measurements is making sure that the amplifier can support and mitigate the errors that are inherent to high common-mode voltage. Designers can attenuate the common-mode voltage by using a difference amplifier, but significant gain and input impedance trade-offs exist. High input impedance and large gain is especially critical when measuring small currents. In such cases, an instrumentation amplifier provides the required input impedance, and gain.

The trade-off is that instrumentation amplifiers have a complex input voltage range that depends on the common-mode voltage, differential voltage, gain, and reference voltage. The input stage alone is bound by the input common-mode voltage limitation and the maximum power supply voltage range of the operational amplifier. Fortunately, the OPAx591 offers a high operating power supply voltage that enables designers to build a very high common-mode, high impedance, high gain, high common-mode rejection instrumentation amplifier. This instrumentation amplifier can be used to measure small differential signals in the presence of very high common-mode voltage.

7.2.1.1 Design Requirements

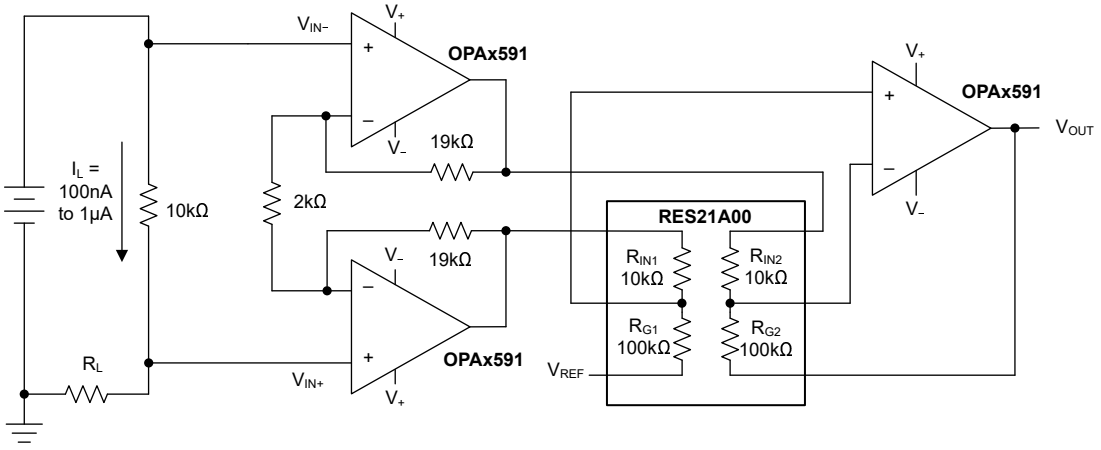


Figure 7-1. OPAx591 Instrumentation Amplifier With RES31A

The OPAx591 is used to build a high precision instrumentation amplifier that is capable of operating with high common-mode voltages. This instrumentation is an attractive option for high voltage, high-side current sensing. A high-voltage, high-side current sense application is discussed here.

Use the following parameters for this design example:

- Common-mode voltage: 54V
- Current output range: 100nA to 1µA
- Typical uncalibrated error: < 1%

7.2.1.2 Detailed Design Procedure

The OPAx591 can be configured as a three operational amplifier (op amp) to achieve a very high input common-mode voltage range. The instrumentation amplifier can be compartmentalized as a two stage amplifier with an input or gain stage, and a difference amplifier stage. Figure 7-2 illustrates a generic three op amp instrumentation amplifier.

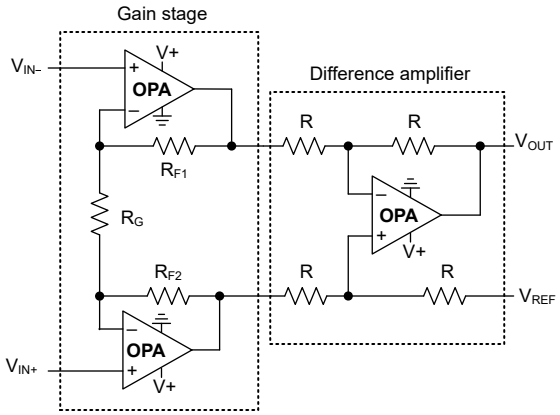


Figure 7-2. Instrumentation Amplifier

To support the high common-mode voltage range requirement, the OPAx591 is powered with 85V, yielding a 81.5V input common-mode voltage. The OPAx591 has an input voltage range of (V−) − 0.1V to (V+) − 3.5V. The output voltage swing also limits the common-mode voltage for a given differential voltage. The relationship is given below in Equation 4. Note that 85V is the maximum operating power supply voltage of the OPAx591 and the 1.5V accounts for the linear output voltage swing for 10kΩ as given in *Electrical Characteristics*.

$$V_{IN+} + (V_{IN+} - V_{IN-})\left(\frac{R_F}{R_G}\right) < 85V - 1.5V \quad (4)$$

The shunt resistor is set to be as small as possible to minimize the voltage drop. Given practical amplifier error sources, choose a shunt resistor that provides a voltage drop large enough to meet the accuracy requirements of the application. The largest error source in current sense applications is the amplifier and resistor drift and typically set the lower bound on the shunt resistor value. In most general purpose applications, a voltage drop of no more than 100mV is acceptable.

The OPAx591 provides very low offset and offset drift to enable high accuracy measurements to be made even at low current values. Another benefit of the OPAx591 is the low input bias current of 15pA, maximum. The low input bias current enables high accuracy measurements down to the nanoampere range.

OPAx591 circuit is configured to provide a maximum output voltage of 20V for a full scale current of 1µA, corresponding to a 100mV drop across the 10kΩ shunt resistor. The gain of the first stage is set to 20V/V and the difference amplifier stage gain is set to 10V/V for a total gain of 200V/V. The lower bound of the current measurement capability of the circuit is determined by the maximum error tolerance of the application such that the percent error of the circuit increases as the voltage drop across the shunt resistor decreases. The transfer function of the amplifier given by Equation 5.

Copyright © 2026 Texas Instruments Incorporated

$$V_{OUT} = (V_{IN+} - V_{IN-})\left(1 + \frac{2R_F}{R_G}\right)\left(\frac{R_{G2}}{R_{IN2}}\right) + V_{REF} \quad (5)$$

This application uses the RES31A matched resistor chip from Texas Instruments. The resistors provide excellent matching and temperature drift when compared to discrete 0.1% resistors. Resistor matching is critical to achieving high common-mode rejection and low gain error. Figure 7-1 shows the final circuit. The circuit results are shown in Figure 7-4, Figure 7-5. Note that the error is a simulated result at room temperature with typical dc error values and worst case resistor matching values. Room temperature calibration is recommended to achieve higher accuracy measurements.

To simplify this circuit further, the OPAx591 can be used to gain and buffer a readily available monolithic difference amplifier, like INA132. The OPAx591 provide high gain and high input impedance necessary to measure small current values.

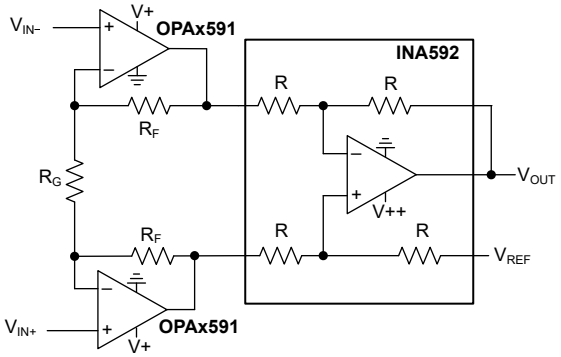


Figure 7-3. OPA591 Buffer for INA132

7.2.1.3 Application Curves

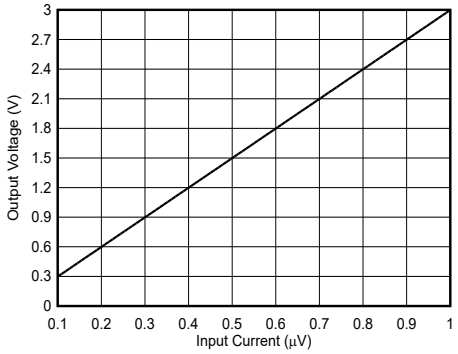


Figure 7-4. Output Voltage

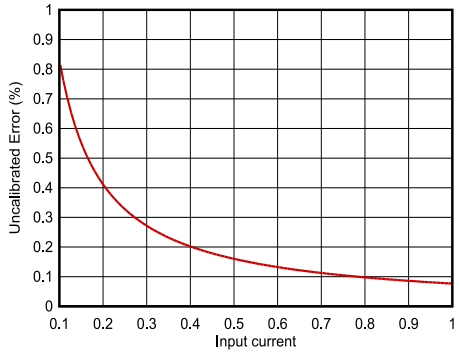


Figure 7-5. Output Voltage and Error

Copyright © 2026 Texas Instruments Incorporated

7.2.2 DAC Output Gain and Buffer

Many applications require precise control of a high voltage signal, but existing digital-to-analog converters (DACs) have a limited output range of 0V to 5V. The OPAx591 is designed for use as an output driver stage with gain to provide a high voltage, bipolar output voltage. The OPAx591 offers excellent dc precision at high voltage, small form factor packages, and low power consumption, making these amplifiers a great choice for high-channel, high density systems common in many test and measurement applications.

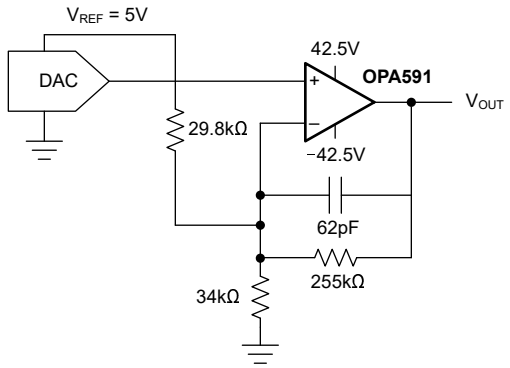


Figure 7-6. DAC Output Gain and Buffer

7.2.3 Single-Supply Piezoelectric Driver

Some piezoelectric transducers can be referenced to ground as shown in Figure 7-7. The piezoelectric load presents a large capacitance at the output of the amplifier and proper compensation is required to avoid instability. Figure 7-7 uses a dual-feedback compensation scheme to improve phase margin and enable accurate voltage setting to the load. Also consider the output current drive requirement. The current drive demand is determined by the frequency of operation and the effective capacitance of the load. High frequency and large capacitance reduce the effective impedance of the load and thereby increase the current drive requirement. The OPAx591 are an excellent choice to drive piezoelectric loads at dc and low frequency.

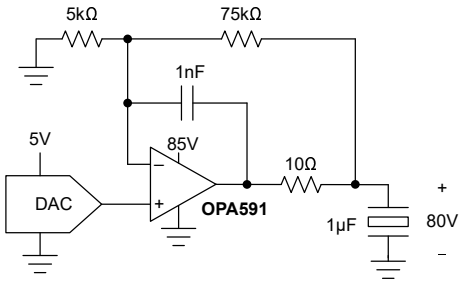


Figure 7-7. 80V Single-Supply Piezoelectric Driver

Copyright © 2026 Texas Instruments Incorporated

7.2.4 Current Booster

Some instances exists where designers require more output current drive from the OPAx591. Fig shows a simple current booster circuit that enables high voltage, high current drive capability. The circuit can be built with a couple of power MOSFETs or BJTs. One advantage of this circuit over monolithic power amplifiers is the significantly better thermal performance. The external transistors deliver the power and the OPAx591 is kept relatively cool to prevent any thermally related performance degradation.

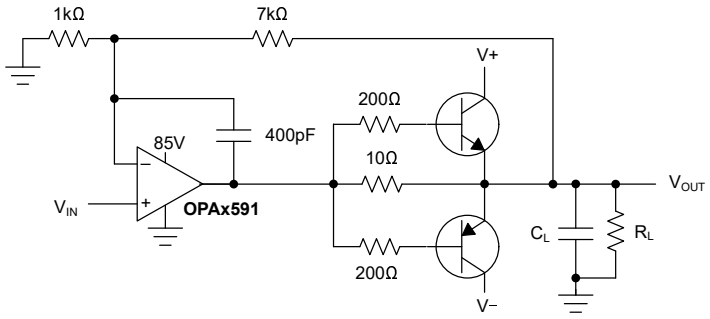


Figure 7-8. Current Booster Circuit

7.3 Power Supply Recommendations

The OPAx591 operates from power supplies up to ±42.5V (85V), and as little as ±4V (8V) with excellent performance. Most behavior remains unchanged throughout the full operating voltage range, but parameters can vary with operating voltage. A power-supply bypass capacitor of at least 0.1µF is required for proper operation. Make sure that the capacitor voltage is rated for high voltage across the full operating temperature range. The OPAx591 can be powered with asymmetrical supplies to optimize power dissipation in applications that do not require an equal positive and negative output voltage swing.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including the following guidelines:

- Noise can propagate into analog circuitry through the power pins of the op amp and the circuit as a whole. Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground. Place the capacitors as close to the device as possible. A single bypass capacitor from V+ to ground is sufficient for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

Copyright © 2026 Texas Instruments Incorporated

7.4.1.1 Thermal Considerations

Through normal operation, the op amps can self-heat. Self-heating is a natural increase in the die junction temperature that occurs in every amplifier. This self-heating is a result of several factors, including quiescent power consumption, package thermal resistance, PCB layout, and device operating conditions.

Operate the OPAx591 within the rated junction temperature, T_J, range to avoid thermal shutdown. Use the Equation 6 to determine the estimated T_J

$$T_J = P_D \times R_{\theta JA} + T_A \tag{6}$$

In a quiescent state, P_D is given by the product of the power supply and the quiescent current of the op amp. Equation 7 shows the calculation of T_J for the OPAx591 assuming an 85V power supply is used and an operating temperature of 25°C.

$$T_J = (85V \times 550\mu A) \times 165.4°\frac{C}{W} + 25°C \tag{7}$$

$$T_J = 32.73°C \tag{8}$$

The low power consumption of the OPAx591 causes minimal self-heating even in a small SOT23-5 package as given by Equation 8. In a loaded condition, P_D is equal to addition of the quiescent power, P_{DQ} and the power dissipated by the output stage, P_{DL}. The worst-case condition is given when the output voltage is equal to ½ of either supply rail (assuming symmetrical supplies, V+ and V-). In a worst-case condition, P_{DL} is given by Equation 9.

$$P_{DL} = \frac{(V+)^2}{4 \times R_L} \tag{9}$$

For example, assume the OPAx591 is powered with bipolar ±42.5V power supplies and drives a 5kΩ load, R_L, to ground. The maximum increase in T_J is expected to be about 22°C as given by Equation 10. In this example, to keep the op amp within the *Absolute Maximum Ratings*, operate in T_A well under 128°C to account for different factors.

$$\Delta T_J = (46.75mW + 90.3mW) \times 165.4\frac{°C}{W} \tag{10}$$

For high-voltage amplifiers such as the OPAx591, the junction temperature can easily be tens of degrees higher than the ambient temperature in a quiescent (unloaded) condition. As shown by Equation 6, the junction temperature depends on the thermal properties of the package, as expressed by the junction-to-ambient thermal resistance ($R_{\Theta JA}$).

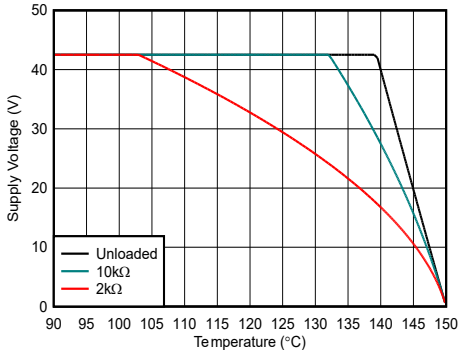


Figure 7-9. OPA591 (SOT23-5) Thermal Safe Operating Area

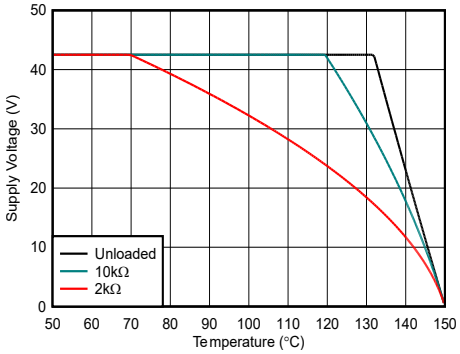


Figure 7-10. OPA2591 (VSSOP-8) Thermal Safe Operating Area

Copyright © 2026 Texas Instruments Incorporated

If the device then begins to drive a heavy load, the junction temperature can rise and trip the thermal-shutdown circuit. Figure 7-9 shows the maximum output voltage versus ambient temperature to avoid exceeding the *Absolute Maximum Ratings* in both loaded and unloaded conditions for the SOT23-5 package version of the OPA591. The curve assumes a typical quiescent current and does not account for any temperature variation of quiescent current.

7.4.1.2 Creepage and Clearance

When designing and building electrical systems with high voltage, two important concepts to consider are creepage and clearance. Creepage distance refers to the shortest path that an electric current can take along the surface of an insulating material, such as a printed circuit board (PCB) or a plastic enclosure. Clearance distance refers to the shortest distance between two conductive parts, such as wires, terminals, or components, through the air. Figure 7-11 illustrates creepage and clearance for a typical integrated circuit (IC).

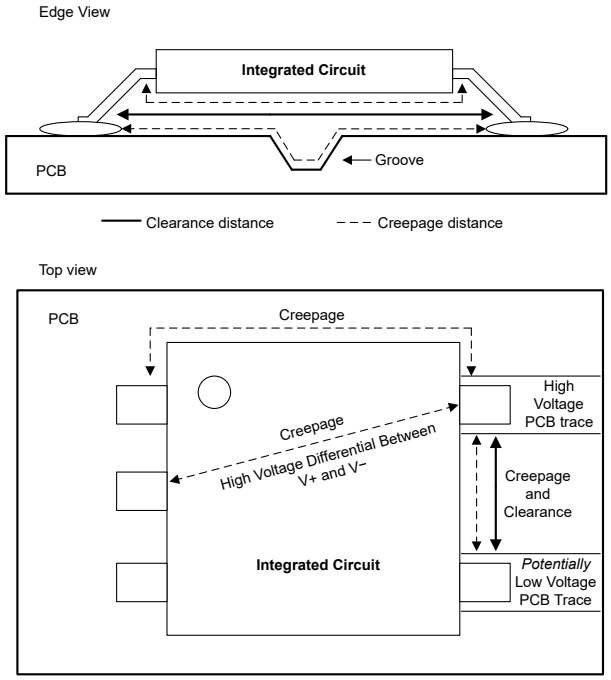


Figure 7-11. Creepage and Clearance in Integrated Circuits

Several standards exist with creepage and clearance guidance, but how the standards pertain to operational amplifiers and other integrated circuits is largely left to interpretation and internal requirements. The guidance distances are significantly affected by pollution degree, maximum voltage, and the underlying application. In the case of creepage, the comparative tracking index (CTI) rating of the insulating material is a major factor. Different design techniques exist to improve creepage and clearance if deemed necessary, including adding PBC grooves, conformal coating, and, or derating the operating voltage.

Texas Instruments offers modern packaging with small dimensions that are designed to minimize PCB area. However, the requirement to meet any creepage or clearance specifications depends on the designer's interpretation and implementation of any relevant IEC or system-level standards. For more information on this topic, visit the *Demystifying Clearance and Creepage Distance for High-Voltage End Equipment* document.

Copyright © 2026 Texas Instruments Incorporated

7.4.2 Layout Example

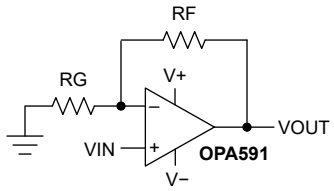


Figure 7-12. Schematic Representation of Noninverting Configuration

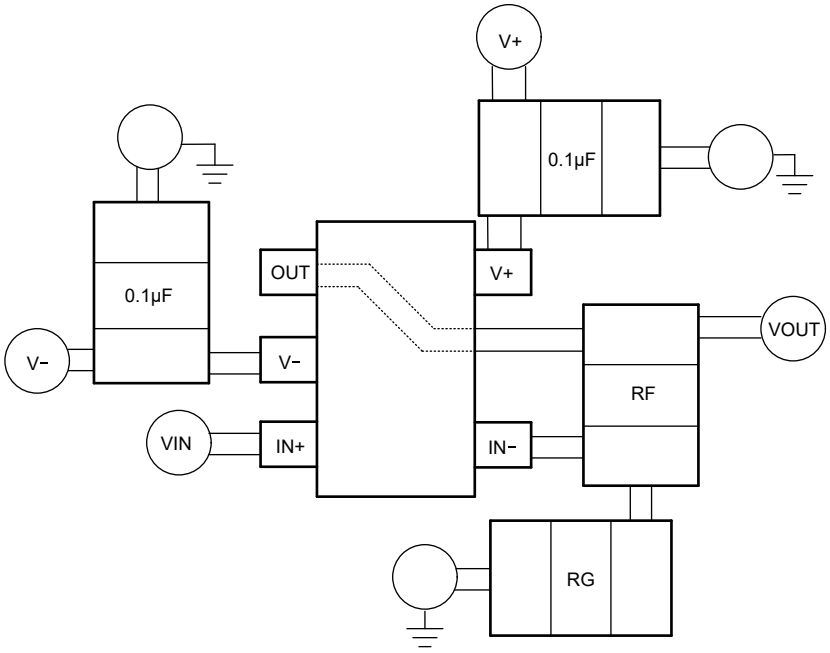


Figure 7-13. Board Layout for Noninverting Configuration of the SOT23-5 Package

Copyright © 2026 Texas Instruments Incorporated

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2026) to Revision B (November 2026)	Page
• Changed OPA2591DGK from Advance Information to Production Data	1

Changes from Revision * (February 2026) to Revision A (September 2026)	Page
• Changed OPA591DBV from Advance Information to Production Data	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2026 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA591DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O591
POPA2591DGKR	Active	Preproduction	VSSOP (DGK) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

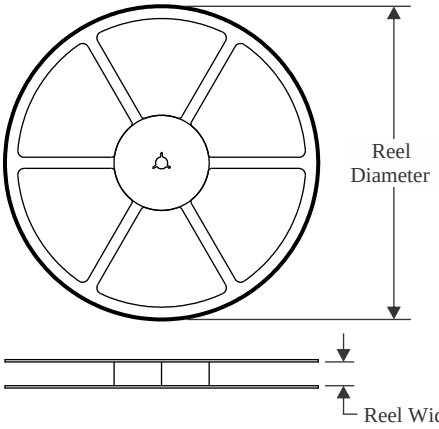
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

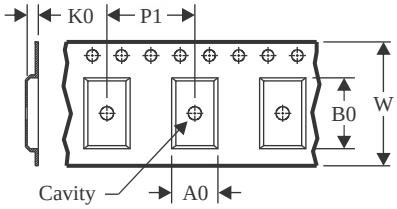
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

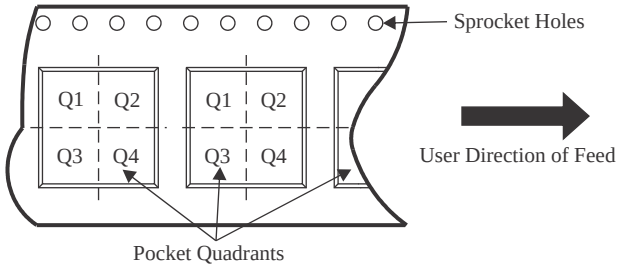


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

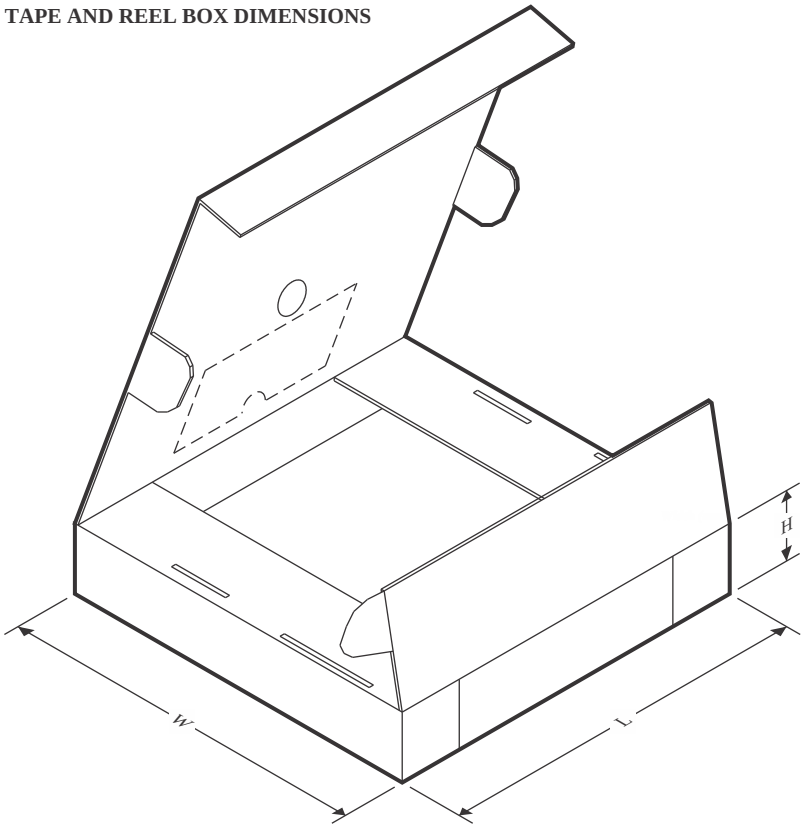
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA591DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

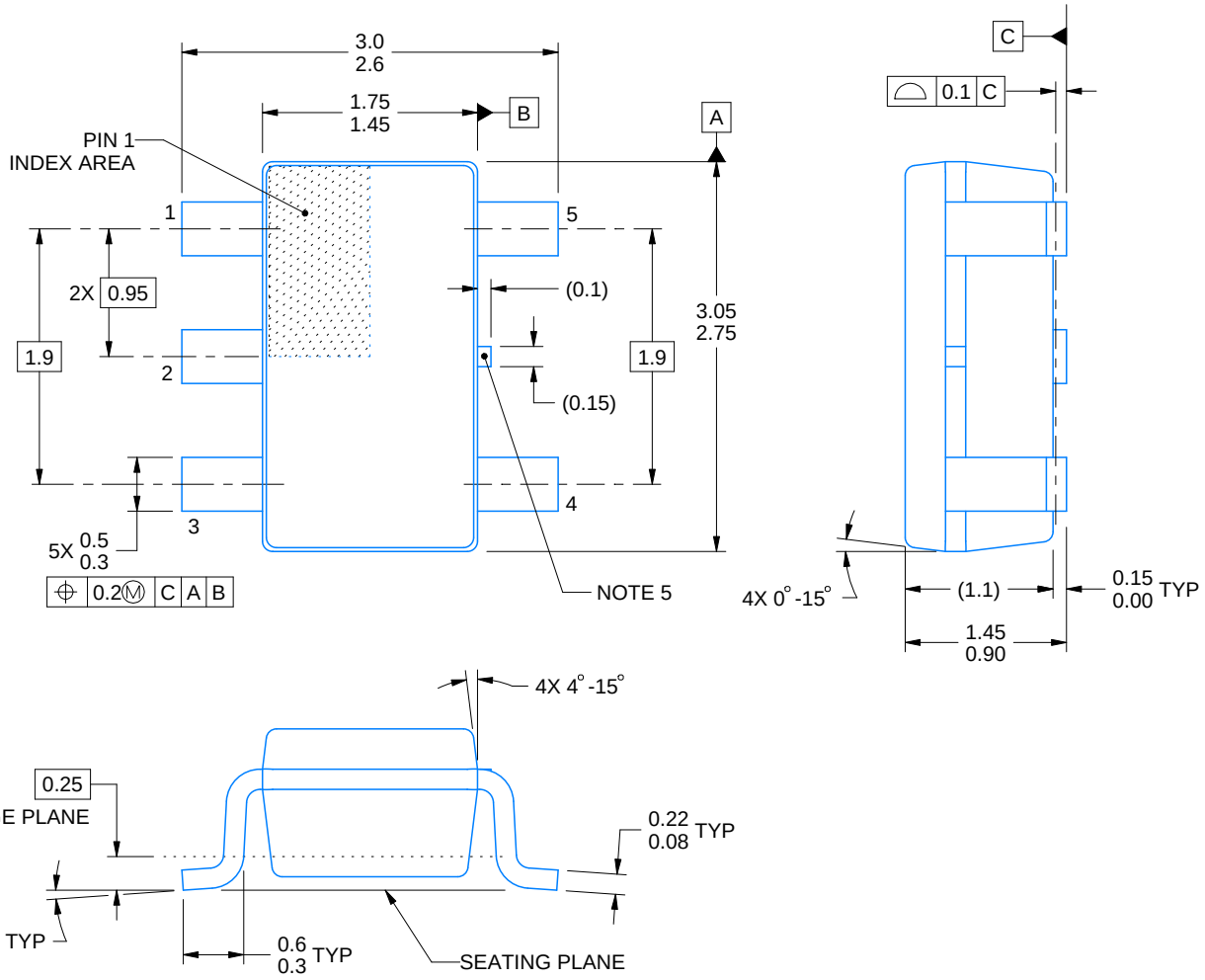
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA591DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

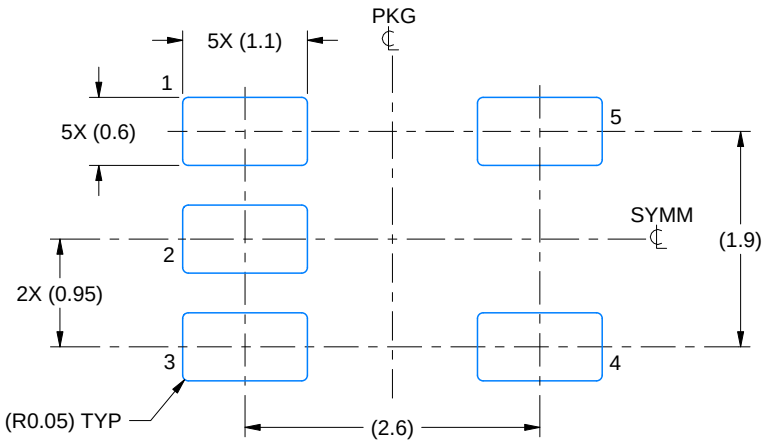
SMALL OUTLINE TRANSISTOR



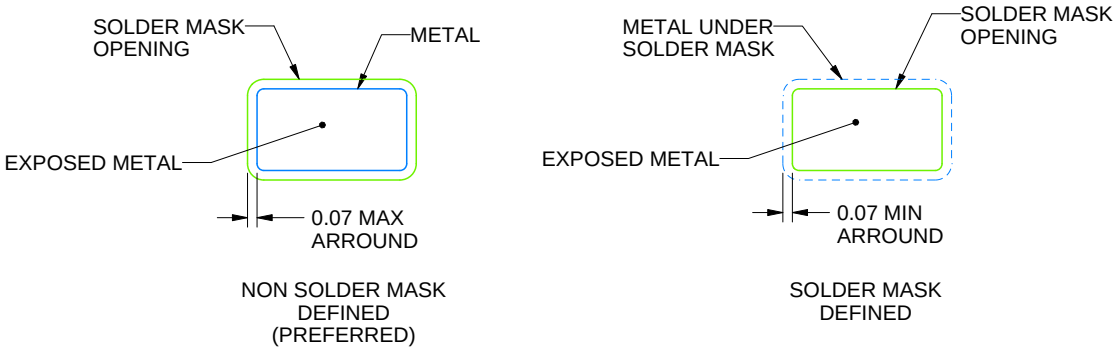
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

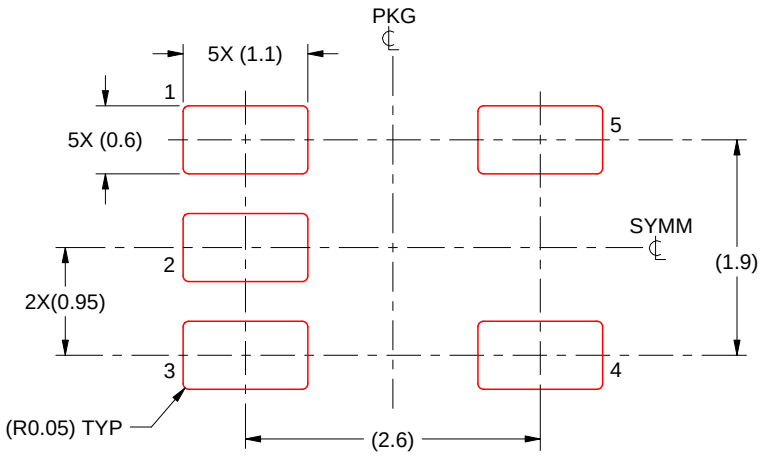


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

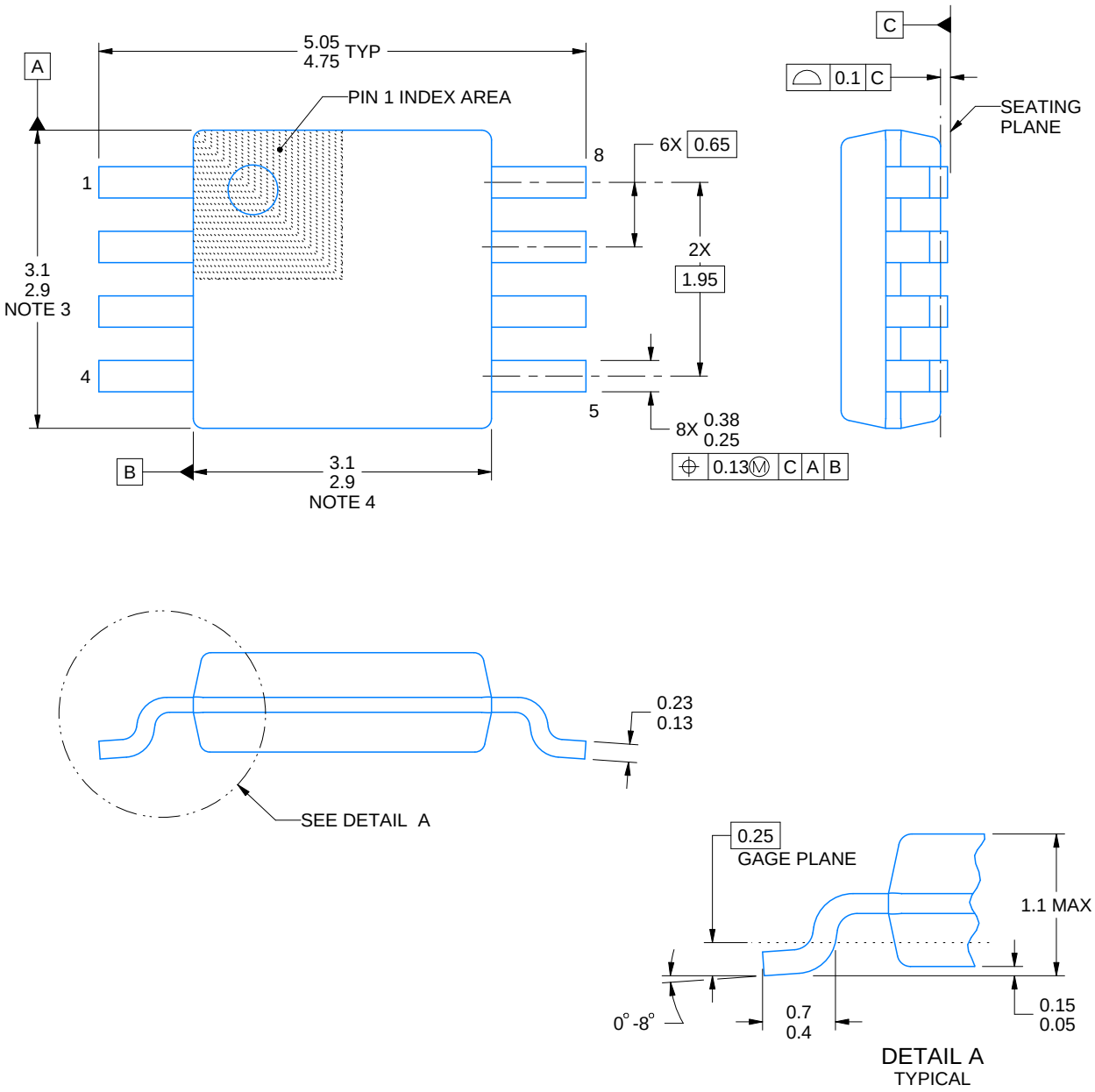
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

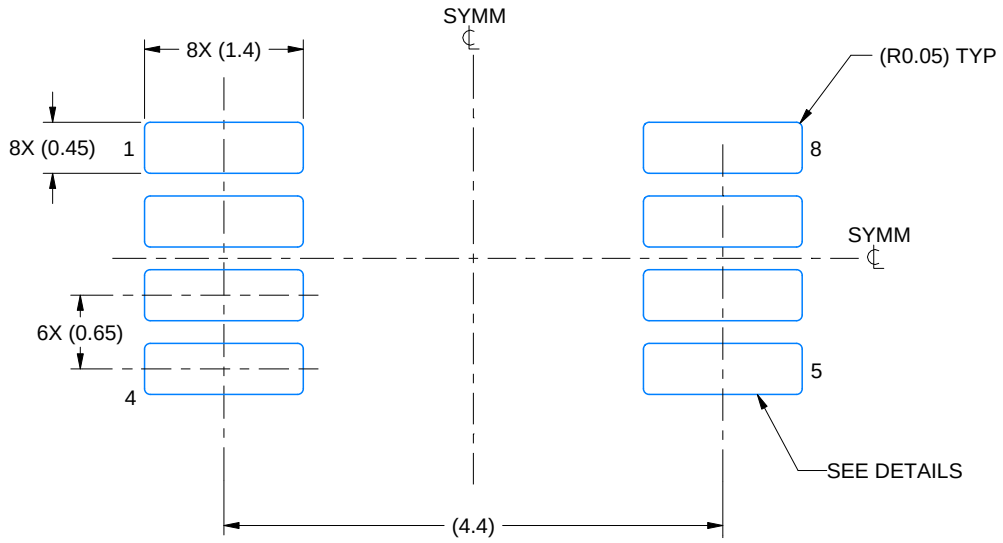
SMALL OUTLINE PACKAGE



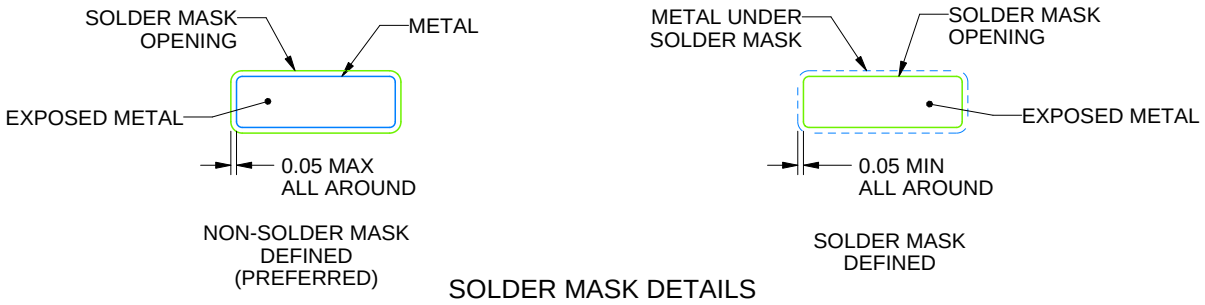
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

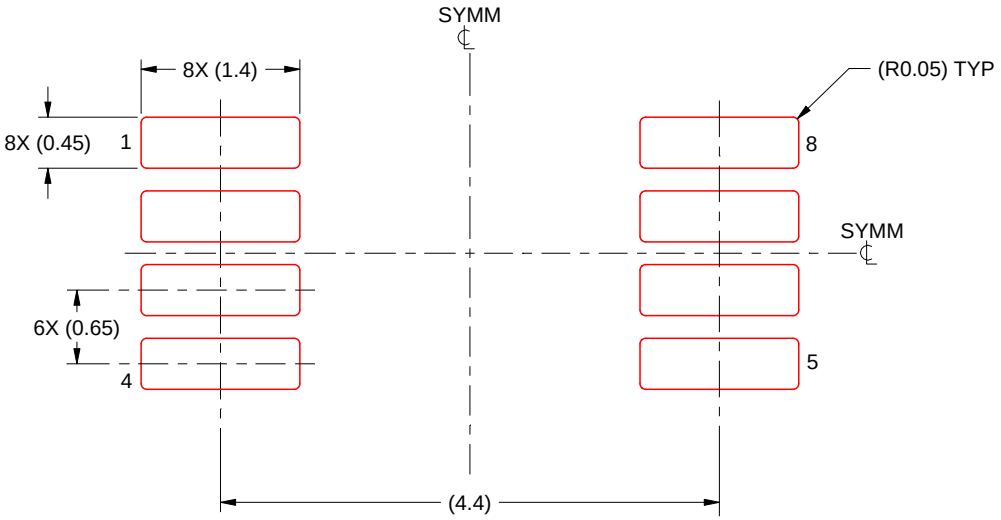


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025