

OPA703
OPA2703
OPA4703
OPA704
OPA2704
OPA4704

SBOS180A – MARCH 2001

CMOS, Rail-to-Rail, I/O OPERATIONAL AMPLIFIERS

FEATURES

- **RAIL-TO-RAIL INPUT AND OUTPUT**
- **WIDE SUPPLY RANGE:**
  Single Supply: 4V to 12V
  Dual Supplies: ±2 to ±6
- **LOW QUIESCENT CURRENT: 160µA**
- **FULL-SCALE CMRR: 90dB**
- **LOW OFFSET: 160µV**
- **HIGH SPEED:**
  OPA703: 1MHz, 0.6V/µs
  OPA704: 3MHz, 3V/µs
- ***Micro*SIZE PACKAGES:**
  SOT23-5, MSOP-8, TSSOP-14
- **LOW INPUT BIAS CURRENT: 1pA**

APPLICATIONS

- **AUTOMOTIVE APPLICATIONS:**
  Audio, Sensor Applications, Security Systems
- **PORTABLE EQUIPMENT**
- **ACTIVE FILTERS**
- **TRANSDUCER AMPLIFIER**
- **TEST EQUIPMENT**
- **DATA ACQUISITION**

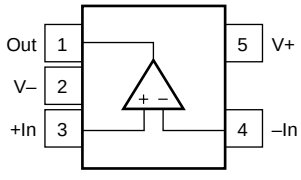
DESCRIPTION

The OPA703 and OPA704 series op amps are optimized for applications requiring rail-to-rail input and output swing. Single, dual, and quad versions are offered in a variety of packages. While the quiescent current is less than 200µA per amplifier, the OPA703 still offers excellent dynamic performance (1MHz GBW and 0.6V/µs SR) and unity-gain stability. The OPA704 is optimized for gains of 5 or greater and provides 3MHz GBW and 3V/µs slew rate.

The OPA703 and OPA704 series are fully specified and guaranteed over the supply range of ±2V to ±6V. Input swing extends 300mV beyond the rail and the output swings to within 40mV of the rail.

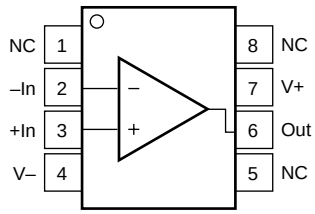
The single versions (OPA703 and OPA704) are available in the *Micro*SIZE SOT23-5 and in the standard SO-8 surface-mount, as well as the DIP-8 packages. Dual versions (OPA2703 and OPA2704) are available in the MSOP-8, SO-8, and DIP-8 packages. The quad OPA4703 and OPA4704 are available in the TSSOP-14 and SO-14 packages. All are specified for operation from –40°C to +85°C.

OPA703
OPA704



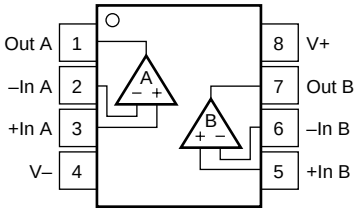
SOT23-5

OPA703
OPA704



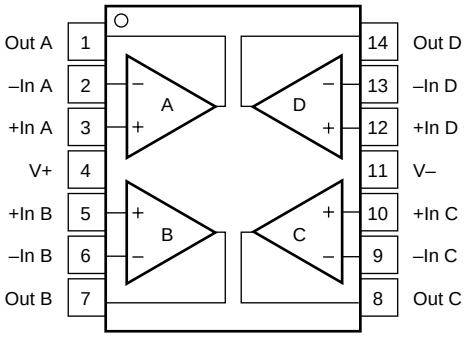
SO-8, DIP-8

OPA2703
OPA2704



MSOP-8, SO-8, DIP-8

OPA4703
OPA4704



TSSOP-14, SO-14

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V+ to V–	13.2V
Signal Input Terminals, Voltage[2]	(V–) –0.3V to (V+) +0.3V
Current[2]	10mA
Output Short-Circuit[3]	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	DESCRIPTION	MINIMUM RECOMMENDED GAIN	PACKAGE	PACKAGE DRAWING NUMBER	PACKAGE MARKING	ORDERING NUMBER[1]	TRANSPORT MEDIA
OPA703NA	Single, GBW = 1MHz	1	SOT23-5	331	A03	OPA703NA/250	Tape and Reel
"	"	"	"	"	"	OPA703NA/3K	Tape and Reel
OPA703UA	Single, GBW = 1MHz	1	SO-8	182	OPA703UA	OPA703UA	Rails
"	"	"	"	"	"	OPA703UA/2K5	Tape and Reel
OPA703PA	Single, GBW = 1MHz	1	DIP-8	006	OPA703PA	OPA703PA	Rails
OPA2703EA	Dual, GBW = 1MHz	1	MSOP-8	337	B03	OPA2703EA/250	Tape and Reel
"	"	"	"	"	"	OPA2703EA/2K5	Tape and Reel
OPA2703UA	Dual, GBW = 1MHz	1	SO-8	182	OPA2703UA	OPA2703UA	Rails
"	"	"	"	"	"	OPA2703UA/2K5	Tape and Reel
OPA2703PA	Dual, GBW = 1MHz	1	DIP-8	006	OPA2703PA	OPA2703PA	Rails
OPA4703EA	Quad, GBW = 1MHz	1	TSSOP-14	357	OPA4703EA	OPA4703EA/250	Tape and Reel
"	"	"	"	"	"	OPA4703EA/2K5	Tape and Reel
OPA4703UA	Quad, GBW = 1MHz	1	SO-14	235	OPA4703UA	OPA4703UA	Rails
"	"	"	"	"	"	OPA4703UA/2K5	Tape and Reel
OPA704NA	Single, GBW = 5MHz	5	SOT23-5	331	A04	OPA704NA/250	Tape and Reel
"	"	"	"	"	"	OPA704NA/3K	Tape and Reel
OPA704UA	Single, GBW = 5MHz	5	SO-8	182	OPA704UA	OPA704UA	Tape and Reel
"	"	"	"	"	"	OPA704UA/2K5	Tape and Reel
OPA704PA	Single, GBW = 5MHz	5	DIP-8	006	OPA704PA	OPA704PA	Rails
OPA2704EA	Dual, GBW = 5MHz	5	MSOP-8	337	B04	OPA2703EA/250	Tape and Reel
"	"	"	"	"	"	OPA2703EA/2K5	Tape and Reel
OPA2704UA	Dual, GBW = 5MHz	5	SO-8	182	OPA2704UA	OPA2704UA	Rails
"	"	"	"	"	"	OPA2704UA/2K5	Tape and Reel
OPA2704PA	Dual, GBW = 5MHz	5	DIP-8	006	OPA2704PA	OPA2704PA	Rails
OPA4704EA	Quad, GBW = 5MHz	5	TSSOP-14	357	OPA4704EA	OPA4704EA/250	Tape and Reel
"	"	"	"	"	"	OPA4704EA/2K5	Tape and Reel
OPA4704UA	Quad, GBW = 5MHz	5	SO-14	235	OPA4704UA	OPA4704UA	Rails
"	"	"	"	"	"	OPA4704UA/2K5	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /3K indicates 3000 devices per reel). Ordering 3000 pieces of "OPA703NA/3K" will get a single 3000-piece Tape and Reel.

OPA703 ELECTRICAL CHARACTERISTICS: V_S = 4V to 12V

Boldface limits apply over the specified temperature range, **T_A = –40°C to +85°C**

At T_A = +25°C, R_L = 20kΩ connected to V_S/2 and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		CONDITION	OPA703NA, UA, PA OPA2703EA, UA, PA OPA4703EA, UA MIN	TYP	MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = ±5V, V_{CM} = 0V		±160	±750	µV
Drift	**dV_{OS}/dT**	**T_A = –40°C to +85°C**		**±4**		**µV/°C**
vs Power Supply	PSRR	V_S = ±2V to ±6V, V_{CM} = 0V		20	100	µV/V
Over Temperature		**V_S = ±2V to ±6V, V_{CM} = 0V**			**200**	**µV/V**
Channel Separation, dc		R_L = 20kΩ		1		µV/V
f = 1kHz				98		dB
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V–) – 0.3		(V+) + 0.3	V
Common-Mode Rejection Ratio	CMRR	V_S = ±5V, (V–) – 0.3V < V_{CM} < (V+) + 0.3V	70	90		dB
over Temperature		**V_S = ±5V, (V–) < V_{CM} < (V+)**	**68**			**dB**
		V_S = ±5V, (V–) – 0.3V < V_{CM} < (V+) – 2V	80	96		dB
over Temperature		**V_S = ±5V, (V–) < V_{CM} < (V+) – 2V**	**74**			**dB**
INPUT BIAS CURRENT						
Input Bias Current	I_B	V_S = ±5V, V_{CM} = 0V		±1	±10	pA
Input Offset Current	I_{OS}	V_S = ±5V, V_{CM} = 0V		±0.5	±10	pA
INPUT IMPEDANCE						
Differential				$4 \cdot 10^9$ || 4		Ω || pF
Common-Mode				$5 \cdot 10^{12}$ || 4		Ω || pF
NOISE						
Input Voltage Noise, f = 0.1Hz to 10Hz		V_S = ±5V, V_{CM} = 0V		6		µVp-p
Input Voltage Noise Density, f = 1kHz	e_n	V_S = ±5V, V_{CM} = 0V		45		nV/√Hz
Current Noise Density, f = 1kHz	i_n	V_S = ±5V, V_{CM} = 0V		2.5		fA/√Hz
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	R_L = 100kΩ, (V–)+0.1V < V_O < (V+)–0.1V		120		dB
		R_L = 20kΩ, (V–)+0.075V < V_O < (V+)–0.075V	100	110		dB
over Temperature		**R_L = 20kΩ, (V–)+0.075V < V_O < (V+)–0.075V**	**96**			**dB**
		R_L = 5kΩ, (V–)+0.15V < V_O < (V+)–0.15V	100	110		dB
over Temperature		**R_L = 5kΩ, (V–)+0.15V < V_O < (V+)–0.15V**	**96**			**dB**
OUTPUT						
Voltage Output Swing from Rail		R_L = 100kΩ, A_{OL} > 80dB		40		mV
		R_L = 20kΩ, A_{OL} > 100dB			75	mV
over Temperature		**R_L = 20kΩ, A_{OL} > 96dB**			**75**	**mV**
		R_L = 5kΩ, A_{OL} > 100dB			150	mV
over Temperature		**R_L = 5kΩ, A_{OL} > 96dB**			**150**	**mV**
Output Current	I_{OUT}	|V_S – V_{OUT}| < 1V		±10		mA
Short-Circuit Current	I_{SC}			±40		mA
Capacitive Load Drive	C_{LOAD}		See Typical Performance Curves			
FREQUENCY RESPONSE		C_L = 100pF				
Gain-Bandwidth Product	GBW	G = +1		1		MHz
Slew Rate	SR	V_S = ±5V, G = +1		0.6		V/µs
Settling Time, 0.1%	t_S	V_S = ±5V, 5V Step, G = +1		15		µs
0.01%		V_S = ±5V, 5V Step, G = +1		20		µs
Overload Recovery Time		V_{IN} • Gain = V_S		3		µs
Total Harmonic Distortion + Noise	THD+N	V_S = ±5V, V_O = 3Vp-p, G = +1, f = 1kHz		0.02		%
POWER SUPPLY						
Specified Voltage Range, Single Supply	V_S		4		12	V
Specified Voltage Range, Dual Supplies	V_S		±2		±6	V
Operating Voltage Range				3.6 to 12		V
Quiescent Current (per amplifier)	I_Q	I_O = 0		160	200	µA
over Temperature					**300**	**µA**
TEMPERATURE RANGE						
Specified Range			–40		85	°C
Operating Range			–55		125	°C
Storage Range			–65		150	°C
Thermal Resistance	θ_{JA}					
SOT23-5 Surface-Mount				200		°C/W
MSOP-8 Surface-Mount				150		°C/W
TSSOP-14 Surface-Mount				100		°C/W
SO-8 Surface Mount				150		°C/W
SO-14 Surface Mount				100		°C/W
DIP-8				100		°C/W

OPA704 ELECTRICAL CHARACTERISTICS: V_S = 4V to 12V

Boldface limits apply over the specified temperature range, **T_A = –40°C to +85°C**

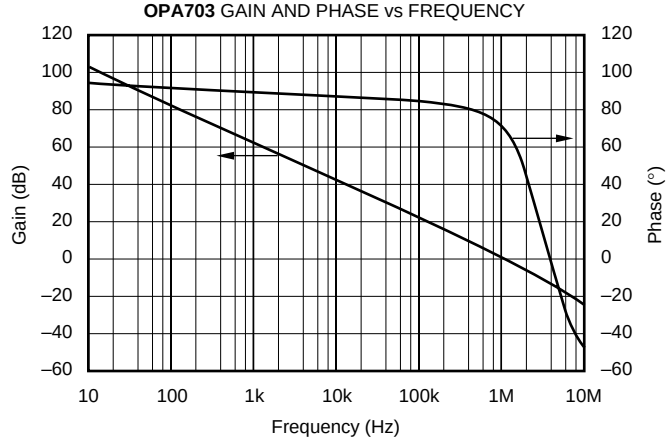
At T_A = +25°C, R_L = 20kΩ connected to V_S/2 and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		CONDITION	OPA704NA, UA, PA OPA2704EA, UA, PA OPA4704EA, UA MIN	TYP	MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = ±5V, V_{CM} = 0V		±160	±750	µV
Drift	**dV_{OS}/dT**	**T_A = –40°C to +85°C**		**±4**		**µV/°C**
vs Power Supply	PSRR	V_S = ±2V to ±6V, V_{CM} = 0V		20	100	µV/V
Over Temperature		**V_S = ±2V to ±6V, V_{CM} = 0V**			**200**	**µV/V**
Channel Separation, dc		R_L = 20kΩ		1		µV/V
f = 1kHz				98		dB
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V–) – 0.3		(V+) + 0.3	V
Common-Mode Rejection Ratio	CMRR	V_S = ±5V, (V–) – 0.3V < V_{CM} < (V+) + 0.3V	70	90		dB
over Temperature		**V_S = ±5V, (V–) < V_{CM} < (V+)**	**68**			**dB**
		V_S = ±5V, (V–) – 0.3V < V_{CM} < (V+) – 2V	80	96		dB
over Temperature		**V_S = ±5V, (V–) < V_{CM} < (V+) – 2V**	**74**			**dB**
INPUT BIAS CURRENT						
Input Bias Current	I_B	V_S = ±5V, V_{CM} = 0V		±1	±10	pA
Input Offset Current	I_{OS}	V_S = ±5V, V_{CM} = 0V		±0.5	±10	pA
INPUT IMPEDANCE						
Differential				$4 \cdot 10^9$ || 4		Ω || pF
Common-Mode				$5 \cdot 10^{12}$ || 4		Ω || pF
NOISE						
Input Voltage Noise, f = 0.1Hz to 10Hz		V_S = ±5V, V_{CM} = 0V		6		µVp-p
Input Voltage Noise Density, f = 1kHz	e_n	V_S = ±5V, V_{CM} = 0V		45		nV/√Hz
Current Noise Density, f = 1kHz	i_n	V_S = ±5V, V_{CM} = 0V		2.5		fA/√Hz
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	R_L = 100kΩ, (V–)+0.1V < V_O < (V+)–0.1V		120		dB
		R_L = 20kΩ, (V–)+0.075V < V_O < (V+)–0.075V	100	110		dB
over Temperature		**R_L = 20kΩ, (V–)+0.075V < V_O < (V+)–0.075V**	**96**			**dB**
		R_L = 5kΩ, (V–)+0.15V < V_O < (V+)–0.15V	100	110		dB
over Temperature		**R_L = 5kΩ, (V–)+0.15V < V_O < (V+)–0.15V**	**96**			**dB**
OUTPUT						
Voltage Output Swing from Rail		R_L = 100kΩ, A_{OL} > 80dB		40		mV
		R_L = 20kΩ, A_{OL} > 100dB			75	mV
over Temperature		**R_L = 20kΩ, A_{OL} > 96dB**			**75**	**mV**
		R_L = 5kΩ, A_{OL} > 100dB			150	mV
over Temperature		**R_L = 5kΩ, A_{OL} > 96dB**			**150**	**mV**
Output Current	I_{OUT}	|V_S – V_{OUT}| < 1V		±10		mA
Short-Circuit Current	I_{SC}			±40		mA
Capacitive Load Drive	C_{LOAD}		See Typical Performance Curves			
FREQUENCY RESPONSE		C_L = 100pF				
Gain-Bandwidth Product	GBW	G = +5		3		MHz
Slew Rate	SR	V_S = ±5V, G = +5		3		V/µs
Settling Time, 0.1%	t_S	V_S = ±5V, 5V Step, G = +5		18		µs
0.01%		V_S = ±5V, 5V Step, G = +5		21		µs
Overload Recovery Time		V_{IN} • Gain = V_S		0.6		µs
Total Harmonic Distortion + Noise	THD+N	V_S = ±5V, V_O = 3Vp-p, G = +5, f = 1kHz		0.025		%
POWER SUPPLY						
Specified Voltage Range, Single Supply	V_S		4		12	V
Specified Voltage Range, Dual Supplies	V_S		±2		±6	V
Operating Voltage Range				3.6 to 12		V
Quiescent Current (per amplifier)	I_Q	I_O = 0		160	200	µA
over Temperature					**300**	**µA**
TEMPERATURE RANGE						
Specified Range			–40		85	°C
Operating Range			–55		125	°C
Storage Range			–65		150	°C
Thermal Resistance	θ_{JA}					
SOT23-5 Surface-Mount				200		°C/W
MSOP-8 Surface-Mount				150		°C/W
TSSOP-14 Surface-Mount				100		°C/W
SO-8 Surface Mount				150		°C/W
SO-14 Surface Mount				100		°C/W
DIP-8				100		°C/W

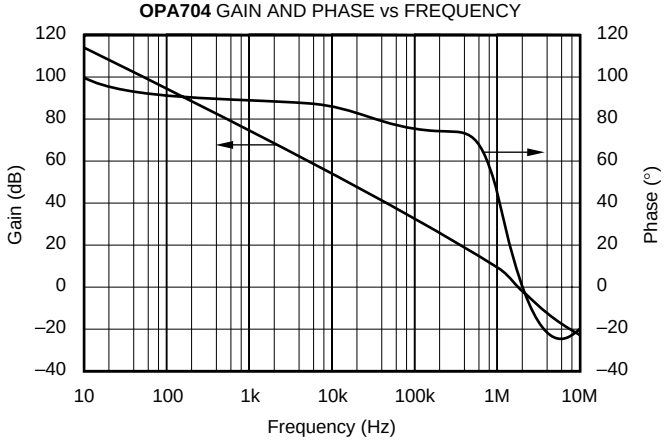
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = ±5V, and R_L = 20kΩ, unless otherwise noted.

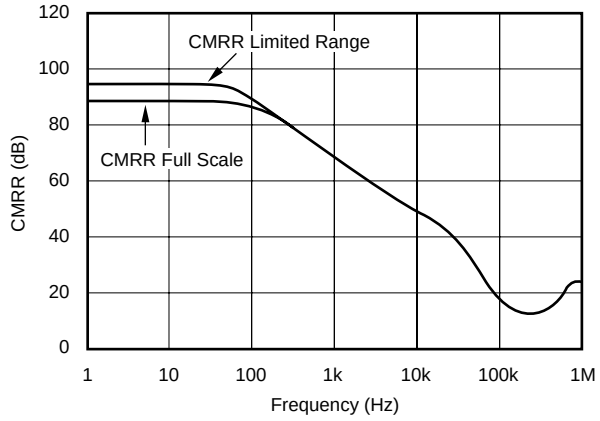
OPA703 GAIN AND PHASE vs FREQUENCY



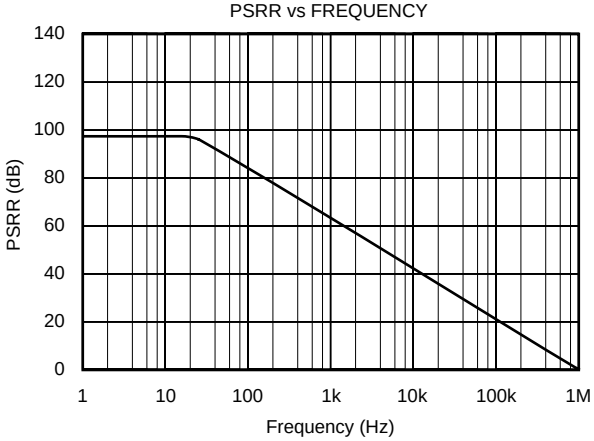
OPA704 GAIN AND PHASE vs FREQUENCY



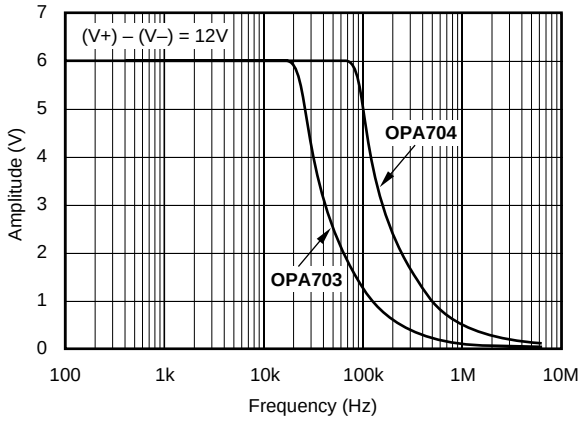
CMRR vs FREQUENCY



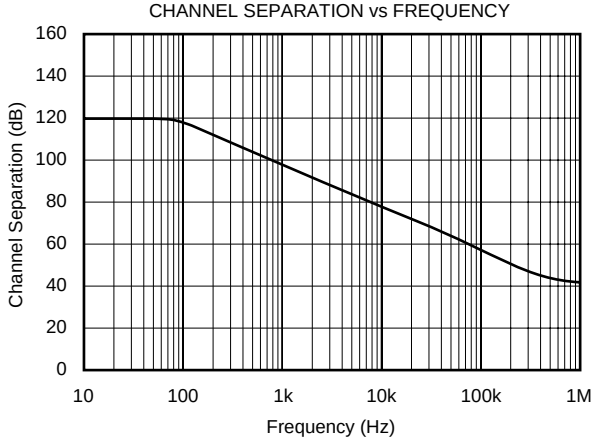
PSRR vs FREQUENCY



MAXIMUM AMPLITUDE vs FREQUENCY



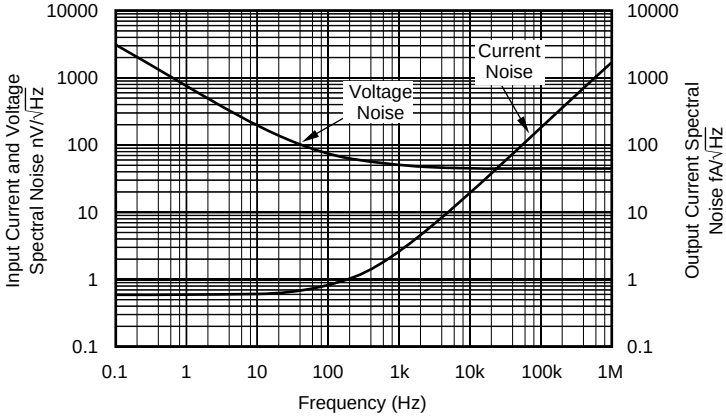
CHANNEL SEPARATION vs FREQUENCY



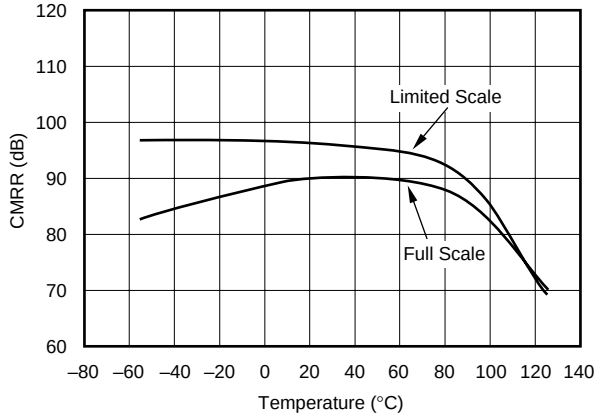
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = ±5V, and R_L = 20kΩ, unless otherwise noted.

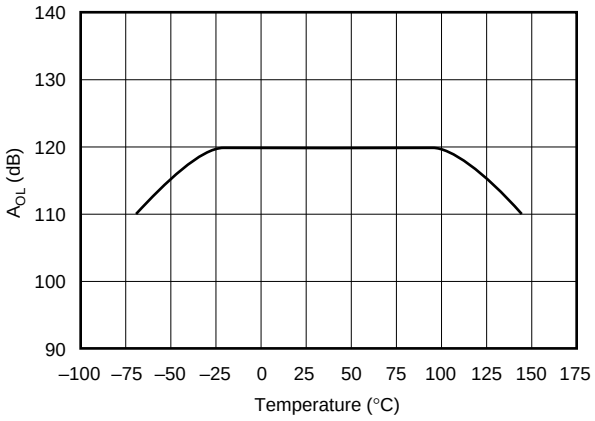
INPUT CURRENT AND VOLTAGE
SPECTRAL NOISE vs FREQUENCY



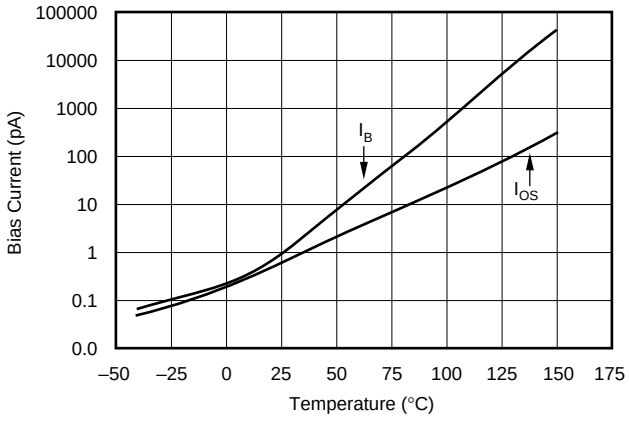
COMMON-MODE REJECTION RATIO
vs TEMPERATURE



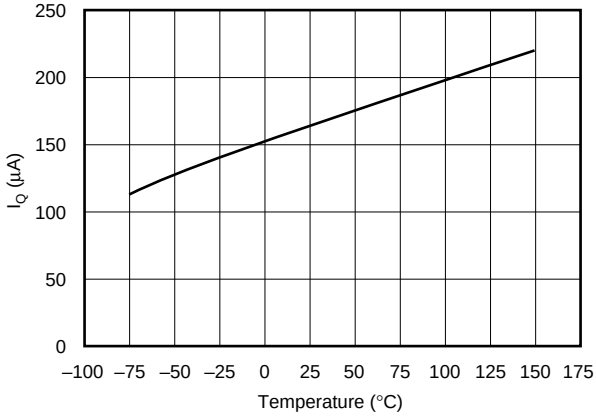
OPEN-LOOP GAIN vs TEMPERATURE



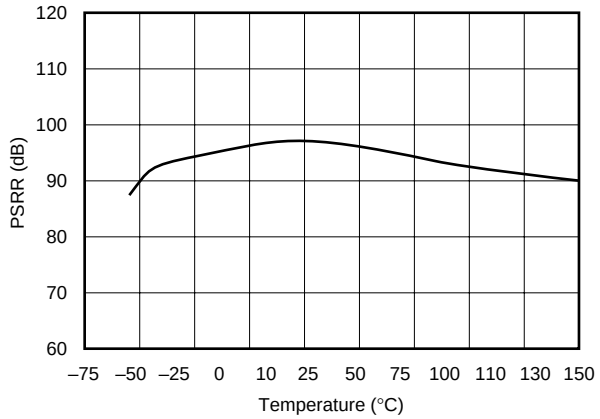
INPUT BIAS (I_B) AND OFFSET (I_{OS})
CURRENT vs TEMPERATURE



QUIESCENT CURRENT vs TEMPERATURE



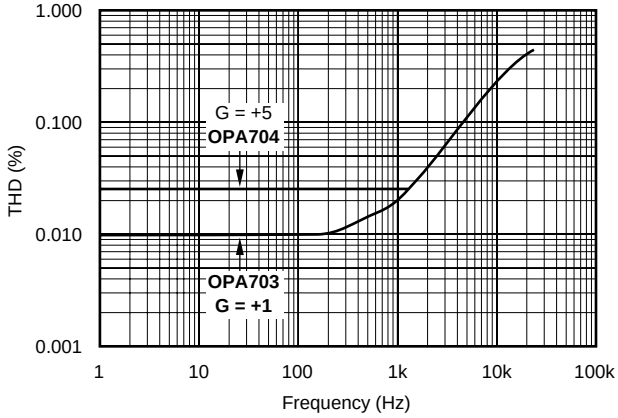
PSRR vs TEMPERATURE



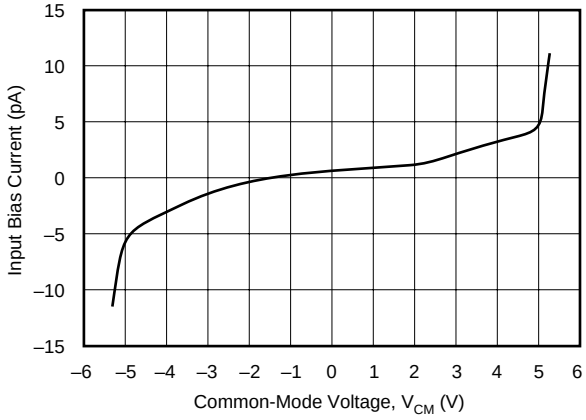
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = ±5V, and R_L = 20kΩ, unless otherwise noted.

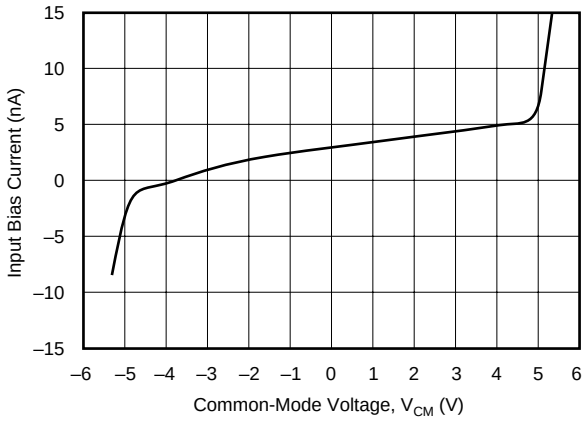
TOTAL HARMONIC DISTORTION PLUS NOISE
(Load = 5kΩ, BW = 8kHz, 1.0Vrms)



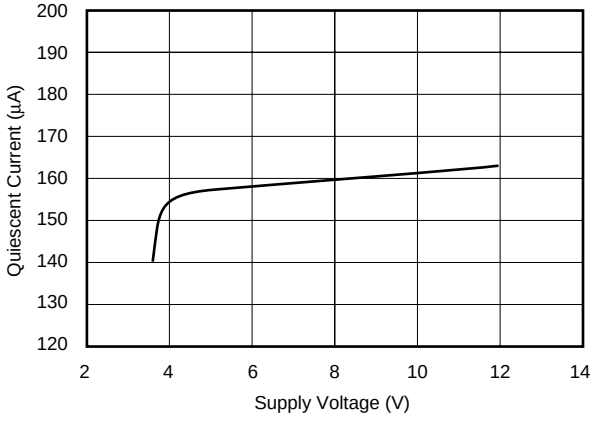
INPUT BIAS CURRENT (I_B)
vs COMMON-MODE VOLTAGE (V_{CM})
TEMPERATURE = °25C



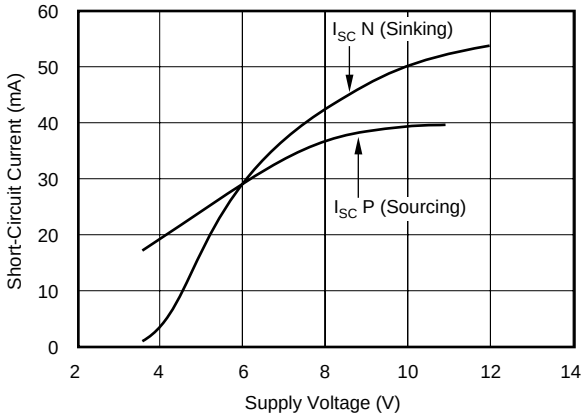
INPUT BIAS CURRENT (I_B)
vs COMMON-MODE VOLTAGE (V_{CM})
TEMPERATURE = 125°C



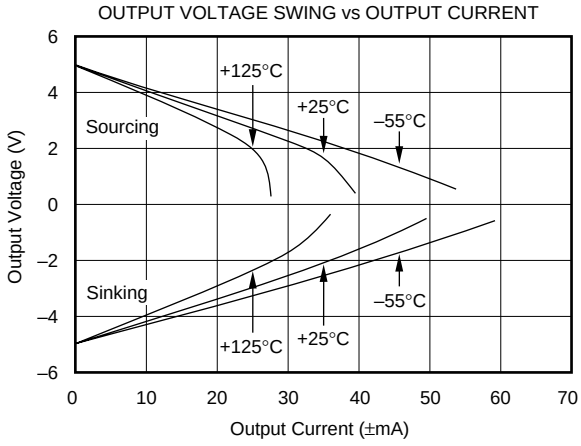
QUIESCENT CURRENT vs SUPPLY VOLTAGE



SHORT-CIRCUIT CURRENT
vs SUPPLY VOLTAGE



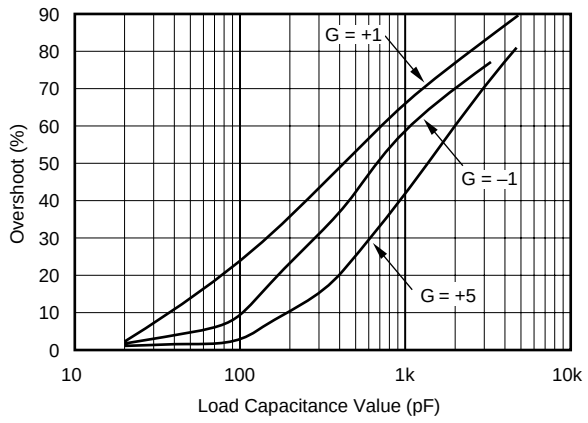
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



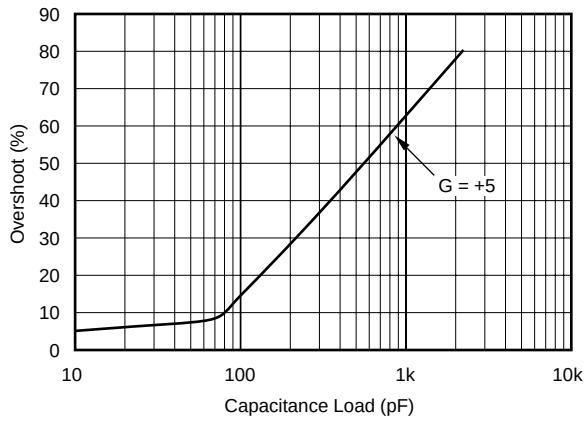
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = ±5V, and R_L = 20kΩ, unless otherwise noted.

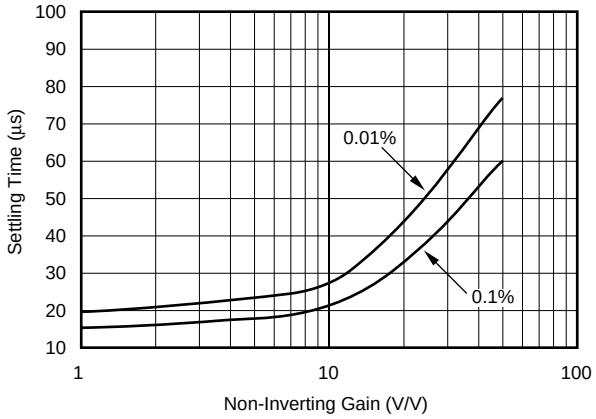
OPA703 SMALL-SIGNAL OVERSHOOT (%) vs CAPACITIVE LOAD AND GAIN



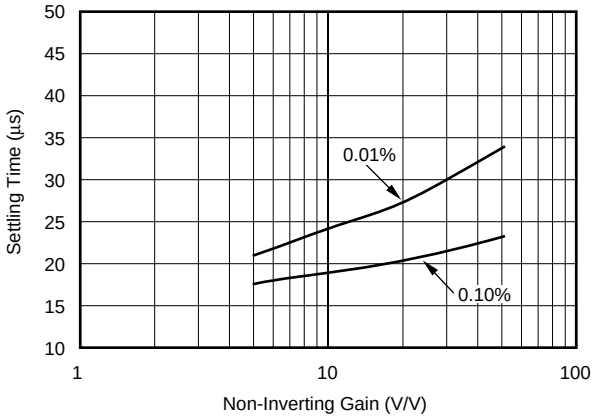
OPA704 SMALL-SIGNAL OVERSHOOT (%) vs CAPACITIVE LOAD



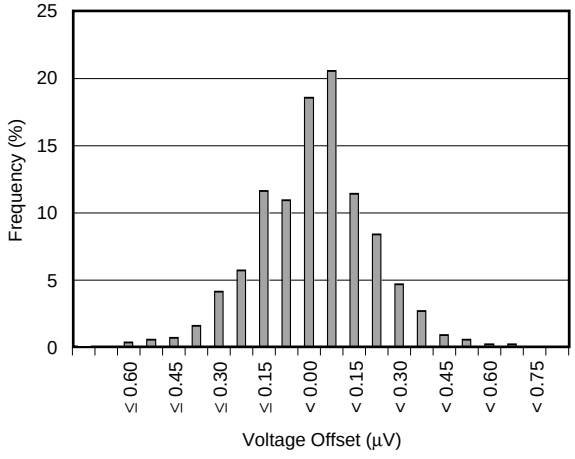
OPA703 SETTLING TIME vs GAIN



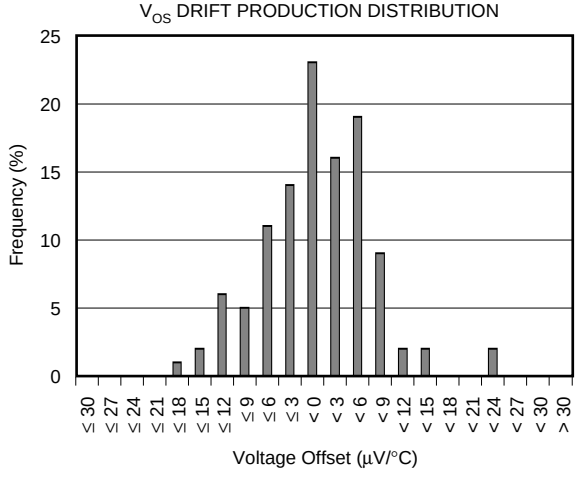
OPA704 SETTLING TIME vs GAIN



V_{OS} PRODUCTION DISTRIBUTION



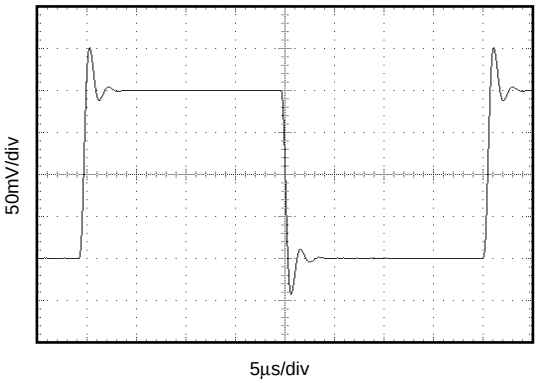
V_{OS} DRIFT PRODUCTION DISTRIBUTION



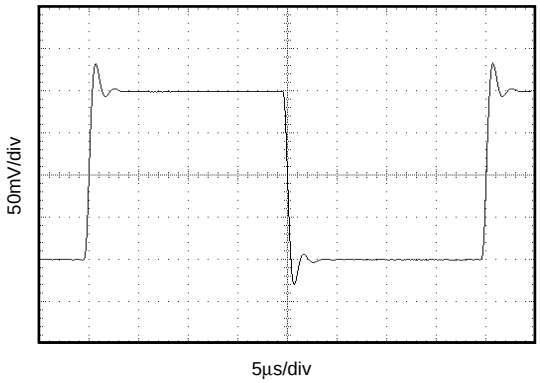
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = ±5V, and R_L = 20kΩ, unless otherwise noted.

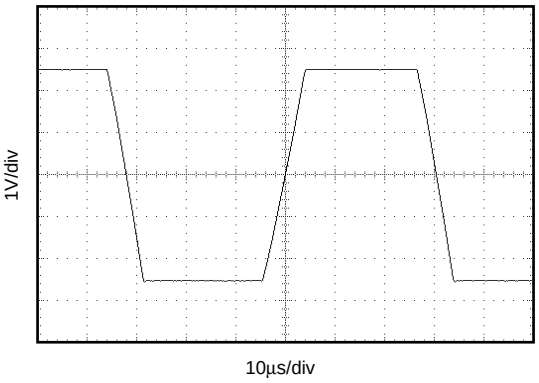
OPA703 SMALL SIGNAL STEP RESPONSE
(G = +1V/V, R_L = 20kΩ, C_L = 100pF)



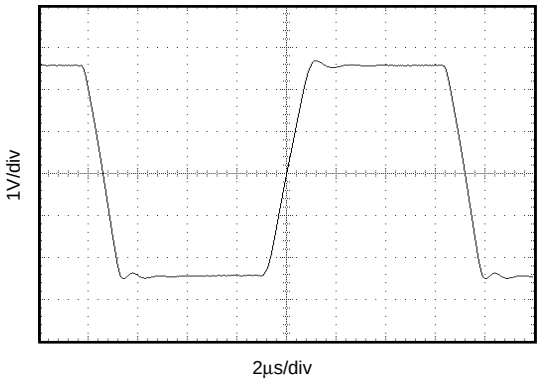
OPA704 SMALL SIGNAL STEP RESPONSE
(G = +5V/V, C_F = 3pF, R_F = 100kΩ,
C_L = 100pF, R_L = 20kΩ,)



OPA703 LARGE SIGNAL STEP RESPONSE
(G = +1V/V, R_L = 20kΩ, C_L = 100pF)



OPA704 LARGE SIGNAL STEP RESPONSE
(G = +5V/V, R_L = 20kΩ, C_F = 3pF, C_L = 100pF)



APPLICATIONS INFORMATION

OPA703 and OPA704 series op amps can operate on 160µA quiescent current from a single (or split) supply in the range of 4V to 12V (±2V to ±6V), making them highly versatile and easy to use. The OPA703 is unity-gain stable and offers 1MHz bandwidth and 0.6V/µs slew rate. The OPA704 is optimized for gains of 5 or greater with a 3MHz bandwidth and 3V/µs slew rate.

Rail-to-rail input and output swing helps maintain dynamic range, especially in low supply applications. Figure 1 shows the input and output waveforms for the OPA703 in unity-gain configuration. Operation is from a ±5V supply with a 100kΩ load connected to $V_S/2$. The input is a 10Vp-p sinusoid. Output voltage is approximately 10Vp-p.

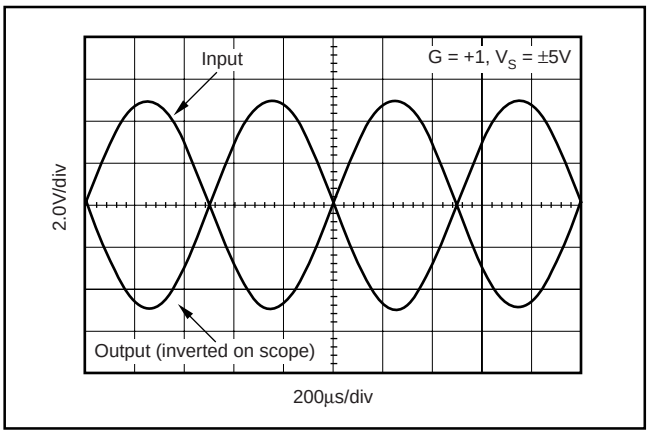


FIGURE 1. Rail-to-Rail Input and Output.

Power-supply pins should be bypassed with 1000pF ceramic capacitors in parallel with 1µF tantalum capacitors.

OPERATING VOLTAGE

OPA703 and OPA704 series op amps are fully specified and guaranteed from +4V to +12V over a temperature range of –40ºC to +85ºC. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Performance Curves.

RAIL-TO-RAIL INPUT

The input common-mode voltage range of the OPA703 series extends 300mV beyond the supply rails at room temperature. This is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair, as shown in Figure 2. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 2.0V to 300mV above the positive supply, while the P-channel pair is on for inputs from 300mV below the negative supply to approximately (V+) – 1.5V. There is a small transition region, typically (V+) – 2.0V to (V+) – 1.5V, in which both pairs are on. This 500mV transition region can vary ±100mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 2.1V to (V+) – 1.4V on the low end, up to (V+) – 1.9V to (V+) – 1.6V on the high end. Within the 500mV transition region PSRR, CMRR, offset voltage, and offset drift, and THD may vary compared to operation outside this region.

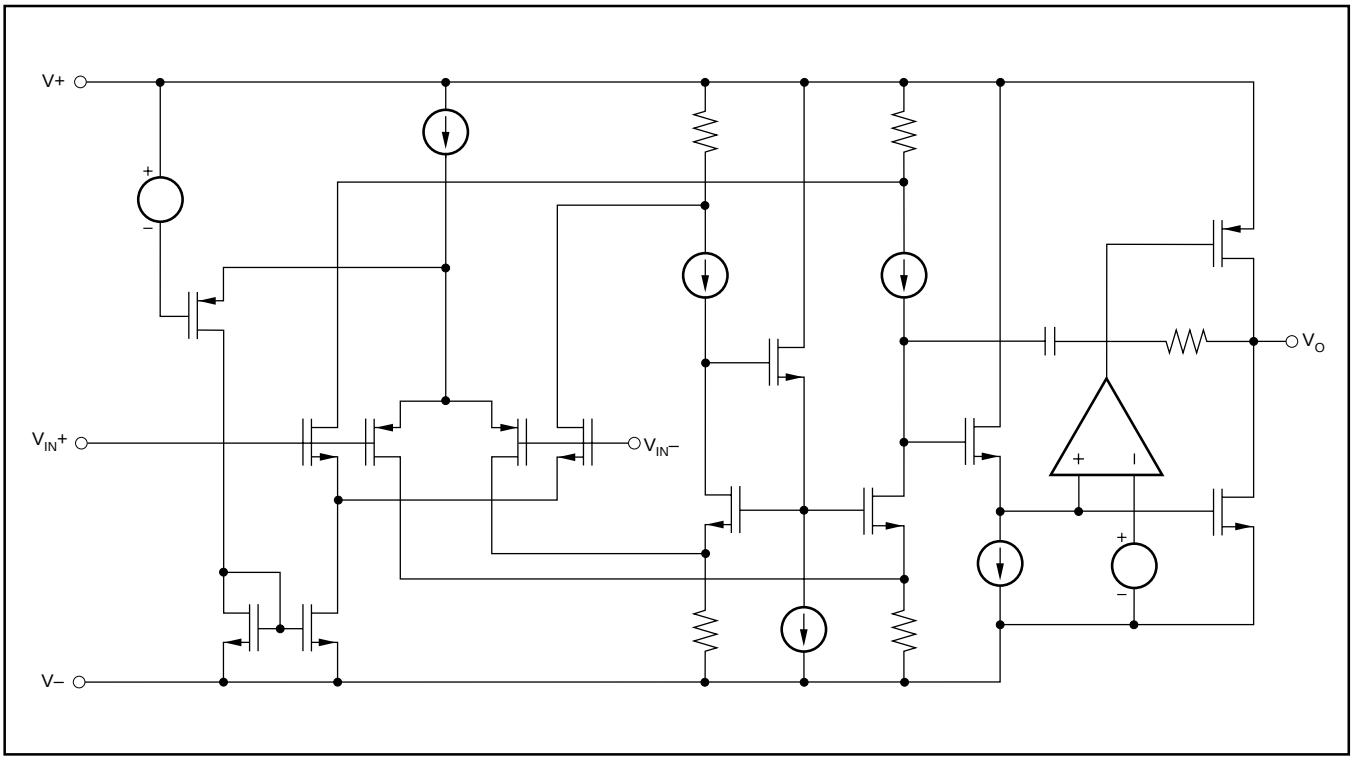


FIGURE 2. Simplified Schematic.

INPUT VOLTAGE

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than approximately 300mV. Momentary voltages greater than 300mV beyond the power supply can be tolerated if the current is limited to 10mA. This is easily accomplished with an input resistor, as shown in Figure 3. Many input signals are inherently current-limited to less than 10mA; therefore, a limiting resistor is not always required. The OPA703 features no phase inversion when the inputs extend beyond supplies if the input current is limited, as seen in Figure 4.

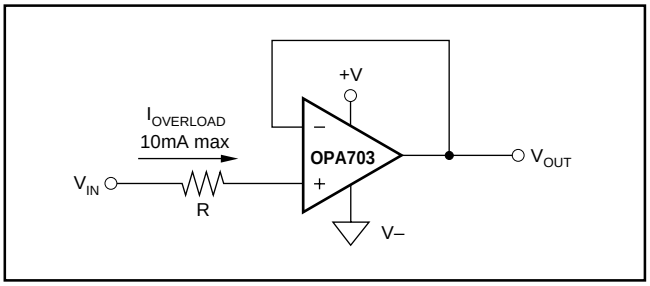


FIGURE 3. Input Current Protection for Voltages Exceeding the Supply Voltage.

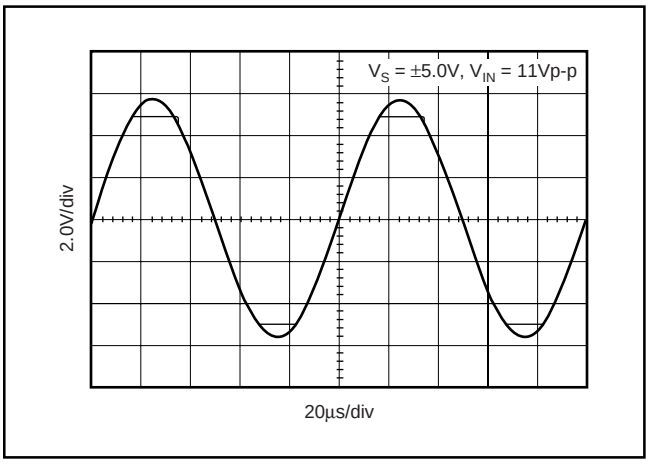


FIGURE 4. OPA703—No Phase Inversion with Inputs Greater than the Power-Supply Voltage.

RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. This output stage is capable of driving 1kΩ loads connected to any point between V+ and ground. For light resistive loads (> 100kΩ), the output voltage can swing to 40mV from the supply rail. With moderate resistive loads (20kΩ), the output can swing to within 75mV from the supply rails while maintaining high open-loop gain (see the typical performance curve "Output Voltage Swing vs Output Current").

CAPACITIVE LOAD AND STABILITY

The OPA703 and OPA704 series op amps can drive up to 1000pF pure capacitive load. Increasing the gain enhances the amplifier's ability to drive greater capacitive loads (see the typical performance curve "Small Signal Overshoot vs Capacitive Load").

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10Ω to 20Ω resistor inside the feedback loop, as shown in Figure 5. This reduces ringing with large capacitive loads while maintaining DC accuracy.

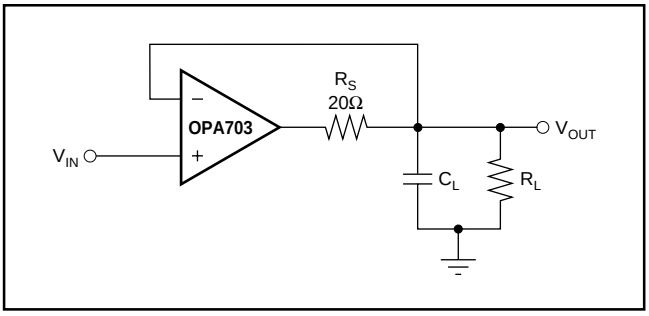


FIGURE 5. Series Resistor in Unity-Gain Buffer Configuration Improves Capacitive Load Drive.

APPLICATION CIRCUITS

Figure 6 shows a G = 5 non-inverting amplifier implemented with the OPA703 and OPA704 op amps. It demonstrates the increased speed characteristics (bandwidth, slew rate and settling time) that can be achieved with the OPA704 family when used in gains of five or greater. Some optimization of feedback capacitor value may be required to achieve best dynamic response. Circuits with closed-loop gains of less than five should use the OPA703 family for good stability and capacitive load drive. The OPA703 can be used in gains greater than five, but will not provide the increased speed benefits of the OPA704 family.

The OPA703 series op amps are optimized for driving medium-speed sampling data converters. The OPA703 op amps buffer the converter's input capacitance and resulting charge injection while providing signal gain.

Figure 7 shows the OPA2703 in a dual-supply buffered reference configuration for the DAC7644. The DAC7644 is a 16-bit, low-power, quad-voltage output converter. Small size makes the combination ideal for automatic test equipment, data acquisition systems, and other low-power space-limited applications.

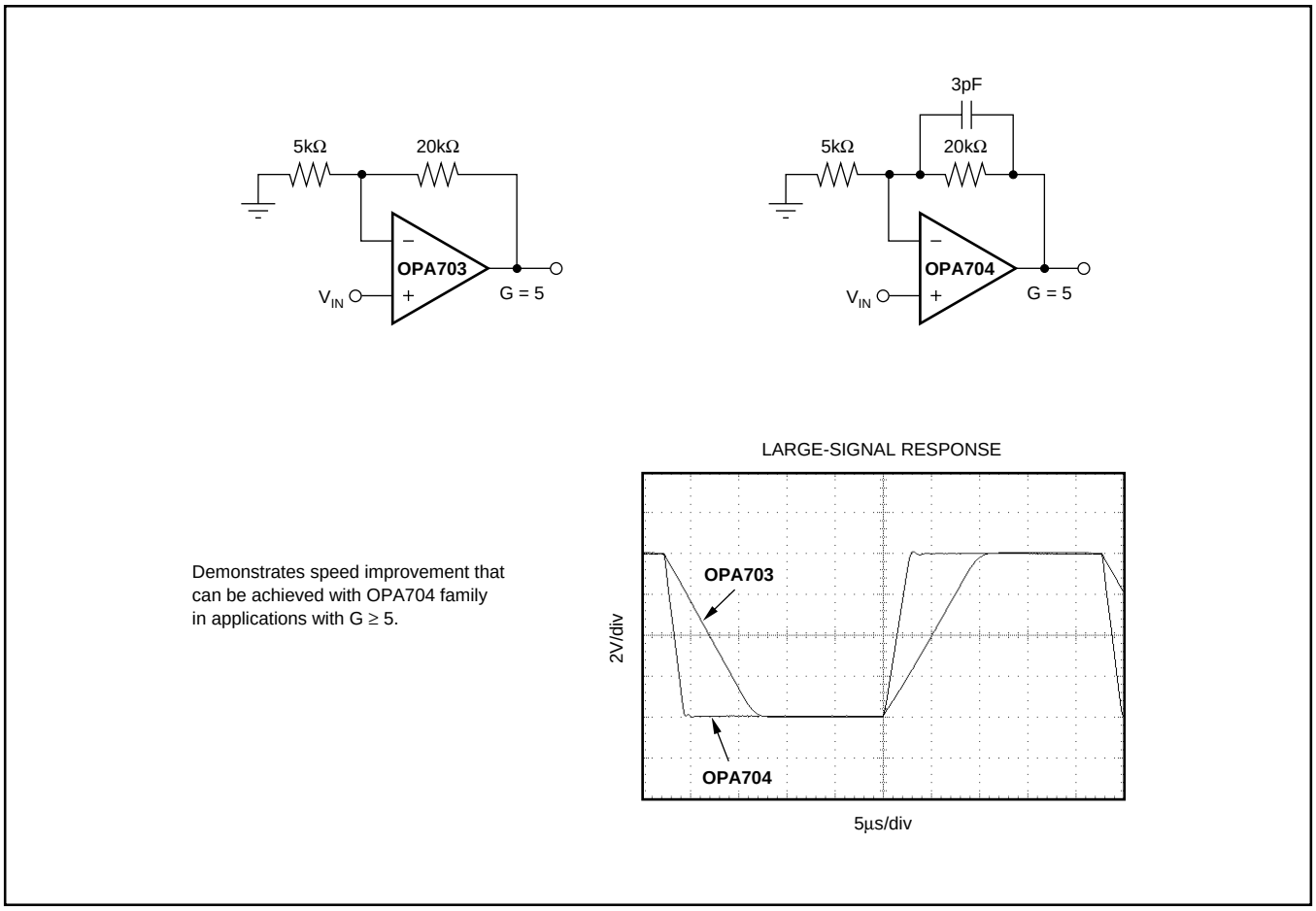


FIGURE 6. OPA704 Provides higher Speed in G ≥ 5.

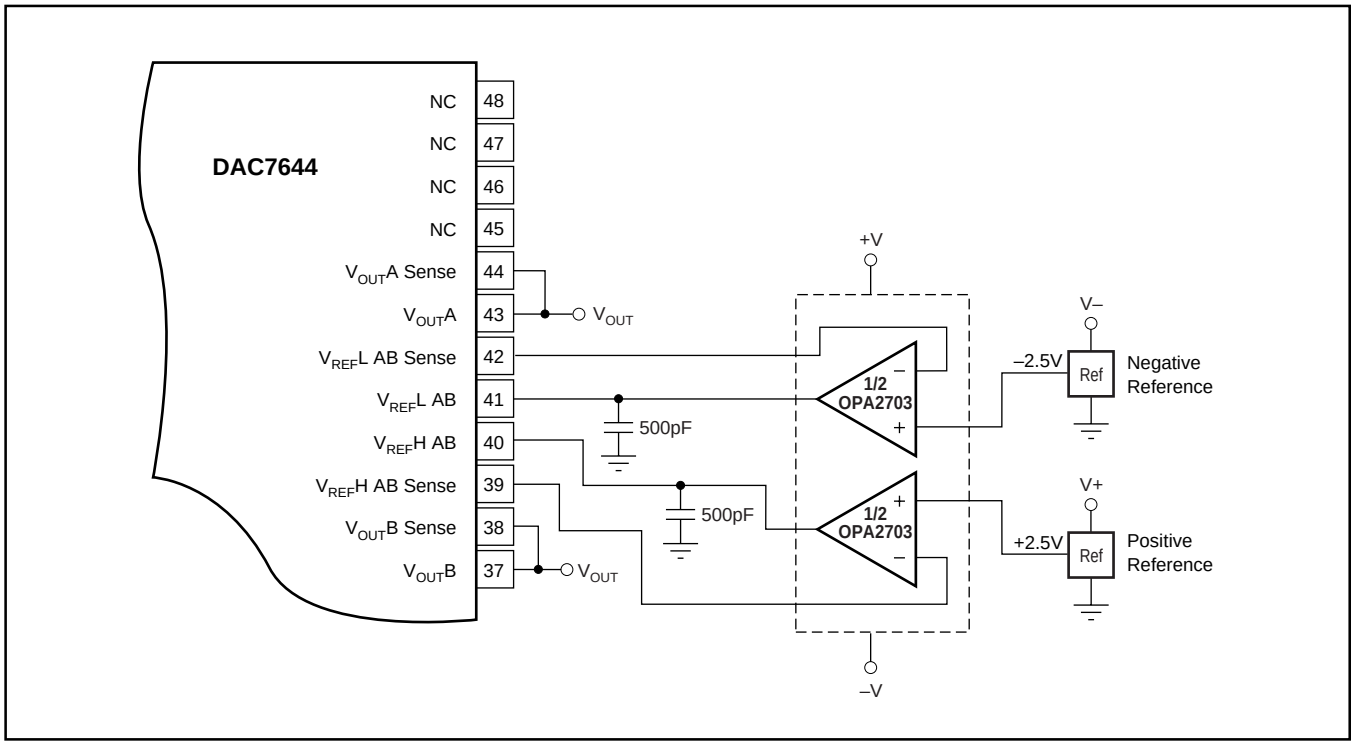


FIGURE 7. OPA703 as Dual Supply Configuration-Buffered References for the DAC7644.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2703EA/250	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI | Nipdauag	Level-2-260C-1 YEAR	-40 to 85	B03
OPA2703EA/250.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	B03
OPA2703EA/2K5	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdauag	Level-2-260C-1 YEAR	-40 to 85	B03
OPA2703EA/2K5.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	B03
OPA2703UA	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2703UA
OPA2703UA.B	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2703UA
OPA2703UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2703UA
OPA2703UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2703UA
OPA2703UA/2K5G4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2703UA
OPA2703UAG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2703UA
OPA2703UAG4.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2703UA
OPA2704EA/250	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI | Nipdauag	Level-2-260C-1 YEAR	-40 to 85	B04
OPA2704EA/250.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	B04
OPA2704UA	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2704UA
OPA2704UA.B	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2704UA
OPA2704UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2704UA
OPA2704UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2704UA
OPA4703EA/250	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4703EA
OPA4703EA/250.B	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4703EA

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA4703EA/250G4	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4703EA
OPA4703EA/250G4.B	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4703EA
OPA4703EA/2K5	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4703EA
OPA4703EA/2K5.B	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4703EA
OPA4703EA/2K5G4	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4703EA
OPA4703UA	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4703UA
OPA4703UA.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4703UA
OPA4704EA/250	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4704EA
OPA4704EA/250.B	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4704EA
OPA4704EA/250G4	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4704EA
OPA4704EA/250G4.B	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4704EA
OPA4704EA/2K5	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4704EA
OPA4704EA/2K5.B	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4704EA
OPA4704UA	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4704UA
OPA4704UA.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4704UA
OPA703NA/250	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A03
OPA703NA/250.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A03
OPA703NA/250G4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A03
OPA703NA/3K	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A03
OPA703NA/3K.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A03
OPA703NA/3KG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A03
OPA703PA	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA703PA
OPA703PA.B	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA703PA

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA703UA	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 703UA
OPA703UA.B	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 703UA
OPA703UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 703UA
OPA703UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 703UA
OPA704NA/250	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A04
OPA704NA/250.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A04
OPA704NA/250G4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A04
OPA704NA/3K	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A04
OPA704NA/3K.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A04
OPA704NA/3KG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A04
OPA704UA	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 704UA
OPA704UA.B	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 704UA
OPA704UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 704UA
OPA704UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 704UA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

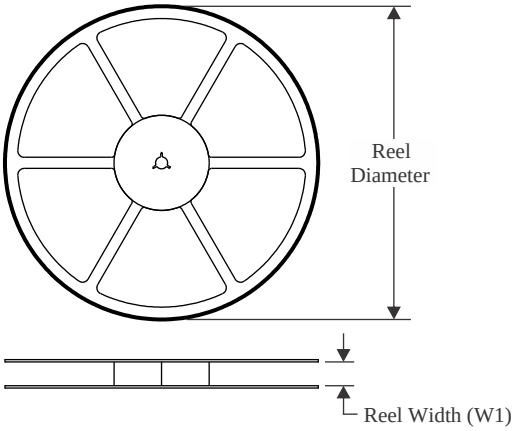
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

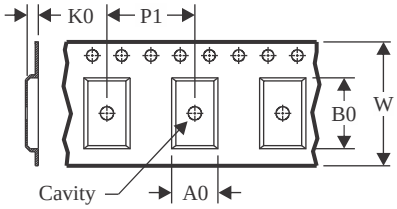
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

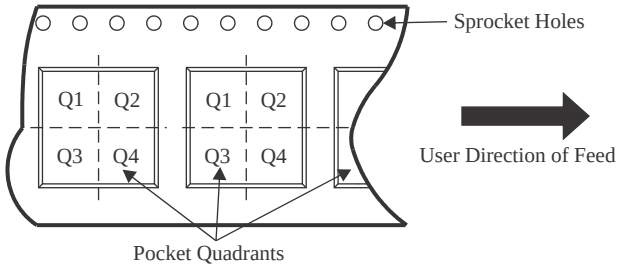


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

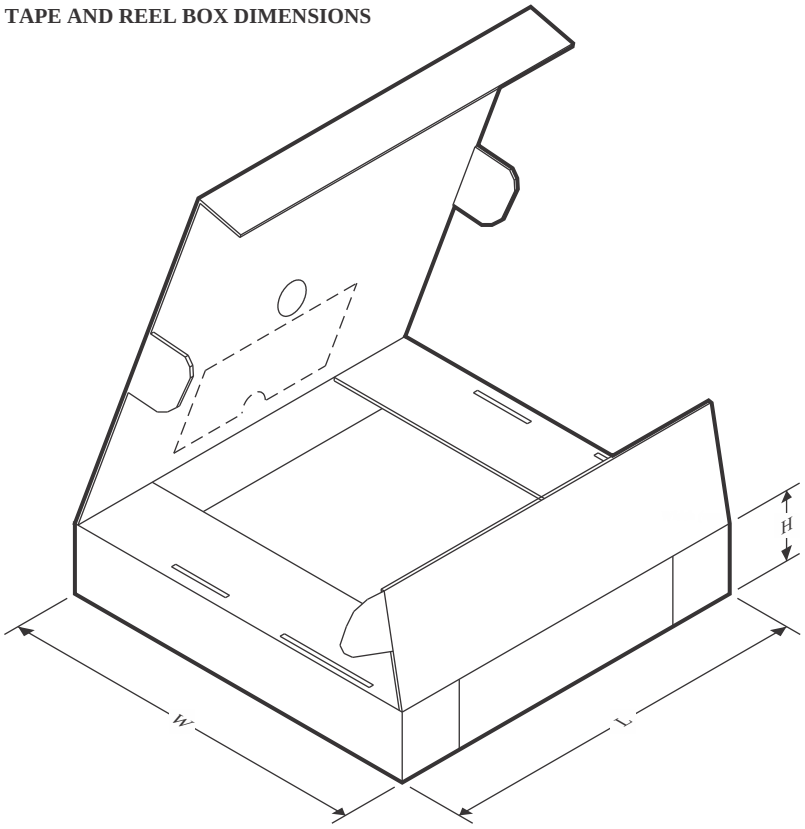


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2703EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2703EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2703UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2704EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2704UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4703EA/250	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4703EA/250G4	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4703EA/2K5	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4704EA/250	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4704EA/250G4	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4704EA/2K5	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA703NA/250	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA703NA/3K	SOT-23	DBV	5	3000	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA703UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA704NA/250	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA704NA/3K	SOT-23	DBV	5	3000	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA704UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

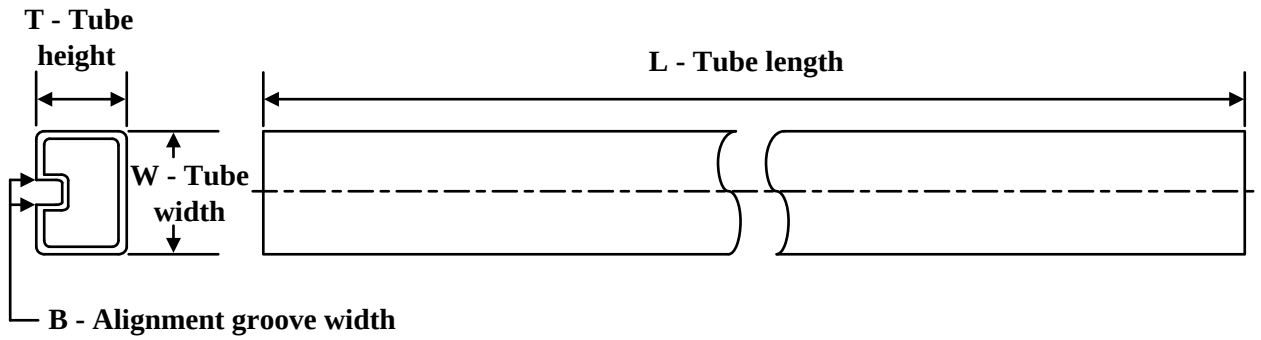
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

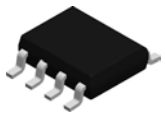
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2703EA/250	VSSOP	DGK	8	250	213.0	191.0	35.0
OPA2703EA/2K5	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2703UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA2704EA/250	VSSOP	DGK	8	250	213.0	191.0	35.0
OPA2704UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA4703EA/250	TSSOP	PW	14	250	213.0	191.0	35.0
OPA4703EA/250G4	TSSOP	PW	14	250	213.0	191.0	35.0
OPA4703EA/2K5	TSSOP	PW	14	2500	353.0	353.0	32.0
OPA4704EA/250	TSSOP	PW	14	250	213.0	191.0	35.0
OPA4704EA/250G4	TSSOP	PW	14	250	213.0	191.0	35.0
OPA4704EA/2K5	TSSOP	PW	14	2500	353.0	353.0	32.0
OPA703NA/250	SOT-23	DBV	5	250	565.0	140.0	75.0
OPA703NA/3K	SOT-23	DBV	5	3000	565.0	140.0	75.0
OPA703UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA704NA/250	SOT-23	DBV	5	250	565.0	140.0	75.0
OPA704NA/3K	SOT-23	DBV	5	3000	565.0	140.0	75.0
OPA704UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2703UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2703UA.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2703UAG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA2703UAG4.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2704UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2704UA.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA4703UA	D	SOIC	14	50	506.6	8	3940	4.32
OPA4703UA.B	D	SOIC	14	50	506.6	8	3940	4.32
OPA4704UA	D	SOIC	14	50	506.6	8	3940	4.32
OPA4704UA.B	D	SOIC	14	50	506.6	8	3940	4.32
OPA703PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA703PA.B	P	PDIP	8	50	506	13.97	11230	4.32
OPA703UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA703UA.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA704UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA704UA.B	D	SOIC	8	75	506.6	8	3940	4.32

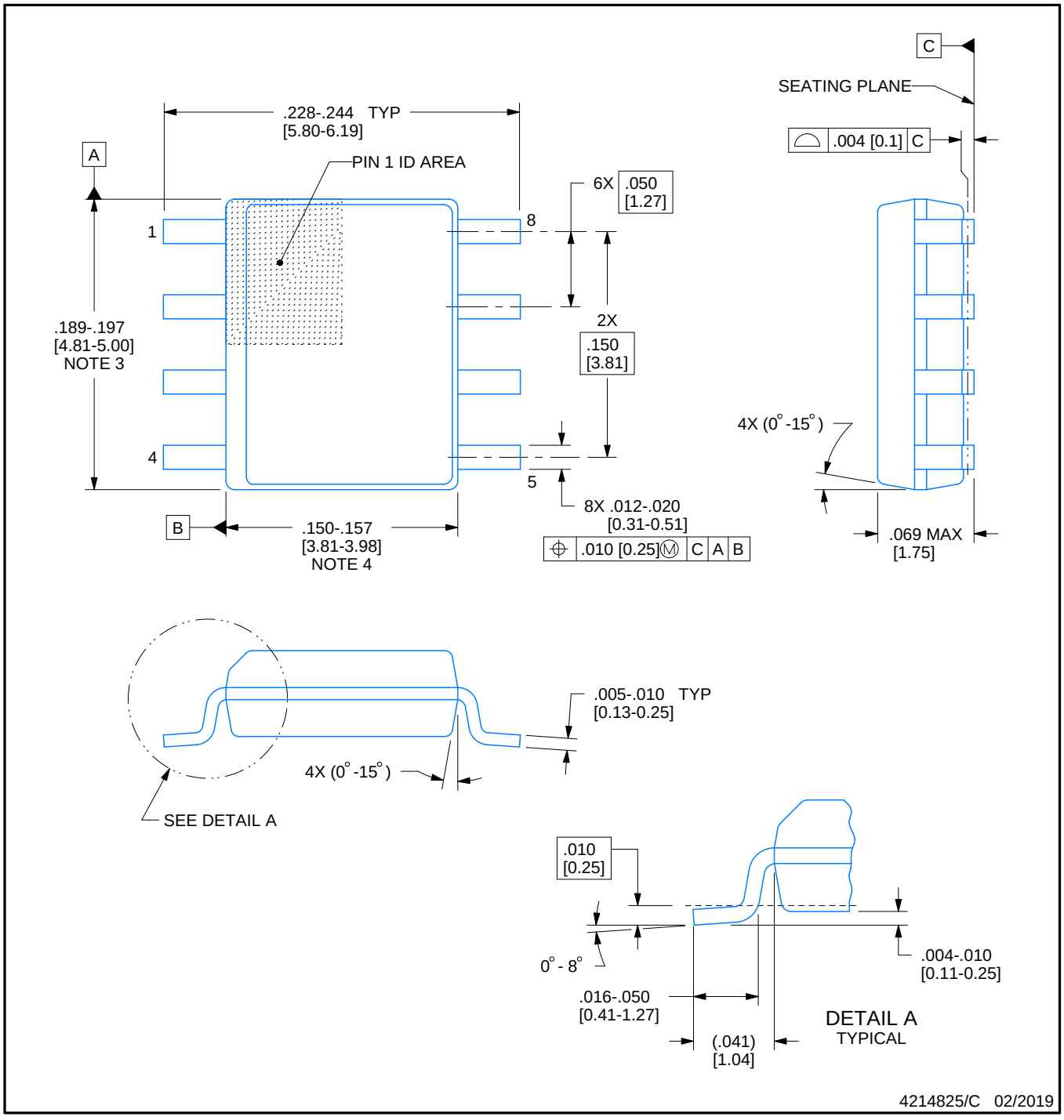


PACKAGE OUTLINE

D0008A

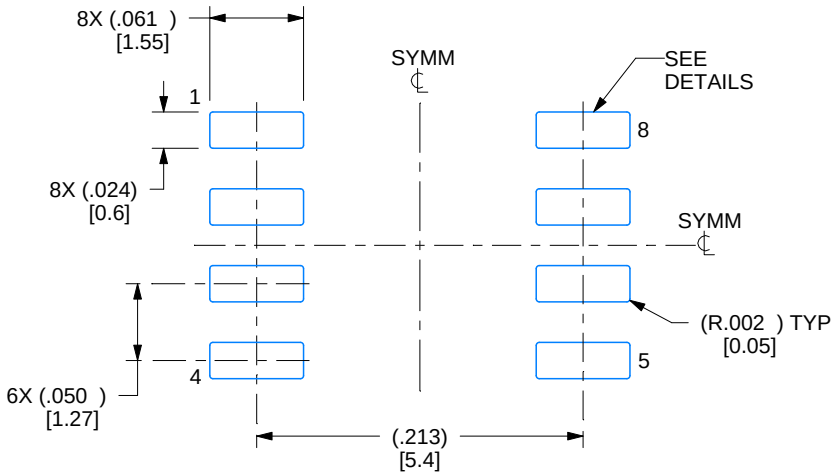
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

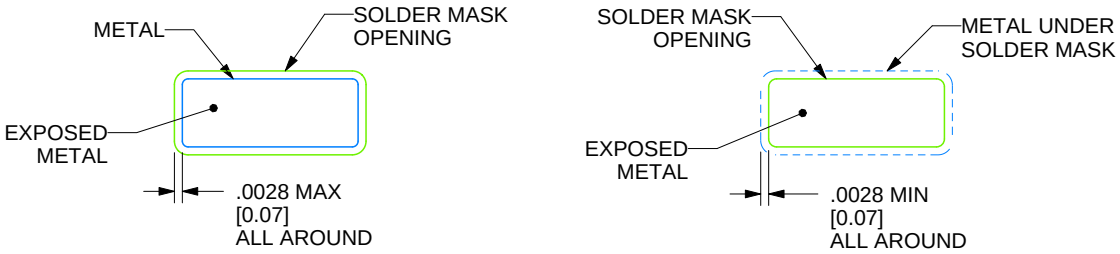


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

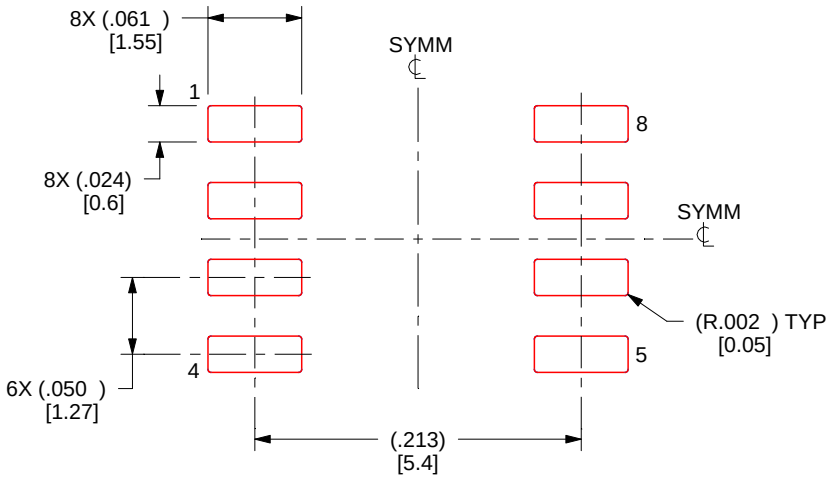
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



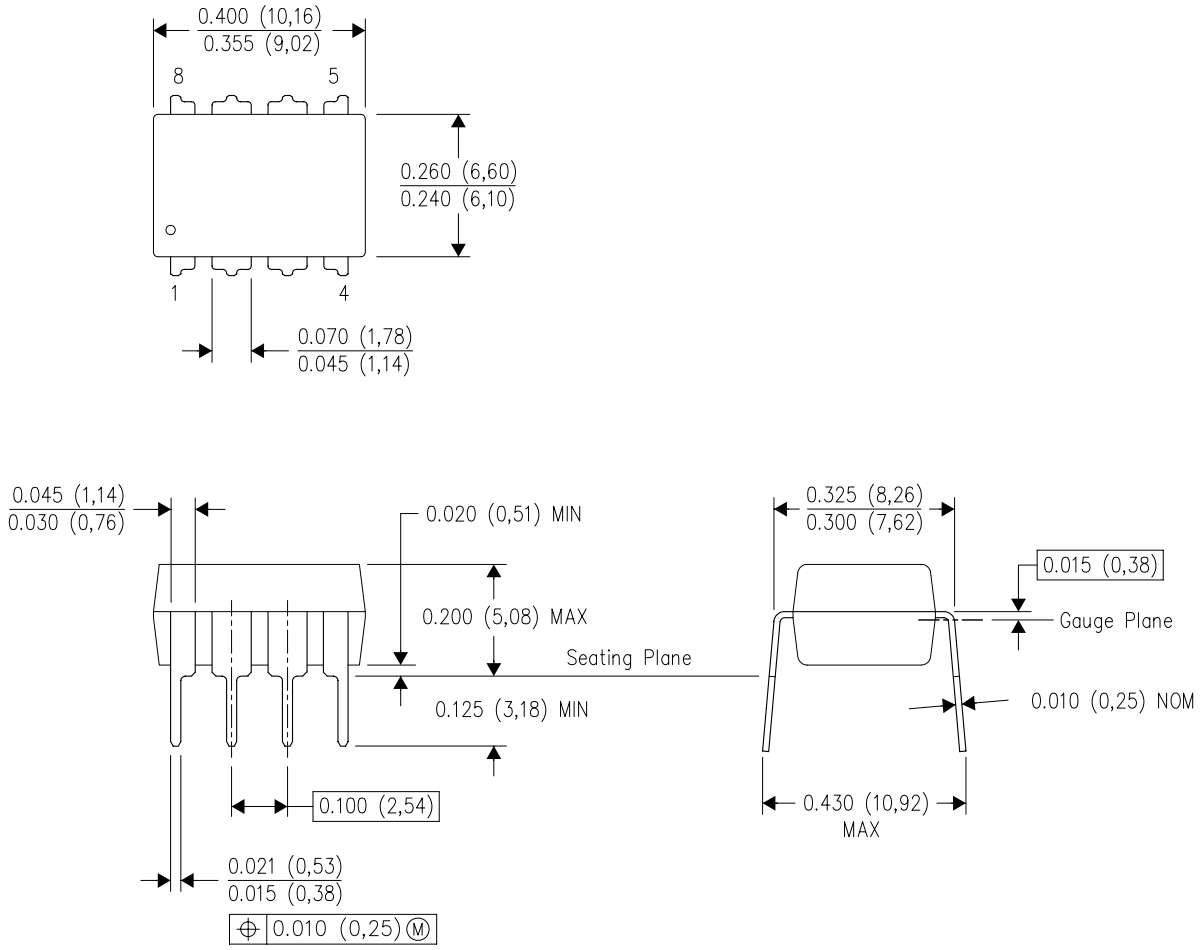
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



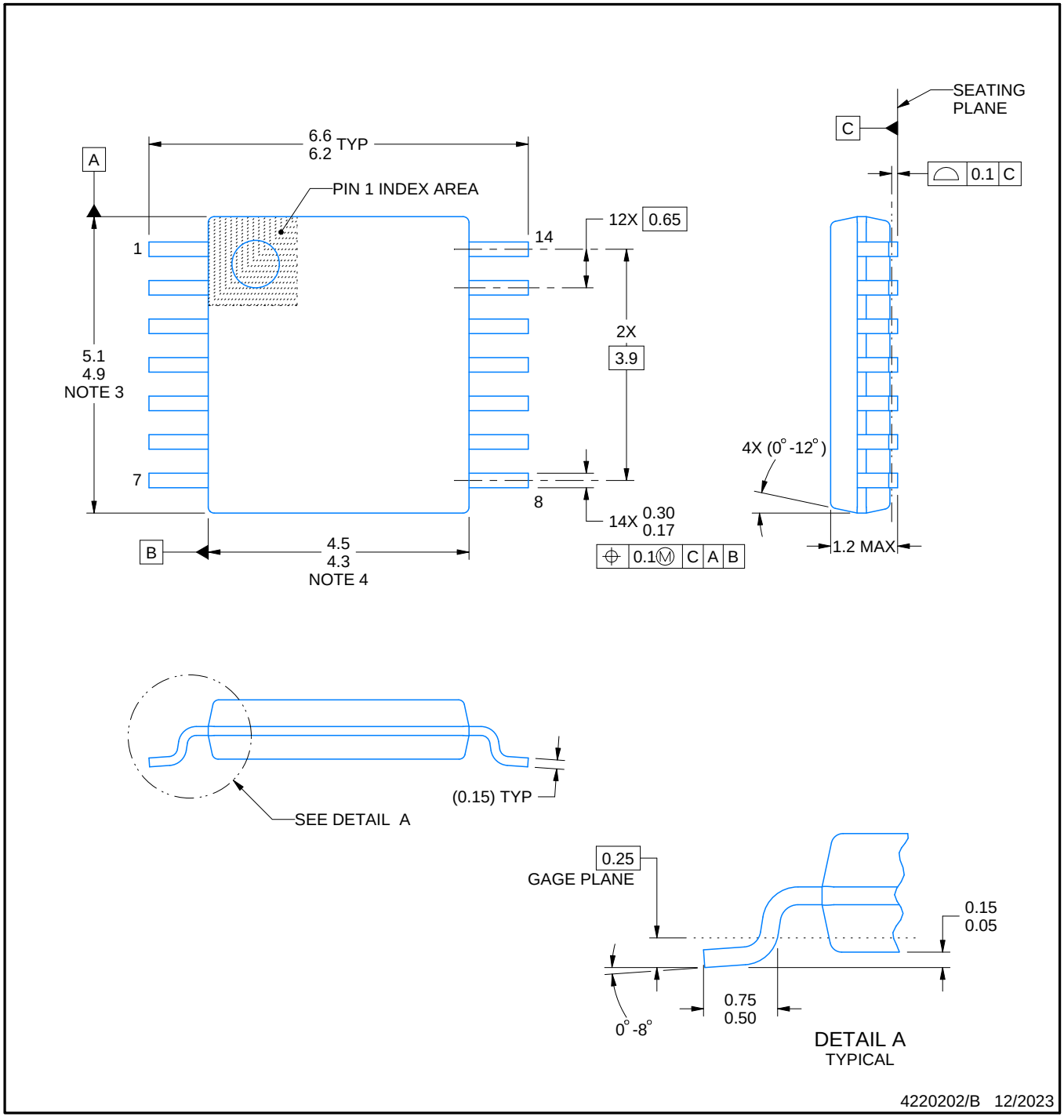
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

PW0014A

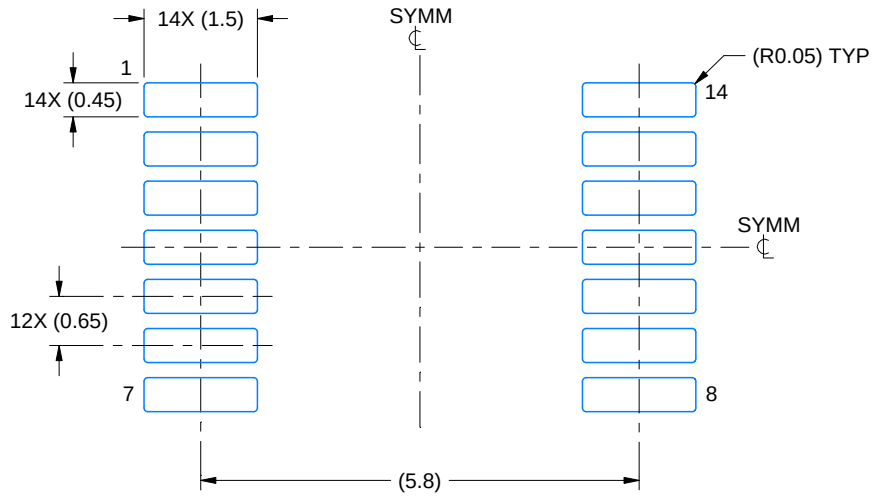
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

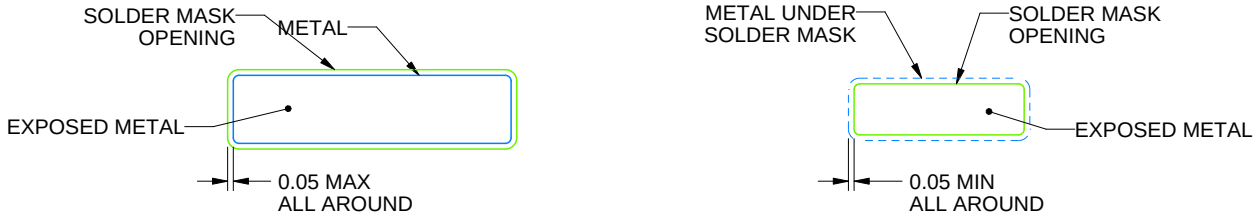


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

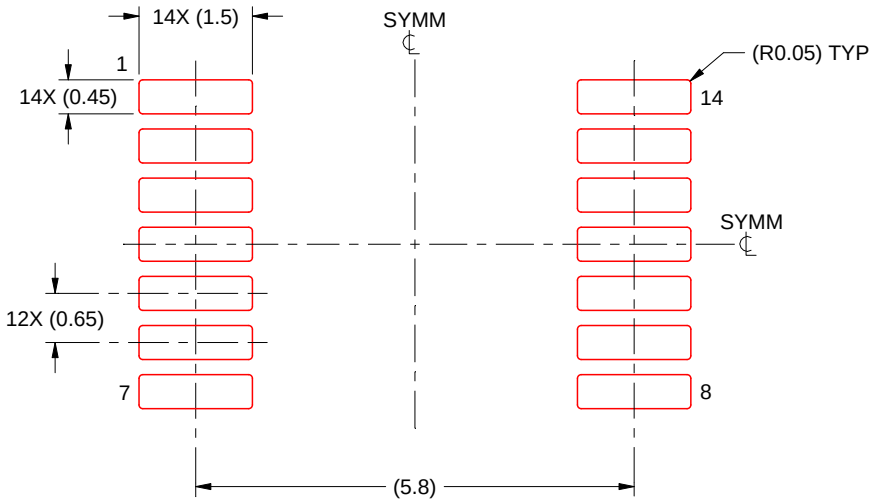


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

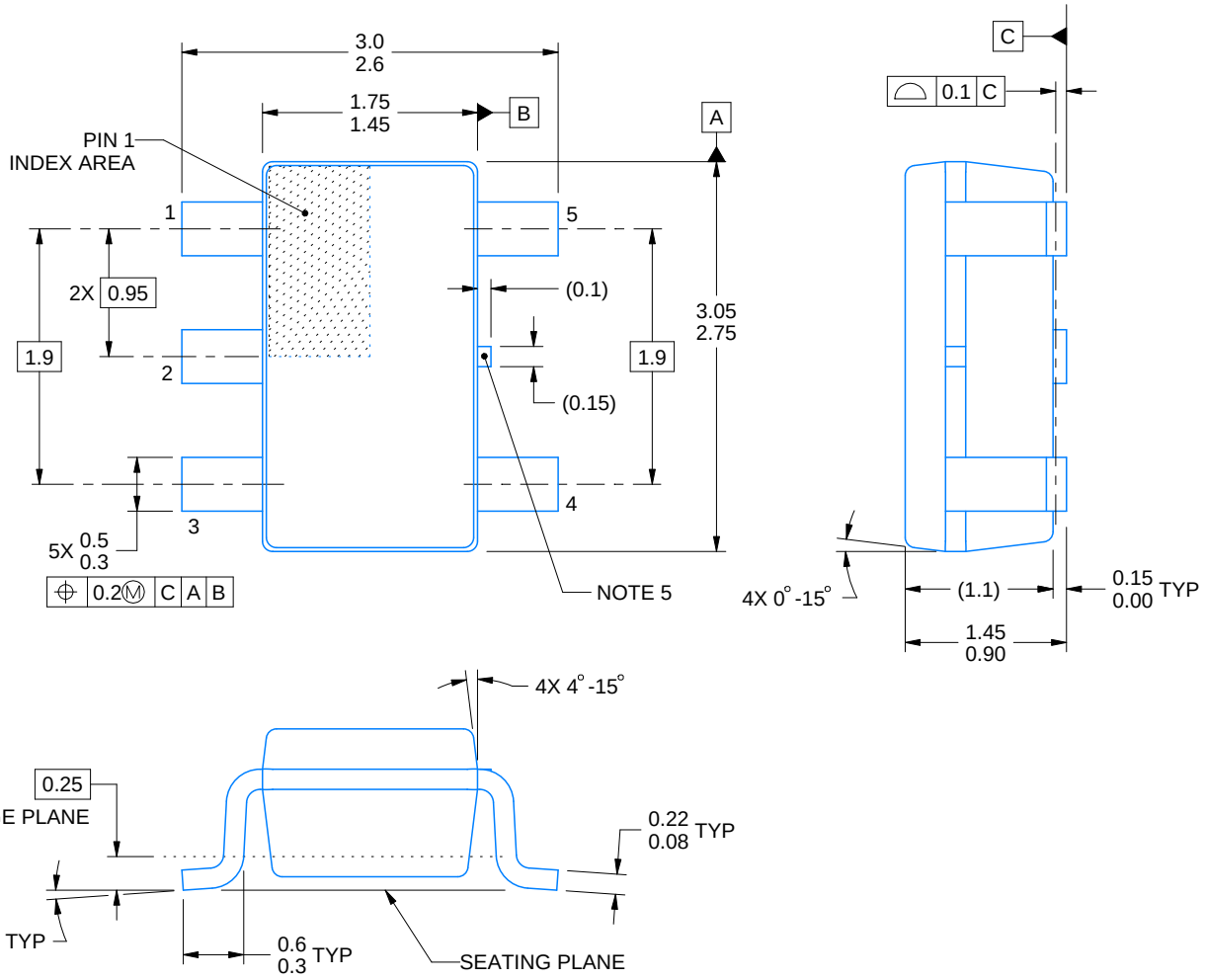
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

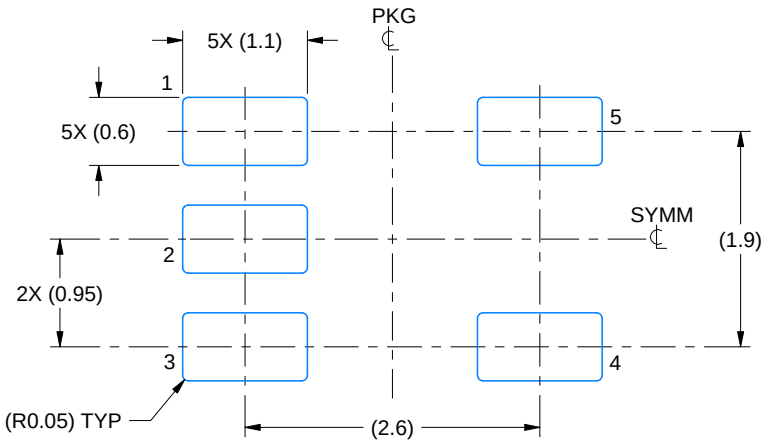
SMALL OUTLINE TRANSISTOR



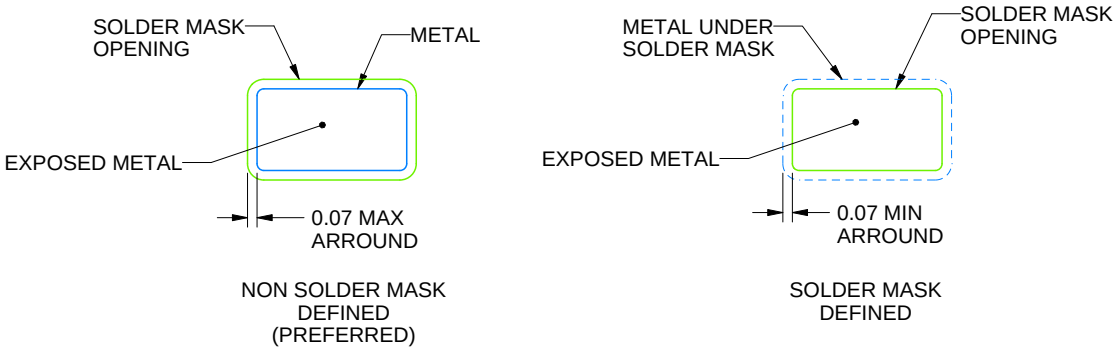
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

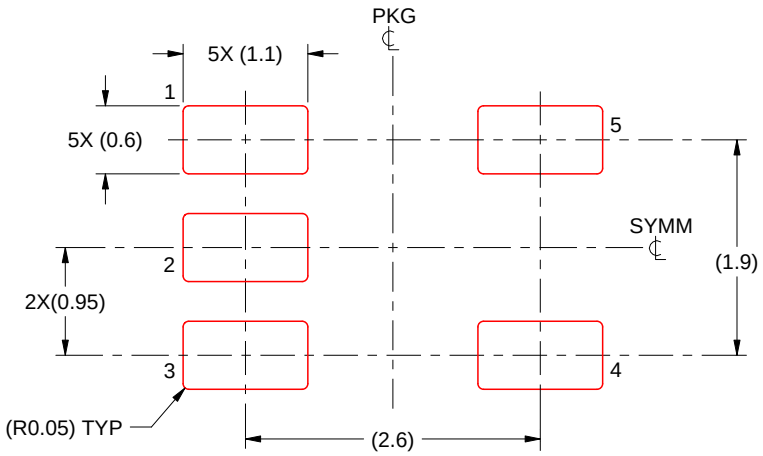


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

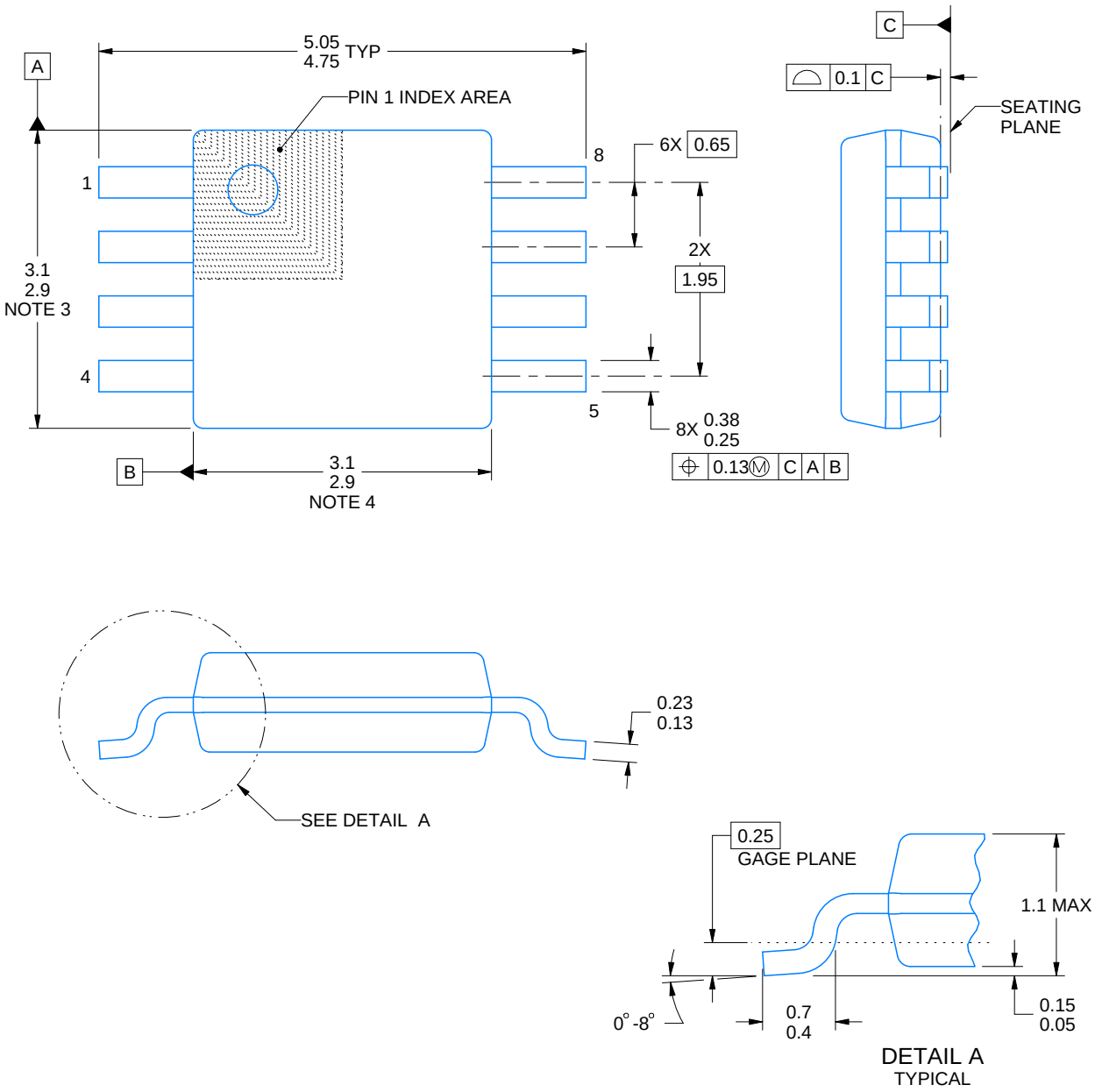
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

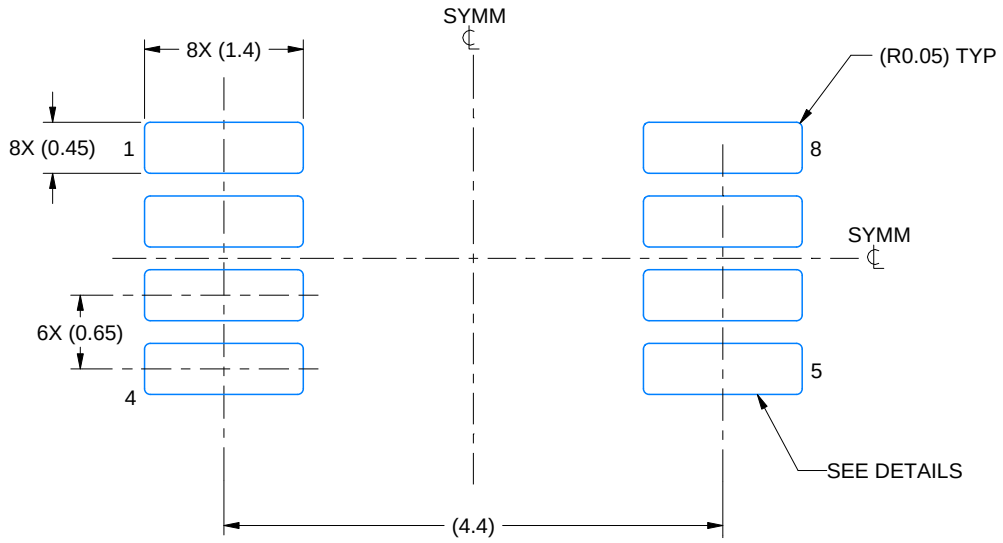
SMALL OUTLINE PACKAGE



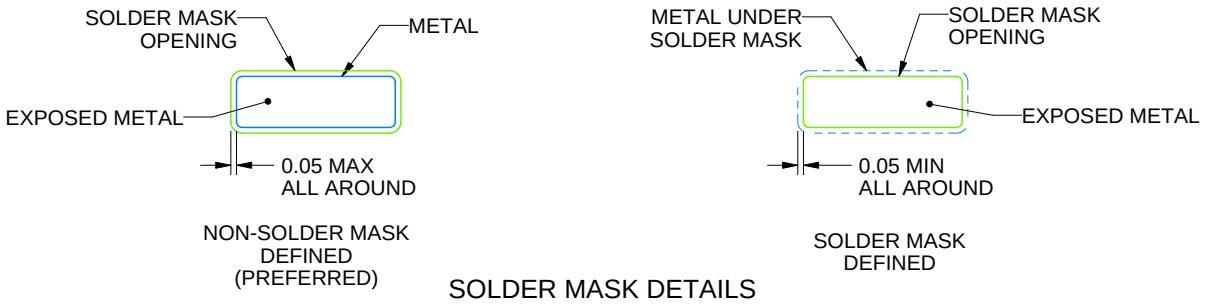
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

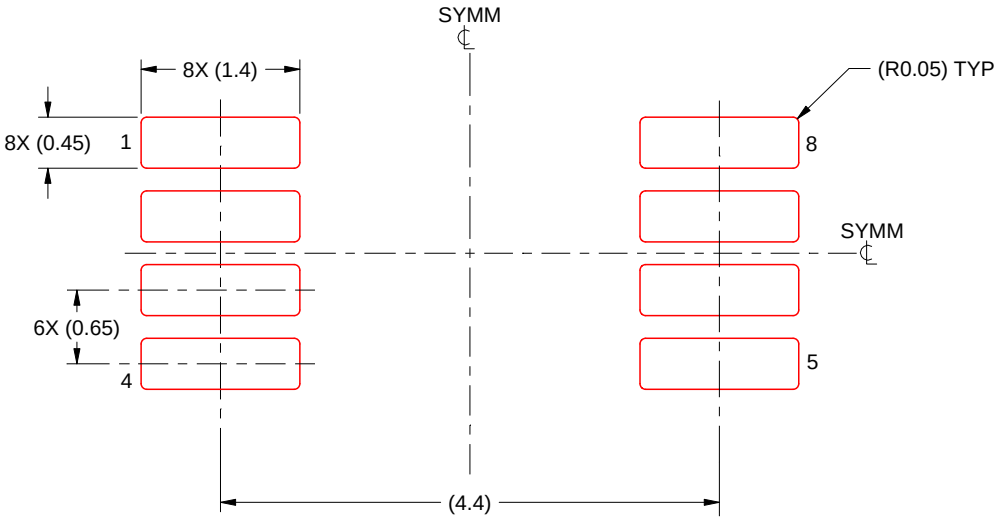


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

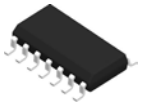


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

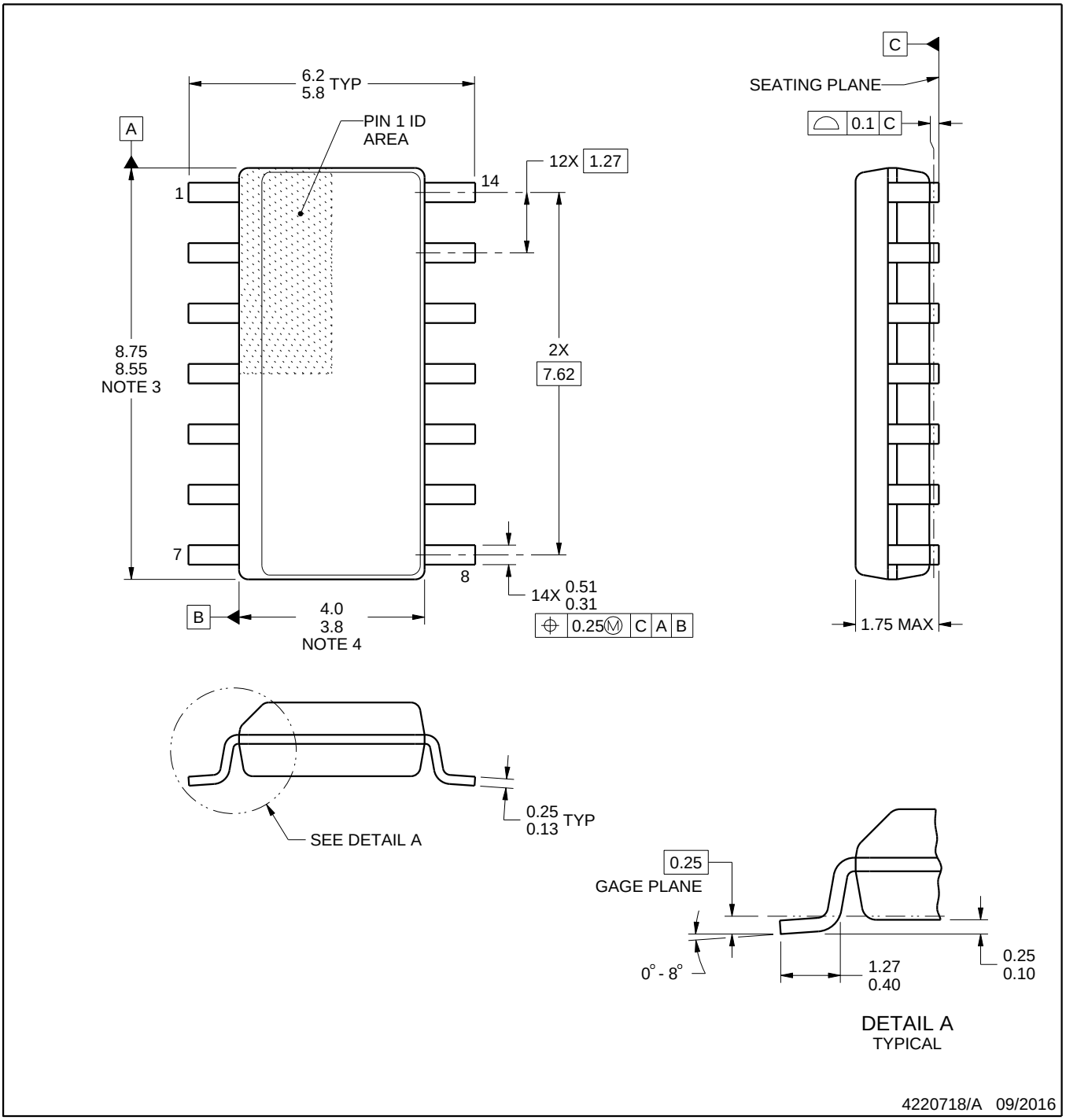


PACKAGE OUTLINE

D0014A

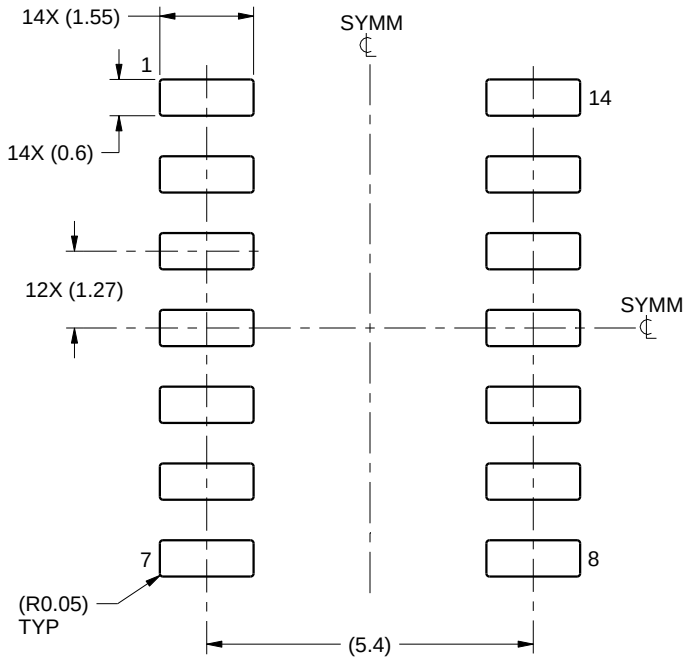
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

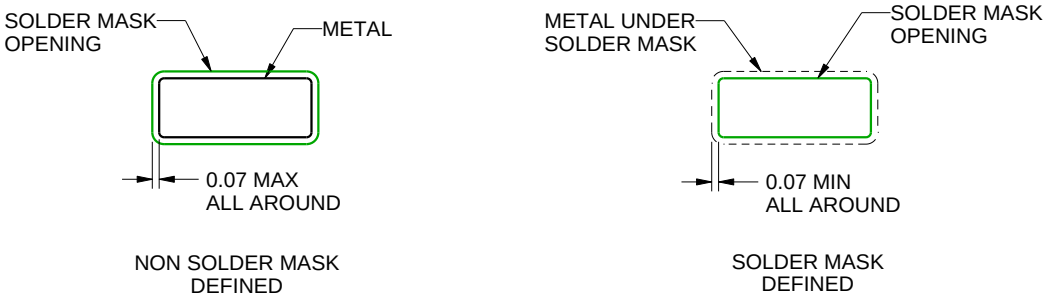


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

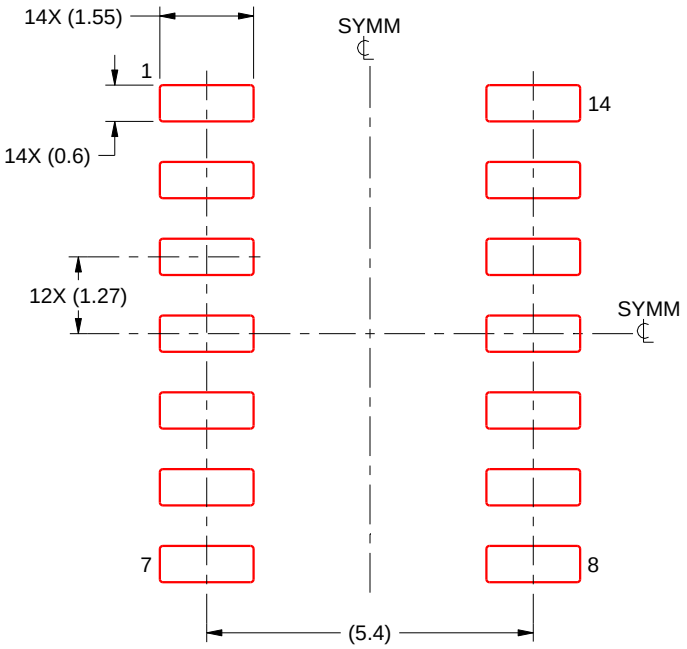
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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