OPAx991-EP 40V, Rail-to-Rail Input/Output, Low Offset Voltage, Low Noise Op Amps in Enhanced Plastic

1 Features

- Enhanced plastic
  - Single controlled baseline
  - One fabrication, assembly and test site
  - Gold wire
  - NiPdAu lead finish
  - Available in military (–55°C to 125°C) temperature range
  - Extended product life cycle
  - Extended product-change notification
  - Product traceability
  - Enhanced mold compound for low outgassing
- Low offset voltage: ±125µV
- Low noise: 10.8nV/√Hz at 1kHz
- High common-mode rejection: 130dB
- Low bias current: ±10pA
- Rail-to-rail input and output
- Wide bandwidth: 4.5MHz GBW
- High peak slew rate: 21V/µs
- High capacitive load drive: 1nF
- MUX-friendly inputs
- Low quiescent current: 560µA per amplifier
- Wide supply: ±1.35V to ±20V, 2.7V to 40V
- Robust EMIRR performance: EMI/RFI filters on input and supply pins

2 Applications

- Land mobile radio
- Sonar
- Low-power audio preamplifier
- Multiplexed data-acquisition systems
- Test and measurement equipment
- ADC driver amplifiers
- SAR ADC reference buffers
- Programmable logic controllers
- High-side and low-side current sensing

3 Description

The OPAx991-EP are high voltage (40V) general purpose operational amplifiers available in enhanced plastic packaging. The devices offer exceptional DC precision and AC performance, including rail-to-rail input/output, low offset (±125µV, typ), low offset drift (±0.3µV/°C, typ), low noise (10.8nV/√Hz and 1.8µV_{PP}), and 4.5MHz bandwidth.

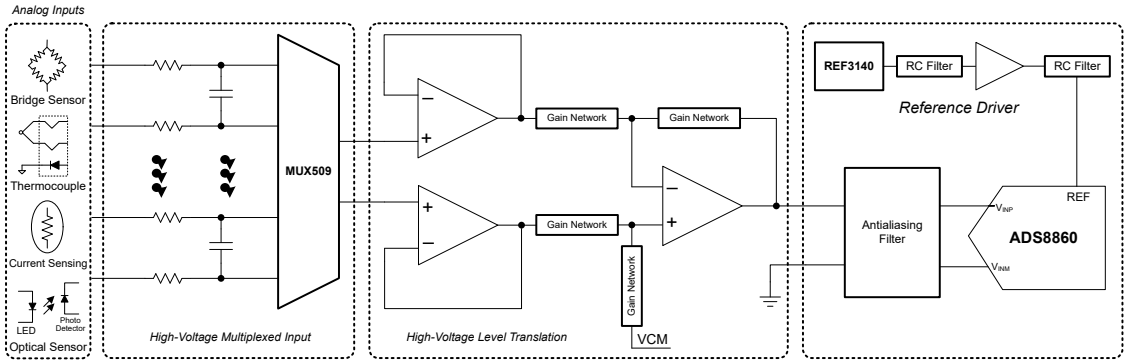
Unique features such as differential and common-mode input-voltage range to the supply rail, high output current (±75mA), high peak slew rate (21V/µs), and high capacitive load drive (1nF) make the OPAx991-EP a robust, high-performance operational amplifier for high-voltage applications.

The OPA4991-EP is available in a 14-pin SOT-23 (DYY) package, and the OPA991-EP is available in a 5-pin SOT-23 (DBV) package, with both specified from –55°C to 125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
OPA991-EP(3)	DBV (SOT-23, 5)	2.90mm × 2.80mm
OPA4991-EP	DYY (SOT-23, 14)	4.20mm × 1.90mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Package is preview only.



OPAx991-EP in a High-Voltage Signal Chain

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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4 Pin Configuration and Functions

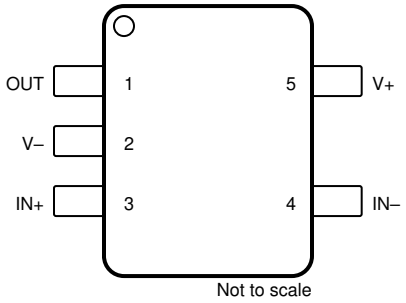


Figure 4-1. OPA991-EP DBV Package
5-Pin SOT-23
(Top View)

Table 4-1. Pin Functions: OPA991-EP

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+	3	I	Noninverting input
IN-	4	I	Inverting input
OUT	1	O	Output
V+	5	—	Positive (highest) power supply
V–	2	—	Negative (lowest) power supply

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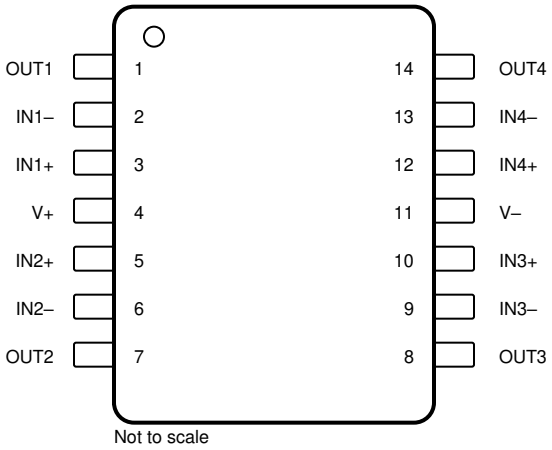


Figure 4-2. OPA4991-EP DYY Package
14-Pin SOT-23
(Top View)

Table 4-2. Pin Functions: OPA4991-EP

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1–	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2–	6	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3–	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4–	13	I	Inverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V+	4	—	Positive (highest) power supply
V–	11	—	Negative (lowest) power supply

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5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	42	V
Signal input pins	Common-mode voltage(3)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage, V_{ID} = | (V_{IN+}) – ($V_{IN–}$) |(3)		V_S + 0.2	V
	Current(3)	–10	10	mA
Output short-circuit(2)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings,* the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package. This device has been designed to limit *electrical* damage due to excessive output current, but extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual *thermal* destruction. See the *Thermal Protection* section for more information.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	OPA4991-EP	±2000	V
			OPA991-EP	±1000	
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)		±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	2.7	40	V
V_I	Input voltage range	(V–) – 0.1	(V+) + 0.1	V
T_A	Specified ambient temperature	–55	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		OPA4991-EP	OPA991-EP	UNIT
		DYY (SOT-23)	DBV (SOT-23)	
		14 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	121.6	187.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.6	86.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.8	54.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.1	27.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.6	54.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the*Semiconductor and IC Package Thermal Metrics* application report.

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5.5 Electrical Characteristics

For V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = V–			±125	±895	µV
			T_A = –55°C to 125°C			±925	
dV_{OS}/dT	Input offset voltage drift	T_A = –55°C to 125°C			±0.3		µV/°C
PSRR	Input offset voltage versus power supply	V_{CM} = V–, T_A = –55°C to 125°C	V_S = 4V to 40V		±0.3	±1	µV/V
			V_S = 2.7V to 40V[2]		±1	±5	
	Channel separation	f = 0Hz			5		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±10		pA
I_{OS}	Input offset current				±10		pA
NOISE							
E_N	Input voltage noise	f = 0.1Hz to 10Hz			1.8		μV_{PP}
					0.3		μV_{RMS}
e_N	Input voltage noise density	f = 1kHz			10.8		nV/√Hz
		f = 10kHz			9.4		
i_N	Input current noise	f = 1kHz			82		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1V < V_{CM} < (V+) – 2V (Main input pair), T_A = –55°C to 125°C	V_S = 40V	107	130		dB
			V_S = 4V	82	100		
			V_S = 2.7V[2]	75	95		
		V_S = 2.7V to 40V, (V+) – 1V < V_{CM} < (V+) + 0.1V (Aux input pair), T_A = –55°C to 125°C			85		
INPUT CAPACITANCE							
Z_{ID}	Differential				100 || 9		MΩ || pF
Z_{ICM}	Common-mode				6 || 1		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 40V, V_{CM} = V–, (V–) + 0.1V < V_O < (V+) – 0.1V		120	145		dB
			T_A = –55°C to 125°C		142		
		V_S = 4V, V_{CM} = V–, (V–) + 0.1V < V_O < (V+) – 0.1V		104	130		
			T_A = –55°C to 125°C		125		
		V_S = 2.7V, V_{CM} = V–, (V–) + 0.1V < V_O < (V+) – 0.1V[2]		101	120		
			T_A = –55°C to 125°C		118		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				4.5		MHz
SR	Slew rate[3]	V_S = 40V, G = +1, C_L = 20pF	20mV < V_{ID} < 150mV		0.5		V/µs
			V_{ID} > 150mV		21		
t_S	Settling time	To 0.01%, V_S = 40V, G = +1, C_L = 20pF	V_{STEP} = 10V		2.5		µs
			V_{STEP} = 2V		1.5		
		To 0.1%, V_S = 40V, G = +1, C_L = 20pF	V_{STEP} = 10V		2		
			V_{STEP} = 2V		1		
	Phase margin	G = +1, R_L = 10kΩ, C_L = 20pF			60		°
	Overload recovery time	V_{IN} × gain > V_S			400		ns
THD+N	Total harmonic distortion + noise [1]	V_S = 40V, V_O = 3V_{RMS}, G = +1, f = 1kHz			0.00021		%

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5.5 Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

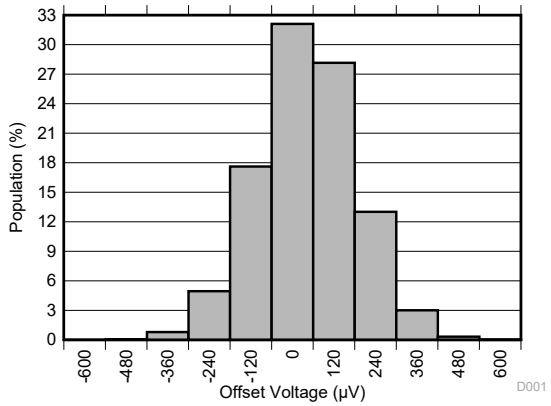
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Voltage output swing from rail	Positive and negative rail headroom	V_S = 40V, R_L = no load(2)		5	10	mV
			V_S = 40V, R_L = 10kΩ		50	70	
			V_S = 40V, R_L = 2kΩ		300	350	
			V_S = 2.7V, R_L = no load(2)		1	6	
			V_S = 2.7V, R_L = 10kΩ		5	12	
			V_S = 2.7V, R_L = 2kΩ		25	40	
I_{SC}	Short-circuit current				±75		mA
C_{LOAD}	Capacitive load drive				1000		pF
Z_O	Open-loop output impedance	f = 1MHz, I_O = 0A			525		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_{CM} = V–, I_O = 0A	OPA4991-EP		560	685	µA
			OPA991-EP		560	691	
		V_{CM} = V–, I_O = 0A, T_A = –55°C to 125°C	OPA4991-EP			750	
			OPA991-EP			769	

(1) Third-order filter; bandwidth = 80kHz at –3dB.
(2) Specified by characterization only.
(3) Refer to *Slew Boost* for detailed discussion.

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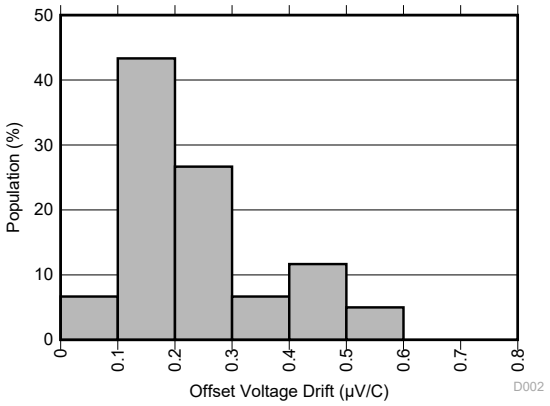
5.6 Typical Characteristics

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 10pF (unless otherwise noted)



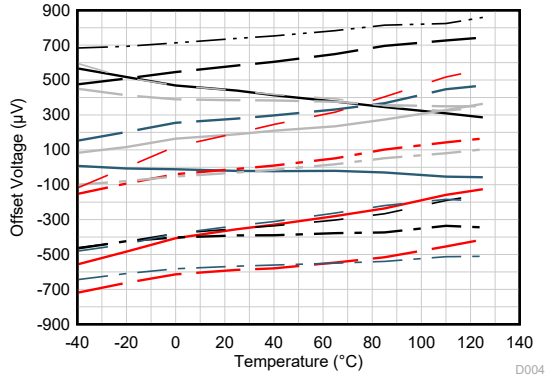
Distribution from 15462 amplifiers, T_A = 25°C

Figure 5-1. Offset Voltage Production Distribution



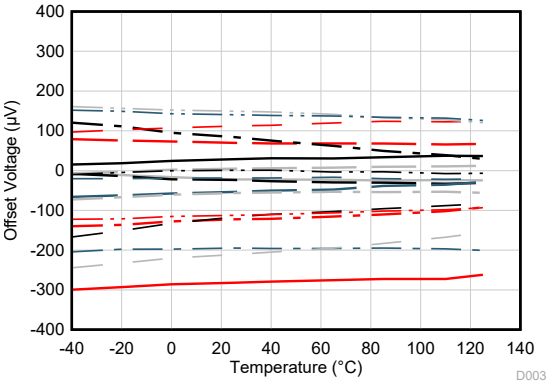
Distribution from 60 amplifiers

Figure 5-2. Offset Voltage Drift Distribution



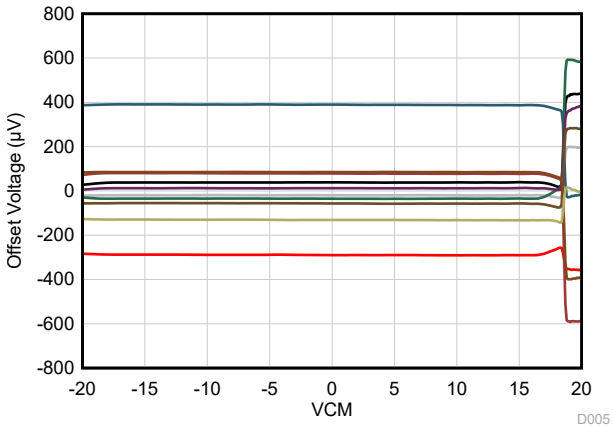
V_{CM} = V+

Figure 5-3. Offset Voltage vs Temperature



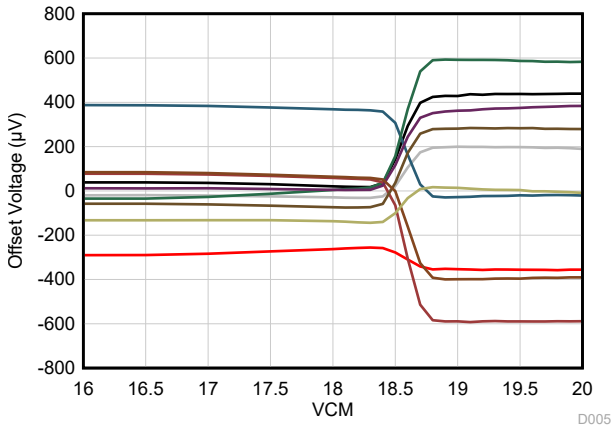
V_{CM} = V–

Figure 5-4. Offset Voltage vs Temperature



T_A = 25°C

Figure 5-5. Offset Voltage vs Common-Mode Voltage



T_A = 25°C

Figure 5-6. Offset Voltage vs Common-Mode Voltage (Transition Region)

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5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 10pF (unless otherwise noted)

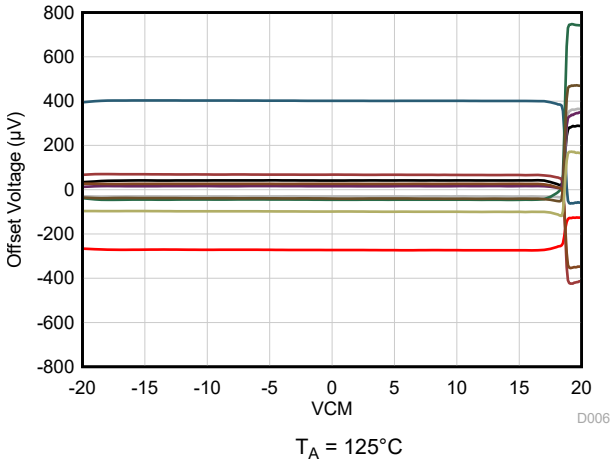


Figure 5-7. Offset Voltage vs Common-Mode Voltage

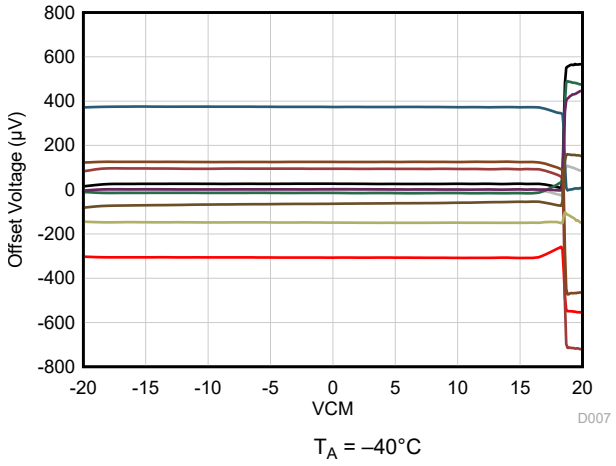


Figure 5-8. Offset Voltage vs Common-Mode Voltage

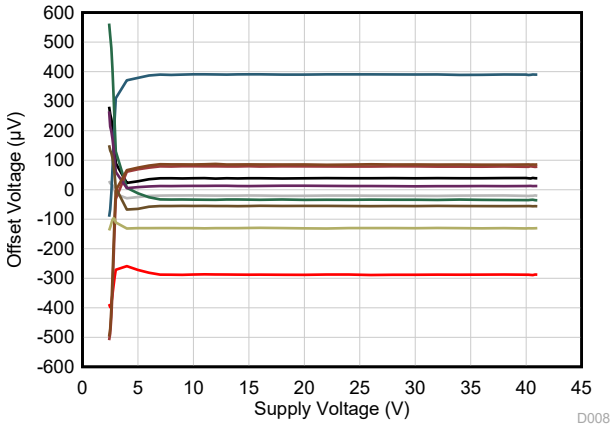


Figure 5-9. Offset Voltage vs Power Supply

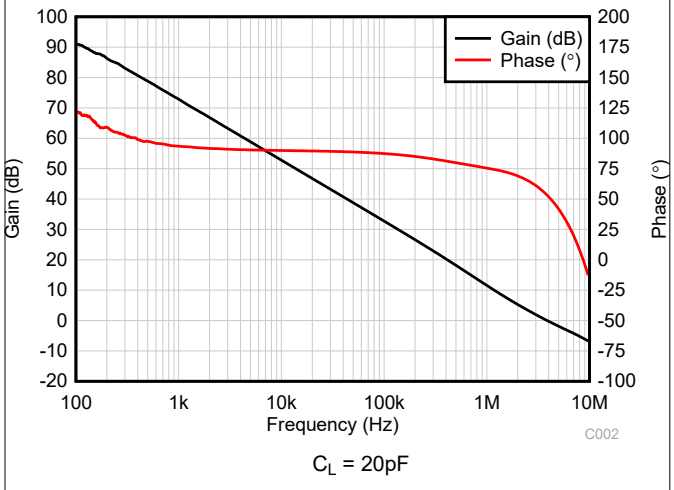


Figure 5-10. Open-Loop Gain and Phase vs Frequency

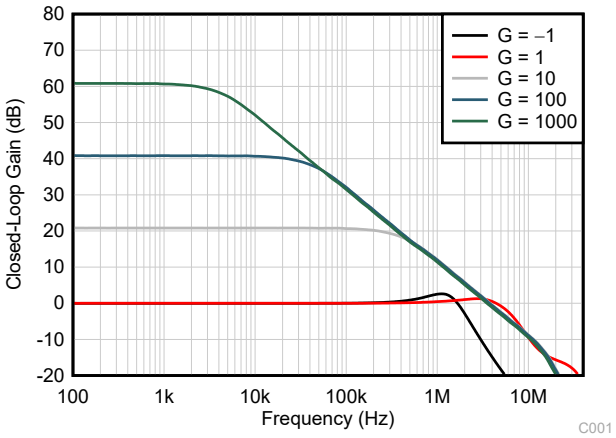


Figure 5-11. Closed-Loop Gain vs Frequency

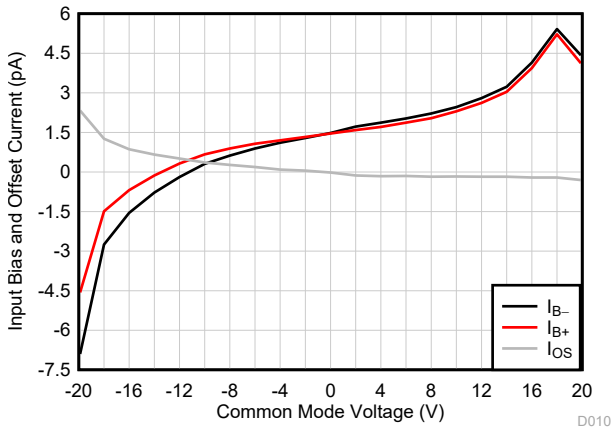


Figure 5-12. Input Bias Current vs Common-Mode Voltage

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5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 10pF (unless otherwise noted)

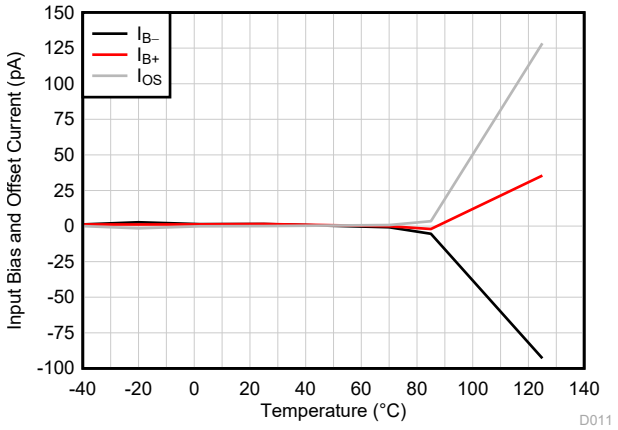


Figure 5-13. Input Bias Current vs Temperature

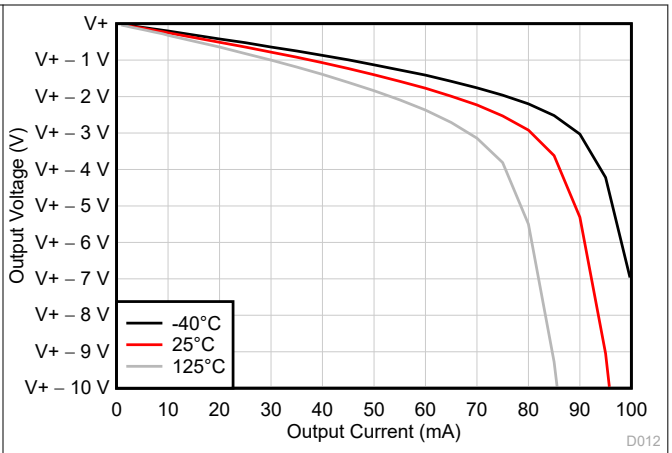


Figure 5-14. Output Voltage Swing vs Output Current (Sourcing)

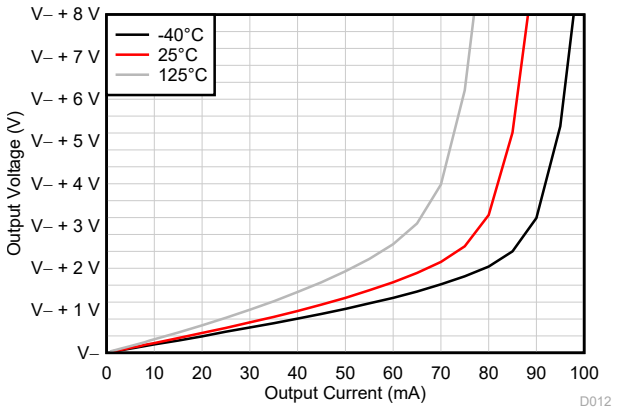


Figure 5-15. Output Voltage Swing vs Output Current (Sinking)

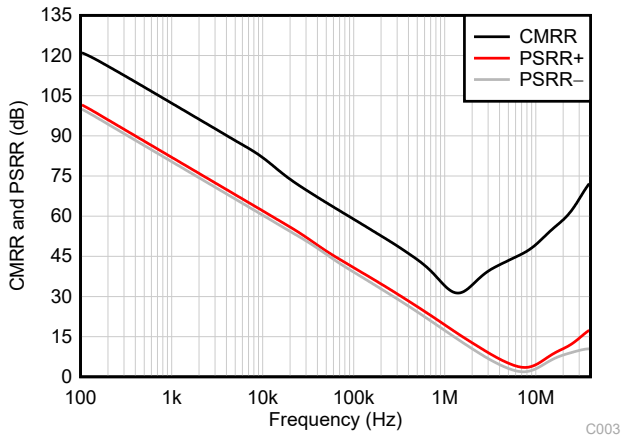


Figure 5-16. CMRR and PSRR vs Frequency

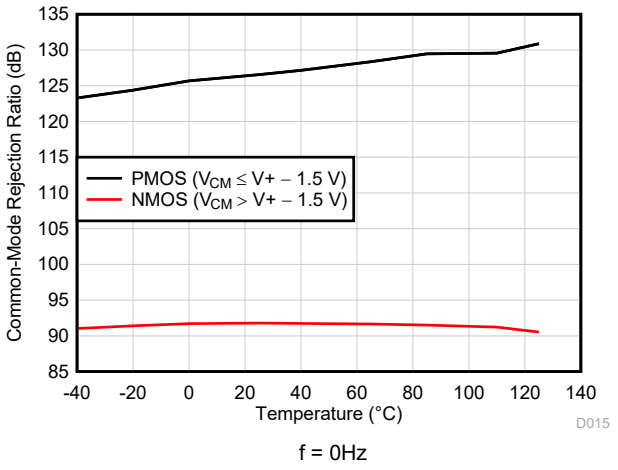


Figure 5-17. CMRR vs Temperature (dB)

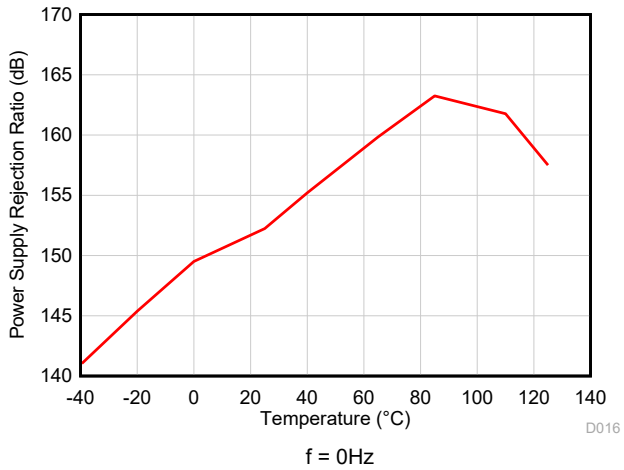


Figure 5-18. PSRR vs Temperature (dB)

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5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 10pF (unless otherwise noted)

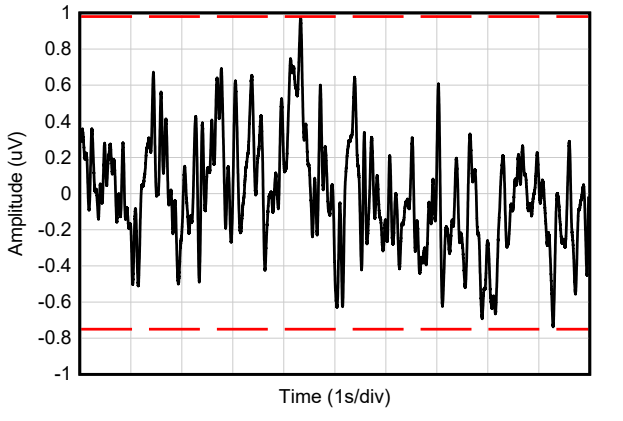


Figure 5-19. 0.1Hz to 10Hz Noise

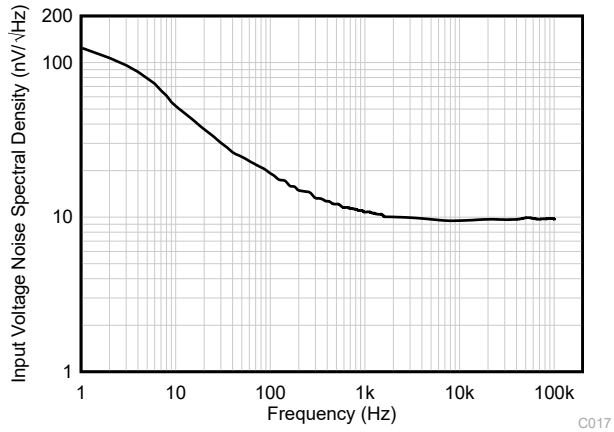
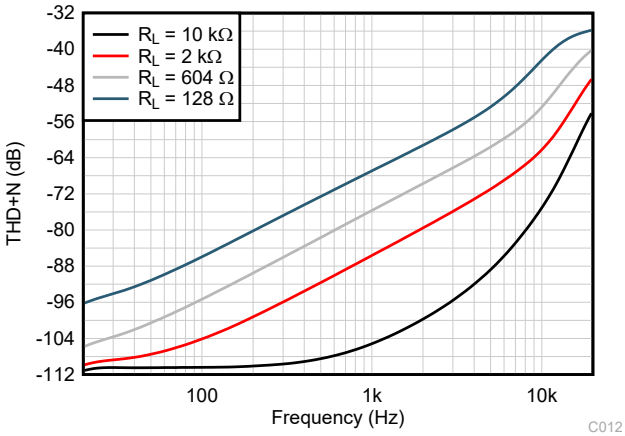
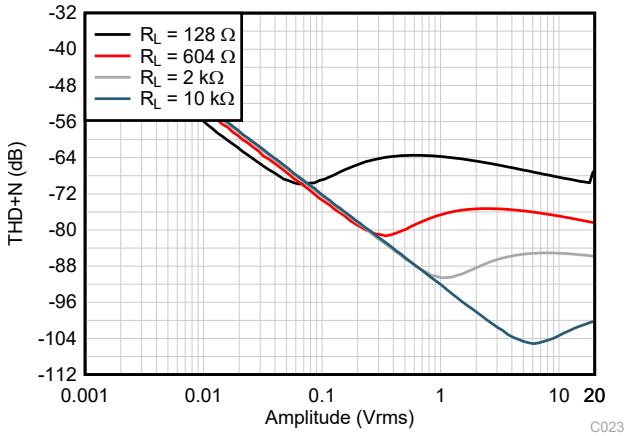


Figure 5-20. Input Voltage Noise Spectral Density vs Frequency



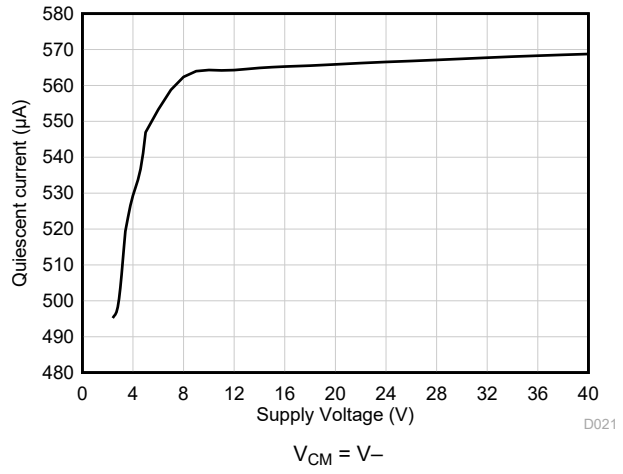
BW = 80kHz, V_{OUT} = 1V_{RMS}

Figure 5-21. THD+N Ratio vs Frequency



BW = 80kHz, f = 1kHz

Figure 5-22. THD+N vs Output Amplitude



V_{CM} = V–

Figure 5-23. Quiescent Current vs Supply Voltage

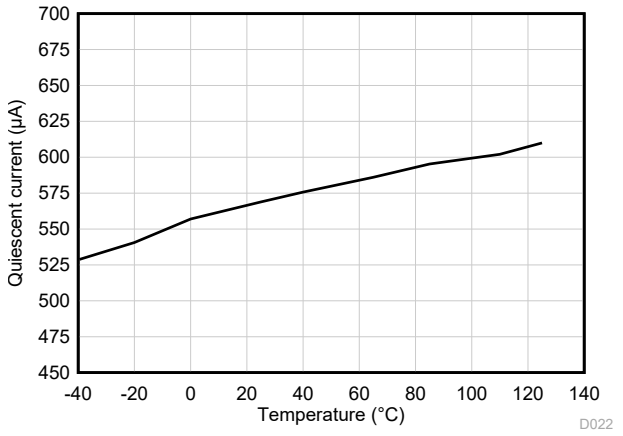


Figure 5-24. Quiescent Current vs Temperature

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5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 10pF (unless otherwise noted)

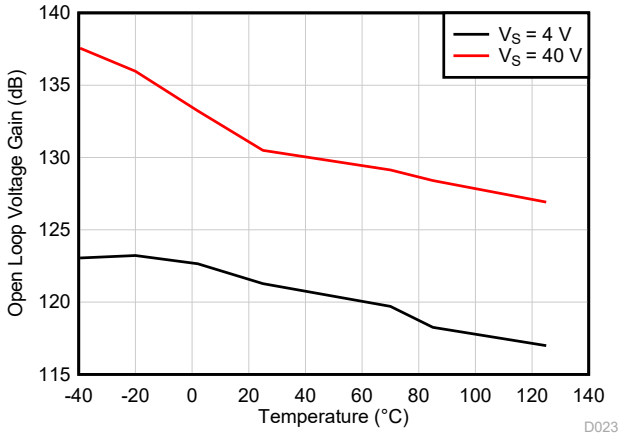


Figure 5-25. Open Loop Voltage Gain vs Temperature (dB)

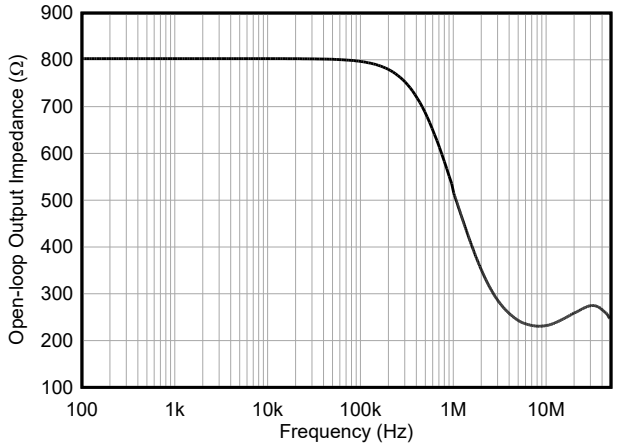
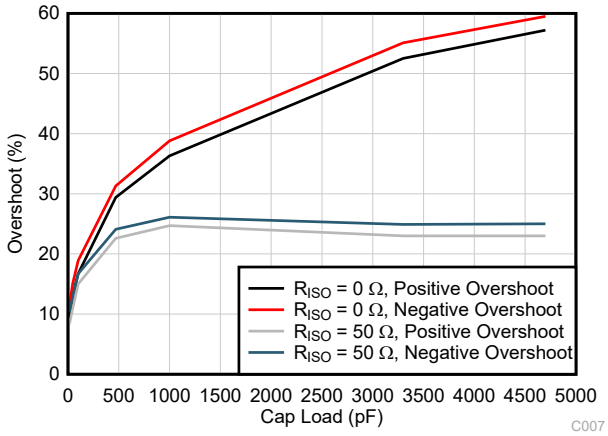
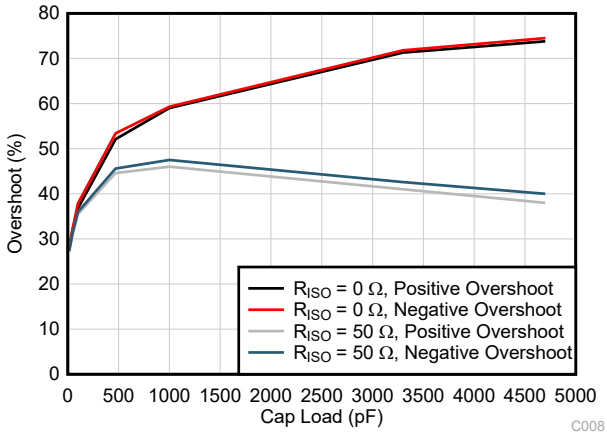


Figure 5-26. Open-loop Output Impedance vs Frequency



G = –1, 10mV output step

Figure 5-27. Small-Signal Overshoot vs Capacitive Load



G = 1, 10mV output step

Figure 5-28. Small-Signal Overshoot vs Capacitive Load

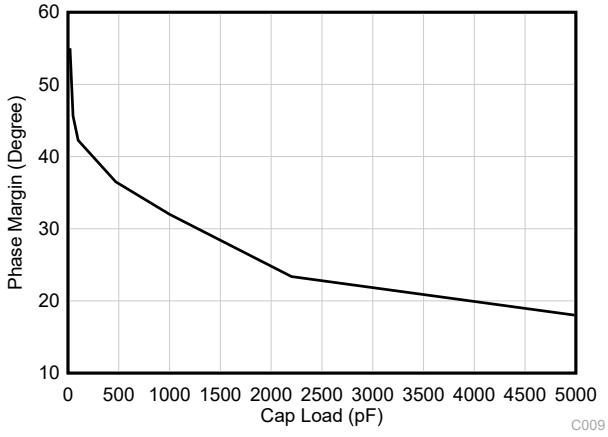
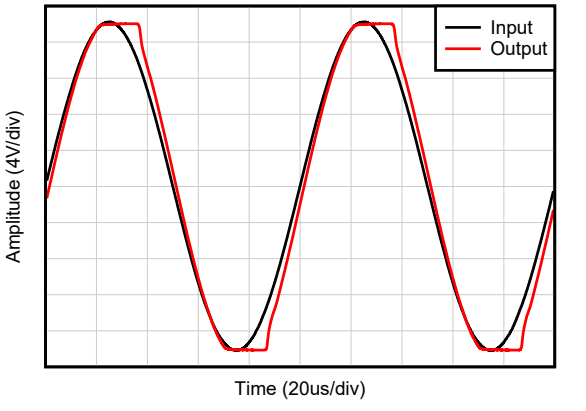


Figure 5-29. Phase Margin vs Capacitive Load



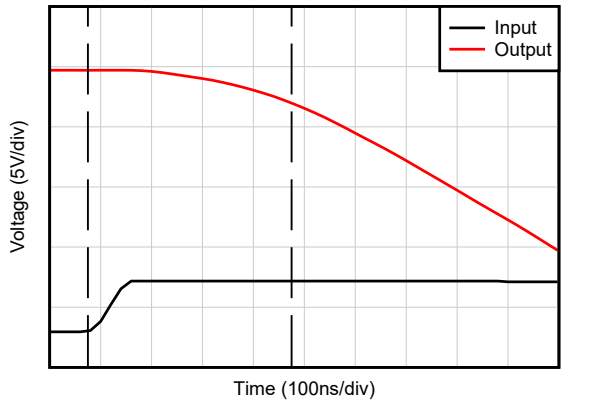
V_{IN} = ±20V; V_S = V_{OUT} = ±17V

Figure 5-30. No Phase Reversal

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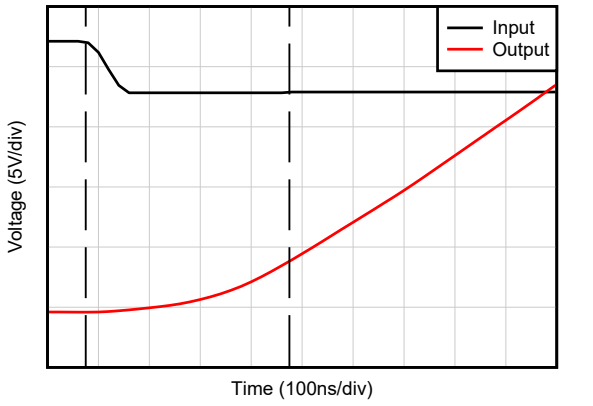
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 10pF (unless otherwise noted)



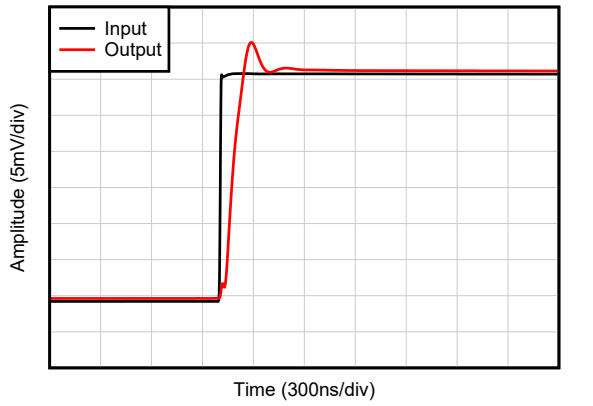
G = –10

Figure 5-31. Positive Overload Recovery



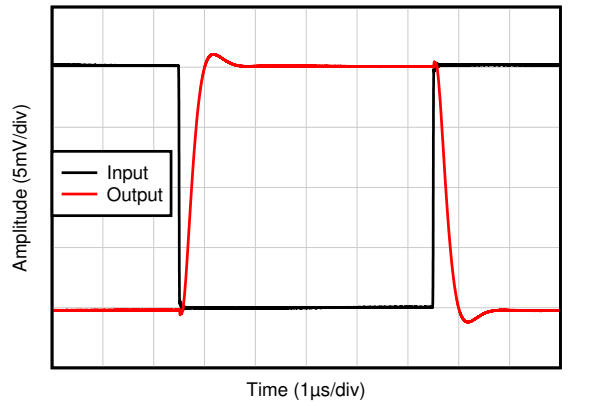
G = –10

Figure 5-32. Negative Overload Recovery



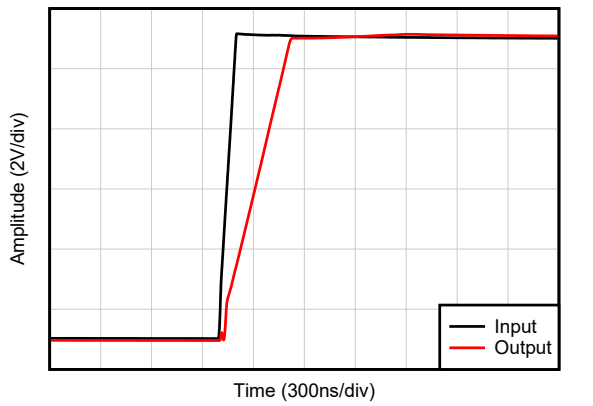
C_L = 20pF, G = 1, 20mV step response

Figure 5-33. Small-Signal Step Response, Rising



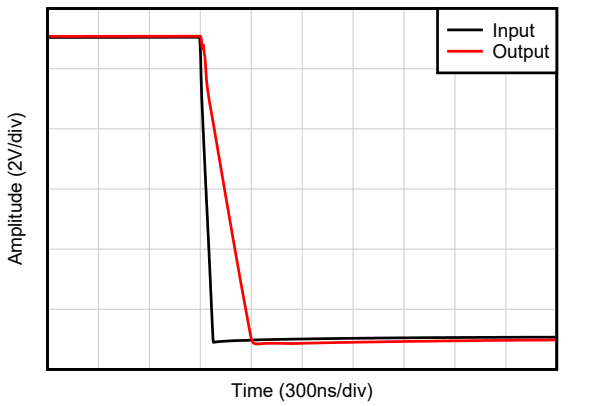
C_L = 20pF, G = -1, 20mV step response

Figure 5-34. Small-Signal Step Response



C_L = 20pF, G = 1

Figure 5-35. Large-Signal Step Response (Rising)



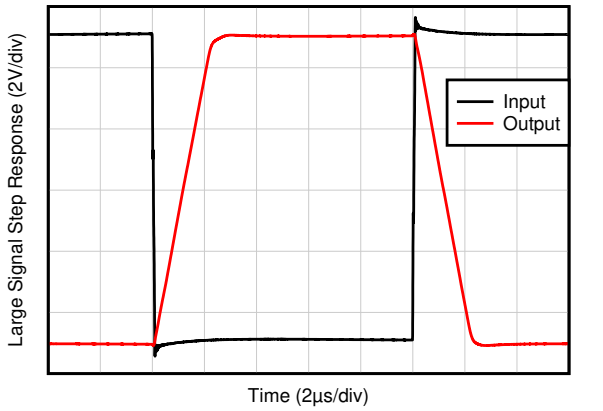
C_L = 20pF, G = 1

Figure 5-36. Large-Signal Step Response (Falling)

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5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 10pF (unless otherwise noted)



C_L = 20pF, G = –1

Figure 5-37. Large-Signal Step Response

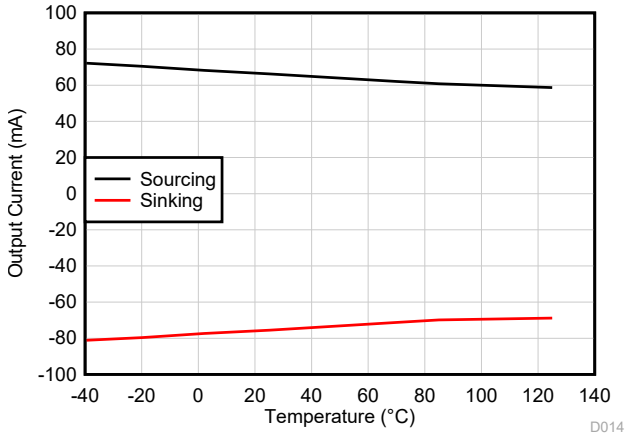


Figure 5-38. Short-Circuit Current vs Temperature

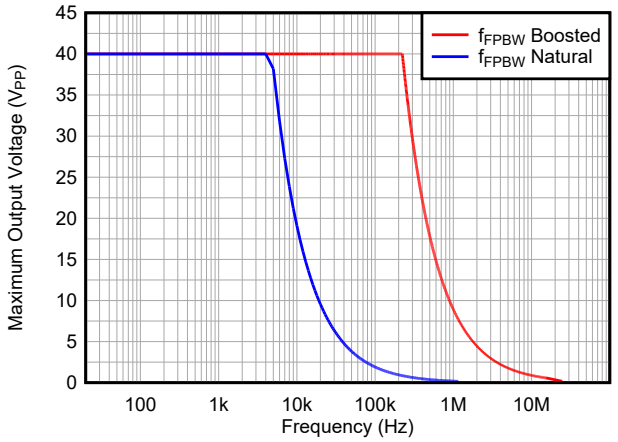


Figure 5-39. Maximum Output Voltage vs Frequency

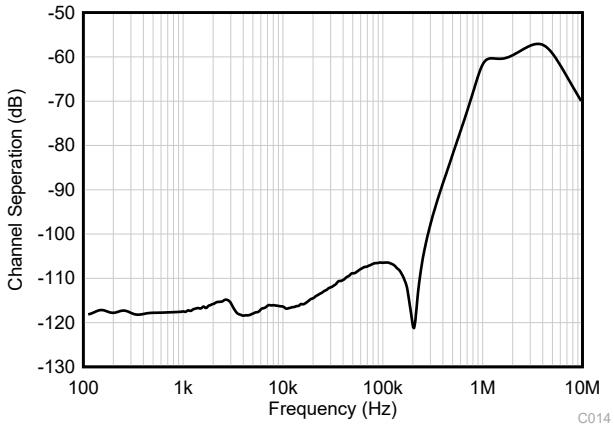


Figure 5-40. Channel Separation vs Frequency

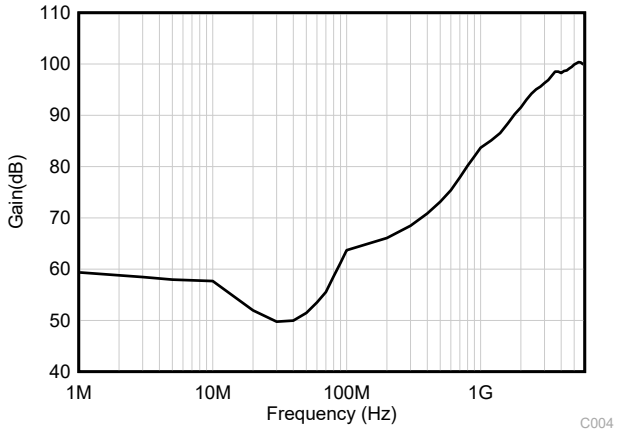


Figure 5-41. EMIRR (Electromagnetic Interference Rejection Ratio) at Inputs vs Frequency

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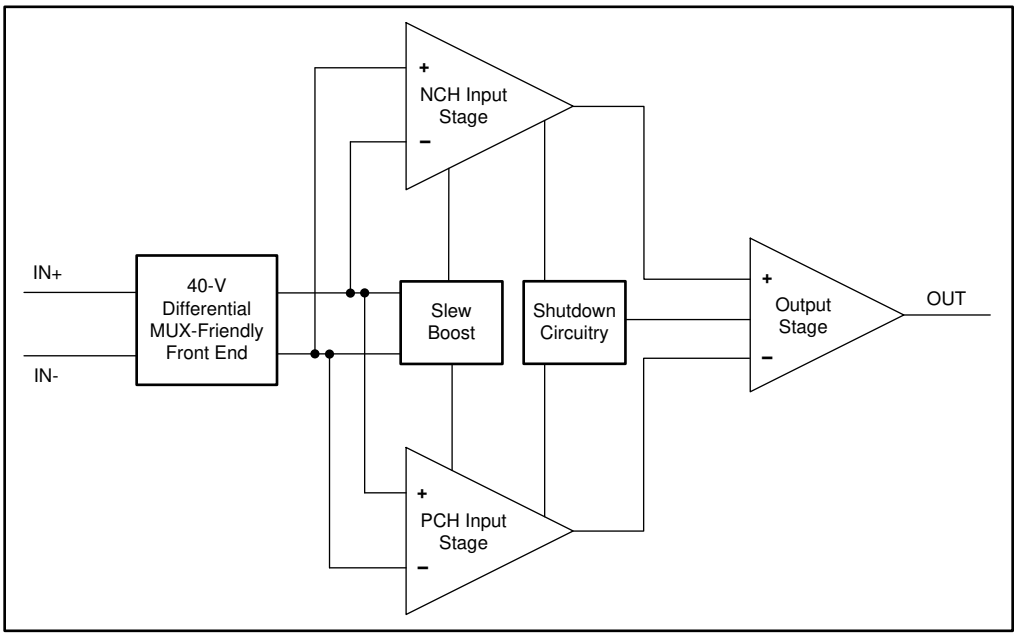
6 Detailed Description

6.1 Overview

The OPAx991-EP is a 40V general purpose operational amplifier. This device offers excellent DC precision and AC performance, including rail-to-rail input/output, low offset (±125µV, typ), low offset drift (±0.3µV/°C, typ), and 4.5MHz bandwidth.

Unique features such as differential and common-mode input-voltage range to the supply rail, high output current (±75mA) and high peak slew rate (21V/µs) make the OPAx991-EP a robust, high-performance operational amplifier for high-voltage applications.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Input Protection Circuitry

The OPAx991-EP uses a unique input architecture to eliminate the requirement for input protection diodes but still provides robust input protection under transient conditions. Figure 6-1 shows conventional input diode protection schemes that are activated by fast transient step responses and introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 6-2. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current and resulting in extended settling time.

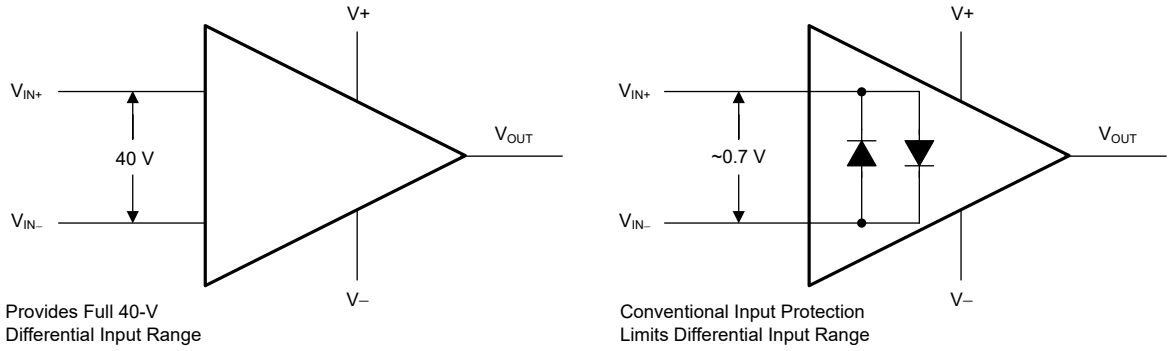


Figure 6-1. OPAx991-EP Input Protection Does Not Limit Differential Input Capability

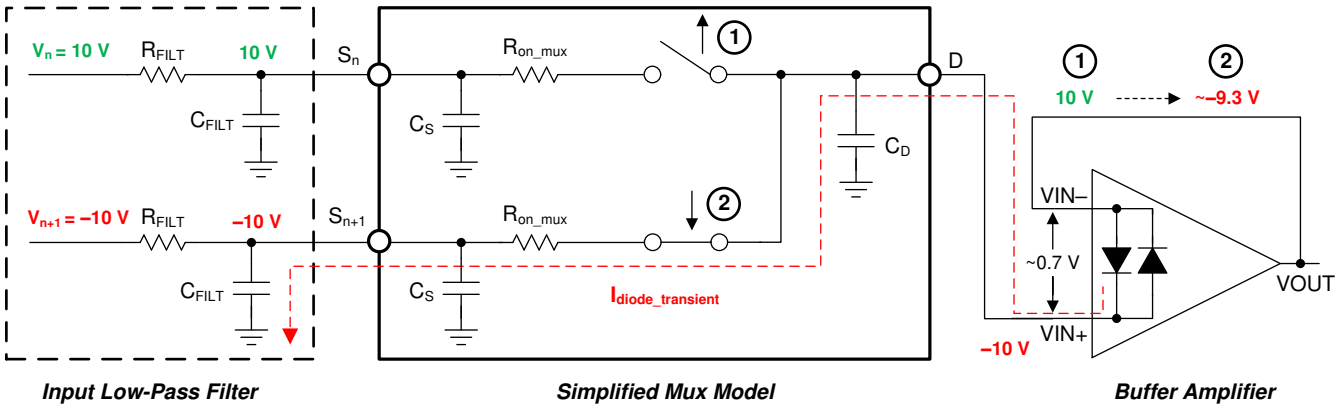


Figure 6-2. Back-to-Back Diodes Create Settling Issues

The OPAx991-EP family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications using a patented input protection architecture that does not introduce additional signal distortion or delayed settling time, making the device designed for op amp for multichannel, high-switched, input applications. The OPAx991-EP tolerates a maximum differential swing (voltage between inverting and non-inverting pins of the op amp) of up to 40V, meaning the device can be used as a comparator or in applications with fast-ramping input signals such as data-acquisition systems; see the TI TechNote *MUX-Friendly Precision Operational Amplifiers* for more information.

6.3.2 EMI Rejection

The OPAx991-EP uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx991-EP benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. Figure 6-3 shows the results of this testing on the OPAx991-EP.Table 6-1 shows the EMIRR IN+ values for the OPAx991-EP at particular frequencies commonly encountered in real-world applications. The *EMI*

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Rejection Ratio of Operational Amplifiers application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

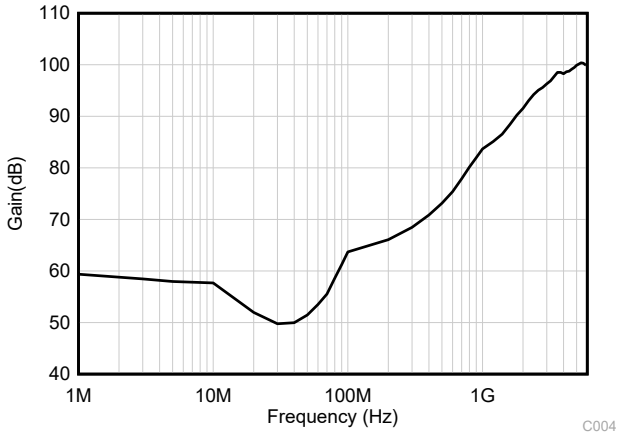


Figure 6-3. EMIRR Testing

Table 6-1. OPAx991-EP EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	73.2dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	82.5dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	89.7dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	93.9dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	95.7dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	98.0dB

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6.3.3 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the OPAx991-EP is 150°C. Exceeding this temperature causes damage to the device. The OPAx991-EP has a thermal protection feature that reduces damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 170°C. Figure 6-4 shows an application example for the OPA4991-EP that has significant self heating because of its power dissipation (0.81W). Thermal calculations indicate that for an ambient temperature of 65°C, the device junction temperature will reach 177°C. The actual device, however, turns off the output drive to recover towards a safe junction temperature. Figure 6-4 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3V. When self heating causes the device junction temperature to increase above the internal limit, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor R_L. If the condition that caused excessive power dissipation is not removed, the amplifier will oscillate between a shutdown and enabled state until the output fault is corrected.

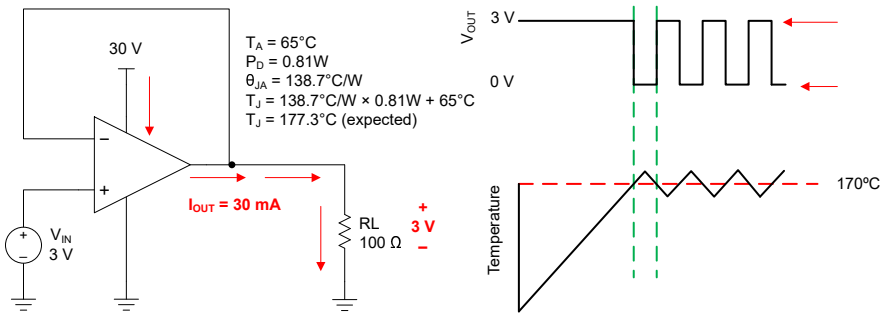


Figure 6-4. Thermal Protection

If the device continues to operate at high junction temperatures with high output power over a long period of time, regardless if the device is or is not entering thermal shutdown, the thermal dissipation of the device can slowly degrade performance of the device and eventually cause catastrophic destruction. Designers should be careful to limit output power of the device at high temperatures, or control ambient and junction temperatures under high output power conditions.

6.3.4 Capacitive Load and Stability

The OPAx991-EP features a resistive output stage capable of driving moderate capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive large capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see Figure 6-5 and Figure 6-6. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.

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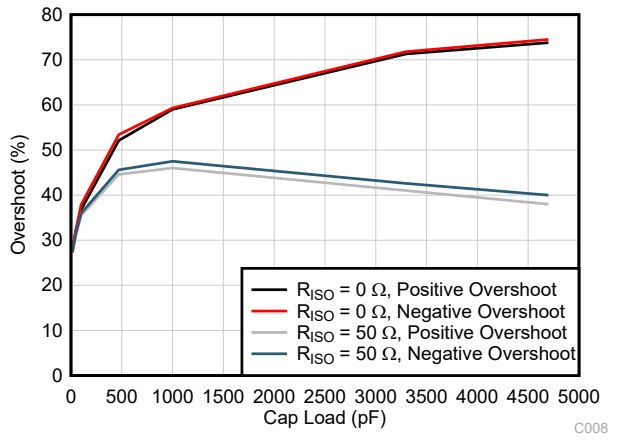


Figure 6-5. Small-Signal Overshoot vs Capacitive Load (10mV Output Step, G = 1)

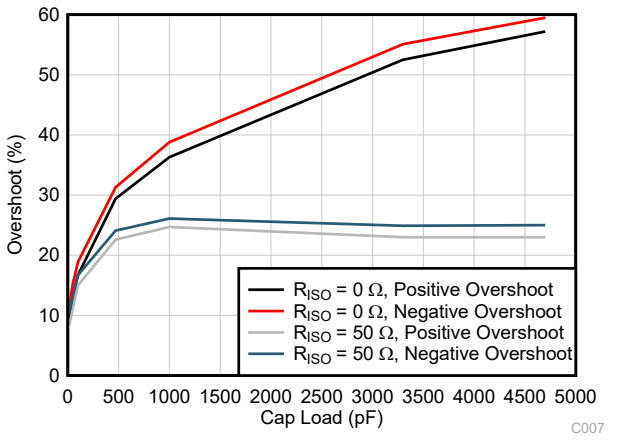


Figure 6-6. Small-Signal Overshoot vs Capacitive Load (10mV Output Step, G = –1)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small resistor, R_{ISO}, in series with the output, as shown in Figure 6-7. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the OPAx991-EP an excellent choice for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in Figure 6-7 uses an isolation resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin.

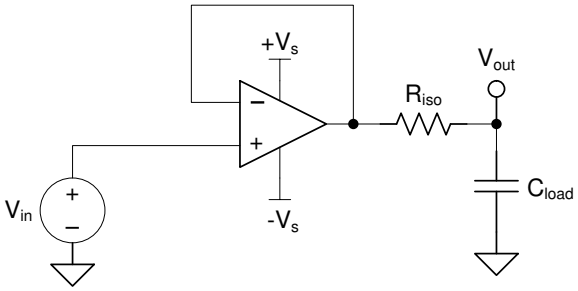


Figure 6-7. Extending Capacitive Load Drive With the OPAx991-EP

6.3.5 Common-Mode Voltage Range

The OPAx991-EP is a 40V, true rail-to-rail input operational amplifier with an input common-mode range that extends 100mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in Figure 6-8. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1V to 100mV above the positive supply. The P-channel pair is active for inputs from 100mV below the negative supply to approximately (V+) – 2V. There is a small transition region, typically (V+) – 2V to (V+) – 1V in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

Figure 5-5 shows this transition region for a typical device in terms of input voltage offset in more detail.

For more information on common-mode voltage range and PMOS/NMOS pair interaction, see *Op Amps With Complementary-Pair Input Stages* application note.

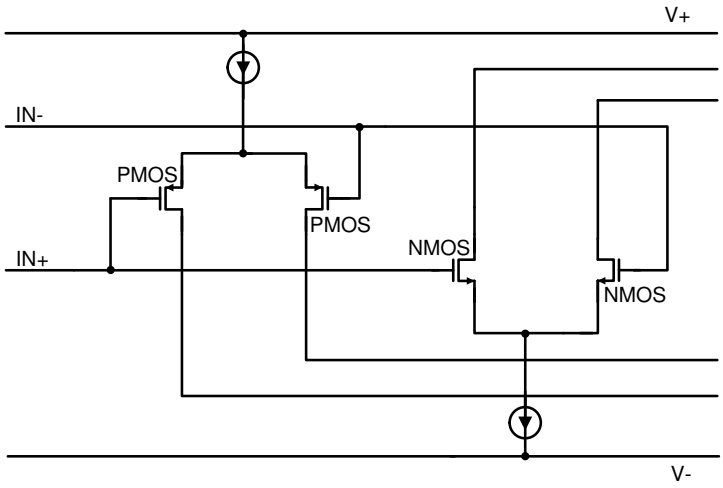


Figure 6-8. Rail-to-Rail Input Stage

6.3.6 Phase Reversal Protection

The OPAx991-EP family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx991-EP is a rail-to-rail input op amp; therefore, the common-mode range can extend beyond the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in Figure 6-9. For more information on phase reversal, see *Op Amps With Complementary-Pair Input Stages* application note.

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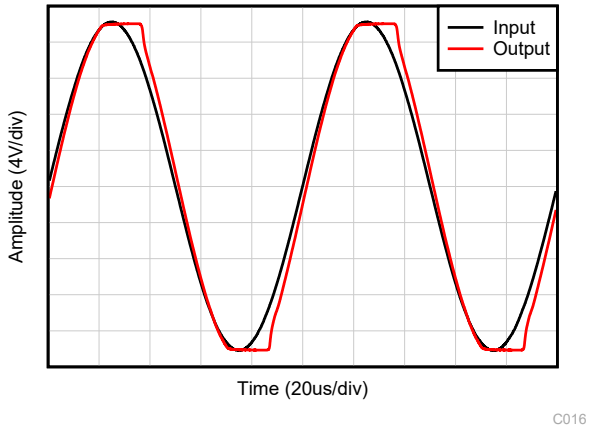


Figure 6-9. No Phase Reversal

6.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 6-10 shows an illustration of the ESD circuits contained in the OPAx991-EP (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

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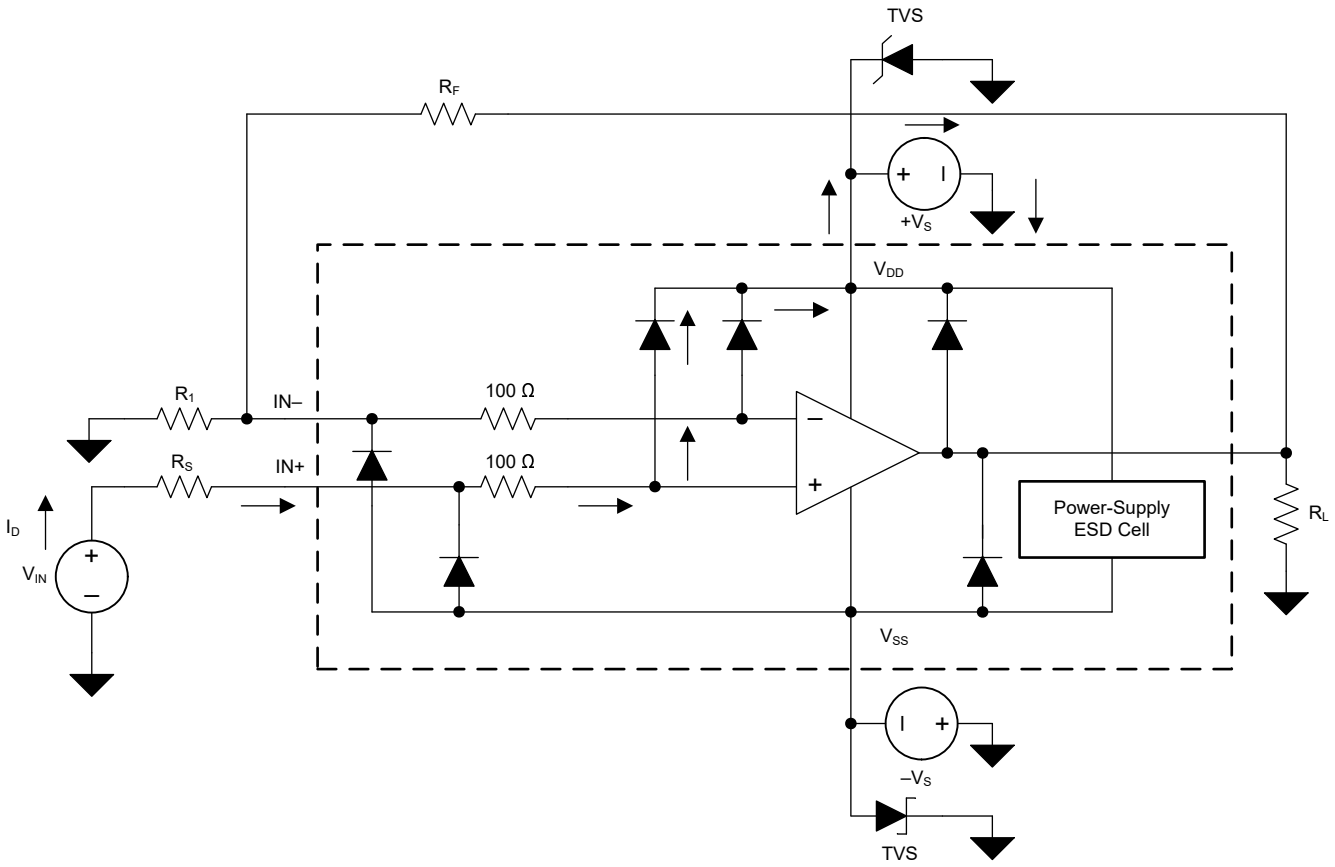


Figure 6-10. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example; 1kV, 100ns), whereas an EOS event is long duration and lower voltage (for example; 50V, 100ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

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6.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx991-EP is approximately 400ns.

6.3.9 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier can exhibit some amount of deviation from the preferred value, like the input offset voltage of the amplifier. These deviations often follow *Gaussian* (bell curve), or *normal* distributions, and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in the *Electrical Characteristics*.

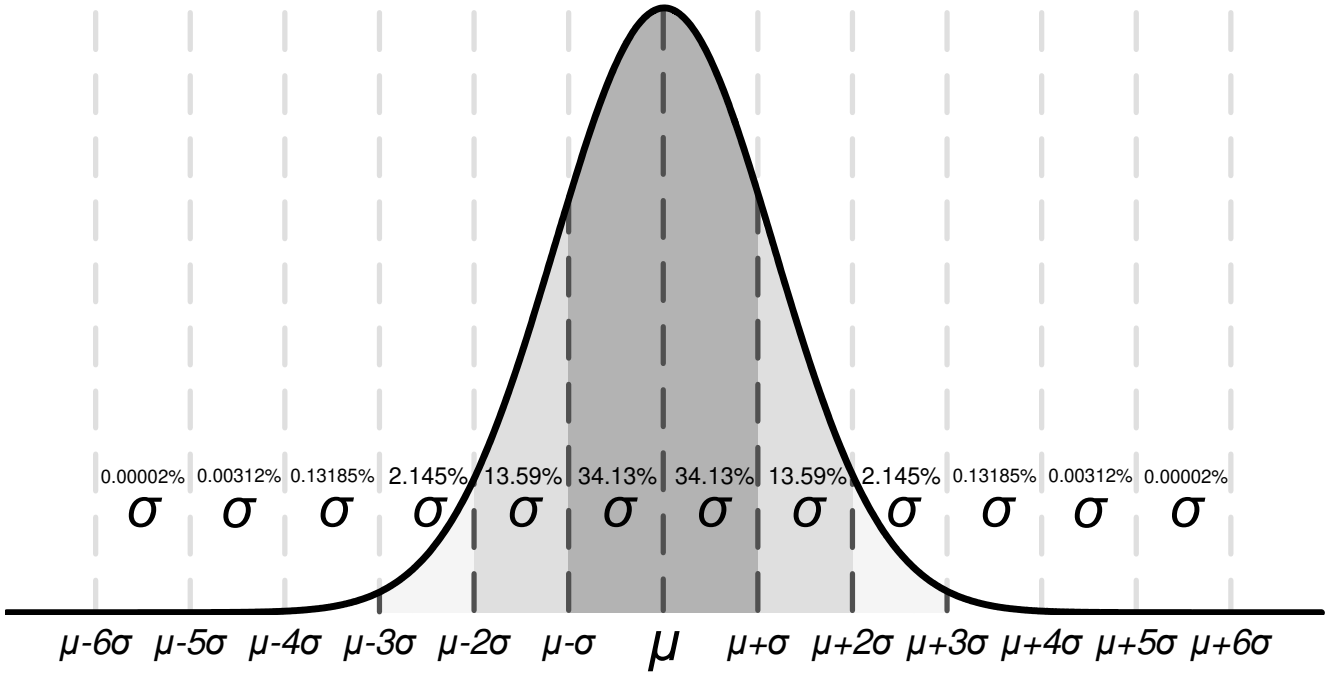


Figure 6-11. Ideal Gaussian Distribution

Figure 6-11 shows an example distribution, where μ, or *mu*, is the mean of the distribution, and where σ, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu - \sigma$ to $\mu + \sigma$).

Depending on the specification, values listed in the *typical* column of the *Electrical Characteristics* table are represented in different ways. As a general rule of thumb, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) to most accurately represent the typical value.

You can use this chart to calculate approximate probability of a specification in a unit; for example, for OPAx991-EP, the typical input voltage offset is 125μV, so 68.2% of all OPAx991-EP devices are expected to have an offset

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from –125µV to 125µV. At 4 σ (±500µV), 99.9937% of the distribution has an offset voltage less than ±500µV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are specified by TI, and units outside these limits will be removed from production material. For example, the OPAx991-EP family has a maximum offset voltage of 895µV at 25°C, and even though this corresponds to more than 5 σ (≈1 in 1.7 million units), which is extremely unlikely, any unit with larger offset than 895µV will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for your application, and design worst-case conditions using this value. For example, the 6-σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and can be an option as a wide guardband to design a system around. In this case, the OPAx991-EP family does not have a maximum or minimum for offset voltage drift, but based on Figure 5-2 and the typical value of 0.3µV/°C in the *Electrical Characteristics*, the 6-σ value for offset voltage drift is about 1.8µV/°C when calculated. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot be sure of the performance of a device. This information must be used only to estimate the performance of a device.

6.4 Device Functional Modes

The OPAx991-EP has a single functional mode and is operational when the power-supply voltage is greater than 2.7V (±1.35V). The maximum power supply voltage for the OPAx991-EP is 40V (±20V).

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPAx991-EP family offers excellent DC precision and AC performance. These devices operate up to 40V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 4.5MHz bandwidth and high output drive. These features make the OPAx991-EP a robust, high-performance operational amplifier for high-voltage industrial applications.

7.1.1 Slew Boost

The OPAx991-EP family features a slew-boosted architecture, to accelerate recovery from large-scale input steps. The rate of change of the device output scales according to the differential input voltage (V_{ID}), leading to three distinct modes of operation: a small-signal or linear region, a natural slew region, and a slew-boosted region. The effective slew rate of the device is therefore a function of the input signal, rather than having a fixed characteristic. During a large-signal input step, the output typically exhibits a fast rising edge while the inputs are held apart (V_{ID} > 150mV); then as the input voltages approach each other (V_{ID} < 150mV), the device output rate of change decreases and the output settles.

Note that the amplifier output rate of change in a given application depends on the circuit configuration, parastitics, and other factors. The data below reflect the open-loop step response of the device, while the values specified in *Electrical Characteristics* describe the closed-loop step response as expected in a typical circuit implementation.

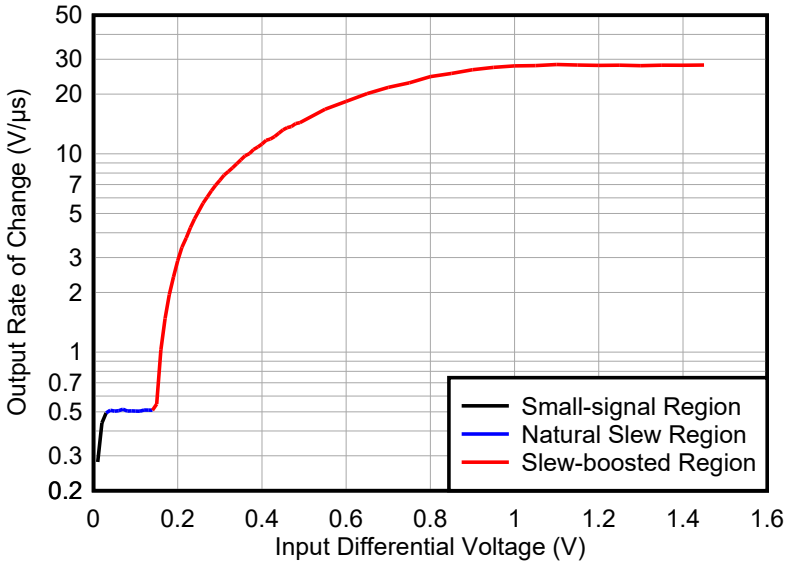


Figure 7-1. Output Rate of Change vs Input Differential Voltage for the OPAx991-EP

When an amplifier enters a slew condition, the quiescent current typically increases slightly while the internal Miller capacitance is charging. When the output slew-boost circuitry of the OPAx991-EP is activated, the charging rate of the Miller capacitance is "boosted" and a temporary rise in supply current occurs, as illustrated in Figure 7-2. For applications and use cases where the inputs are pulled apart and the slew-boost feature activated, this higher supply current must be considered for power budgeting purposes.

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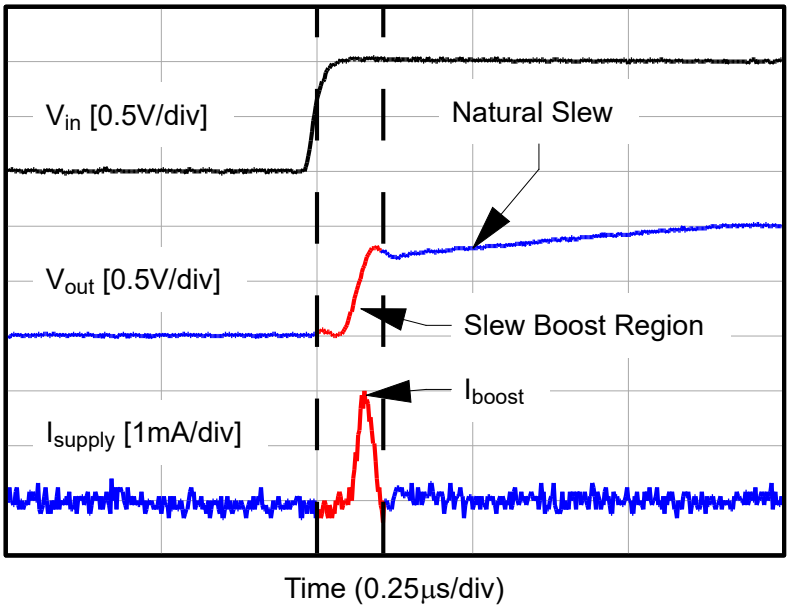


Figure 7-2. Large-Signal Step Response Characteristics of the OPAx991-EP

The full-power bandwidth (FPBW) curve of the device describes the maximum peak to peak voltage (V_{PP}) at a given frequency that the amplifier can reproduce without significant visual distortion. Operating inside of the full power bandwidth curve with a pure sine wave input signal results in a visually undistorted output signal, while operating beyond the full power bandwidth boundary results in a visually highly distorted triangle wave that is caused by the slew rate limit. This type of output distortion is known as slew-induced distortion.

Because the device slew rate scales according to the differential input voltage (V_{ID}), the OPAx991-EP exhibits two distinct slew-rate limited FPBW boundaries: one for the slew-boosted mode of operation, and another for the natural slew region. Note that as the natural FPBW is exceeded, the expected total harmonic distortion (THD) increases. To reduce slew-induced distortion, operation within the natural FPBW curve is advised.

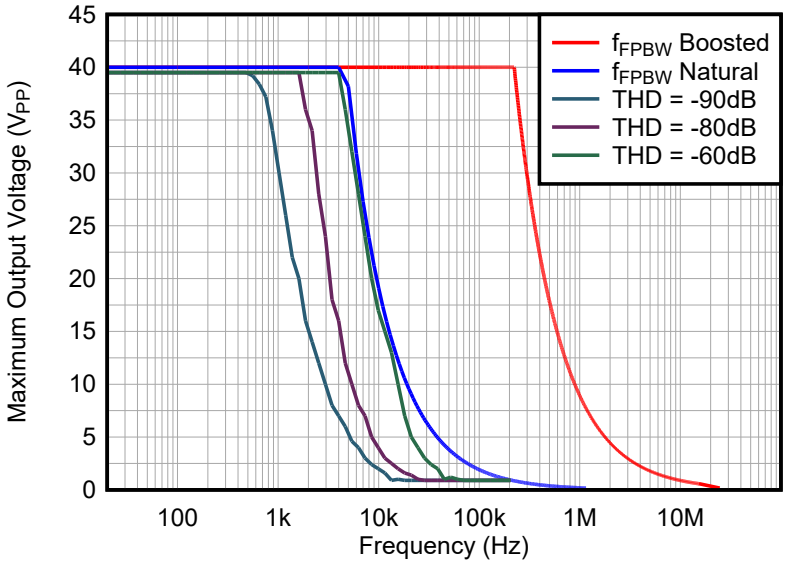


Figure 7-3. Maximum Output Voltage vs Frequency in Natural and Boosted Slew for the OPAx991-EP

For detailed discussion of slew-boosted architectures and the associated effects on THD, including empirical measurements for the OPAx991 family, refer to the *Full Power Bandwidth and Op Amp Distortion* application note.

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7.2 Typical Applications

7.2.1 Low-Side Current Measurement

Figure 7-4 shows the OPAx991-EP configured in a low-side current sensing application. For a full analysis of the circuit shown in Figure 7-4 including theory, calculations, simulations, and measured data, see TI Precision Design TIPD129, *0A to 1A Single-Supply Low-Side Current-Sensing Solution*.

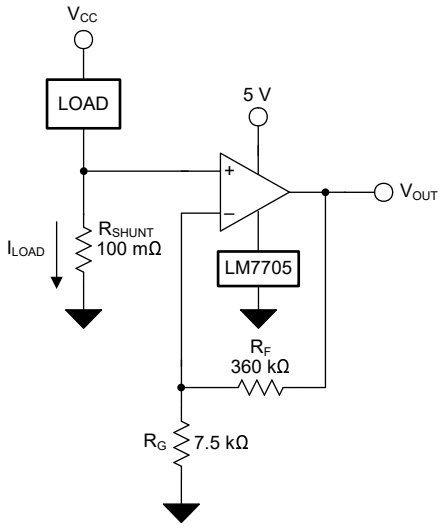


Figure 7-4. OPAx991-EP in a Low-Side, Current-Sensing Application

7.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0A to 1A
- Output voltage: 4.9V
- Maximum shunt voltage: 100mV

7.2.1.2 Detailed Design Procedure

The transfer function of the circuit in Figure 7-4 is given in Equation 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{1}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is defined using Equation 2.

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100mV}{1A} = 100m\Omega \tag{2}$$

Using Equation 2, R_{SHUNT} is calculated to be 100mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the OPAx991-EP to produce an output voltage of 0V to 4.9V. The gain needed by the OPAx991-EP to produce the necessary output voltage is calculated using Equation 3.

$$Gain = \frac{\left(V_{OUT_MAX} - V_{OUT_MIN}\right)}{\left(V_{IN_MAX} - V_{IN_MIN}\right)} \tag{3}$$

Using Equation 3, the required gain is calculated to be 49V/V, which is set with resistors R_F and R_G. Equation 4 is used to size the resistors, R_F and R_G, to set the gain of the OPAx991-EP to 49V/V.

$$Gain = 1 + \frac{\left(R_F\right)}{\left(R_G\right)} \tag{4}$$

Choosing R_F as 360kΩ, R_G is calculated to be 7.5kΩ. R_F and R_G were chosen as 360kΩ and 7.5kΩ because they are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. Figure 7-5 shows the measured transfer function of the circuit shown in Figure 7-4.

7.2.1.3 Application Curve

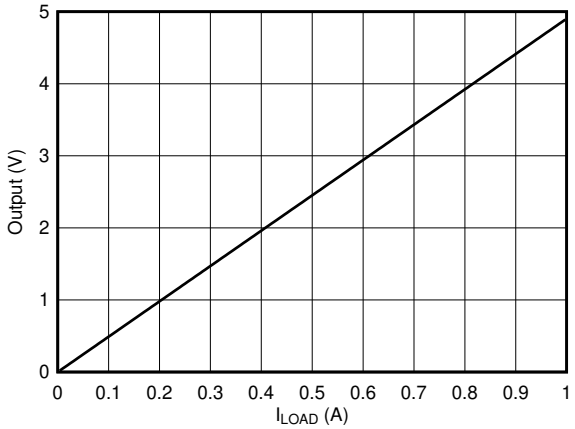


Figure 7-5. Low-Side, Current-Sense, Transfer Function

7.3 Power Supply Recommendations

The OPAx991-EP is specified for operation from 2.7V to 40V (±1.35V to ±40V); many specifications apply from –55°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

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CAUTION

Supply voltages larger than 40V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to *Layout*.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 7-7, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

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7.4.2 Layout Example

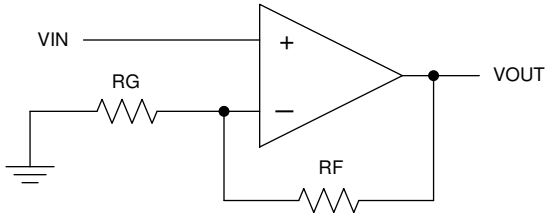


Figure 7-6. Schematic Representation

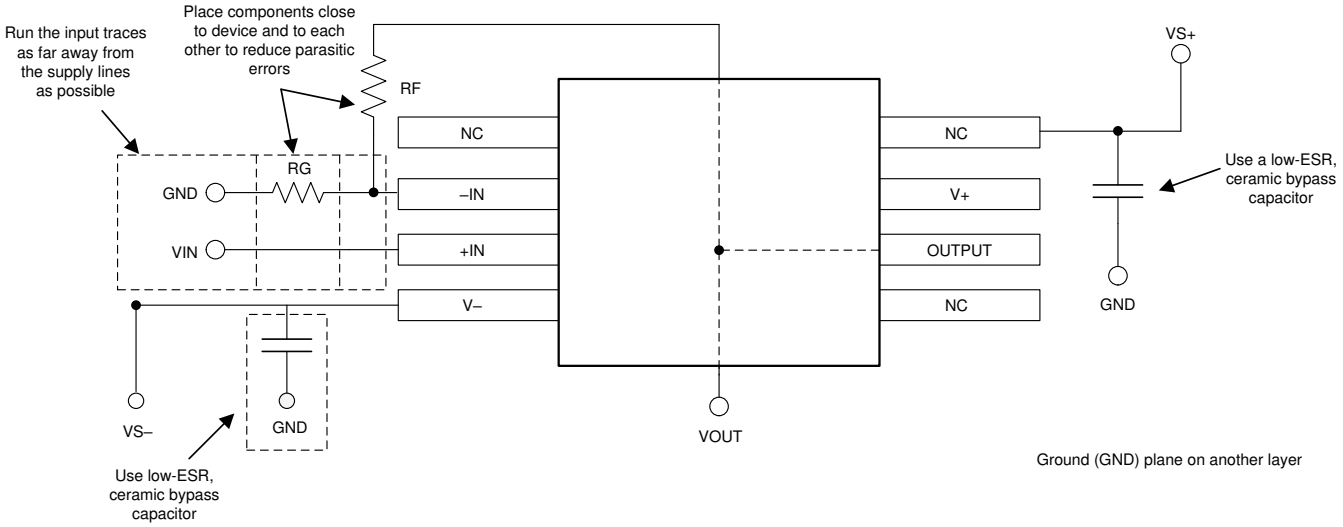


Figure 7-7. Operational Amplifier Board Layout for Noninverting Configuration

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8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *Analog Engineer's Circuit Cookbook: Amplifiers* solution guide

Texas Instruments, *AN31 Amplifier Circuit Collection* application note

Texas Instruments, *MUX-Friendly Precision Operational Amplifiers* application brief

Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report

Texas Instruments, *Op Amps With Complementary-Pair Input Stages* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2022) to Revision C (September 2026)	Page
• Changed wording of slew rate to "high *peak* slew rate" in *Features* and *Description* and wording of inputs from "MUX-friendly/comparator" to "Mux-friendly" in *Features*	1
• Updated description of input structure in *Features* and *Input Protection Circuitry*	1
• Added single-channel OPA991-EP in DBV package to *Package Information* table and throughout document.	1
• Added OPA991-EP to *ESD Ratings*	5
• Added OPA991-EP (DBV) to *Thermal Information*	5
• Added V_{ID} > 150mV condition to slew rate specification, and added 20mV < V_{ID} < 150mV condition	6
• Changed Figures 6-26 and 6-39	8
• Added *Slew Boost* section with discussion of device slew rate in natural slew and slew-boosted conditions.	25

Changes from Revision A (August 2022) to Revision B (November 2022)	Page
• Updated thermal resistance values	5
• Increased maximum output voltage swing (V_S = 40V, R_L = 10kΩ) from 55mV to 70mV	6

Changes from Revision * (June 2022) to Revision A (August 2022)	Page
• Changed device status from *Advance Information* to *Production Data*	1
• Deleted preview note from SOT-23 (14) package in *Device Information* table	1

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA4991MDYYREP	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	OPA4991EP
OPA4991MDYYREP.A	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	OPA4991EP
POPA991MDBVREP	Active	Preproduction	SOT-23 (DBV) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-55 to 125	
V62/21615-01XE	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	OPA4991EP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA4991-EP, OPA991-EP :

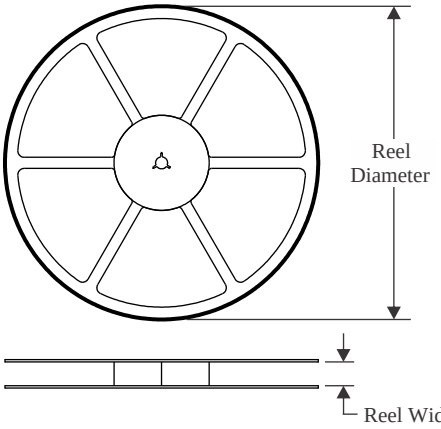
- Catalog : OPA4991, OPA991
- Automotive : OPA4991-Q1, OPA991-Q1

NOTE: Qualified Version Definitions:

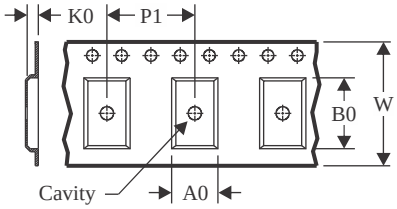
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

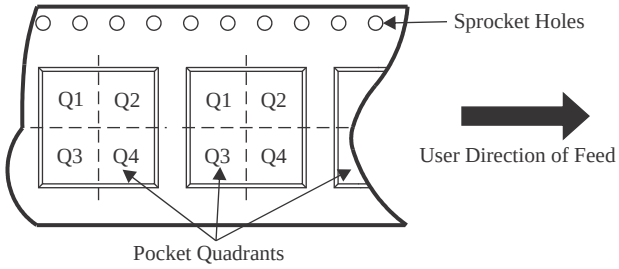


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

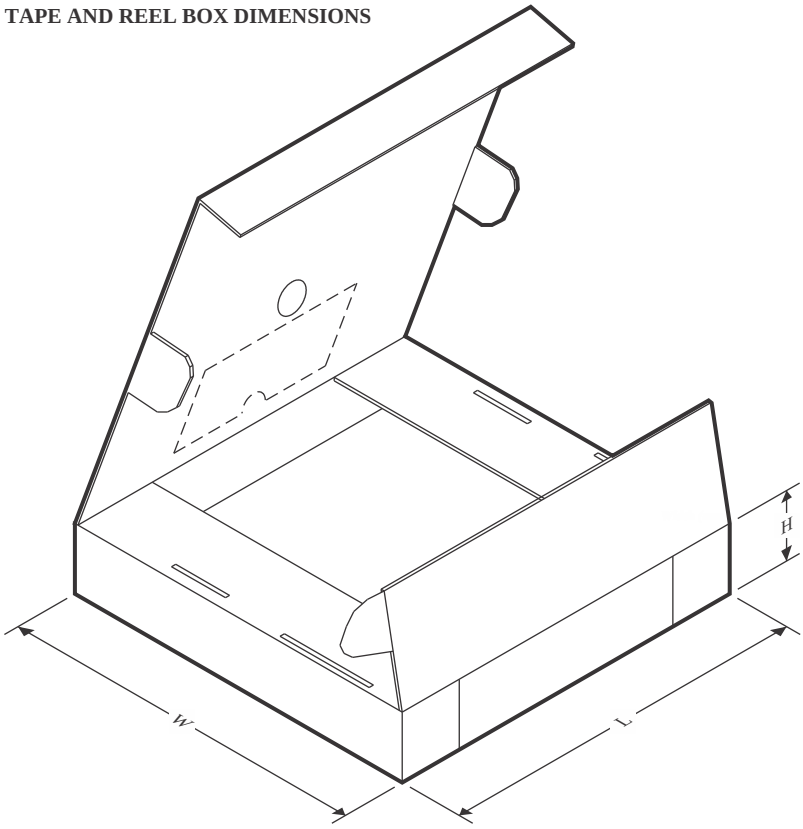
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA4991MDYYREP	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

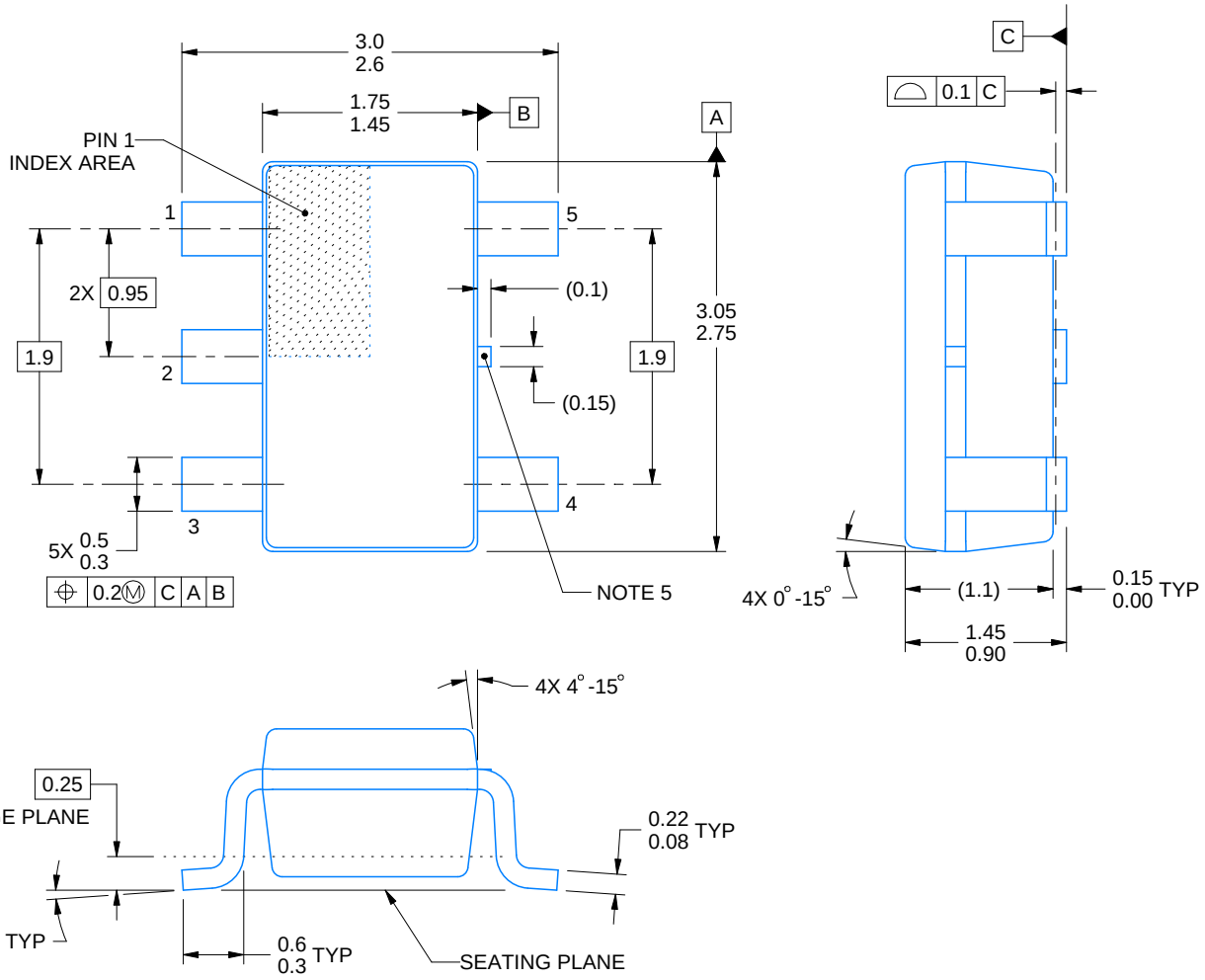
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA4991MDYYREP	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

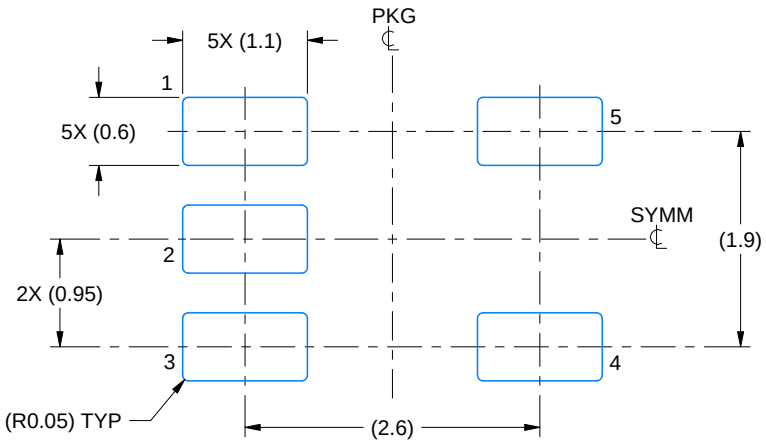
SMALL OUTLINE TRANSISTOR



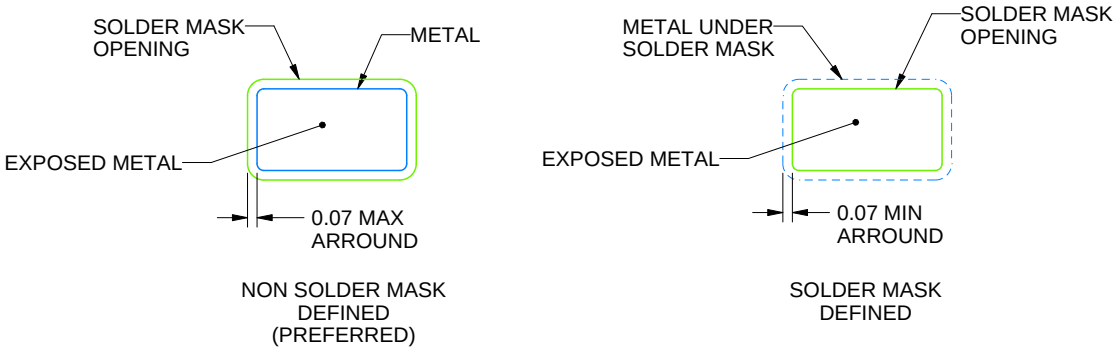
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

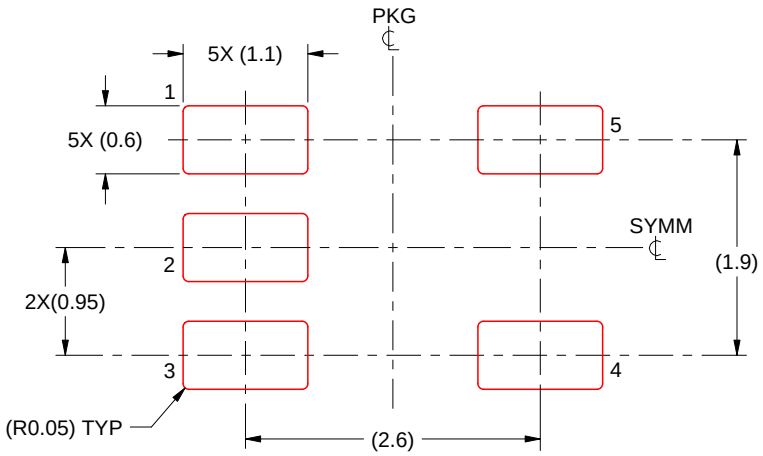


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

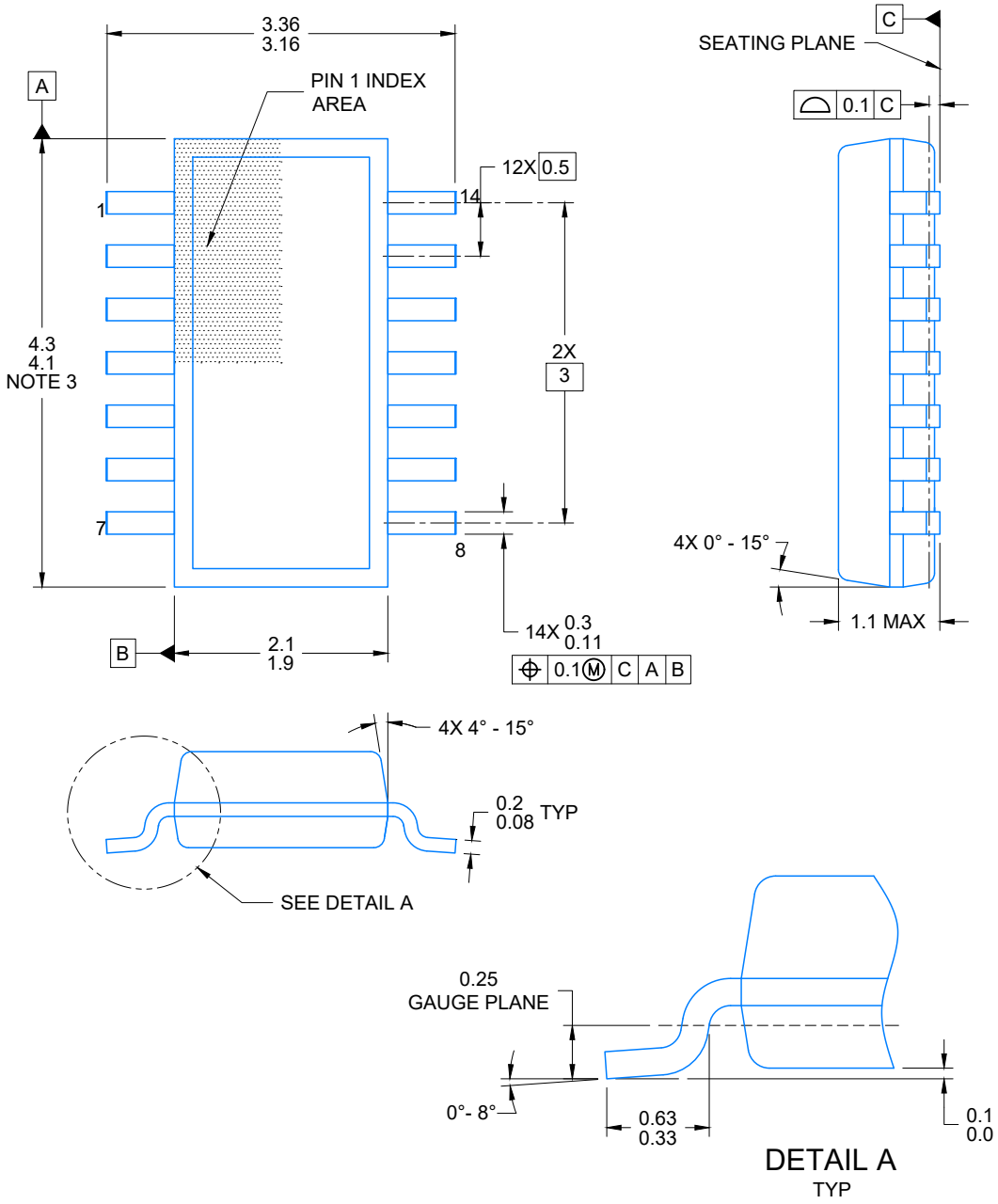
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DYY0014A

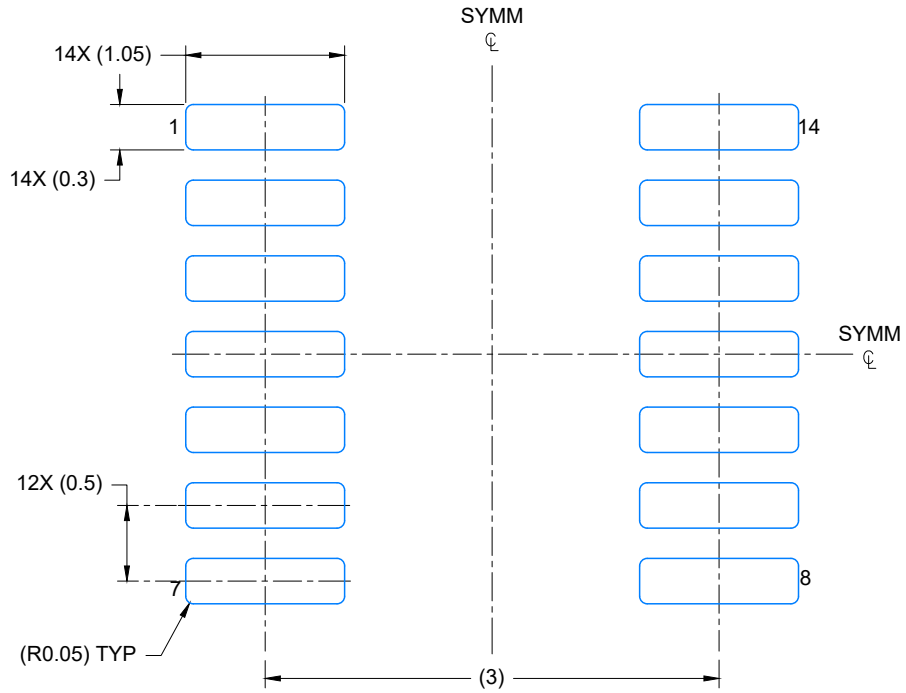
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

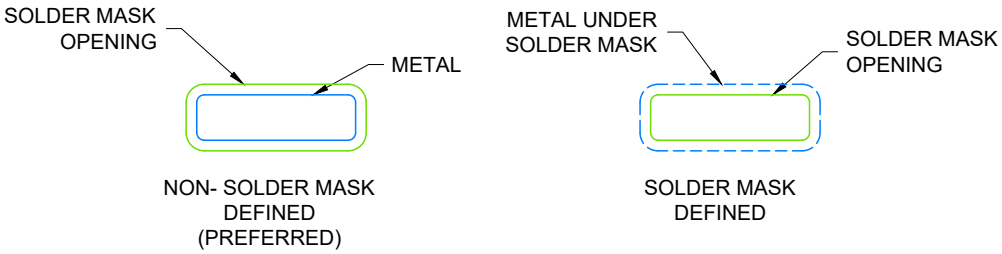


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

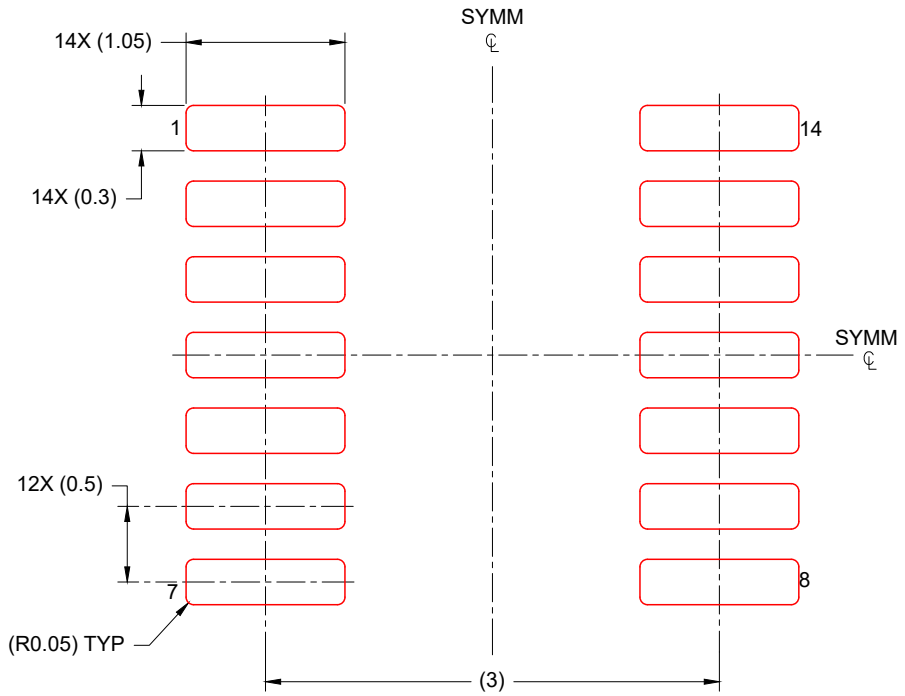


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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