

# PCM1744

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## *SoundPLUS™* 24 Bits, 96kHz, Sampling Stereo Audio DIGITAL-TO-ANALOG CONVERTER

### FEATURES

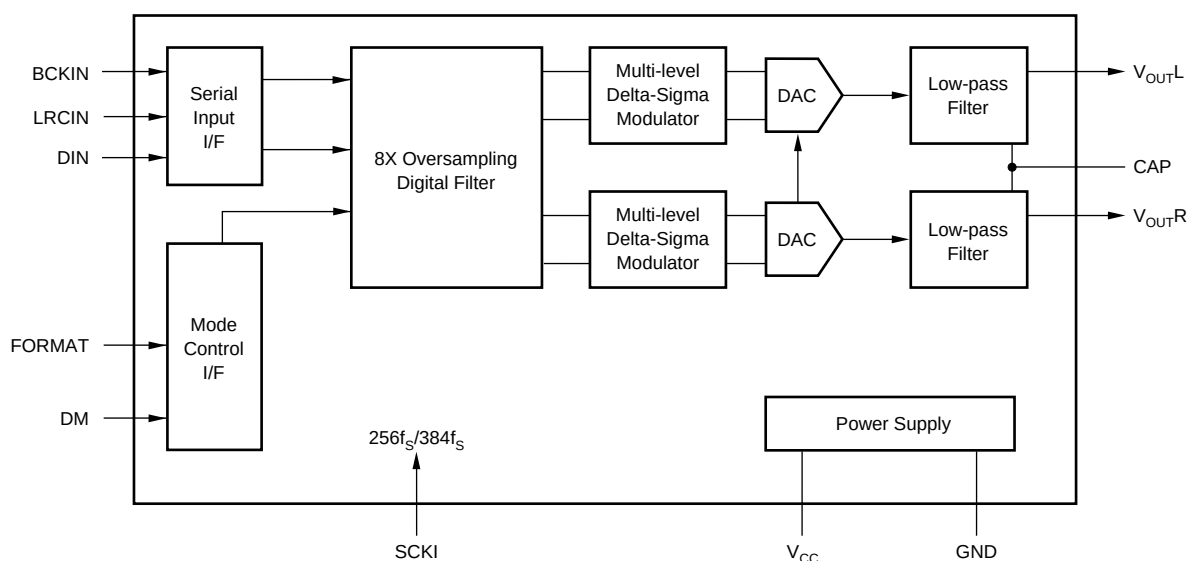
- **COMPLETE STEREO DAC:** Includes Digital Filter and Output Amp
- **DYNAMIC RANGE:** 95dB
- **MULTIPLE SAMPLING FREQUENCIES:** Up to 96kHz
- **8x OVERSAMPLING DIGITAL FILTER**
- **SYSTEM CLOCK:**  $256f_s/384f_s$
- **24-BIT I<sup>2</sup>S DATA INPUT FORMAT**
- **SMALL 14-PIN SOIC PACKAGE**

### DESCRIPTION

The PCM1744 is a complete low cost stereo audio digital-to-analog converter (DAC), operating off of a  $256f_s$  or  $384f_s$  system clock. The DAC contains a 3rd-order  $\Delta\Sigma$  modulator, a digital interpolation filter, and an analog output amplifier. The PCM1744 accepts 24-bit input data in a I<sup>2</sup>S format.

The digital filter performs an 8x interpolation function and includes de-emphasis at 44.1kHz. The PCM1744 can accept digital audio sampling frequencies from 16kHz to 96kHz, always at 8X oversampling.

The PCM1744 is ideal for low-cost, CD-quality consumer audio applications.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111  
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# SPECIFICATIONS

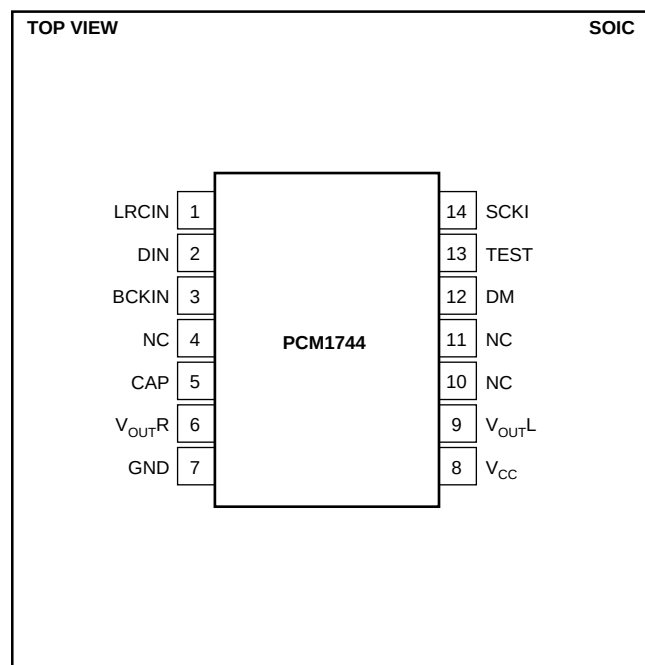
All specifications at +25°C, +V<sub>CC</sub> = +5V, f<sub>s</sub> = 44.1kHz, and 18-bit input data, SYSCLK = 384f<sub>s</sub>, unless otherwise noted.

| PARAMETER                                                                                                                                                                                  | CONDITIONS                                             | PCM1744                |                                              |                      | UNITS                                               |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------|------------------------|----------------------------------------------|----------------------|-----------------------------------------------------|
|                                                                                                                                                                                            |                                                        | MIN                    | TYP                                          | MAX                  |                                                     |
| <b>RESOLUTION</b>                                                                                                                                                                          |                                                        | 24                     |                                              |                      | Bits                                                |
| <b>DATA FORMAT</b><br>Audio Data Interface Format<br>Audio Data Format<br>Sampling Frequency (f <sub>s</sub> )<br>Internal System Clock Frequency                                          |                                                        |                        | I <sup>2</sup> S<br>Two's Binary Complement  |                      |                                                     |
|                                                                                                                                                                                            |                                                        | 16                     | 256f <sub>s</sub> /384f <sub>s</sub>         | 96                   | kHz                                                 |
| <b>DIGITAL INPUT/OUTPUT</b><br>Logic Level<br>Input Logic Level<br>V <sub>IH</sub> <sup>(1)</sup><br>V <sub>IL</sub> <sup>(1)</sup><br>Input Logic Current: I <sub>IN</sub> <sup>(1)</sup> |                                                        | 2.0                    | TTL                                          | 0.8<br>±0.8          | VDC<br>VDC<br>μA                                    |
| <b>DYNAMIC PERFORMANCE</b> <sup>(2)</sup><br>THD+N at FS (0dB)<br>THD+N at -60dB<br>Dynamic Range<br>Signal-to-Noise Ratio<br>Channel Separation                                           | f = 991kHz<br><br>EIAJ, A-weighted<br>EIAJ, A-weighted | <br><br>90<br>90<br>88 | <br><br>-83<br>-32<br>95<br>97<br>95         | <br><br>-79          | <br><br>dB<br>dB<br>dB<br>dB<br>dB                  |
| <b>DC ACCURACY</b><br>Gain Error<br>Gain Mismatch, Channel-to-Channel<br>Bipolar Zero Error                                                                                                | V <sub>OUT</sub> = V <sub>CC</sub> /2 at BPZ           |                        | ±1.0<br>±1.0<br>±20                          | ±10.0<br>±5.0<br>±50 | % of FSR<br>% of FSR<br>mV                          |
| <b>ANALOG OUTPUT</b><br>Output Voltage<br>Center Voltage<br>Load Impedance                                                                                                                 | Full Scale (0dB)<br><br>AC Load                        | <br><br>10             | 0.62 × V <sub>CC</sub><br>V <sub>CC</sub> /2 |                      | Vp-p<br>VDC<br>kΩ                                   |
| <b>DIGITAL FILTER PERFORMANCE</b><br>Passband<br>Stopband<br>Passband Ripple<br>Stopband Attenuation<br>Delay Time                                                                         |                                                        | 0.555<br><br>-35       | <br><br>11.125/f <sub>s</sub>                | 0.445<br><br>±0.17   | f <sub>s</sub><br>f <sub>s</sub><br>dB<br>dB<br>sec |
| <b>INTERNAL ANALOG FILTER</b><br>-3dB Bandwidth<br>Passband Response                                                                                                                       | f = 20kHz                                              |                        | 100<br>-0.16                                 |                      | kHz<br>dB                                           |
| <b>POWER SUPPLY REQUIREMENTS</b><br>Voltage Range<br>Supply Current<br>Power Dissipation                                                                                                   |                                                        | 4.5                    | 5<br>13<br>65                                | 5.5<br>18<br>90      | VDC<br>mA<br>mW                                     |
| <b>TEMPERATURE RANGE</b><br>Operation<br>Storage                                                                                                                                           |                                                        | -25<br>-55             |                                              | +85<br>+125          | °C<br>°C                                            |

NOTES: (1) Pins 1, 2, 3, 12, 13, 14: LRCIN, DIN, BCKIN, DM, FORMAT, SCKI. (2) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average-Mode.

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## PIN CONFIGURATION



## PIN ASSIGNMENTS

| PIN               | NAME               | I/O | FUNCTION                                                            |
|-------------------|--------------------|-----|---------------------------------------------------------------------|
| 1 <sup>(1)</sup>  | LRCIN              | IN  | Sample Rate Clock Input                                             |
| 2 <sup>(1)</sup>  | DIN                | IN  | Audio Data Input                                                    |
| 3 <sup>(1)</sup>  | BCKIN              | IN  | Bit Clock Input for Audio Data.                                     |
| 4                 | NC                 | —   | No Connection                                                       |
| 5                 | CAP                | —   | Common Pin of Analog Output Amp                                     |
| 6                 | V <sub>OUT</sub> R | OUT | Right-Channel Analog Output                                         |
| 7                 | GND                | —   | Ground                                                              |
| 8                 | V <sub>CC</sub>    | —   | Power Supply                                                        |
| 9                 | V <sub>OUT</sub> L | OUT | Left-Channel Analog Output                                          |
| 10                | NC                 | —   | No Connection                                                       |
| 11                | NC                 | —   | No Connection                                                       |
| 12 <sup>(2)</sup> | DM                 | IN  | De-Emphasis Control<br>HIGH: De-emphasis ON<br>LOW: De-emphasis OFF |
| 13 <sup>(2)</sup> | TEST               | —   | Test Pin. Must be left open.                                        |
| 14 <sup>(1)</sup> | SCKI               | IN  | System Clock Input (256f <sub>S</sub> or 384f <sub>S</sub> )        |

NOTE: (1) Schmitt-Trigger input. (2) Schmitt-Trigger input with internal pull-up.

## ABSOLUTE MAXIMUM RATINGS

|                                                       |                                   |
|-------------------------------------------------------|-----------------------------------|
| Power Supply Voltage .....                            | +6.5V                             |
| +V <sub>CC</sub> to +V <sub>DD</sub> Difference ..... | ±0.1V                             |
| Input Logic Voltage .....                             | –0.3V to (V <sub>DD</sub> + 0.3V) |
| Power Dissipation .....                               | 290mW                             |
| Operating Temperature Range .....                     | –25°C to +85°C                    |
| Storage Temperature .....                             | –55°C to +125°C                   |
| Lead Temperature (soldering, 5s) .....                | +260°C                            |
| Thermal Resistance, θ <sub>JA</sub> .....             | +90°C/W                           |



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

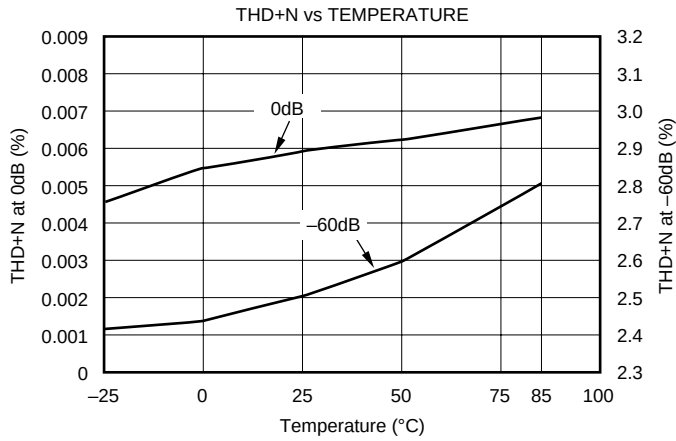
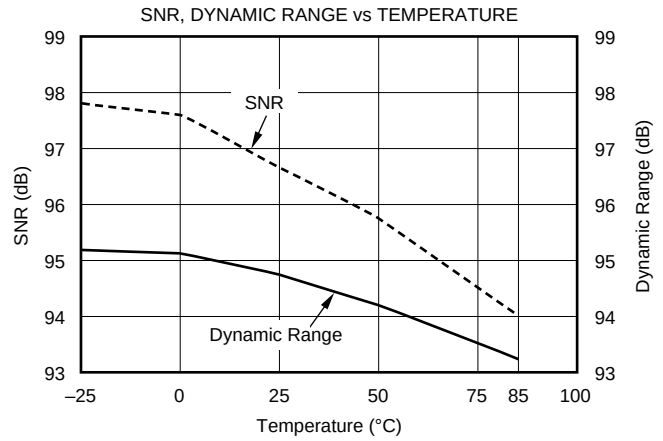
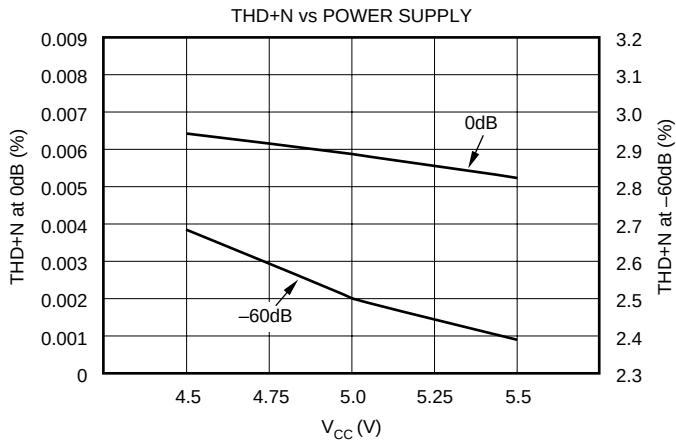
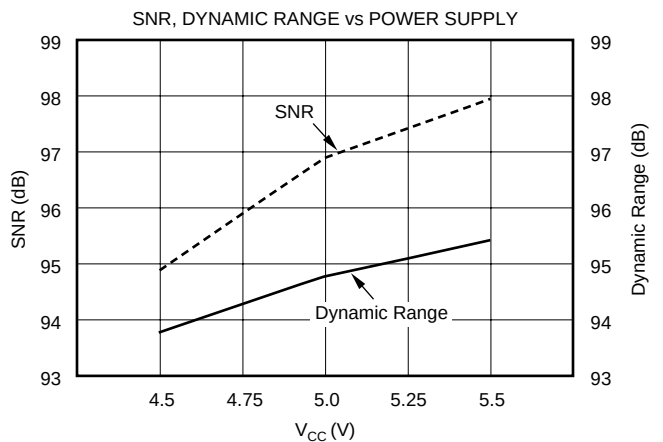
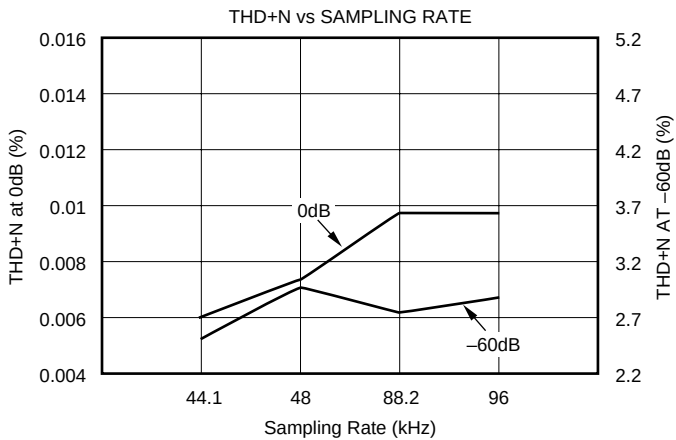
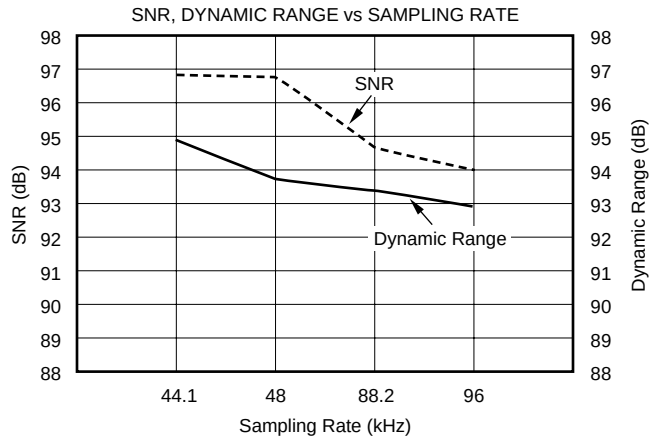
| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER <sup>(1)</sup> | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING      | ORDERING NUMBER <sup>(2)</sup> | TRANSPORT MEDIA        |
|---------|---------|---------------------------------------|-----------------------------|----------------------|--------------------------------|------------------------|
| PCM1744 | SO-14   | 235                                   | –25°C to +85°C              | PCM1744U<br>PCM1744U | PCM1744U<br>PCM1744U/2K        | Rails<br>Tape and Reel |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book, or visit the Burr-Brown web site at [www.burr-brown.com](http://www.burr-brown.com). (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "PCM1744U/2K" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = +5\text{V}$ ,  $f_S = 44.1\text{kHz}$ ,  $\text{SYSCLK} = 256f_S$ , unless otherwise noted.

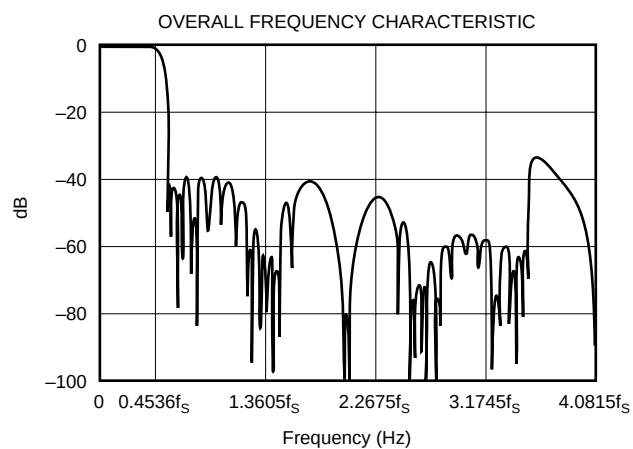
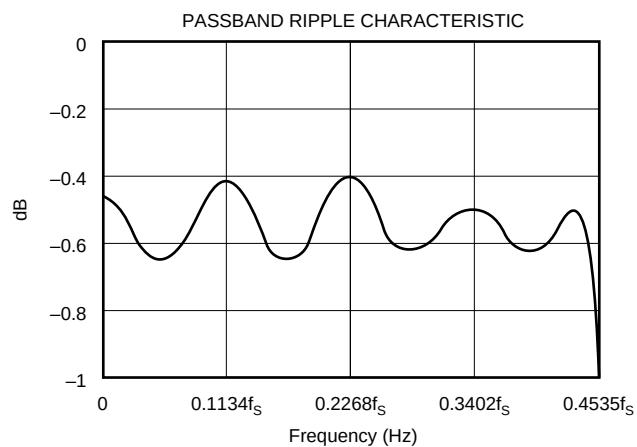
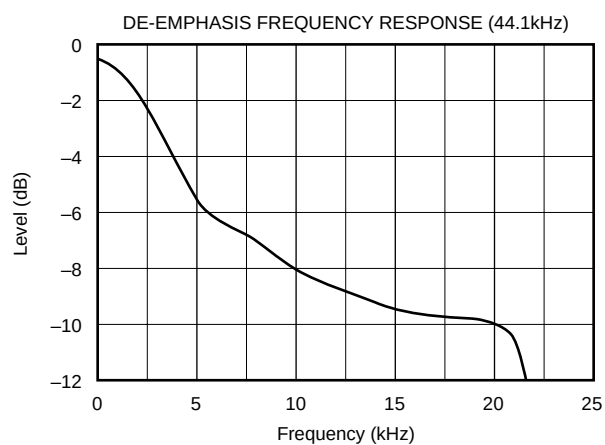
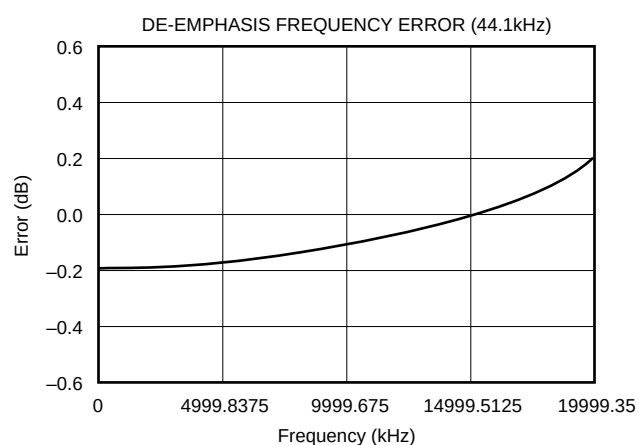
## DYNAMIC PERFORMANCE



# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $+V_{CC} = +V_{DD} = +5\text{V}$ ,  $f_S = 44.1\text{kHz}$ , and 18-bit input data,  $\text{SYSCLK} = 384f_S$ , unless otherwise noted.

## DIGITAL FILTER



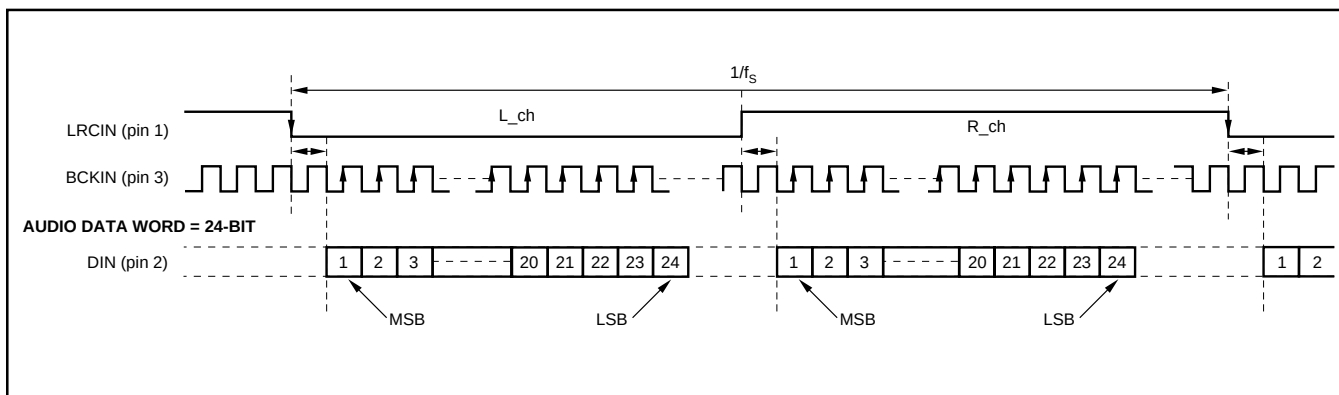


FIGURE 1. I²S Data Input Timing.

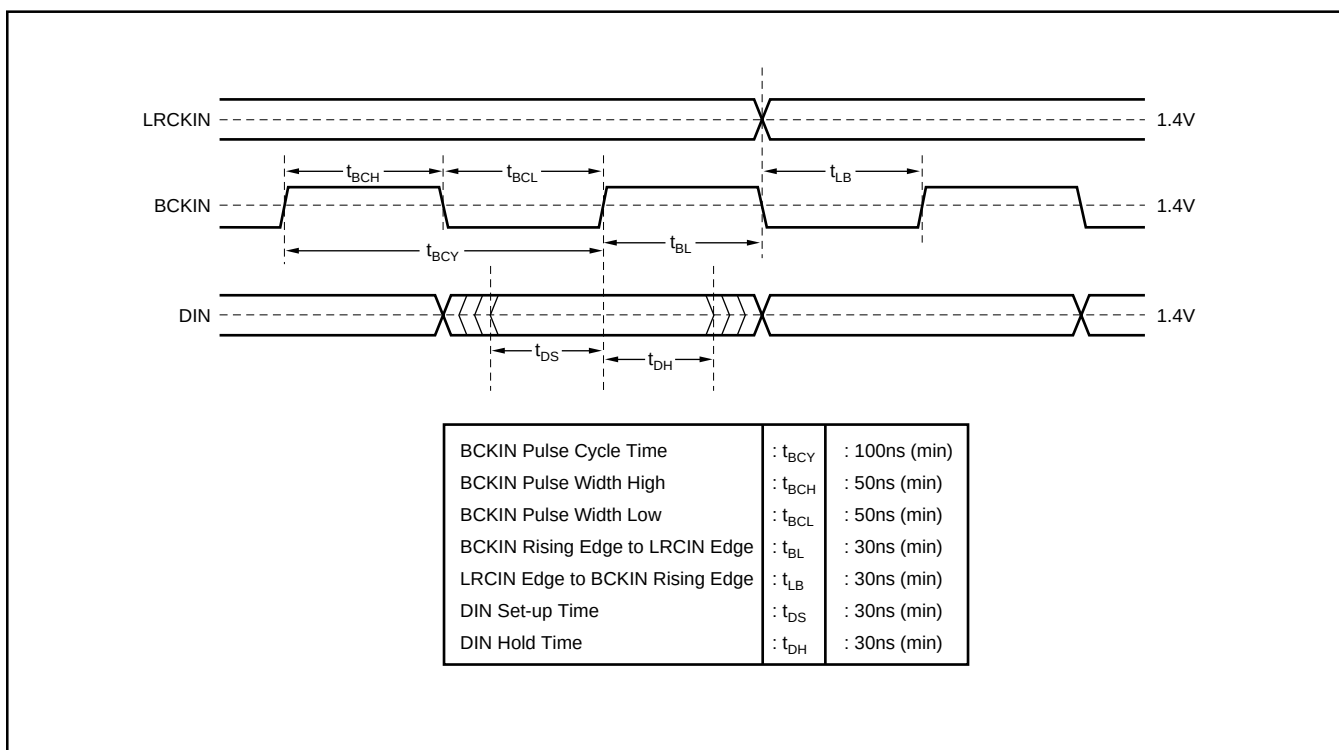


FIGURE 2. Audio Data Input Timing.

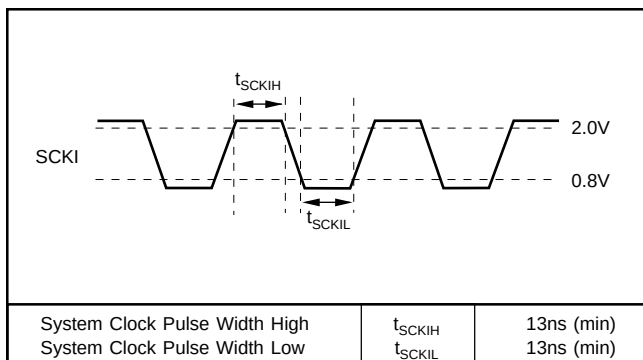


FIGURE 3. System Clock Timing Requirements.

## SYSTEM CLOCK

The system clock for PCM1744 must be either  $256f_s$  or  $384f_s$ , where  $f_s$  is the audio sampling frequency (LRCIN), typically 32kHz, 44.1kHz, 48kHz, 88.2kHz or 96kHz. The system clock is used to operate the digital filter and the noise shaper. The system clock input (SCKI) is at pin 14. Timing conditions for SCKI are shown in Figure 3.

PCM1744 has a system clock detection circuit which automatically detects the frequency, either  $256f_s$  or  $384f_s$ . The system clock should be synchronized with LRCIN (pin 1), but PCM1744 can compensate for phase differences. If the phase difference between LRCIN and system clock is greater

than  $\pm 6$  bit clocks (BCKIN), the synchronization is performed automatically. The analog outputs are forced to a bipolar zero state ( $V_{CC}/2$ ) during the synchronization function. Table I shows the typical system clock frequency inputs for the PCM1744.

| SAMPLING RATE (LRCIN) | SYSTEM CLOCK FREQUENCY (MHz) |          |
|-----------------------|------------------------------|----------|
|                       | $256f_s$                     | $384f_s$ |
| 32kHz                 | 8.192                        | 12.288   |
| 44.1kHz               | 11.2896                      | 16.9340  |
| 48kHz                 | 12.288                       | 18.432   |
| 88.2kHz               | 22.5792                      | 33.868   |
| 96kHz                 | 24.576                       | 36.864   |

TABLE I. System Clock Frequencies vs Sampling Rate.

## TYPICAL CONNECTION DIAGRAM

Figure 4 illustrates the typical connection diagram for PCM1744 used in a stand-alone application.

## INPUT DATA FORMAT

PCM1744 can accept input data a 24-bit I<sup>2</sup>S format, as shown in Figure 1.

## RESET

PCM1744 has an internal power-on reset circuit. The internal power-on reset initializes (resets) when the supply voltage  $V_{CC} > 2.2V$  (typ). The power-on reset has an initialization period equal to 1024 system clock periods after  $V_{CC} > 2.2V$ . During the initialization period, the outputs of the DAC are invalid, and the analog outputs are forced to  $V_{CC}/2$ . Figure 5 illustrates the power-on reset and reset-pin reset timing.

## DE-EMPHASIS CONTROL

Pin 12 (DM) enables PCM1744's de-emphasis function. De-emphasis operates only at 44.1kHz.

| DM |                          |
|----|--------------------------|
| 0  | De-emphasis OFF          |
| 1  | De-emphasis ON (44.1kHz) |

TABLE II. De-emphasis Control Selection.

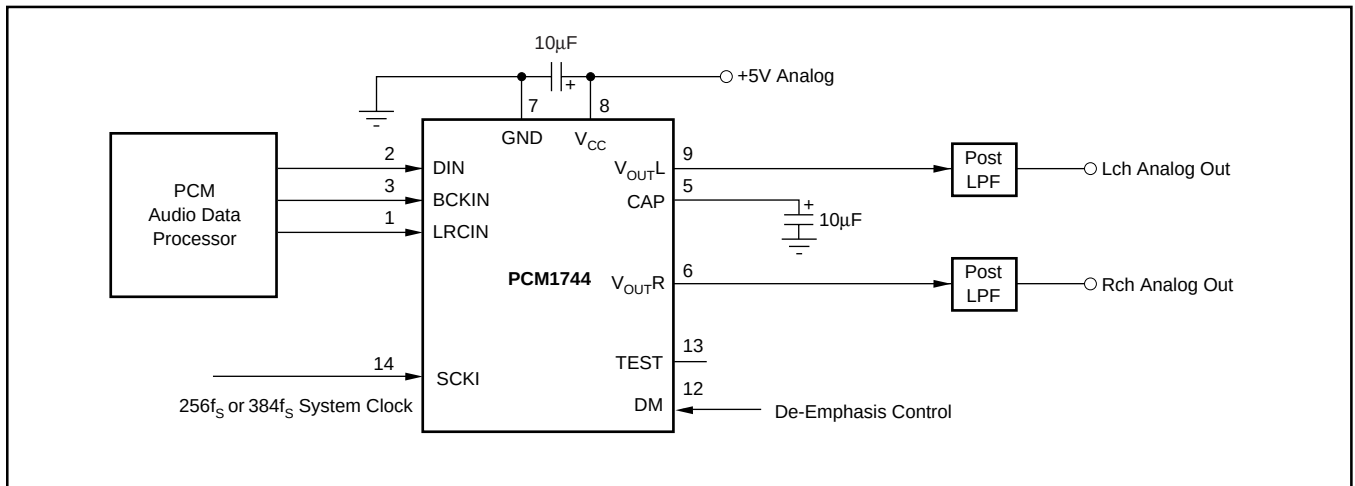


FIGURE 4. Typical Connection Diagram.

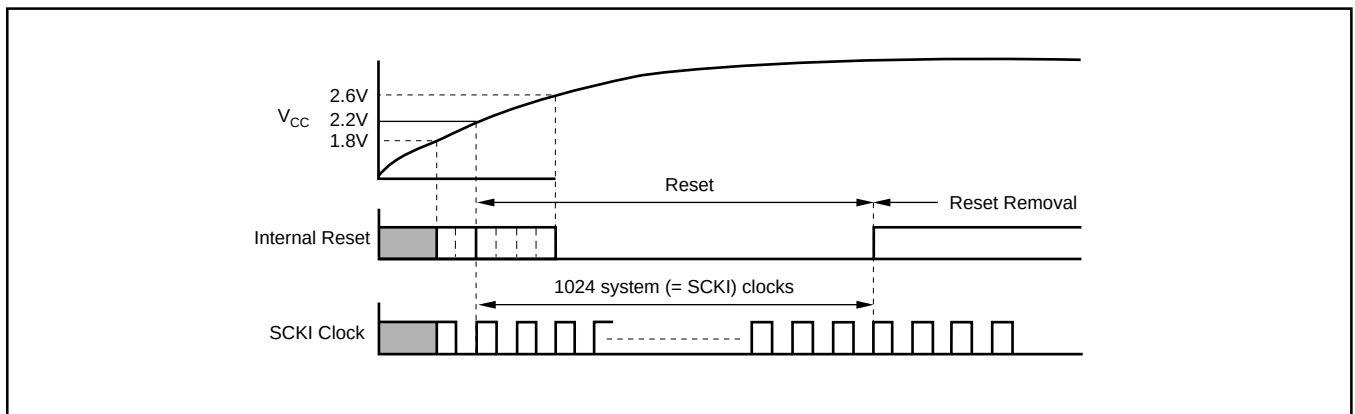


FIGURE 5. Internal Power-On Reset Timing.

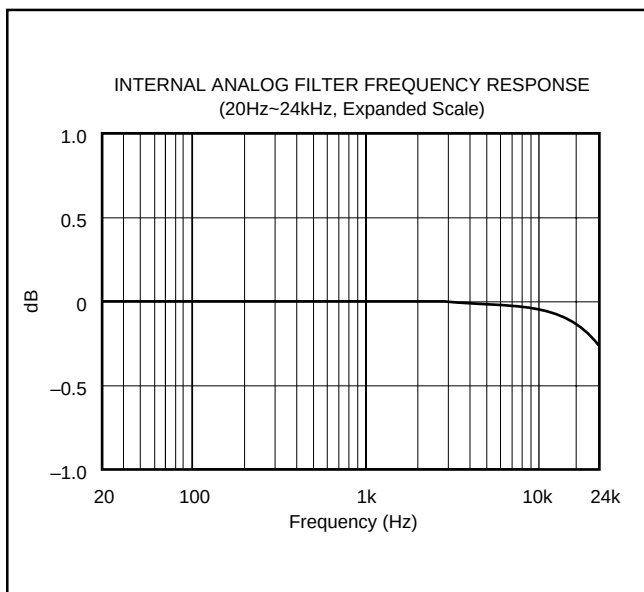


FIGURE 6. Low-Pass Filter Frequency Response.

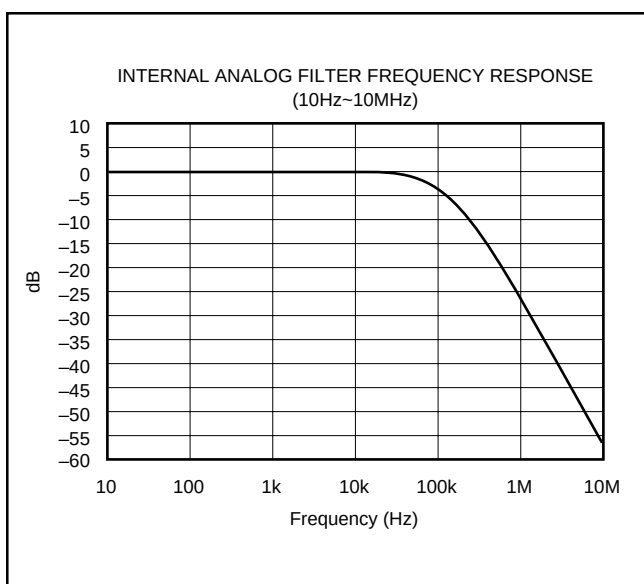


FIGURE 7. Low-Pass Filter Wideband Frequency Response.

## APPLICATION CONSIDERATIONS

### DELAY TIME

There is a finite delay time in delta-sigma converters. In A/D converters, this is commonly referred to as latency. For a delta-sigma D/A converter, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of PCM1744:

$$T_D = 11.125 \times 1/f_s$$

$$\text{For } f_s = 44.1\text{kHz}, T_D = 11.125/44.1\text{kHz} = 251.4\mu\text{s}$$

Applications using data from a disc or tape source, such as CD audio, CD-Interactive, Video CD, DAT, Minidisc, etc., generally are not affected by delay time. For some professional applications such as broadcast audio for studios, it is important for total delay time to be less than 2ms.

### OUTPUT FILTERING

For testing purposes all dynamic tests are done on the PCM1744 using a 20kHz low-pass filter. This filter limits the measured bandwidth for THD+N, etc. to 20kHz. Failure to use such a filter will result in higher THD+N and lower SNR and dynamic range readings than are found in the specifications. The low-pass filter removes out-of-band noise. Although it is not audible, it may affect dynamic specification numbers.

The performance of the internal low pass filter from DC to 24kHz is shown in Figure 6. The higher frequency roll-off of the filter is shown in Figure 7. If the user's application has the PCM1744 driving a wideband amplifier, it is recommended to use an external low-pass filter. A simple 3rd-order filter is shown in Figure 8. For some applications, a passive RC filter or 2nd-order filter may be adequate.

### BYPASSING POWER SUPPLIES

The power supplies should be bypassed as close as possible to the unit. It is also recommended to include a 0.1μF ceramic capacitor in parallel with the 10μF tantalum bypass capacitor.

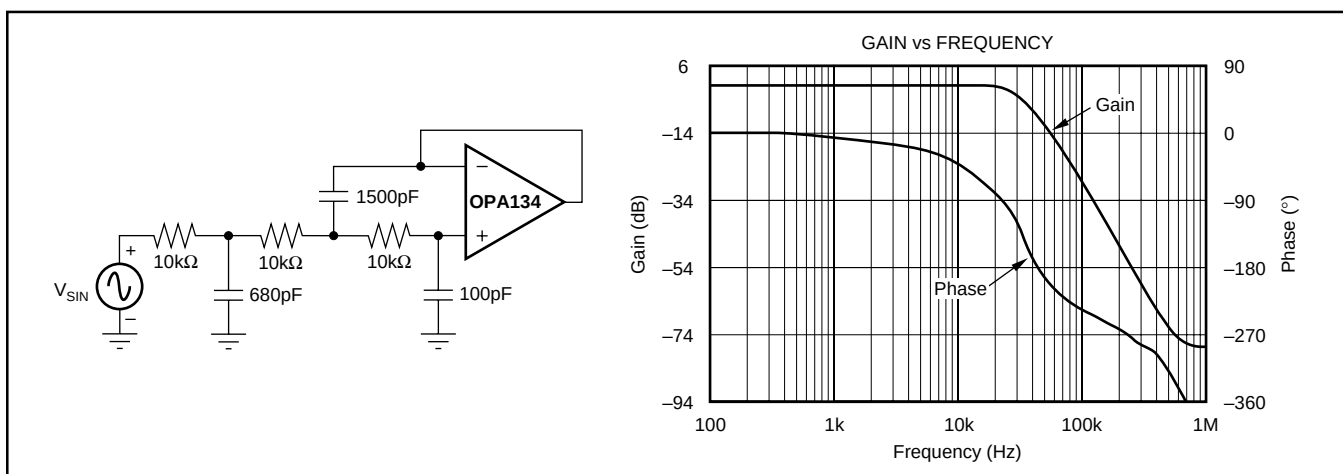


FIGURE 8. 3rd-Order LPF.

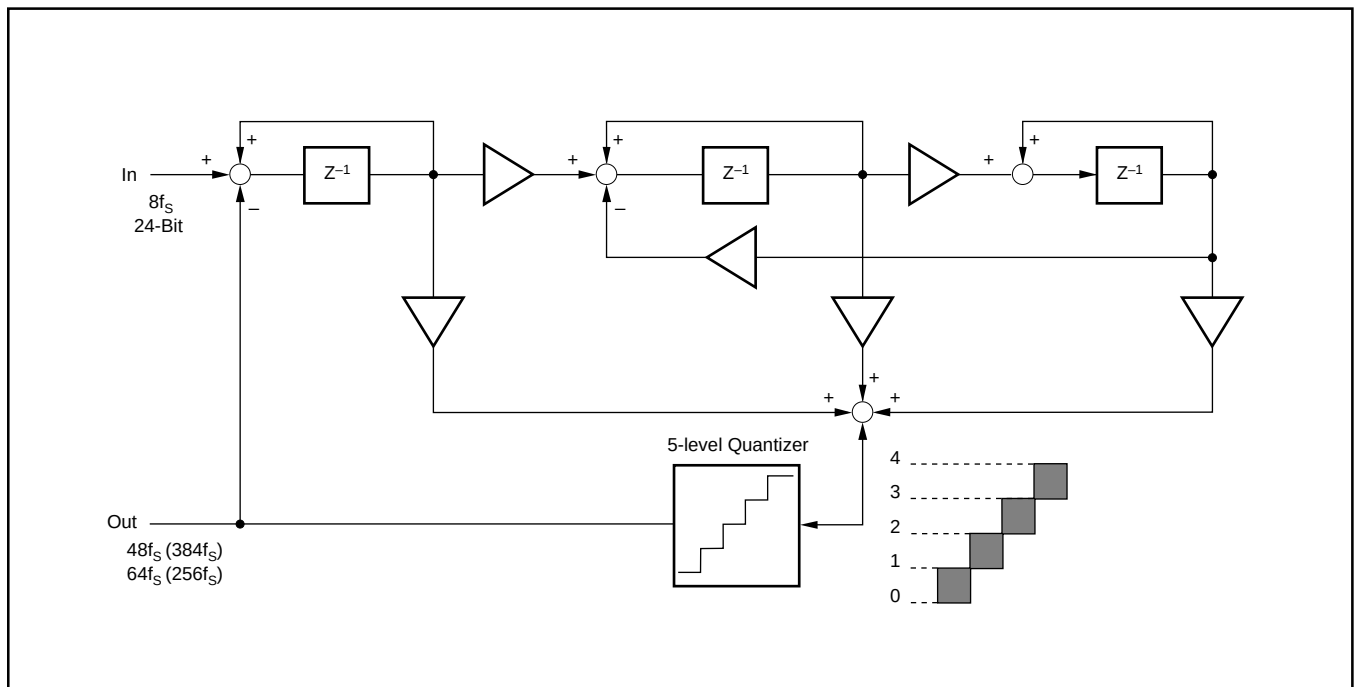


FIGURE 9. 5-Level  $\Delta\Sigma$  Modulator Block Diagram.

## THEORY OF OPERATION

The delta-sigma section of PCM1744 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format. A block diagram of the 5-level delta-sigma modulator is shown in Figure 9. This 5-level delta-sigma modulator has the advantage of stability and clock jitter over the typical one-bit (2-level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8x interpolation filter is  $96f_s$  for a  $384f_s$  system clock, and  $64f_s$  for a  $256f_s$  system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 10.

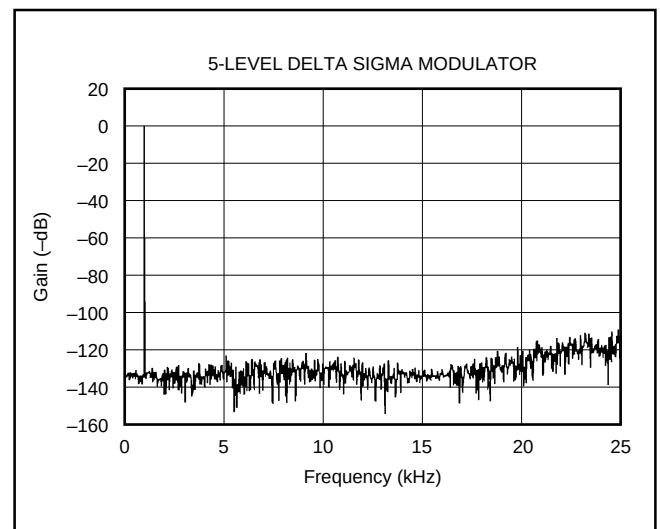


FIGURE 10. Quantization Noise Spectrum.

## PACKAGING INFORMATION

| Orderable part number    | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">PCM1744U</a> | Last Time Buy | Production           | SOIC (D)   14  | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -            | PCM1744U            |
| PCM1744U.B               | Last Time Buy | Production           | SOIC (D)   14  | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | See PCM1744U | PCM1744U            |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

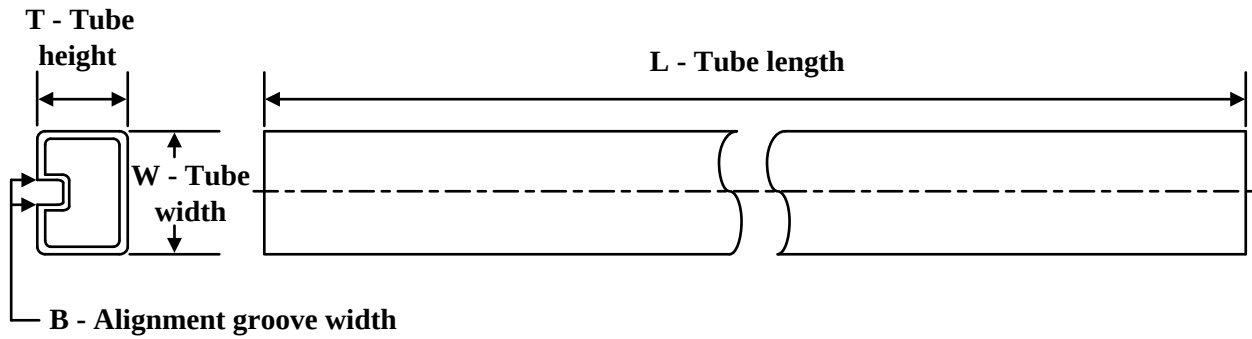
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TUBE



\*All dimensions are nominal

| Device     | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| PCM1744U   | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| PCM1744U.B | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |

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