

REF19xx Low-Drift, Low-Power, Dual-Output, V_{REF} and $V_{REF} / 2$ Voltage References

1 Features

- Two outputs, V_{REF} and $V_{REF} / 2$, for convenient use in single-supply systems
- Excellent temperature drift performance:
 - 25ppm/°C (maximum) from –40°C to 125°C
- High initial accuracy: $\pm 0.1\%$ (maximum)
- V_{REF} and V_{BIAS} tracking overtemperature:
 - 6ppm/°C (maximum) from –40°C to 85°C
 - 7ppm/°C (maximum) from –40°C to 125°C
- Microsize package: SOT23-5
- Low dropout voltage: 10mV
- High output current: $\pm 20\text{mA}$
- Low quiescent current: 360 μA
- Line regulation: 3ppm/V
- Load regulation: 8ppm/mA

2 Applications

- Digital signal processing:
 - Power inverters
 - Motor controls
- Current sensing
- Industrial process controls
- Medical equipment
- Data acquisition systems
- Single-supply systems

3 Description

Applications with only a positive supply voltage often require an additional stable voltage in the middle of the analog-to-digital converter (ADC) input range to

bias input bipolar signals. The REF19xx provides a reference voltage (V_{REF}) for the ADC and a second highly-accurate voltage (V_{BIAS}) that can be used to bias the input bipolar signals.

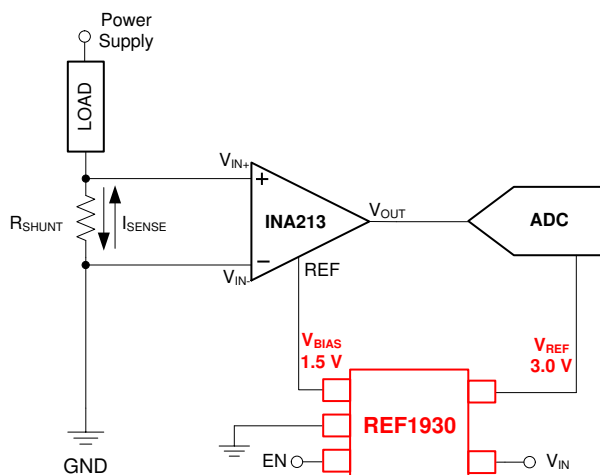
The REF19xx offers excellent temperature drift (25ppm/°C, maximum) and initial accuracy (0.1%) on both the V_{REF} and V_{BIAS} outputs while operating at a quiescent current less than 430 μA . In addition, the V_{REF} and V_{BIAS} outputs track each other with a precision of 6ppm/°C (maximum) across the temperature range from –40°C to 85°C. All these features increase the precision of the signal chain and decrease board space, while reducing the cost of the system as compared to a discrete design. Extremely low dropout voltage of only 10mV allows operation from very low input voltages, which can be very useful in battery-operated systems.

Both the V_{REF} and V_{BIAS} voltages have the same excellent specifications and can sink and source current equally well. Good long-term stability and low-noise levels make these devices designed for high-precision industrial applications.

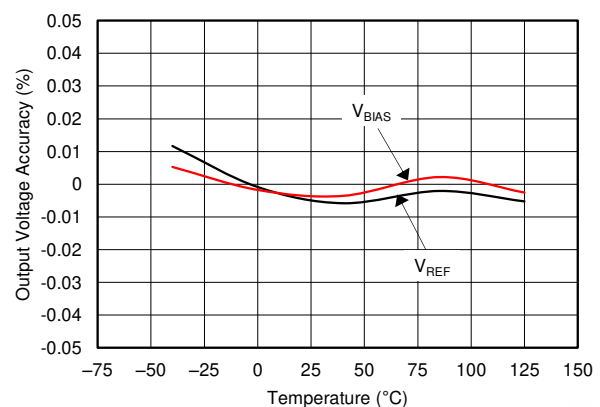
Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
REF19xx	DDC (SOT-23-THN, 5)	2.9mm × 2.8mm

- (1) For more information, see [Section 12](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



Application Example



V_{REF} and V_{BIAS} vs Temperature



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4 Device Comparison Table

PRODUCT	V_{REF}	V_{BIAS}
REF1925	2.5V	1.25V
REF1930	3.0V	1.5V
REF1933	3.3V	1.65V
REF1941	4.096V	2.048V

5 Pin Configuration and Functions

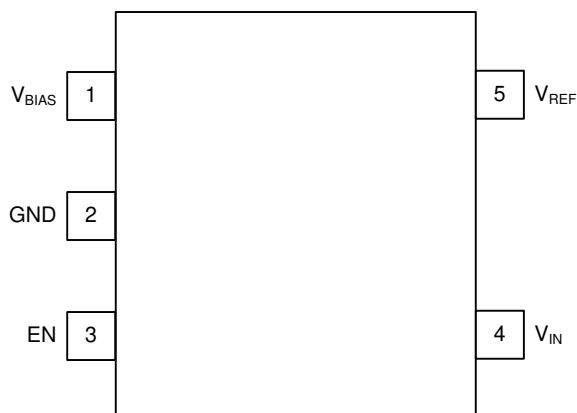


Figure 5-1. DDC Package, SOT-23-THN-5 (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	V_{BIAS}	Output	Bias voltage output ($V_{REF} / 2$)
2	GND	—	Ground
3	EN	Input	Enable ($EN \geq V_{IN} - 0.7V$, device enabled)
4	V_{IN}	Input	Input supply voltage
5	V_{REF}	Output	Reference voltage output (V_{REF})

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	V _{IN}	–0.3	6	V
	EN	–0.3	V _{IN} + 0.3	
Temperature	Operating	–55	150	°C
	Junction, T _J		150	
	Storage, T _{stg}	–65	170	

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾		±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾		±1500	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Supply input voltage range (I _L = 0mA, T _A = 25°C)	V _{REF} + 0.02 ⁽¹⁾		5.5	V

- (1) See [Figure 6-24](#) in the [Typical Characteristics](#) section for the minimum input voltage at different load currents and temperature.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		REF19xx	UNIT
		DDC (SOT-23-THN)	
		5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	193.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	40.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	34.5	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ _{JB}	Junction-to-board characterization parameter	34.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

6.5 Electrical Characteristics

At $T_A = 25^\circ\text{C}$, $I_L = 0\text{mA}$, and $V_{IN} = 5\text{V}$, unless otherwise noted. Both V_{REF} and V_{BIAS} have the same specifications.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT							
Output voltage accuracy				−0.1%		0.1%	
Output voltage temperature coefficient ⁽¹⁾		−40°C ≤ T _A ≤ 125°C		±10		±25	ppm/°C
V _{REF} and V _{BIAS} tracking over temperature ⁽²⁾		−40°C ≤ T _A ≤ 85°C		±1.5		±6	ppm/°C
		−40°C ≤ T _A ≤ 125°C		±2		±7	
LINE AND LOAD REGULATION							
ΔV _{O(ΔVI)} Line regulation		V _{REF} + 0.02V ≤ V _{IN} ≤ 5.5V		3		35	ppm/V
ΔV _{O(ΔIL)} Load regulation	Sourcing	0mA ≤ I _L ≤ 20mA , V _{REF} + 0.6V ≤ V _{IN} ≤ 5.5V		8		20	ppm/mA
	Sinking	0mA ≤ I _L ≤ −20mA, V _{REF} + 0.02V ≤ V _{IN} ≤ 5.5V		8		20	
POWER SUPPLY							
I _{CC} Supply current	Active mode			360		430	μA
		−40°C ≤ T _A ≤ 125°C				460	
	Shutdown mode			3.3		5	
		−40°C ≤ T _A ≤ 125°C				9	
Enable voltage		Device in shutdown mode (EN = 0)		0		0.7	V
		Device in active mode (EN = 1)		V _{IN} − 0.7		V _{IN}	
Dropout voltage				10		20	mV
		I _L = 20mA				600	
I _{SC} Short-circuit current					50		mA
t _{on} Turn-on time			0.1% settling, C _L = 1 μF		500		μs
NOISE							
Low-frequency noise ⁽³⁾		0.1Hz ≤ f ≤ 10Hz		12			ppm _{PP}
Output voltage noise density		f = 100Hz		0.25			ppm/ $\sqrt{\text{Hz}}$
CAPACITIVE LOAD							
Stable output capacitor range				0		10	μF
HYSTERESIS AND LONG-TERM STABILITY							
Long-term stability		0 to 1000 hours		60			ppm
Output voltage hysteresis ⁽⁴⁾		25°C, −40°C, 125°C, 25°C	Cycle 1	60			ppm
			Cycle 2	35			

(1) Temperature drift is specified according to the box method. See the [Feature Description](#) section for more details.

(2) The V_{REF} and V_{BIAS} tracking over temperature specification is explained in more detail in the [Feature Description](#) section.

(3) The peak-to-peak noise measurement procedure is explained in more detail in the [Noise Performance](#) section.

(4) The thermal hysteresis measurement procedure is explained in more detail in the [Thermal Hysteresis](#) section.

6.6 Typical Characteristics

At $T_A = 25^\circ\text{C}$, $I_L = 0\text{mA}$, $V_{IN} = 5\text{V}$ power supply, $C_L = 0\text{ }\mu\text{F}$, and 2.5V output, unless otherwise noted.

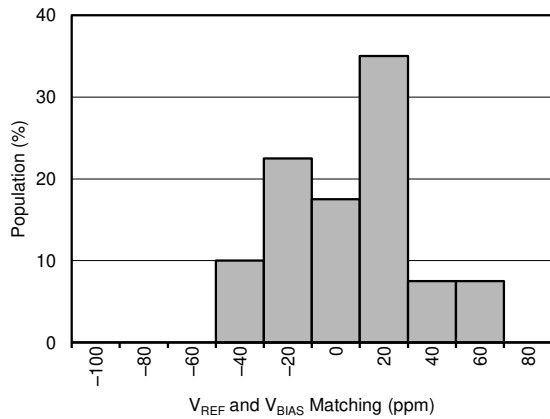
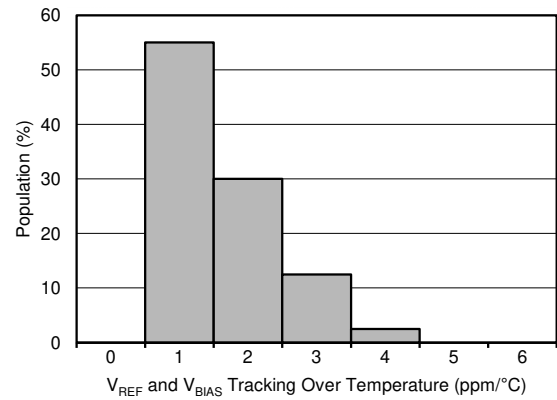
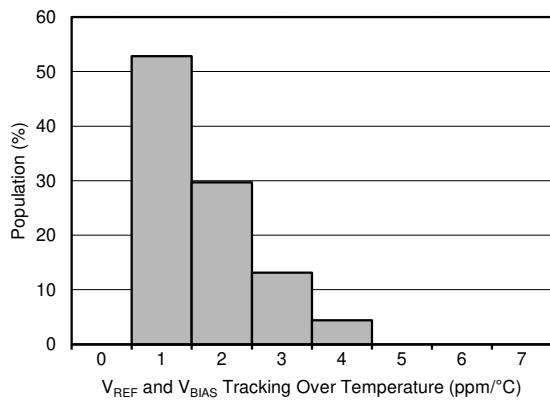


Figure 6-1. $V_{REF} - 2 \times V_{BIAS}$ Distribution



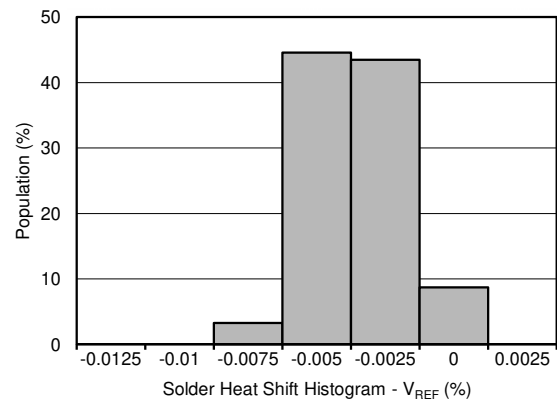
$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$

Figure 6-2. Distribution of $V_{REF} - 2 \times V_{BIAS}$ Drift Tracking Over Temperature



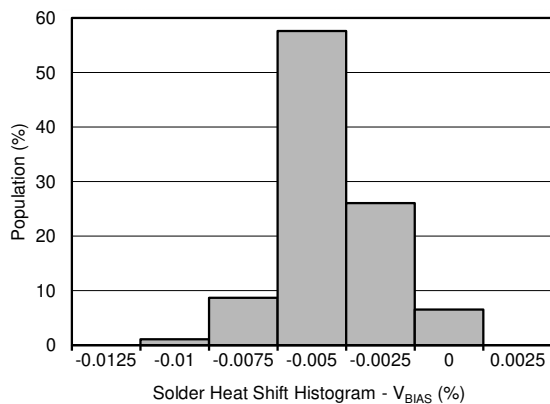
$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$

Figure 6-3. Distribution of $V_{REF} - 2 \times V_{BIAS}$ Drift Tracking Over Temperature



Refer to the [Section 7.1](#) section for more information.

Figure 6-4. Solder Heat Shift Distribution (V_{REF})



Refer to the [Section 7.1](#) section for more information.

Figure 6-5. Solder Heat Shift Distribution (V_{BIAS})

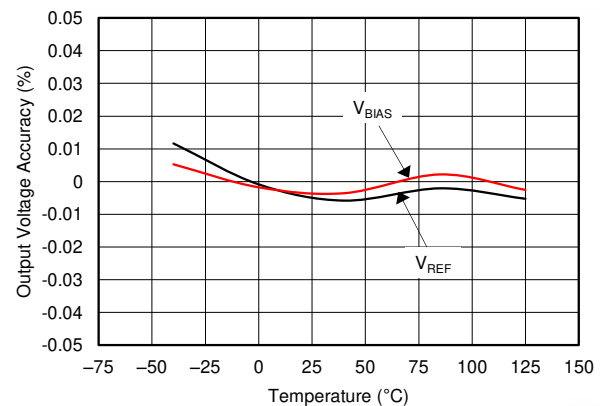


Figure 6-6. Output Voltage Accuracy (V_{REF}) vs Temperature

6.6 Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $I_L = 0\text{mA}$, $V_{IN} = 5\text{V}$ power supply, $C_L = 0\text{ }\mu\text{F}$, and 2.5V output, unless otherwise noted.

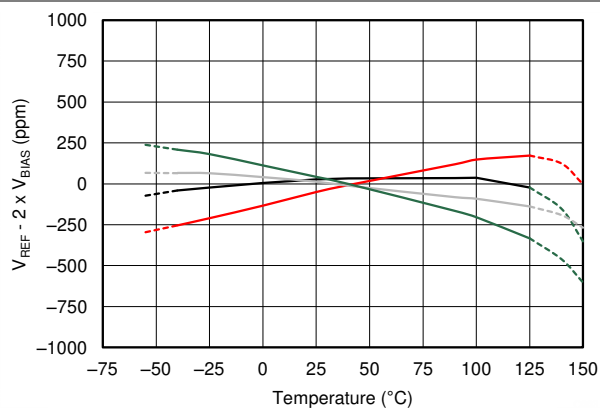


Figure 6-7. $V_{REF} - 2 \times V_{BIAS}$ Tracking vs Temperature

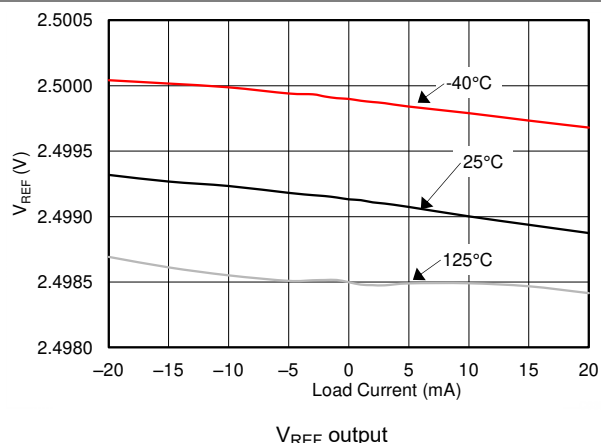


Figure 6-8. Output Voltage Change vs Load Current (V_{REF})

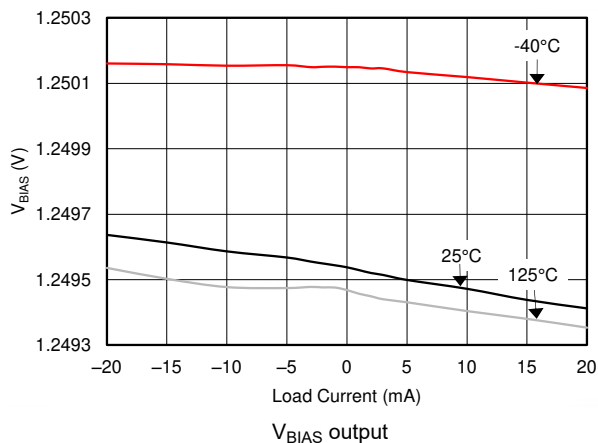


Figure 6-9. Output Voltage Change vs Load Current (V_{BIAS})

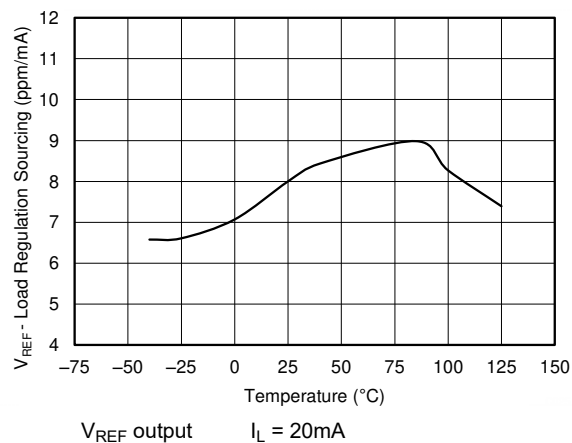


Figure 6-10. Load Regulation Sourcing vs Temperature (V_{REF})

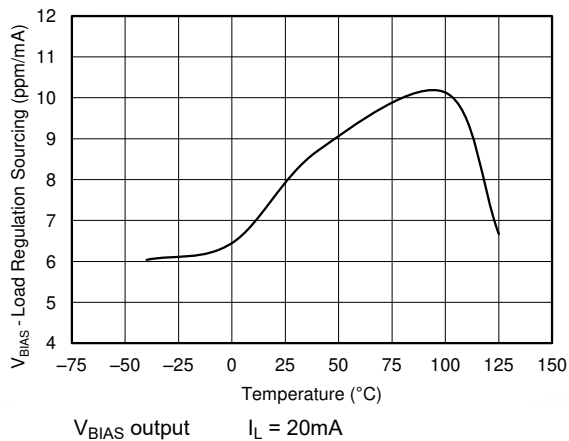


Figure 6-11. Load Regulation Sourcing vs Temperature (V_{BIAS})

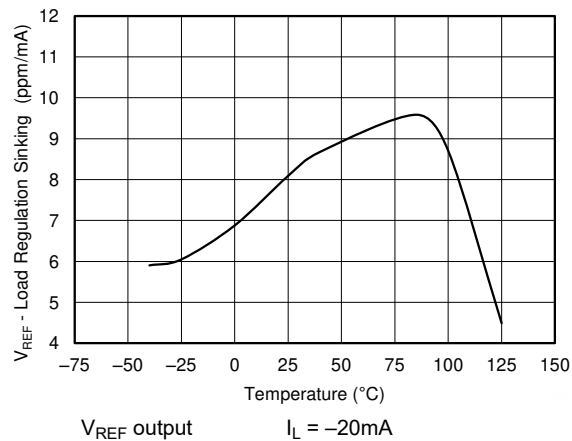


Figure 6-12. Load Regulation Sinking vs Temperature (V_{REF})

6.6 Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $I_L = 0\text{mA}$, $V_{IN} = 5\text{V}$ power supply, $C_L = 0\text{ }\mu\text{F}$, and 2.5V output, unless otherwise noted.

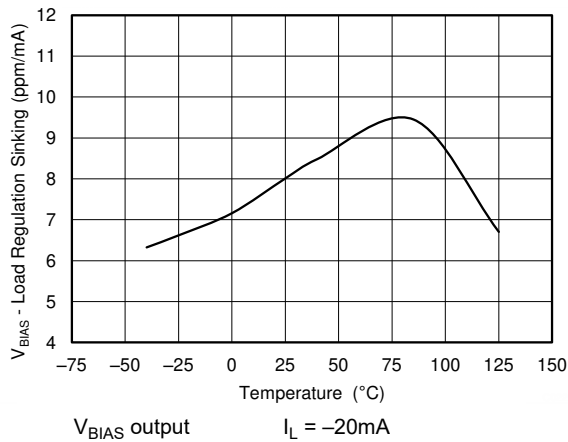


Figure 6-13. Load Regulation Sinking vs Temperature (V_{BIAS})

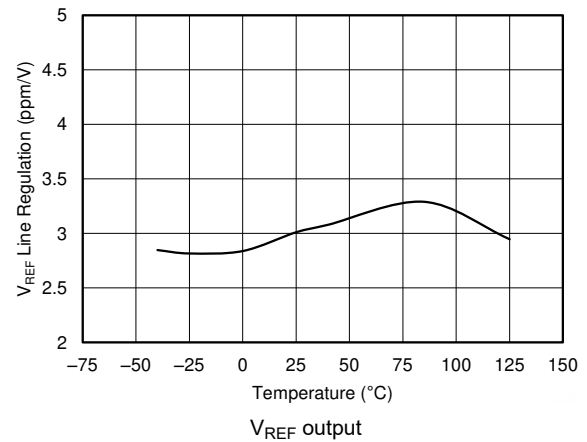


Figure 6-14. Line Regulation vs Temperature (V_{REF})

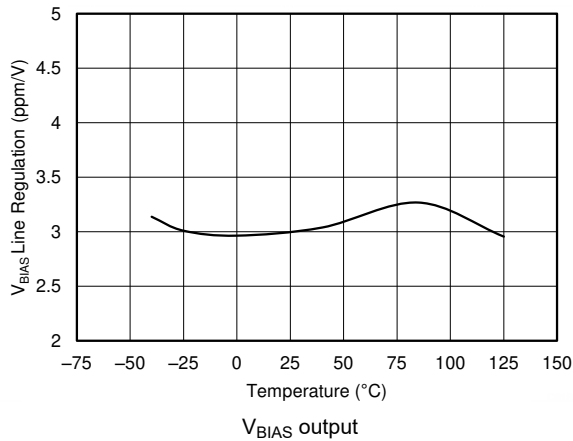


Figure 6-15. Line Regulation vs Temperature (V_{BIAS})

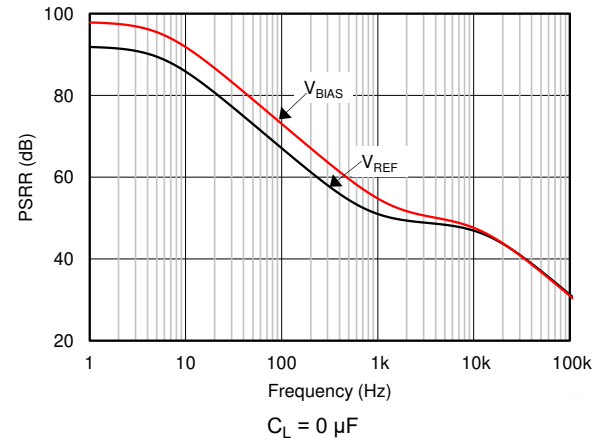


Figure 6-16. Power-Supply Rejection Ratio vs Frequency

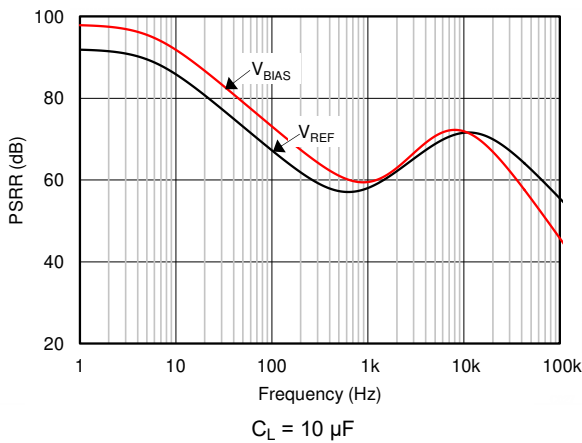


Figure 6-17. Power-Supply Rejection Ratio vs Frequency

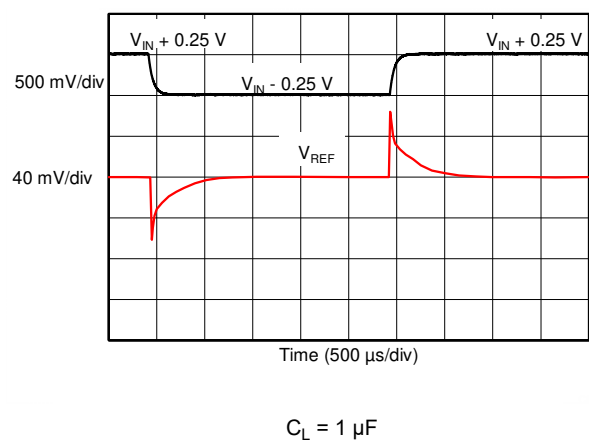
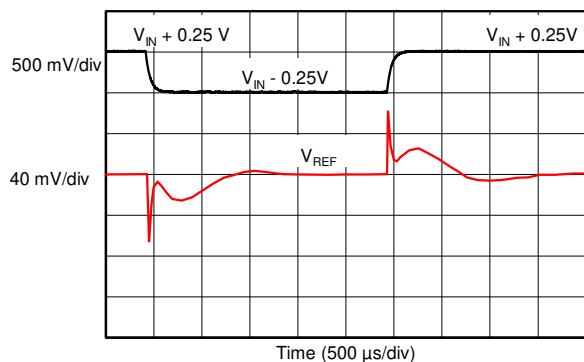


Figure 6-18. Line Transient Response

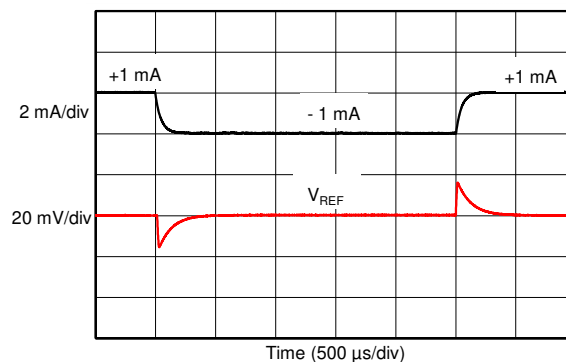
6.6 Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $I_L = 0\text{mA}$, $V_{IN} = 5\text{V}$ power supply, $C_L = 0\text{ }\mu\text{F}$, and 2.5V output, unless otherwise noted.



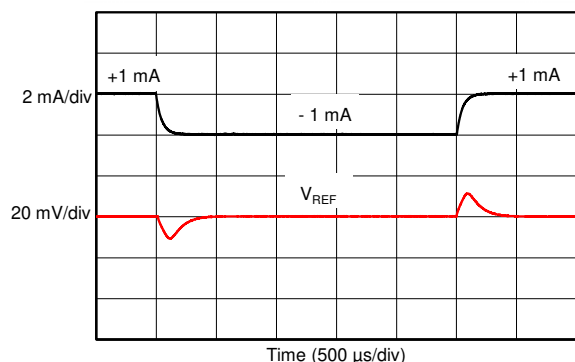
$C_L = 10\text{ }\mu\text{F}$

Figure 6-19. Line Transient Response



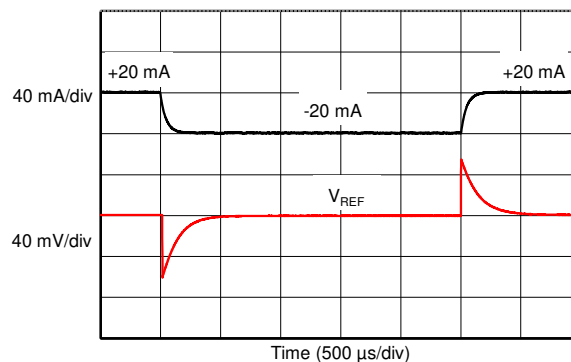
$C_L = 1\text{ }\mu\text{F}$ $I_L = \pm 1\text{mA step}$

Figure 6-20. Load Transient Response



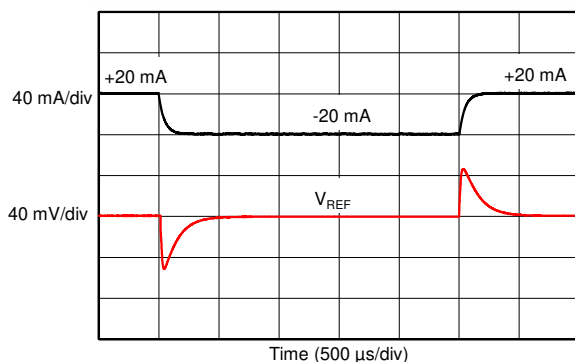
$C_L = 10\text{ }\mu\text{F}$ $I_L = \pm 1\text{mA step}$

Figure 6-21. Load Transient Response



$C_L = 1\text{ }\mu\text{F}$ $I_L = \pm 20\text{mA step}$

Figure 6-22. Load Transient Response



$C_L = 10\text{ }\mu\text{F}$ $I_L = \pm 20\text{mA step}$

Figure 6-23. Load Transient Response

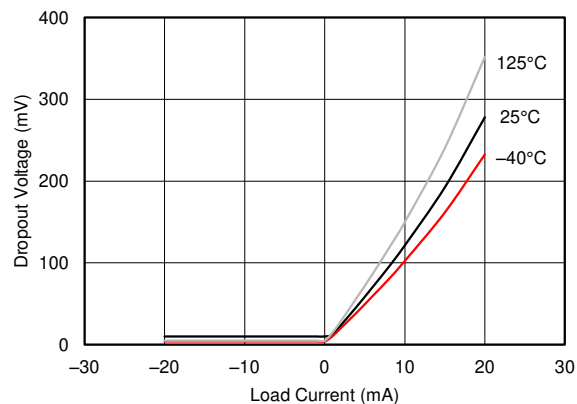
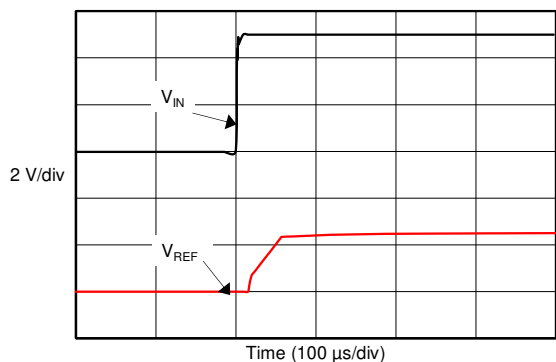


Figure 6-24. Minimum Dropout Voltage vs Load Current

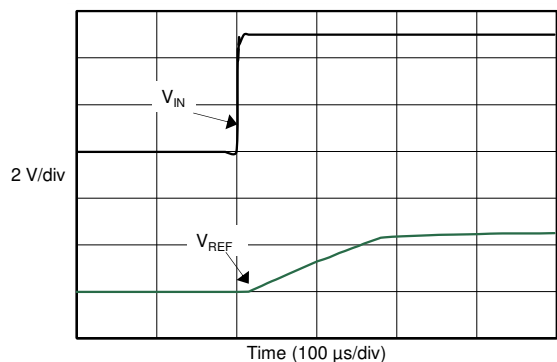
6.6 Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $I_L = 0\text{mA}$, $V_{IN} = 5\text{V}$ power supply, $C_L = 0\text{ }\mu\text{F}$, and 2.5V output, unless otherwise noted.



$C_L = 1\text{ }\mu\text{F}$

Figure 6-25. Turn-On Settling Time



$C_L = 10\text{ }\mu\text{F}$

Figure 6-26. Turn-On Settling Time

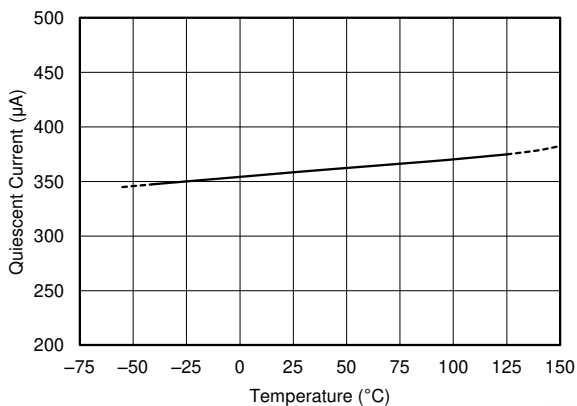


Figure 6-27. Quiescent Current vs Temperature

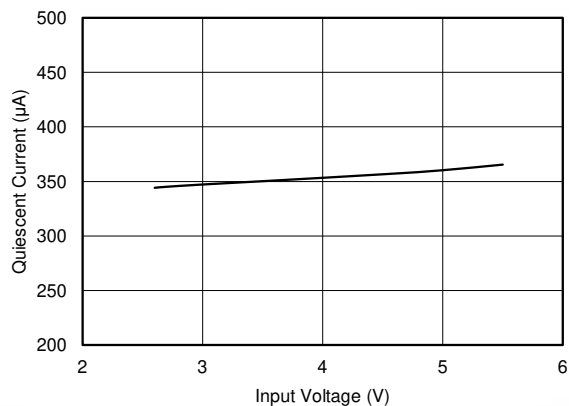
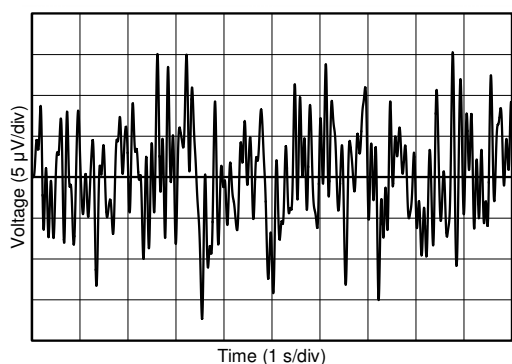
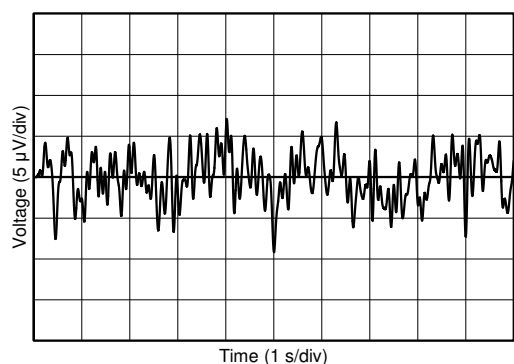


Figure 6-28. Quiescent Current vs Input Voltage



V_{REF} output

Figure 6-29. 0.1Hz to 10Hz Noise (V_{REF})



V_{BIAS} output

Figure 6-30. 0.1Hz to 10Hz Noise (V_{BIAS})

6.6 Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $I_L = 0\text{mA}$, $V_{IN} = 5\text{V}$ power supply, $C_L = 0\ \mu\text{F}$, and 2.5V output, unless otherwise noted.

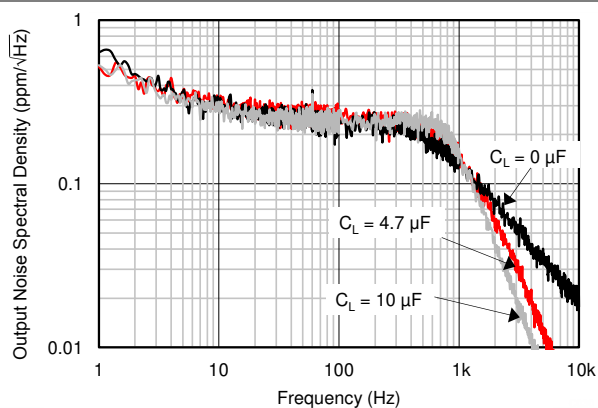


Figure 6-31. Output Voltage Noise Spectrum

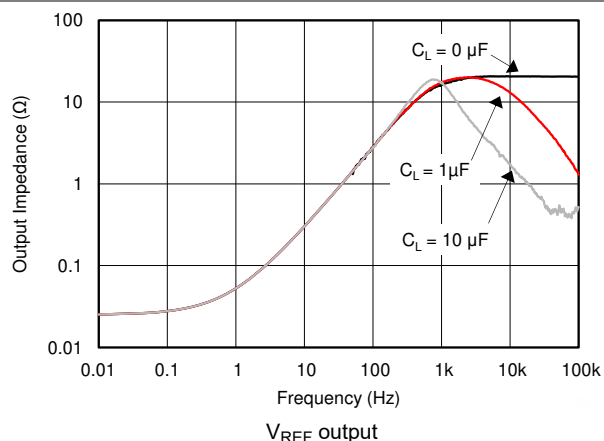


Figure 6-32. Output Impedance vs Frequency (V_{REF})

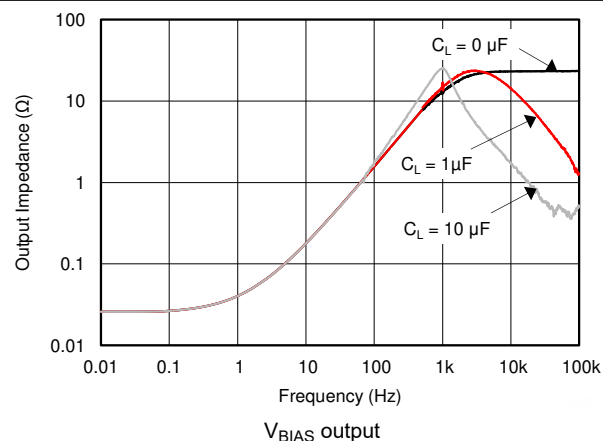


Figure 6-33. Output Impedance vs Frequency (V_{BIAS})

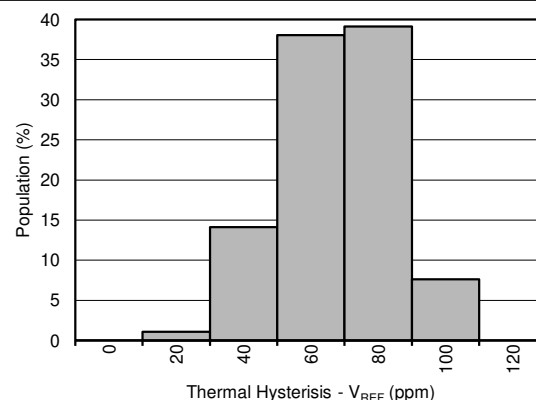


Figure 6-34. Thermal Hysteresis Distribution (V_{REF})

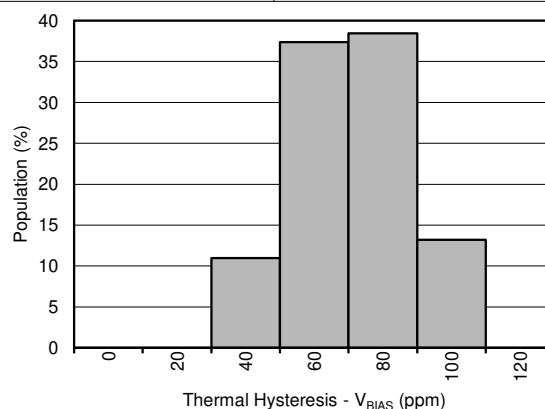


Figure 6-35. Thermal Hysteresis Distribution (V_{BIAS})

7 Parameter Measurement Information

7.1 Solder Heat Shift

The materials used in the manufacture of the REF19xx have differing coefficients of thermal expansion. Because of the differing coefficients, this results in stress on the device die when heating the device. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

To show this effect, a total of 92 devices are soldered on four printed circuit boards [23 devices on each printed circuit board (PCB)] using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in [Figure 7-1](#). The PCB is comprised of FR4 material. The board thickness is 1.57mm and the area is 171.54mm × 165.1mm.

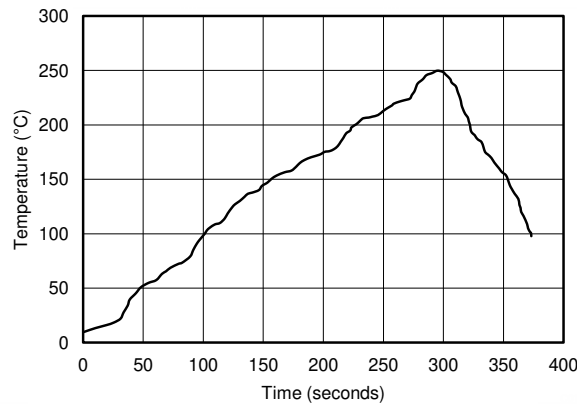


Figure 7-1. Reflow Profile

The reference and bias output voltages are measured before and after the reflow process; [Figure 7-2](#) and [Figure 7-3](#) shows the typical shift. Although all tested units exhibit very low shifts (< 0.01%), higher shifts are also possible depending on the size, thickness, and material of the PCB. An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, which is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If exposing the PCB to multiple reflows, solder the device in the second pass to minimize device exposure to thermal stress.

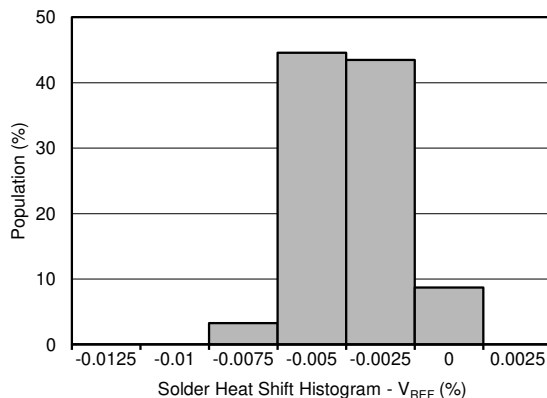


Figure 7-2. Solder Heat Shift Distribution, V_{REF} (%)

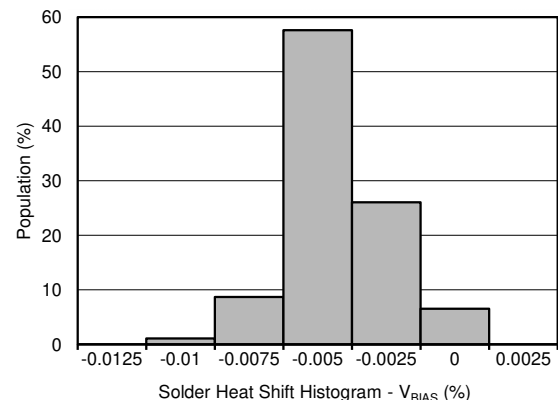


Figure 7-3. Solder Heat Shift Distribution, V_{BIAS} (%)

7.2 Thermal Hysteresis

The measurement of thermal hysteresis occurs with the REF19xx soldered to a PCB, similar to a real-world application. The definitions of thermal hysteresis for the device is the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. Express hysteresis using [Equation 1](#):

$$V_{\text{HYST}} = \left(\frac{|V_{\text{PRE}} - V_{\text{POST}}|}{V_{\text{NOM}}} \right) \times 10^6 (\text{ppm}) \quad (1)$$

where

- V_{HYST} = thermal hysteresis (in units of ppm),
- V_{NOM} = the specified output voltage,
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling, and
- V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range from –40°C to 125°C and returns to 25°C.

Typical thermal hysteresis distribution is as shown in [Figure 7-4](#) and [Figure 7-5](#).

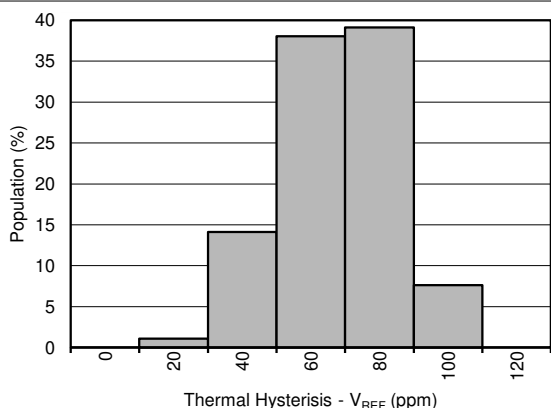


Figure 7-4. Thermal Hysteresis Distribution (V_{REF})

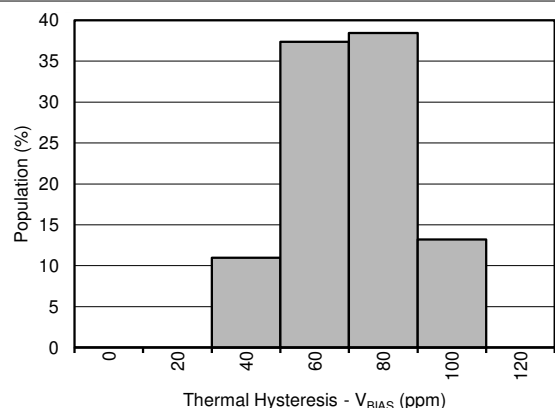


Figure 7-5. Thermal Hysteresis Distribution (V_{BIAS})

7.3 Noise Performance

[Figure 7-6](#) and [Figure 7-7](#) shows the typical 0.1Hz to 10Hz voltage noise. Device noise increases with output voltage and operating temperature. Use additional filtering to improve output noise levels, although take care to establish the output impedance does not degrade AC performance. [Figure 7-8](#) shows the peak-to-peak noise measurement setup.

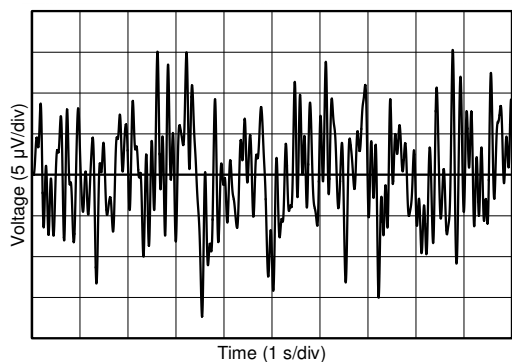


Figure 7-6. 0.1Hz to 10Hz Noise (V_{REF})

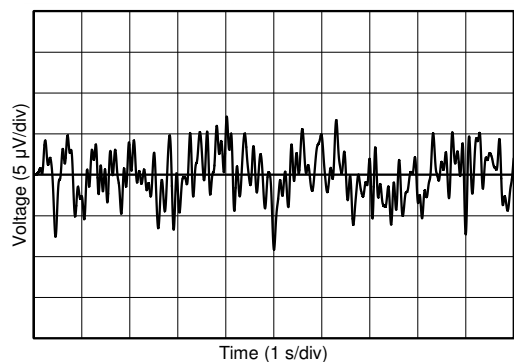


Figure 7-7. 0.1Hz to 10Hz Noise (V_{BIAS})

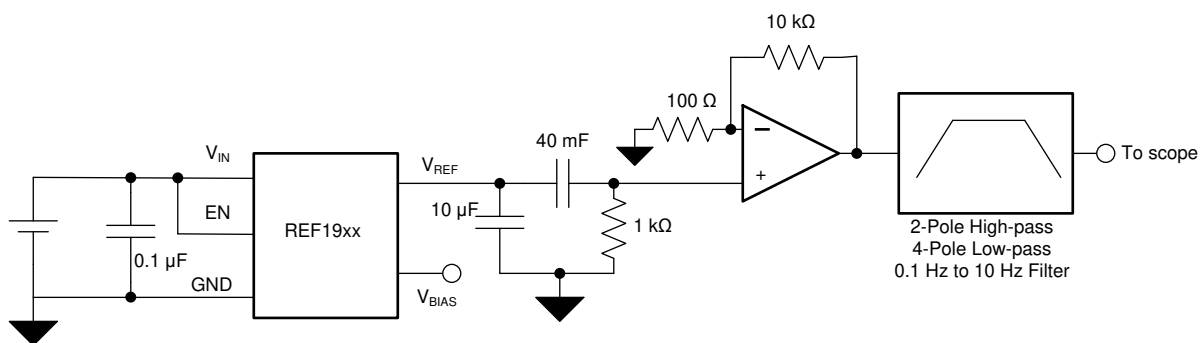


Figure 7-8. 0.1Hz to 10Hz Noise Measurement Setup

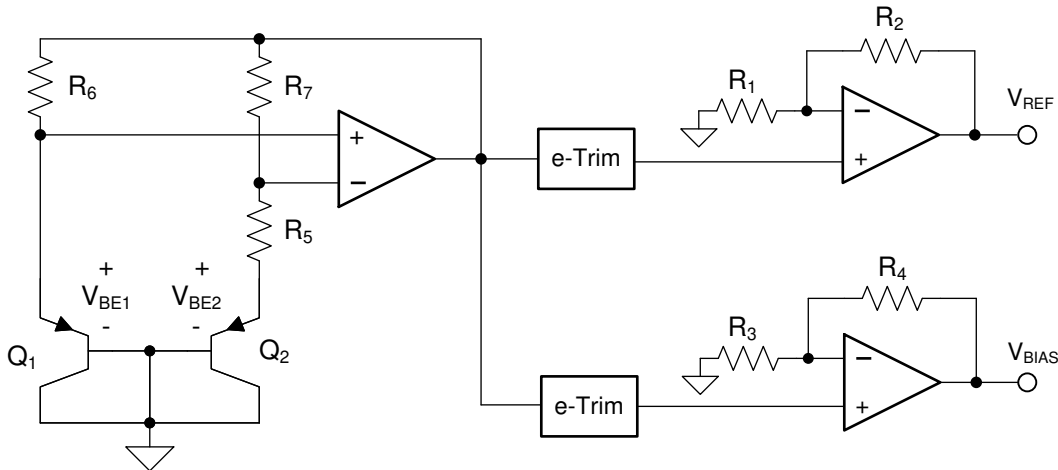
8 Detailed Description

8.1 Overview

The REF19xx is a family of dual-output, V_{REF} and V_{BIAS} ($V_{REF} / 2$) band-gap voltage references. The [Functional Block Diagram](#) section provides a block diagram of the basic band-gap topology and the two buffers used to derive the V_{REF} and V_{BIAS} outputs. Transistors Q_1 and Q_2 are biased such that the current density of Q_1 is greater than that of Q_2 . The difference of the two base emitter voltages ($V_{BE1} - V_{BE2}$) has a positive temperature coefficient and is forced across resistor R_5 . The voltage is amplified and added to the base emitter voltage of Q_2 , which has a negative temperature coefficient. The resulting band-gap output voltage is almost independent of temperature. Two independent buffers are used to generate V_{REF} and V_{BIAS} from the band-gap voltage. The resistors R_1 , R_2 and R_3 , R_4 are sized such that $V_{BIAS} = V_{REF} / 2$.

e-trim™ integrated circuit is a method of package-level trim for the initial accuracy and temperature coefficient of V_{REF} and V_{BIAS} , implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent transistor mismatch, as well as errors induced during package molding. An e-trim™ integrated circuit is implemented in the REF19xx to minimize the temperature drift and maximize the initial accuracy of both the V_{REF} and V_{BIAS} outputs.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 V_{REF} and V_{BIAS} Tracking

Most single-supply systems require an additional stable voltage in the middle of the analog-to-digital converter (ADC) input range to bias input bipolar signals. The V_{REF} and V_{BIAS} outputs of the REF19xx are generated from the same band-gap voltage as shown in the [Functional Block Diagram](#) section. Hence, both outputs track each other over the full temperature range from -40°C to 125°C with an accuracy of 7ppm/ $^{\circ}\text{C}$ (maximum). The tracking accuracy increases to 6ppm/ $^{\circ}\text{C}$ (maximum) when the temperature range limit is from -40°C to 85°C . Calculate the tracking error using the box method, as described by [Equation 2](#):

$$\text{Tracking Error} = \left[\frac{V_{DIFF(MAX)} - V_{DIFF(MIN)}}{V_{REF} \times \text{Temperature Range}} \right] \times 10^6 (\text{ppm}) \quad (2)$$

where

$$V_{DIFF} = V_{REF} - 2 \times V_{BIAS} \quad (3)$$

The tracking accuracy is as shown in [Figure 8-1](#).

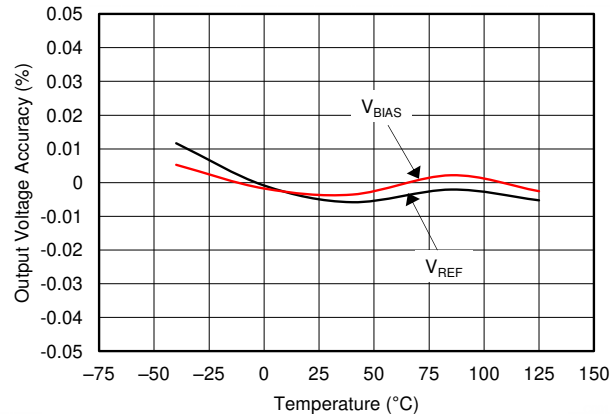


Figure 8-1. V_{REF} and V_{BIAS} Tracking vs Temperature

8.3.2 Low Temperature Drift

The REF19xx is designed for minimal drift error, which is the change in output voltage overtemperature. Calculate the drift using the box method, as described by [Equation 4](#):

$$\text{Drift} = \left[\frac{V_{\text{REF(MAX)}} - V_{\text{REF(MIN)}}}{V_{\text{REF}} \times \text{Temperature Range}} \right] \times 10^6 (\text{ppm}) \quad (4)$$

8.3.3 Load Current

The REF19xx family is specified to deliver a current load of $\pm 20\text{mA}$ per output. Both the V_{REF} and V_{BIAS} outputs of the device are protected from short circuits by limiting the output short-circuit current to 50mA. The device temperature increases according to [Equation 5](#):

$$T_J = T_A + P_D \cdot R_{\theta JA} \quad (5)$$

where

- T_J = junction temperature (°C)
- T_A = ambient temperature (°C)
- P_D = power dissipated (W)
- $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

The REF19xx maximum junction temperature must not exceed the absolute maximum rating of 150°C.

8.4 Device Functional Modes

When the EN pin of the REF19xx pulls high, the device is in active mode. The device must be in active mode for normal operation. Place the REF19xx in a low-power mode by pulling the ENABLE pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 5μA in shutdown mode. See the [Electrical Characteristics](#) for logic high and logic low voltage levels.

9 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The low-drift, bidirectional, single-supply, low-side, current-sensing design described in this section can accurately detect load currents from -2.5A to 2.5A . The linear range of the output is from 250mV to 2.75V . Positive current is represented by output voltages from 1.5V to 2.75V , whereas negative current is represented by output voltages from 250mV to 1.5V . The difference amplifier is the [INA213](#) current-shunt monitor, whose supply and reference voltages are supplied by the low-drift REF1930.

9.2 Typical Application

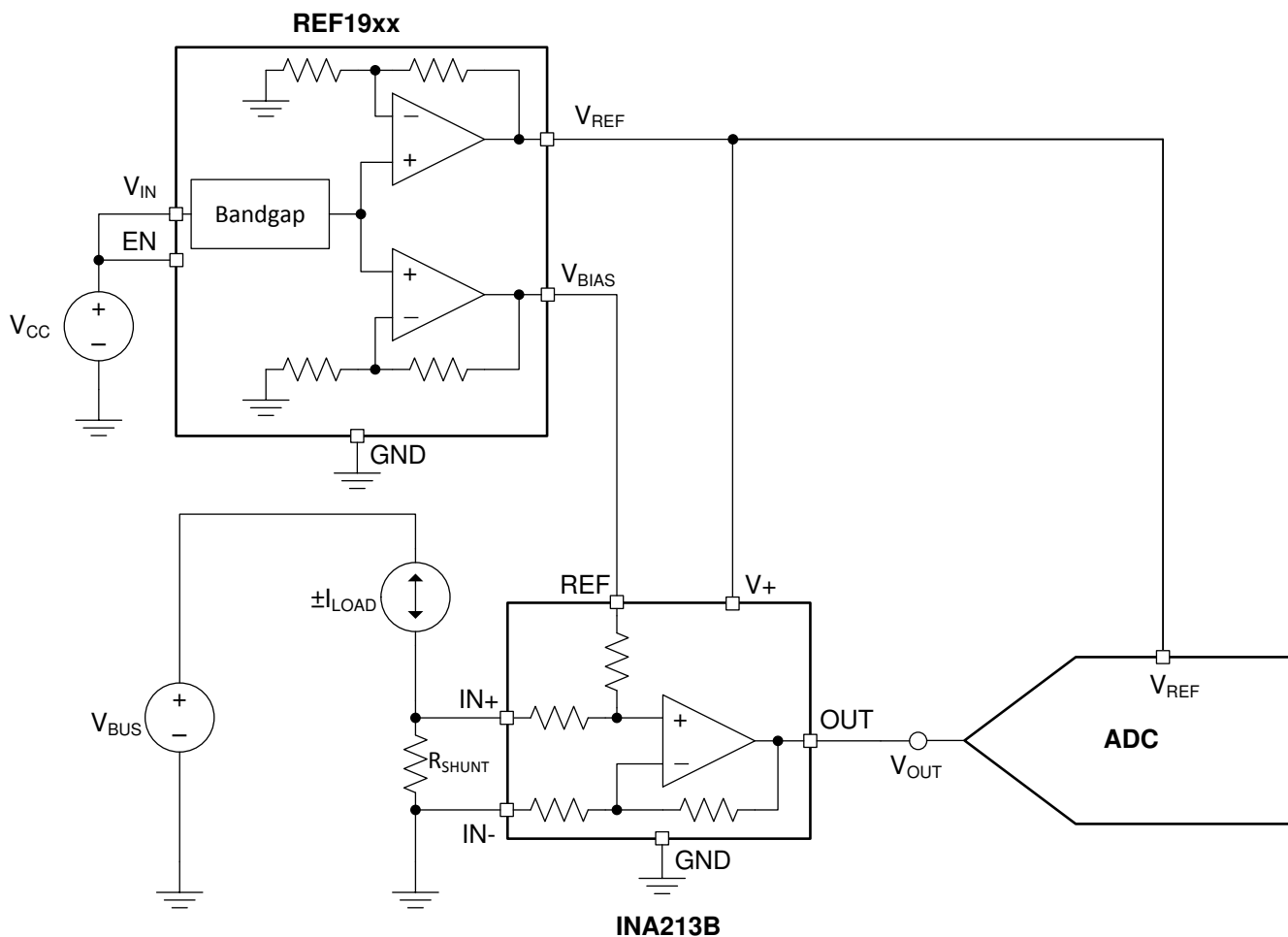


Figure 9-1. Low-Side, Current-Sensing Application

9.2.1 Design Requirements

The design requirements are as follows:

1. Supply voltage: 5.0V

2. Load current: $\pm 2.5\text{A}$
3. Output: 250mV to 2.75V
4. Maximum shunt voltage: $\pm 25\text{mV}$

9.2.2 Detailed Design Procedure

Low-side current sensing is desirable because the common-mode voltage is near ground. Therefore, the current-sensing design is independent of the bus voltage, V_{BUS} . When sensing bidirectional currents, use a differential amplifier with a reference pin. This procedure allows for the differentiation between positive and negative currents by biasing the output stage such that it can respond to negative input voltages. There are a variety of methods for supplying power (V_+) and the reference voltage (V_{REF} , or V_{BIAS}) to the differential amplifier. For a low-drift design, use a monolithic reference that supplies both power and the reference voltage. Figure 9-2 shows the general circuit topology for a low-drift, low-side, bidirectional, current-sensing design. This topology is particularly useful when interfacing with an ADC; see Figure 9-1. Not only do V_{REF} and V_{BIAS} track over temperature, but the matching is much better than alternate topologies. For a more detailed version of the design procedure, see the [Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Design Guide](#).

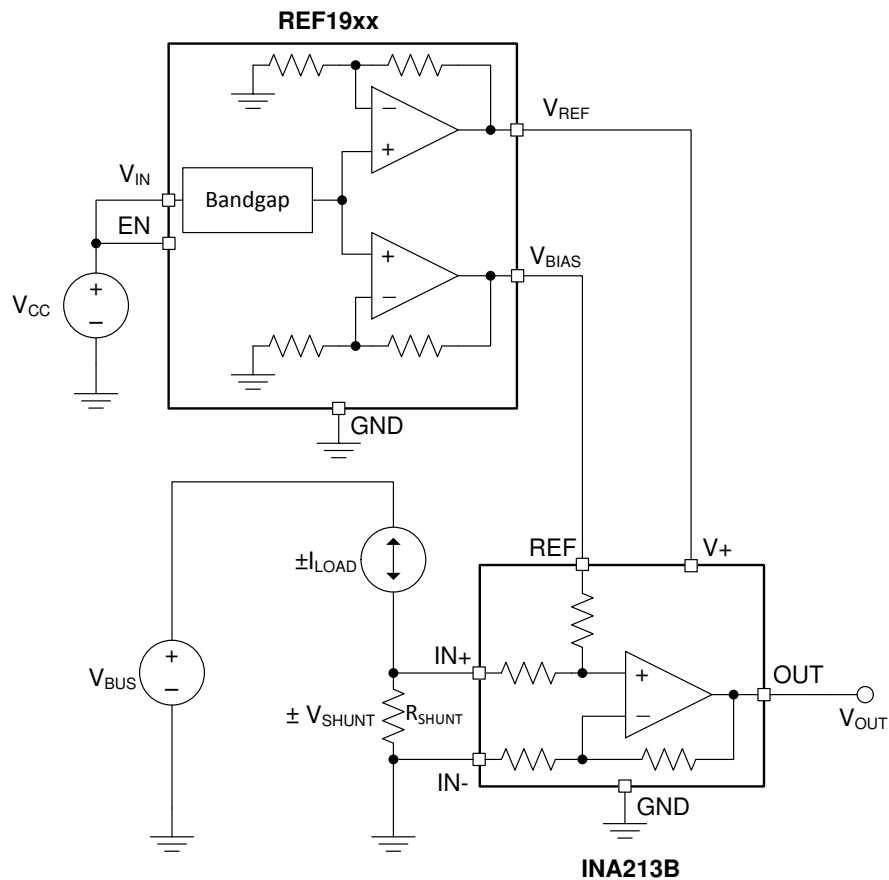


Figure 9-2. Low-Drift, Low-side, Bidirectional, Current-Sensing Circuit Topology

The transfer function for the circuit given in Figure 9-2 is as shown in Equation 6:

$$\begin{aligned} V_{\text{OUT}} &= G \times (\pm V_{\text{SHUNT}}) + V_{\text{BIAS}} \\ &= G \times (\pm I_{\text{LOAD}} \times R_{\text{SHUNT}}) + V_{\text{BIAS}} \end{aligned} \quad (6)$$

9.2.2.1 Shunt Resistor

As illustrated in Figure 9-2, the value of V_{SHUNT} is the ground potential for the system load. If the value of V_{SHUNT} is too large, issues can arise when interfacing with systems whose ground potential is actually 0V . Also, a value

of V_{SHUNT} that is too negative can violate the input common-mode voltage of the differential amplifier in addition to potential interfacing issues. Therefore, limiting the voltage across the shunt resistor is important. Use Equation 7 to calculate the maximum value of R_{SHUNT} .

$$R_{SHUNT(max)} = \frac{V_{SHUNT(max)}}{I_{LOAD(max)}} \quad (7)$$

Given that the maximum shunt voltage is $\pm 25\text{mV}$ and the load current range is $\pm 2.5\text{A}$, calculate the maximum shunt resistance as Equation 8 shows.

$$R_{SHUNT(max)} = \frac{V_{SHUNT(max)}}{I_{LOAD(max)}} = \frac{25\text{mV}}{2.5\text{A}} = 10\text{m}\Omega \quad (8)$$

To minimize errors overtime, select a low-drift shunt resistor. To minimize offset error, select a shunt resistor with the lowest tolerance. This design uses the Y14870R01000B9W resistor.

9.2.2.2 Differential Amplifier

The differential amplifier used for this design must have the following features:

1. Single supply (3V),
2. Reference voltage input,
3. Low initial input offset voltage (V_{OS}),
4. Low-drift,
5. Fixed gain, and
6. Low-side sensing (input common-mode range below ground).

For this design, a current-shunt monitor (INA213) is used. The INA21x family topology is shown in Figure 9-3. The INA213B specifications can be found in the *INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors* datasheet.

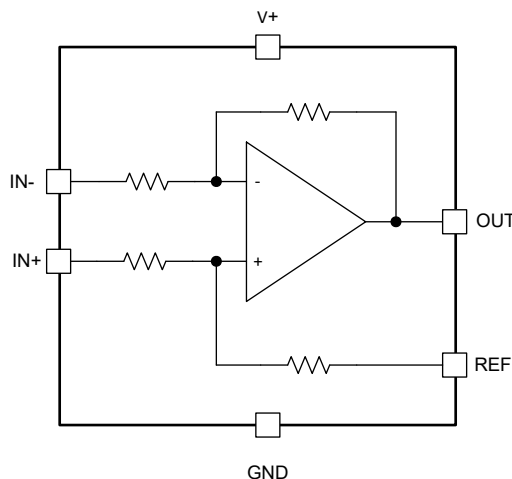


Figure 9-3. INA21x Current-Shunt Monitor Topology

The INA213B is an excellent choice for this application because all the required features are included. In general, instrumentation amplifiers (INAs) do not have the input common-mode swing to ground that is essential for this application. In addition, INAs require external resistors to set the gain, which is not desirable for low-drift applications. Difference amplifiers typically have larger input bias currents, which reduce design accuracy at small load currents. Difference amplifiers typically have a gain of 1V/V . When the gain is adjustable, these amplifiers use external resistors that are not conducive to low-drift applications.

9.2.2.3 Voltage Reference

The voltage reference for this application must have the following features:

1. Dual output (3.0V and 1.5V),
2. Low drift, and
3. Low tracking errors between the two outputs.

For this design, the REF1930 is used. The REF19xx topology is as shown in the [Functional Block Diagram](#) section.

The REF1930 is an excellent choice for this application because of the dual output. The temperature drift of 25ppm/°C and initial accuracy of 0.1% make the errors resulting from the voltage reference minimal in this application. In addition, there is minimal mismatch between the two outputs and both outputs track very well across temperature, as shown in [Figure 9-4](#) and [Figure 9-5](#).

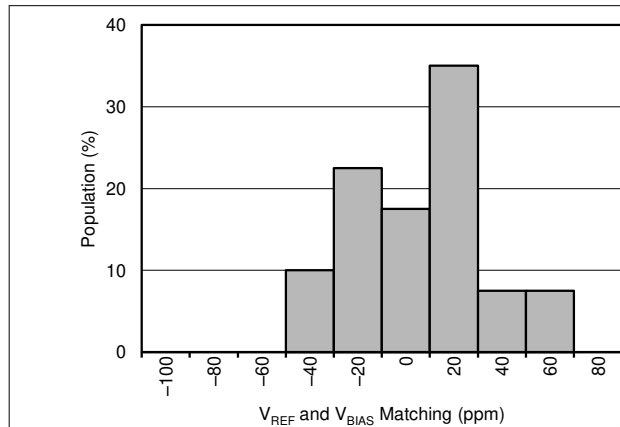


Figure 9-4. $V_{REF} - 2 \times V_{BIAS}$ Distribution (At $T_A = 25^\circ\text{C}$)

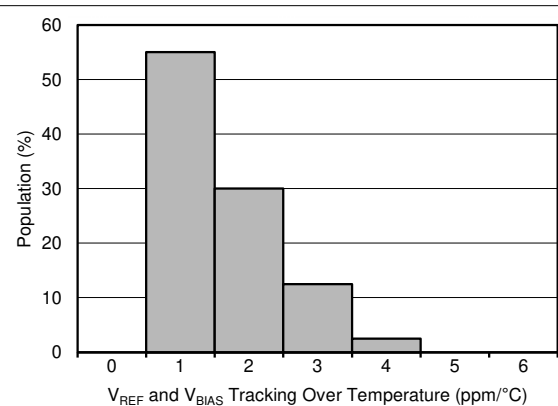


Figure 9-5. Distribution of $V_{REF} - 2 \times V_{BIAS}$ Drift Tracking Over Temperature

9.2.2.4 Results

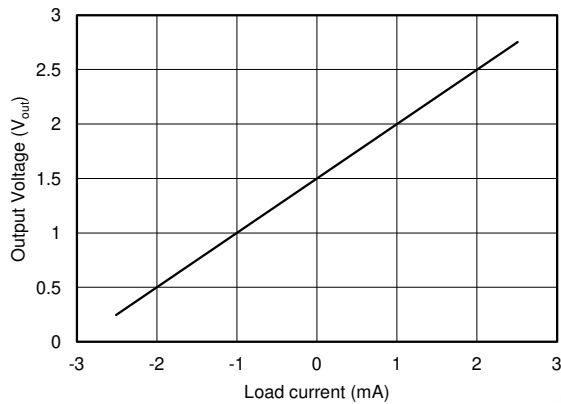
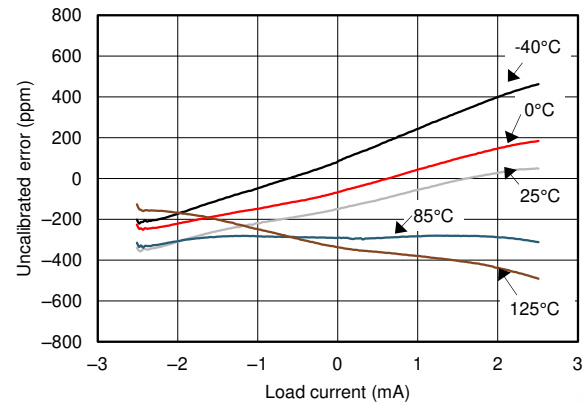
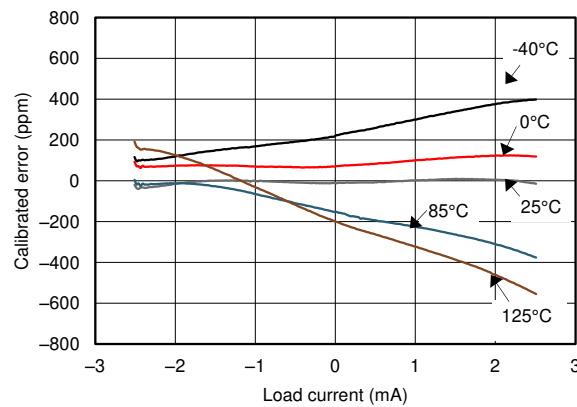
[Table 9-1](#) summarizes the measured results.

Table 9-1. Measured Results

ERROR	UNCALIBRATED (%)	CALIBRATED (%)
Error across the full load current range (25°C)	±0.0355	±0.004
Error across the full load current range (–40°C to 125°C)	±0.0522	±0.0606

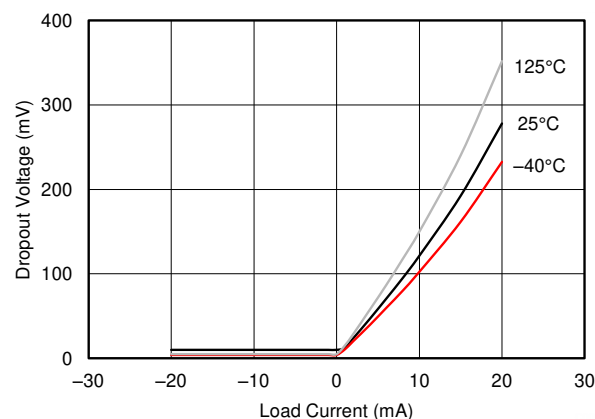
9.2.3 Application Curves

Performing a two-point calibration at 25°C removes the errors associated with offset voltage, gain error, and so forth. [Figure 9-6](#) to [Figure 9-8](#) show the measured error at different conditions. For a more detailed description on measurement procedure, calibration, and calculations, see also the [Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Design Guide](#).

**Figure 9-6. Measured Transfer Function****Figure 9-7. Uncalibrated Error vs Load Current****Figure 9-8. Calibrated Error vs Load Current**

9.3 Power-Supply Recommendations

The REF19xx family of references feature an extremely low-dropout voltage. These references can be operated with a supply of only 20mV above the output voltage. For loaded reference conditions, a typical dropout voltage versus load is shown in [Figure 9-9](#). A supply bypass capacitor ranging between 0.1 μF to 10 μF is recommended.

**Figure 9-9. Dropout Voltage vs Load Current**

9.4 Layout

9.4.1 Layout Guidelines

Figure 9-10 shows an example of a PCB layout for a data acquisition system using the REF1930. Some key considerations are:

- Connect low-ESR, 0.1µF ceramic bypass capacitors at V_{IN} , V_{REF} , and V_{BIAS} of the REF1930.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Minimize trace length between the reference and bias connections to the INA and ADC to reduce noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible and only make perpendicular crossings when absolutely necessary.

9.4.2 Layout Example

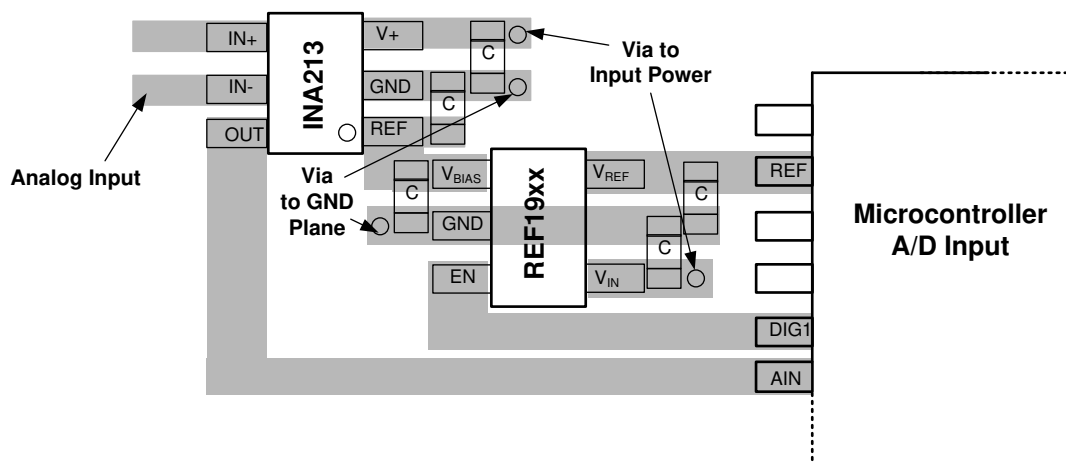


Figure 9-10. Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors datasheet](#)
- Texas Instruments, [Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Reference Design reference guide](#)

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.4 Trademarks

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2017) to Revision B (June 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Moved REF1925, REF1930, REF1933, REF1941 devices to the REF19 product folder on TI.com and updated the datasheet header.....	1

Changes from Revision * (September 2014) to Revision A (January 2017)	Page
• Changed <i>Input</i> to <i>Output</i> in I/O column of pin 1 row in <i>Pin Functions</i> table	4
• Added <i>Storage temperature</i> parameter to <i>Absolute Maximum Ratings</i> table (moved from <i>ESD Ratings</i> table).....	5
• Changed <i>ESD Ratings</i> table: changed title and updated table format	5

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF1925AIDDCR	Active	Production	SOT-23-THIN (DDC) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAGM
REF1925AIDDCR.B	Active	Production	SOT-23-THIN (DDC) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAGM
REF1925AIDDCCT	Active	Production	SOT-23-THIN (DDC) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAGM
REF1925AIDDCCT.B	Active	Production	SOT-23-THIN (DDC) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAGM
REF1925AIDDCCTG4	Active	Production	SOT-23-THIN (DDC) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAGM
REF1925AIDDCCTG4.B	Active	Production	SOT-23-THIN (DDC) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAGM
REF1930AIDDCR	Active	Production	SOT-23-THIN (DDC) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAHM
REF1930AIDDCR.B	Active	Production	SOT-23-THIN (DDC) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAHM
REF1930AIDDCCT	Active	Production	SOT-23-THIN (DDC) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAHM
REF1930AIDDCCT.B	Active	Production	SOT-23-THIN (DDC) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAHM
REF1930AIDDCCTG4	Active	Production	SOT-23-THIN (DDC) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAHM
REF1930AIDDCCTG4.B	Active	Production	SOT-23-THIN (DDC) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAHM
REF1933AIDDCR	Active	Production	SOT-23-THIN (DDC) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAIM
REF1933AIDDCR.B	Active	Production	SOT-23-THIN (DDC) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAIM
REF1933AIDDCCT	Active	Production	SOT-23-THIN (DDC) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAIM
REF1933AIDDCCT.B	Active	Production	SOT-23-THIN (DDC) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAIM

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF1933AIDDCG4	Active	Production	SOT-23-THIN (DDC) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAJM
REF1933AIDDCG4.B	Active	Production	SOT-23-THIN (DDC) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAJM
REF1941AIDDCR	Active	Production	SOT-23-THIN (DDC) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAJM
REF1941AIDDCR.B	Active	Production	SOT-23-THIN (DDC) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAJM
REF1941AIDDC	Active	Production	SOT-23-THIN (DDC) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAJM
REF1941AIDDC.B	Active	Production	SOT-23-THIN (DDC) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAJM

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

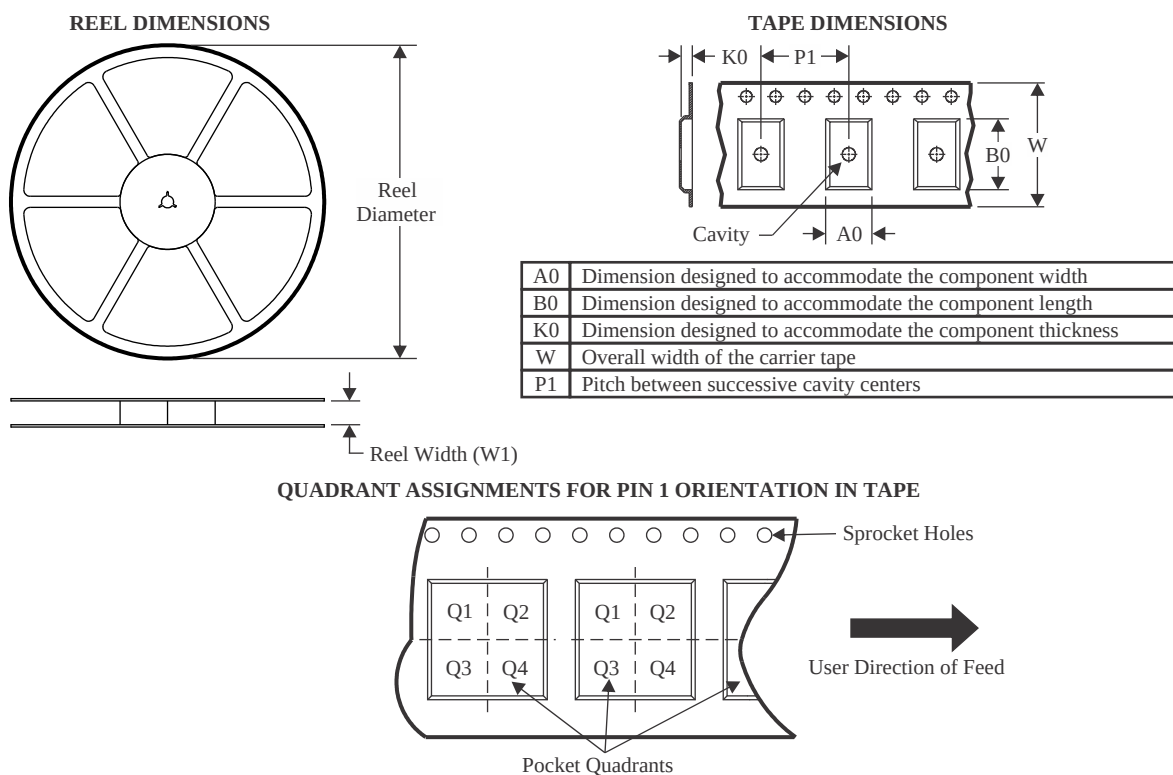
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

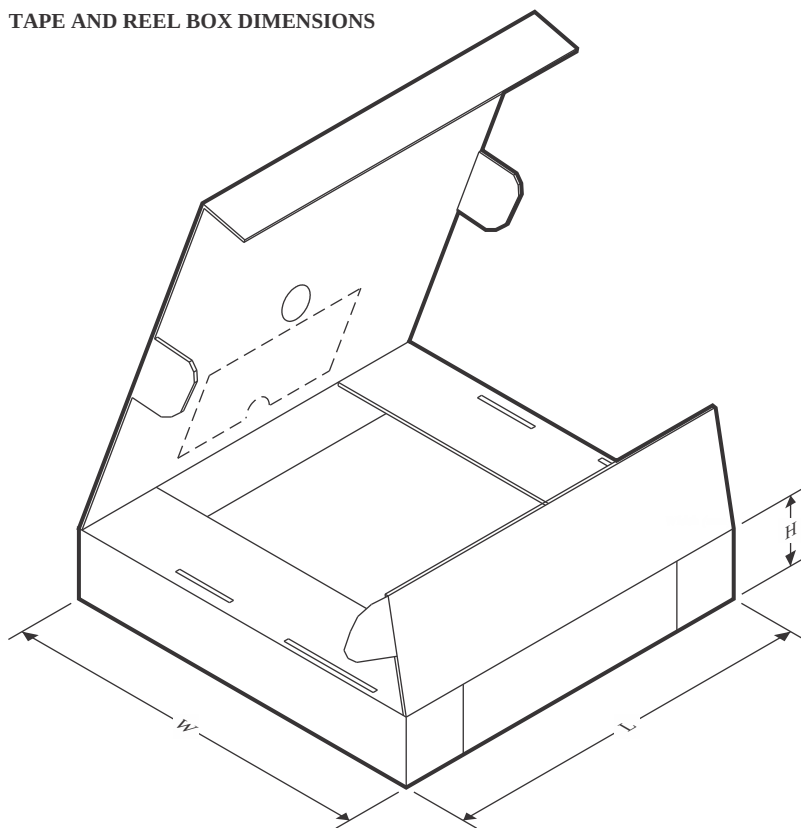


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF1925AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF1925AIDDCR	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF1925AIDDCR	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF1930AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF1930AIDDCR	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF1930AIDDCR	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF1933AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF1933AIDDCR	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF1933AIDDCR	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

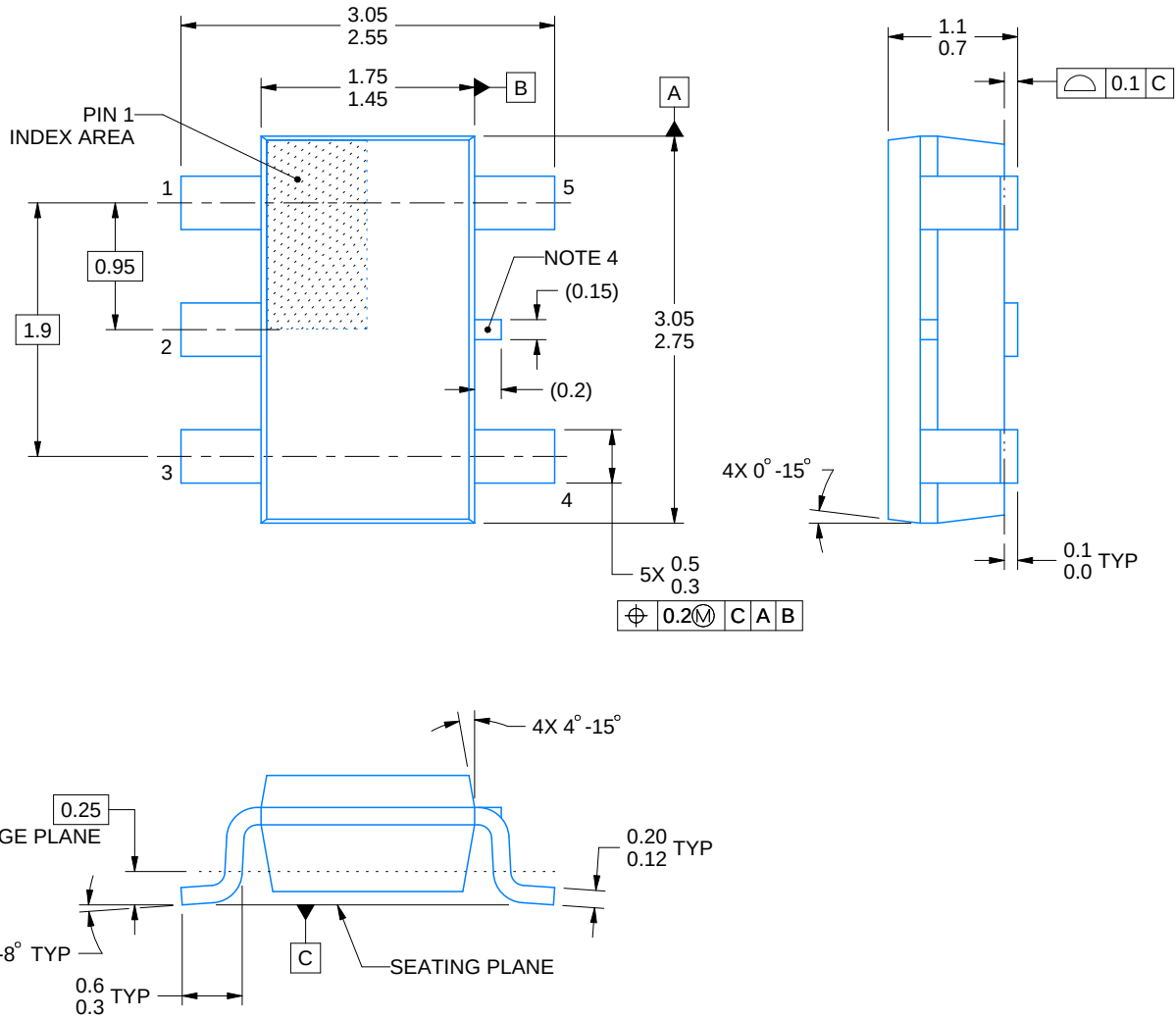
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF1941AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF1941AIDDC	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF1925AIDDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF1925AIDDCR	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
REF1925AIDDCR	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
REF1930AIDDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF1930AIDDCR	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
REF1930AIDDCR	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
REF1933AIDDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF1933AIDDCR	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
REF1933AIDDCR	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
REF1941AIDDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF1941AIDDCR	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0



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NOTES:

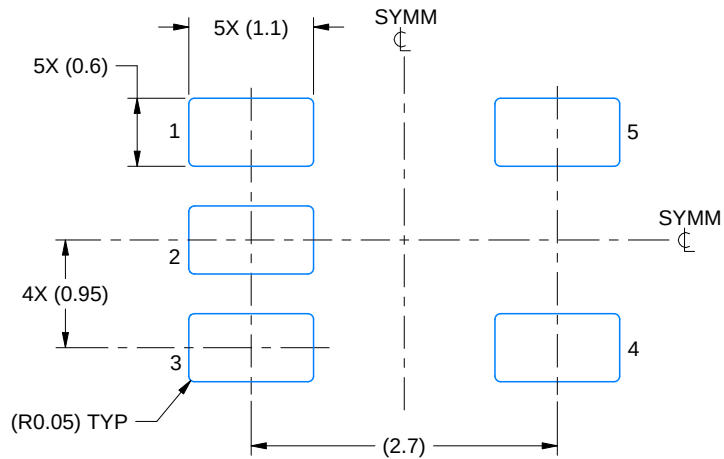
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

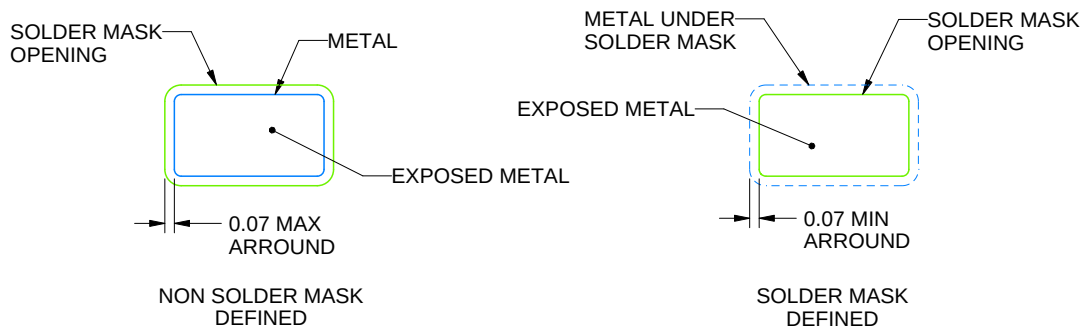
DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPLODED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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NOTES: (continued)

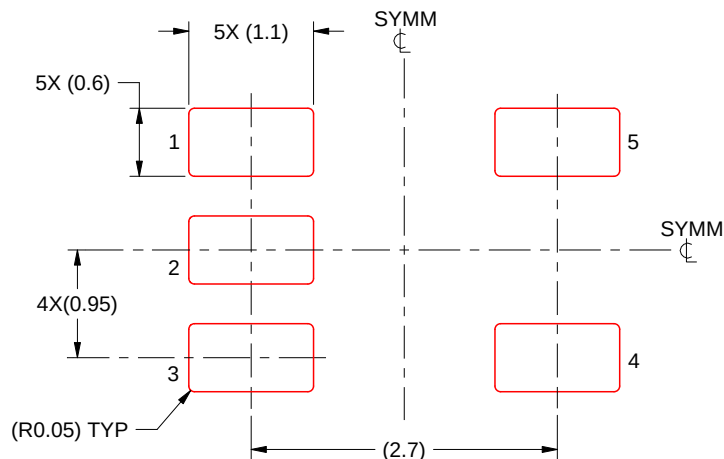
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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