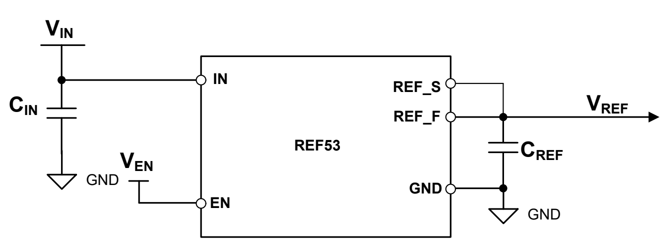
REF53-Q1, 4ppm/°C Maximum Drift, $3ppm_{p-p}$ 1/f Noise, 85µA Current, 30mA Load Current, Precision Voltage Reference

1 Features

- Low temperature drift coefficient: 4ppm/°C maximum
- Low quiescent current: 85µA typical
- Low noise
  - 0.1Hz to 10Hz: $3ppm_{p-p}$
  - 10Hz to 1kHz: $3ppm_{rms}$
- High accuracy: ±0.04% maximum
- Small Size: SOT-23-THN-6 (DDC) package
- Designed for a wide range of applications:
  - Wide input voltage up to 18V
  - Output current: +30mA/-10mA
  - Voltage options: 1.2V, 1.25V, 1.8V, 2.048V, 2.5V, 3V, 3.3V, 4.096V, 4.5V, 5V
- Fit for all design requirement:
  - Stable with 1µF to 50µF output low-ESR capacitor
  - High PSRR: 85dB at 1kHz
  - Specified temperature range: −40°C to +125°C
  - Operational temperature range: −55°C to +125°C

2 Applications

- Field transmitters
- PLC analog I/O modules
- Power monitoring
- Medical Imaging
- Single and multiaxis servo drives
- Hospital patient care
- Electricity meter
- Battery management system
- Automotive camera
- LIDAR
- HEV/EV OBC and DC/DC converter



Basic Connection Diagram

3 Description

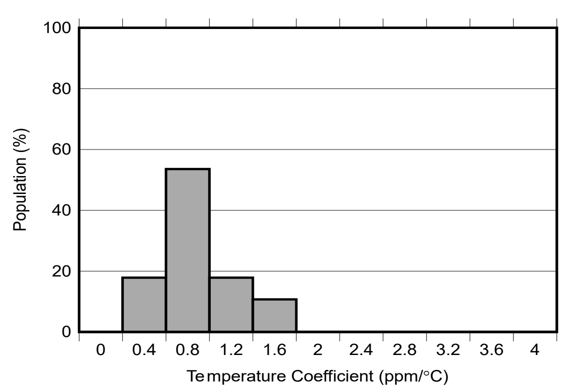
The REF53-Q1 is a family of low-power, low-noise and low-drift series voltage reference devices. The REF53-Q1 family offers low temperature drift coefficient (4ppm/°C) for a temperate range from –40°C to +125°C, low-noise ($2ppm_{p-p}$) and high-accuracy (±0.04%) while consuming 150µA maximum current. The REF53-Q1 with excellent load and line regulation helps to meet strict performance requirements of high precision applications. The device family is designed as a companion device for high-resolution data converters and AFEs. The device is pin compatible performance upgrade to TI's REF34, REF34-Q1 device families.

The REF53-Q1 family supports wide supply voltage rating of 18V. This also protects the device in case of power supply IC failure. The REF53-Q1 device supports up to 30mA load current. The wide load current support allows for direct connection of REF53-Q1 as power supply to precision sensors. The REF53-Q1 is specified for a temperate range from –40°C to +125°C. The wide temperature range enables operation across various industrial and automotive applications.

Package Information

PART NAME	PACKAGE (1)	PACKAGE SIZE(3)
REF53-Q1	SOT-23-THN (6)	2.9mm × 2.8mm
	SOIC (8) (2)	4.9mm × 6mm
	VSSOP (8) (2)	3mm × 4.9mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Preview package.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Temperature Drift Distribution

ADVANCE INFORMATION

Table of Contents

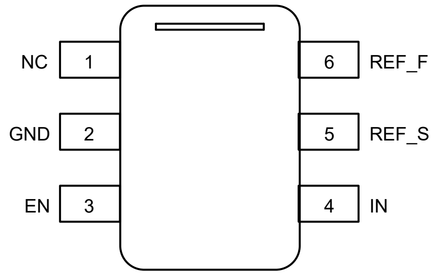
4 Device Comparison Table

PRODUCT (1)			V_{REF}
SOT-23-THN (6)(2)	SOIC (8)(3)	VSSOP (8)(3)	
REF53120AQDDCRQ1	REF53120AQDRQ1	REF53120AQDGKRQ1	1.2V
REF53125AQDDCRQ1	REF53125AQDRQ1	REF53125AQDGKRQ1	1.25V
REF53180AQDDCRQ1	REF53180AQDRQ1	REF53180AQDGKRQ1	1.8V
REF53205AQDDCRQ1	REF53205AQDRQ1	REF53205AQDGKRQ1	2.048V
REF53250AQDDCRQ1	REF53250AQDRQ1	REF53250AQDGKRQ1	2.5V
REF53300AQDDCRQ1	REF53300AQDRQ1	REF53300AQDGKRQ1	3V
REF53330AQDDCRQ1	REF53330AQDRQ1	REF53330AQDGKRQ1	3.3V
REF53410AQDDCRQ1	REF53410AQDRQ1	REF53410AQDGKRQ1	4.096V
REF53450AQDDCRQ1	REF53450AQDRQ1	REF53450AQDGKRQ1	4.5V
REF53500AQDDCRQ1	REF53500AQDRQ1	REF53500AQDGKRQ1	5.0V

(1) Refer to Section 12 for released orderable.
(2) Product preview. Contact local TI support for samples.
(3) Package preview.

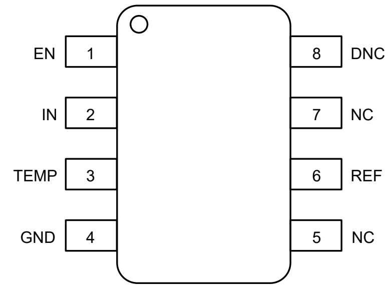
ADVANCE INFORMATION

5 Pin Configuration and Functions



Not to scale

Figure 5-1. DDC 6-Pin THIN SOT23 Top View



Not to scale

Figure 5-2. D, DGK 8-Pin SOIC, VSSOP Top View

Table 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DDC	D, DGK		
NC	1	5,7	No Connect	Not internally connected. Pin can be left floating or connected to GND.
GND	2	4	Ground	Ground connection.
EN	3	1	Input	Device enable control. Low level input disables the reference output and device enters shutdown mode. Device can be enabled by driving voltage > 1.6V or leaving the EN pin floating.
IN	4	2	Power	Input supply voltage connection. Connect a minimum 0.1µF decoupling capacitor to ground for the best performance.
REF_S	5		Output	Reference voltage output sense connection. Connect it to REF_F near the load.
REF_F	6		Output	Reference voltage output force connection. Connect a capacitor between from 1µF to 50µF to ground for best performance.
TEMP		3	Output	Temperature monitoring pin. Provides a temperature-dependent output voltage
REF		6	Output	Reference voltage output. Connect a capacitor between from 1µF to 50µF to ground for best performance.
DNC		8	Do not Connect	Leave the pin floating

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input Voltage	V_{IN}	-0.3	20	V
	EN	-0.3	V_{IN} + 0.3	V
Output voltage	V_{REF_S}, V_{REF_F}	-0.3	5.5	V
Output short circuit current	I_{SC}		80	mA
Junction temperature	(T_J max)		150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	V_{REF} + 0.2[1]		18	V
EN	Enable pin Voltage	0		V_{IN}	V
I_{REF}	Output current	–10		30	mA
T_A	Operating ambient temperature	–40	25	125	°C

(1) For V_{REF} < 1.8V, the minimum supply voltage is 1.71V.

6.4 Thermal Information

THERMAL METRIC[1]		REF53-Q1	REF53-Q1	REF53-Q1	UNIT
		DGK (VSSOP)	D (SOIC)	DDC (SOT-23-THN)	
		8 PINS	8 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance			154.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance			93.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance			61.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter			37.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter			61.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance			N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

ADVANCE INFORMATION

6.5 Electrical Characteristics REF53-Q1

At T_A = 25°C, I_{REF} = 0mA, C_{REF} = 1µF and V_{IN} [1] = (V_{REF} + 0.5V), V_{EN} = V_{IN} unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE						
V_{REF}	Output Voltage	REF53120		1.2		V
		REF53125		1.25		
		REF53180		1.8		
		REF53205		2.048		
		REF53250		2.5		
		REF53300		3		
		REF53330		3.3		
		REF53410		4.096		
		REF53450		4.5		
		REF53500		5		
Initial Accuracy		All voltage options	–0.04		0.04	%
NOISE						
e_{npp}	Low Frequency noise	f = 0.1Hz to 10Hz		3		ppm_{p-p}
e_n	Output Voltage Noise	f = 10Hz to 1kHz		3		ppm_{rms}
OUTPUT VOLTAGE TEMPERATURE DRIFT						
dV_{REF}/dT	Temperature Drift	T_A = –40°C to 125°C		2	4	ppm/°C
LINE REGULATION						
$\Delta V_{REF(\Delta VI)}$	Line regulation	V_{IN} = (V_{REF} + 0.5V) to 18V, T_A = –40°C to 125°C		3	15	ppm/V
PSRR	Power Supply rejection ratio	At 100hz		85		dB
LOAD REGULATION						
$\Delta V_{REF(\Delta IL)}$	Load regulation Sourcing	0 < I_{REF} < 30mA, V_{IN} [2] = V_{REF} + 0.75V		10	15	ppm/mA
		0 < I_{REF} < 30mA, V_{IN} [2] = V_{REF} + 0.75V, T_A = –40°C to 125°C			30	
	Load regulation Sinking	–10mA < I_{REF} < 0, V_{IN} [2] = V_{REF} + 0.75V		20	30	
		–10mA < I_{REF} < 0, V_{IN} = V_{IN} [2] = V_{REF} + 0.75V, T_A = –40°C to 125°C			50	
SHORT-CIRCUIT CURRENT						
I_{SC}	Short circuit current	V_{REF} = 0V		40		mA
THERMAL HYSTERESIS						
	SOT-23-THN	Cycle 1		75		ppm
		Cycle 2		9		
LONG-TERM STABILITY						
	SOT-23-THN	0 to 1000 hours		25		ppm
		1000 to 2000 hours		25		
TURN-ON SETTLING TIME						
Turn-on settling time		To 0.1% with C_{REF} = 1µF		1		ms
CAPACITIVE LOAD						
C_{IN}	Stable input capacitor range	–40°C <T_A<125°C	0.1			µF
C_{REF}	Stable output capacitor range	–40°C <T_A< 125°C	1		50	µF
POWER SUPPLY						

6.5 Electrical Characteristics REF53-Q1 (continued)

At T_A = 25°C, I_{REF} = 0mA, C_{REF} = 1µF and V_{IN} [(1)] = (V_{REF} + 0.5V), V_{EN} = V_{IN} unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_S	Supply voltage	See note [(1)]	V_{REF} + 0.2		18	V
V_{EN}	Enable pin voltage	Active mode (EN = 1)	1.6			V
		Shutdown Mode (EN = 0)			0.5	V
I_{EN}		V_{EN} = V_{IN} = 18V		400		nA
Shutdown Current		V_{EN} = 0, –40°C <T_A<125°C			6	µA
Quiescent Current		–40°C <T_A<125°C		85	150	µA
TEMPERATURE RANGE						
Specified range			–40		125	°C
Operating range			–55		125	°C

(1) For V_{REF} < 1.8V and I_{REF} = 0mA, the minimum supply voltage is 1.71V.
(2) For V_{REF} < 1.8V and I_{REF} = ±10mA, the minimum supply voltage is 1.71V + 0.75V

ADVANCE INFORMATION

6.6 Typical Characteristics

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.5V, I_L = 0mA, C_{REF} = 10µF, C_{IN} = 0.1µF, V_{REF} = 1.25V (unless otherwise noted)

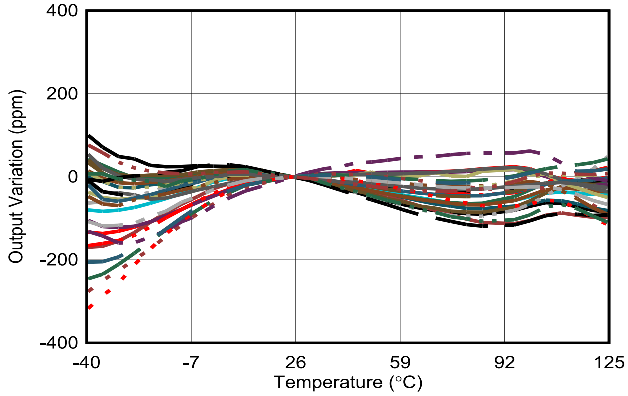


Figure 6-1. Output Voltage Vs Free-Air Temperature

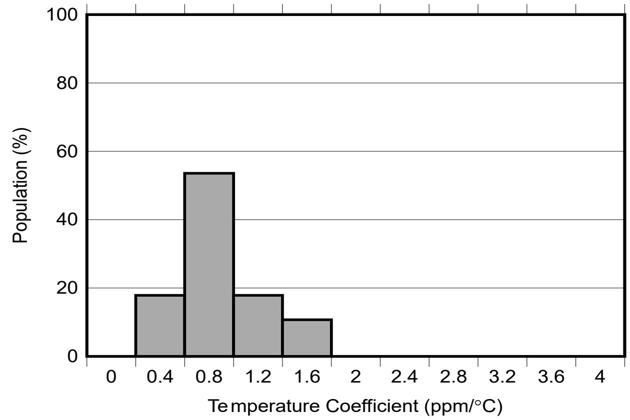


Figure 6-2. Temperature Drift Distribution

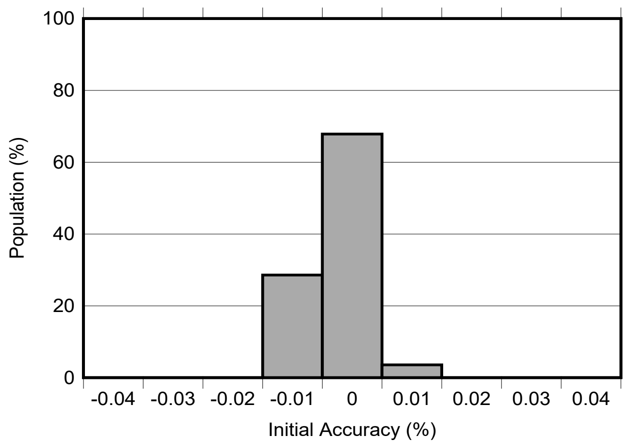


Figure 6-3. Accuracy Distribution

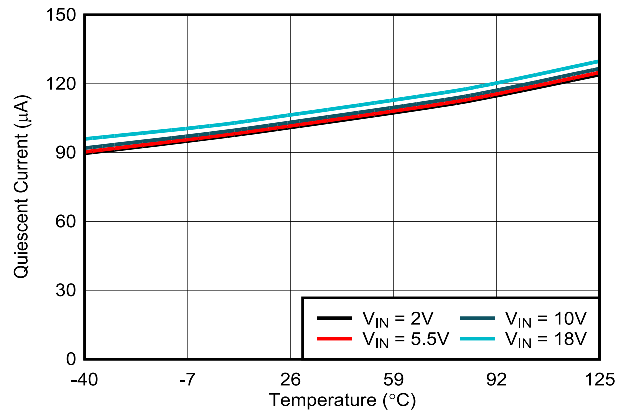


Figure 6-4. Quiescent Current vs Temperature

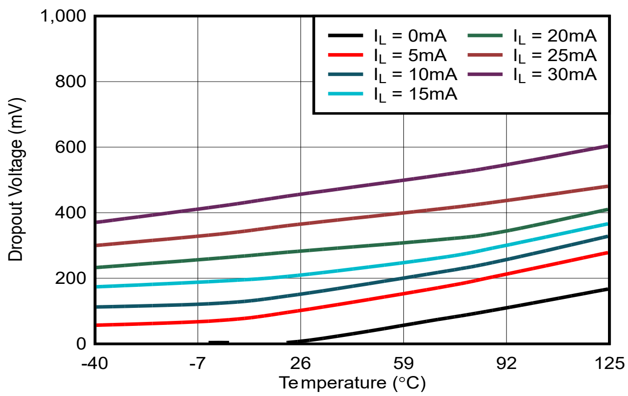


Figure 6-5. Dropout Voltage vs Temperature V_{REF} = 5V

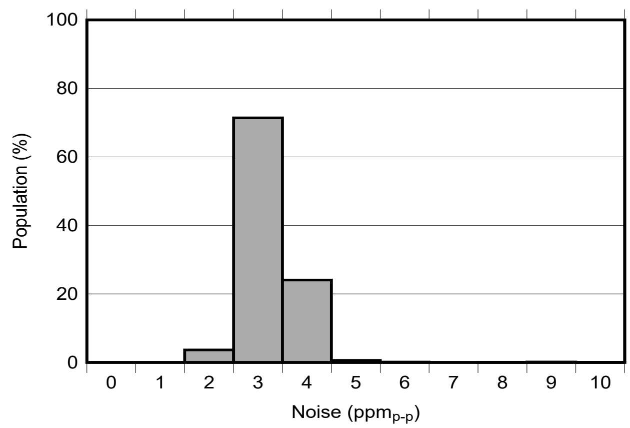


Figure 6-6. 0.1Hz to 10Hz Voltage Noise Distribution

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.5V, I_L = 0mA, C_{REF} = 10µF, C_{IN} = 0.1µF, V_{REF} = 1.25V (unless otherwise noted)

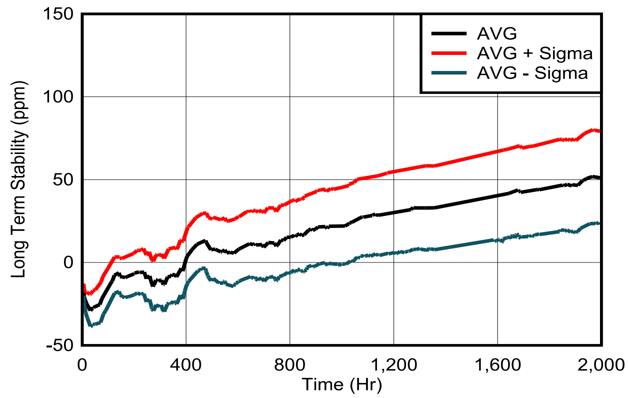


Figure 6-7. Long-Term Stability (First 2000 Hours)

ADVANCE INFORMATION

7 Parameter Measurement Information

7.1 Temperature Drift

The REF53-Q1 is designed and tested for a minimal output voltage temperature drift, which is defined as the change in output voltage over temperature. Every unit shipped is tested at multiple temperatures to make sure that the product meets datasheet specifications. The temperature coefficient is calculated using the box method in which a box is formed by the minimum and maximum limits for the nominal output voltage over the operating temperature range. REF53-Q1 device has maximum temperature coefficient of 4ppm/°C from -40°C to 125°C. The box method specifies limits for the temperature error but does not specify the exact shape and slope of the device under test. Due to temperature curvature correction to achieve low-temperature drift, the temperature drift is expected to be non-linear. See the analog design journal *Precision Voltage References* for more information on the box method. The box method equation is in Equation 1:

$$\text{Drift} = \left(\frac{V_{\text{REF(MAX)}} - V_{\text{REF(MIN)}}}{V_{\text{REF(25°C)}} \times \text{Temperature Range}}\right) \times 10^6 \quad (1)$$

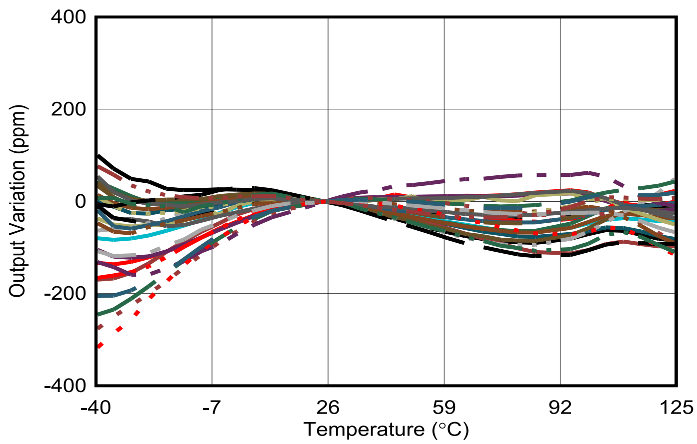


Figure 7-1. Output Voltage vs Free-Air Temperature

7.2 Long-Term Stability

Long-term stability is a key performance parameter for series voltage references in all precision applications. This is defined as variation of reference voltage over time. The long-term stability value is tested in a typical setup that reflects standard PCB board manufacturing practices. The boards are made of standard FR4 material, the board does not have special cuts or grooves around the devices or go through burn-in process to relieve the mechanical stress of the PCB. These conditions reflect real world use case scenario and common manufacturing techniques.

During the long-term stability testing, precautions are taken to make sure that only the long-term stability drift is being measured. The boards are maintained at 35°C ± 0.02°C in an oil bath. The oil bath makes sure that the temperature is constant across the device over time. The measurements are captured every 30 minutes with a calibrated 8.5 digit multimeter.

Typical long-term stability characteristic are expressed as a deviation over time. Figure 7-2 shows the typical drift value for the REF53-Q1 V_{REF} is 25ppm from 0 to 1000 hours.

ADVANCE INFORMATION

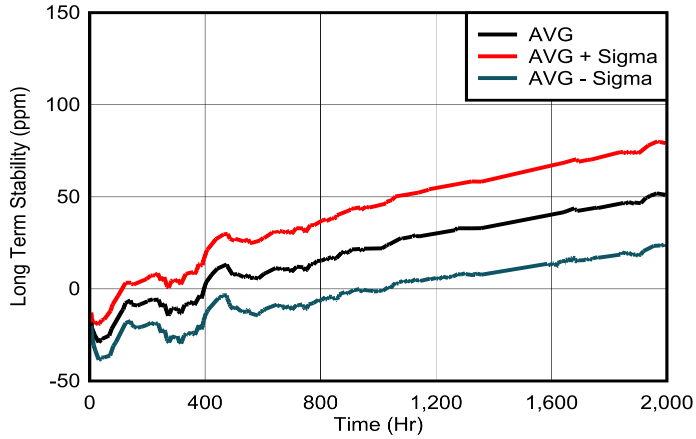


Figure 7-2. Long-Term Stability TSOT -2000 Hours (V_{REF})

7.3 Noise Performance

7.3.1 1/f Noise

1/f noise, also known as flicker noise, is dominant mostly in the lower frequency bands. REF53-Q1 datasheet specifies flicker noise for from 0.1Hz to 10Hz frequency band where 1/f noise has maximum power. Since the 1/f noise is an extremely low value, the frequency of interest is amplified and filtered through a precise band filter with very low-noise floor as Figure 7-3 shows.

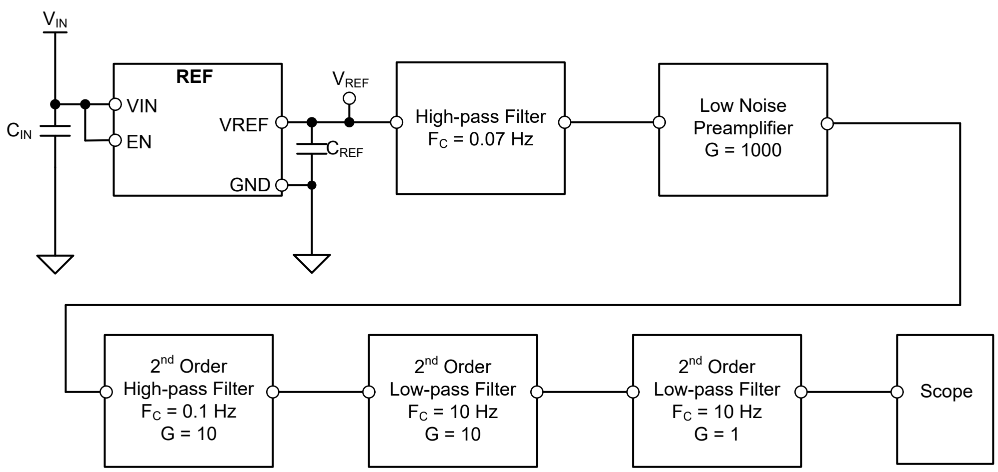


Figure 7-3. 1/f Noise Test Setup

Figure 7-4 shows typical distribution of flicker noise for multiple devices where more than 1000 samples are captured for each device.

ADVANCE INFORMATION

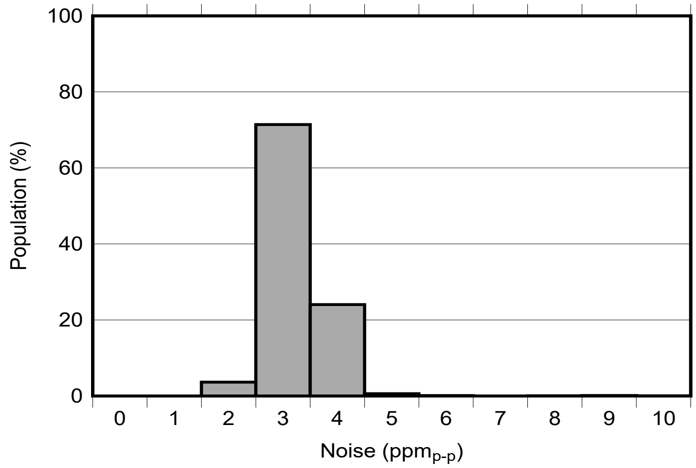


Figure 7-4. From 0.1Hz to 10Hz Voltage Noise Distribution

7.3.2 Broadband Noise

Broadband noise or white noise is flat over the whole spectrum which is restricted by the bandwidth of internal bandgap reference. The broadband noise is measured by high-pass filtering the output of the REF53-Q1 and measuring the result on a precision spectrum analyzer as Figure 7-5 shows. The DC component of the REF53-Q1 is removed by using a high-pass filter and then amplified. Two stages of small gain maximize the noise bandwidth analysis.

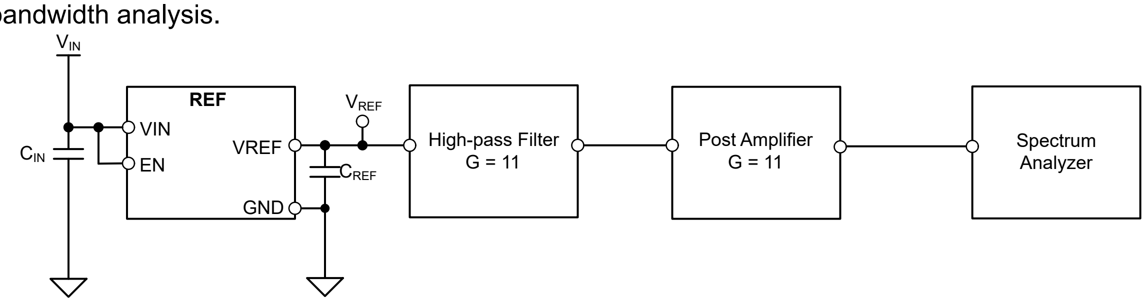


Figure 7-5. Broadband Noise Test Setup

Figure 7-6 shows the typical white noise floor for REF53-Q1.

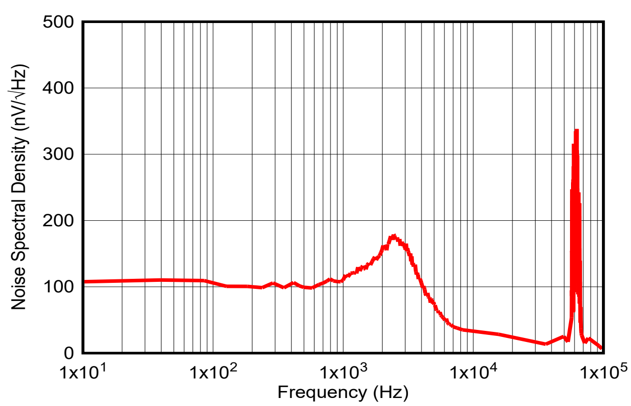


Figure 7-6. Noise Performance From 10Hz to 100kHz (C_{REF}) = 10µF

7.4 Thermal Hysteresis

Thermal hysteresis is measured with the REF53-Q1 soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. The fist thermal cycle is in Figure 7-7 and second cycle is in Figure 7-8. Thermal hysteresis for REF53250CDR settles after first cycle. Express hysteresis by Equation 2

$$V_{HYST} = \left(\frac{|V_{PRE} - V_{POST}|}{V_{NOM}}\right) \times 10^6 \text{ (ppm)} \quad (2)$$

where

- V_{HYST} = thermal hysteresis (in units of ppm)
- V_{NOM} = the specified output voltage
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling
- V_{POST} = output voltage measured after the device cycles from 25°C through the specified temperature range and returns to 25°C

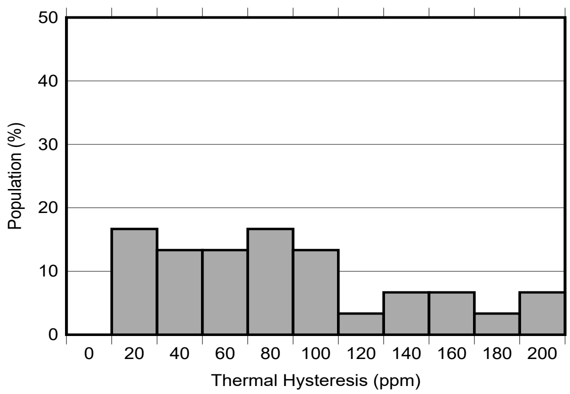


Figure 7-7. Thermal Hysteresis Distribution - Cycle 1

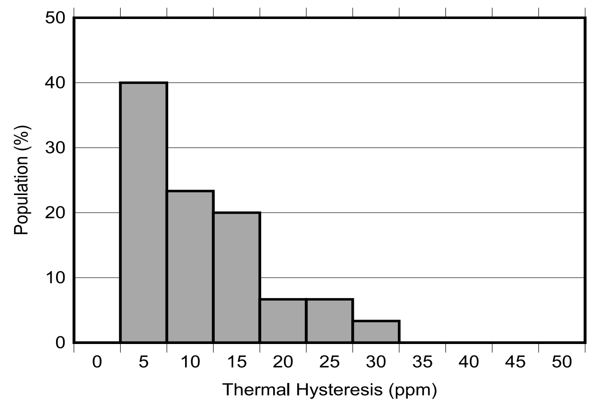


Figure 7-8. Thermal Hysteresis Distribution - Cycle 2

ADVANCE INFORMATION

7.5 Solder Heat Shift

The packaging materials of the REF53-Q1 have different coefficients of thermal expansion than the PCB material. The different coefficients result in stress change on the device die when the part is heated during soldering process and cooled down afterward. Thermal shock due to reflow and stress change on the device die causes the output voltages to shift, degrading the initial accuracy performance of the product. Reflow soldering is a common cause of this error. To quantify the impact, 32 devices are soldered on printed circuit boards using lead-free solder paste and the paste manufacturer suggested reflow profile to show this effect. Figure 7-9 shows the reflow profile. The printed circuit board is comprised of FR4 material. The board thickness is 1.65mm and the area is 137mm × 168mm.

For recommended reflow profiles using 'Sn-Pb Eutectic Assembly' or 'Pb-Free Assembly' please refer JEDEC J-STD-020 standard.

ADVANCE INFORMATION

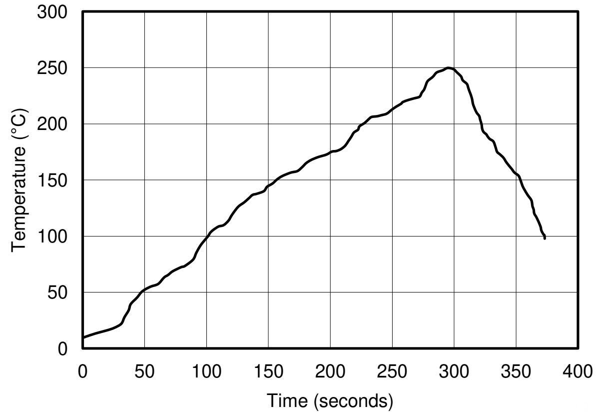


Figure 7-9. Reflow Profile

The reference output voltage is measured before and after the reflow process. Solder shift depends on the size, thickness, and material of the printed circuit board. An important note is that the Figure 7-10 displays the typical shift for exposure to one reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output voltage. If the PCB is exposed to multiple reflows, the device must be soldered in the last pass to minimize the exposure to thermal stress.

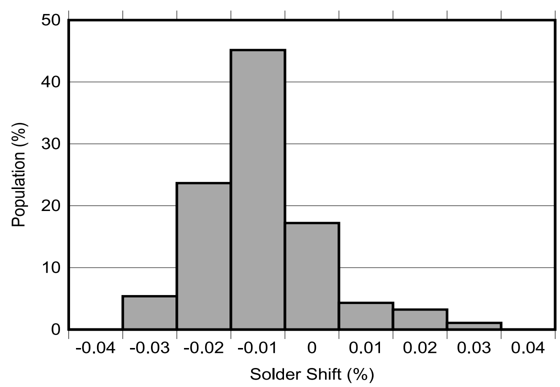


Figure 7-10. Solder Shift

7.6 Power Dissipation

The REF53-Q1 voltage references are capable of source up to 30mA and sink up to 10mA of load current across the rated input voltage range. However, when used in applications subject to high ambient temperatures, the input voltage and load current must be carefully monitored to make sure that the device does not exceed the maximum power dissipation rating. The maximum power dissipation of the device can be calculated with Equation 3:

$$T_J = T_A + P_D \times R_{\theta JA} \quad (3)$$

where

- P_D is the device power dissipation
- T_J is the device junction temperature
- T_A is the ambient temperature
- $R_{\theta JA}$ is the package (junction-to-air) thermal resistance

Because of this relationship, acceptable load current in high temperature conditions can be less than the maximum current-sourcing capability of the device. Do not operate the device outside of the maximum power rating because doing so can result in premature failure or permanent damage to the device.

8 Detailed Description

8.1 Overview

The REF53-Q1 is family of high precision series references that are designed for excellent initial voltage accuracy and drift over time and temperature, and offer excellent noise while consuming low power. Figure 8-1 is a simplified block diagram of the REF53-Q1 showing basic band-gap topology.

8.2 Functional Block Diagram

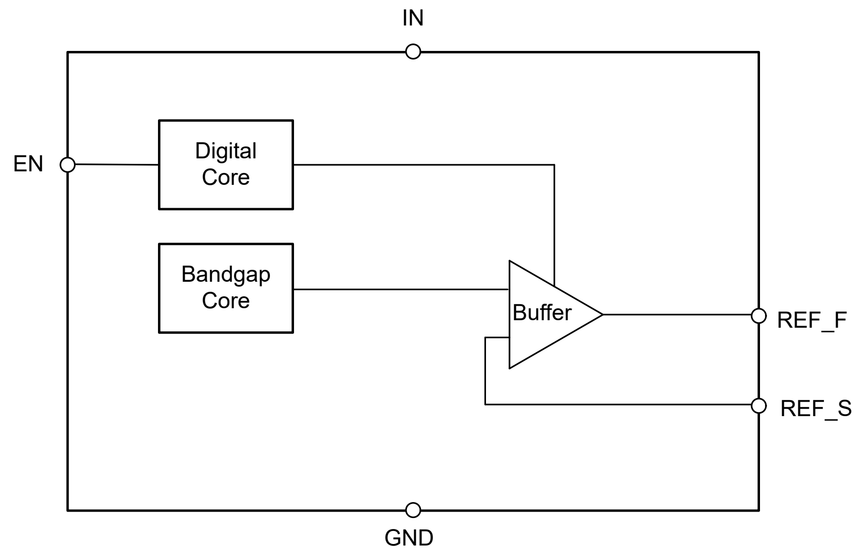


Figure 8-1. REF53-Q1 Functional Block Diagram

8.3 Feature Description

8.3.1 EN Pin

The output of REF53-Q1 comes in active state when EN pin voltage is more than 1.6V or EN pin is left floating. The enable feature of the REF53-Q1 is designed to achieve low quiescent current (I_Q). No current is drawn from EN pin when EN pin is voltage is lower than IN pin voltage. The device must be in active mode for normal operation. The REF53-Q1 can be placed in shutdown mode by pulling the EN pin low. When in shutdown mode, the output of the device is disabled and the quiescent current of the device reduces to 6µA in shutdown mode. The EN pin must not be pulled higher than V_{IN} supply voltage. See the electrical table for logic high and logic low voltage levels.

8.4 Device Functional Modes

8.4.1 Basic Connections

Figure 8-2 shows the typical connections for the REF53-Q1. TI recommends a supply bypass capacitor (C_{IN}) >0.1µF. An output capacitor (C_{REF}) from 1µF to 50µF must connect from REF_F to GND. Connect the REF_S terminal to the VREF connection close to the load. Confirm the REF_S trace is not close to external noise sources and has low resistance. The equivalent series resistance (ESR) value of C_{REF} must be from 10mΩ to 400mΩ to provide output stability.

ADVANCE INFORMATION

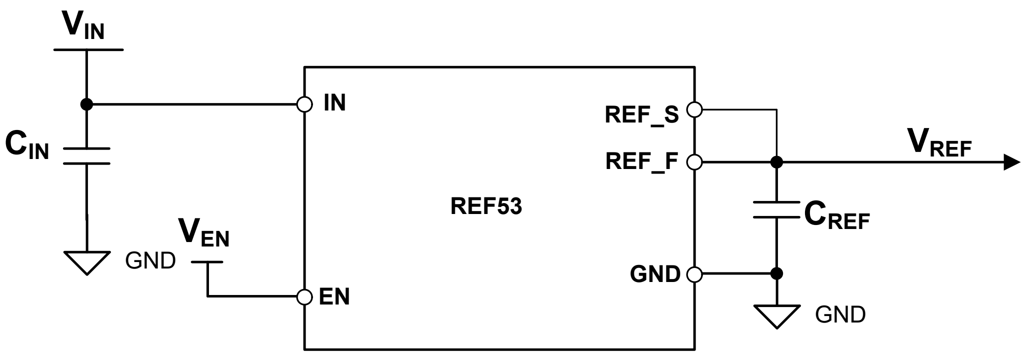


Figure 8-2. Basic Connections

ADVANCE INFORMATION

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The REF53-Q1 is designed for the applications where high precision is required at lower power. Low temperature drift and noise makes the REF53-Q1 excellent attach for high precision data converters to achieve best gain drift and resolution.

9.2 Typical Applications

9.2.1 Basic Voltage Reference Connection

Figure 9-1 shows the basic configuration for the REF53-Q1 references. Connect bypass capacitor C_{IN} and output capacitor C_{REF} as per the guidelines in Section 9.2.1.2.

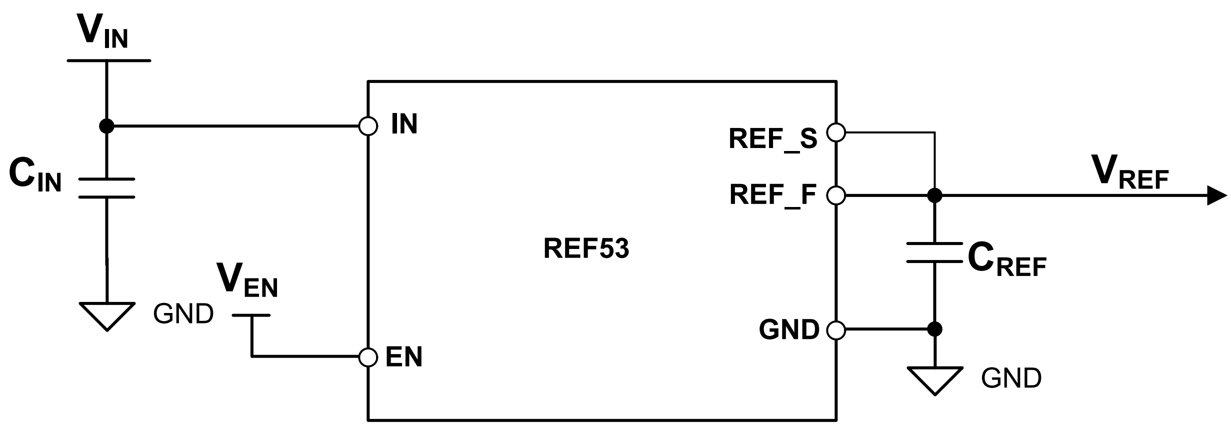


Figure 9-1. Basic Reference Connection

9.2.1.1 Design Requirements

A detailed design procedure is based on a design example. For this design example, use the parameters listed in Table 9-1 as the input parameters.

Table 9-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage, V_{IN}	3V
Input capacitor	0.1µF
Output capacitor	10µF

9.2.1.2 Detailed Design Procedure

A bulk capacitor (from 0.1µF to 10µF) must connect to the supply to improve transient response in the applications where the supply voltage can fluctuate. Connect an additional 0.1µF capacitor at VIN pin closer to the device to bypass high-frequency supply noise.

A low ESR (maximum 1Ω) capacitor from 1µF to 50µF must be connected to the output to provide stable output. For very-low-noise applications, take special care with X7R and other MLCC capacitors due to the piezoelectric effect. Piezoelectric property of multilayer ceramic capacitors (MLCC) can introduce a µV range

ADVANCE INFORMATION

noise due to mechanical vibrations, potentially dominating the noise of the REF53-Q1. More information on how the piezoelectric effect can be explored in systems can be found in Stress-induced outbursts: Microphonics in ceramic capacitors (Part 1) and Stress-induced outbursts: Microphonics in ceramic capacitors (Part 2) . Designer must use film capacitors for noise sensitive applications. TI recommends placing the REF53-Q1 reference as close to the load as possible to minimize IR drop due to trace resistance.

The turn-on time response of the REF53-Q1 is shown in Figure 9-2. The turn-on time of the REF53-Q1 family depends on the reference pin capacitor. Increasing the output capacitor improves the load transient performance of the device, however this also increases the turn-on time. Figure 9-3 shows the turn-on time with C_{REF} = 10µF, increases to 1msec.

9.2.1.3 Application Curves

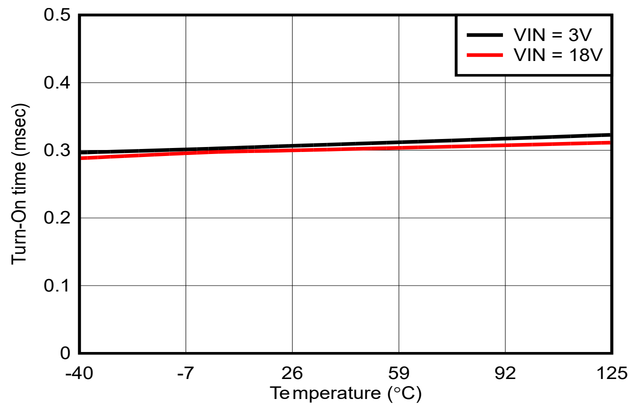


Figure 9-2. REF53250QDDCRQ1 Turn-On time (C_{REF}= 1uF, C_{IN}= 0.1uF)

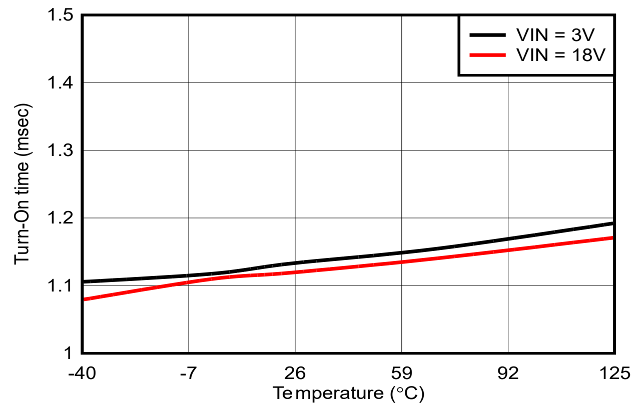


Figure 9-3. REF53250QDDCRQ1 Turn-On time (C_{REF}= 10uF, C_{IN}= 0.1uF)

9.2.2 Constant Current Reference

Multiple applications such as sensor biasing, LED driving, battery charging, and so forth need, precision constant current source. REF53-Q1 device with precision performance, wide input voltage support, multiple output voltage options meets various application level requirements to be configured as constant current source.

Figure 9-4 shows REF53-Q1 configured as a constant current source. REF53-Q1 is configured as floating device with device GND driving the load. The precision voltage reference from REF53-Q1 along with an external precision reference draw a constant current from the input supply denoted as 'I'. The effective current flowing through the load is combination of REF53-Q1 device quiescent current and the programmed value I. The wide VIN voltage support of REF53-Q1 allows for wide voltage variation across the load while still maintaining the constant current accuracy.

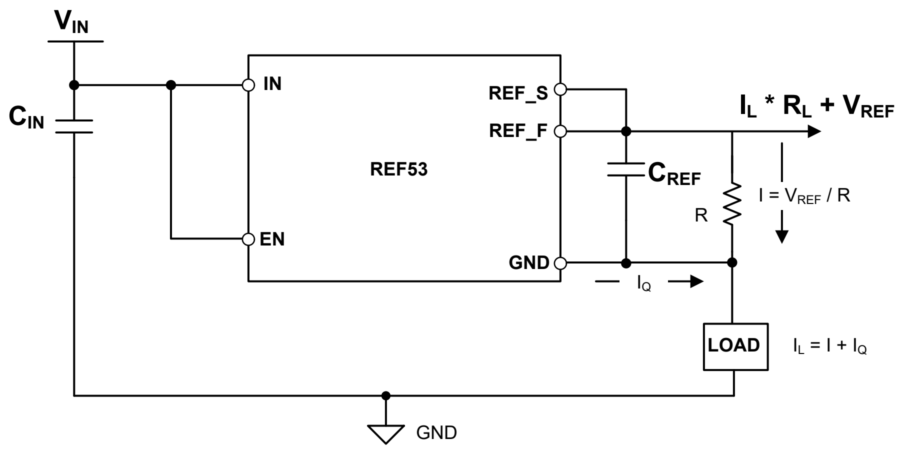


Figure 9-4. REF53-Q1 Configuration as Constant Current Source

Table 9-2 shows the measured results as per the design shown in Figure 9-4.

Table 9-2. Constant Current Source Results

V_{REF}	R	CALCULATED CURRENT	MEASURED CURRENT
1.25V	1.4kΩ	0.978mA	0.998mA
1.25V	127Ω	9.93mA	9.98mA
1.25V	62Ω	20.24mA	20.33mA

9.3 Power Supply Recommendation

The REF53-Q1 family of references features a low-dropout voltage. These references can operate with a supply of only 250mV above the output voltage for 5mA output current conditions at room temperature. TI recommends a supply bypass capacitor ranging from 0.1µF to 10µF. REF53-Q1 family have excellent PSRR which relaxes the requirement of clean power supply for the designer.

During start-up the REF53-Q1 can experience moments of high input current due to the output capacitors. The input current can momentarily rise to short-circuit current I_{SC}.

9.4 Layout

9.4.1 Layout Guidelines

- Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is from 0.1µF to 10µF. If necessary, add additional decoupling capacitance to compensate for noisy or high-impedance power supplies. Place the smallest capacitor closest to the device.
- The output must be decoupled with a from 1µF to 100µF low ESR capacitor.
- Connect the REF_S (sense) to the REF_F (force) pin externally through a trace. Short these traces close to the point of load. Make sure the sense signal path is low resistance and is not exposed to high noise generating devices on the board.

ADVANCE INFORMATION

ADVANCE INFORMATION

9.4.2 Layout Example

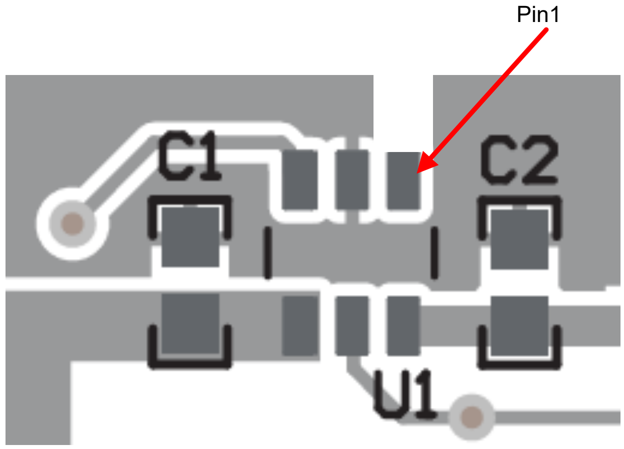


Figure 9-5. Layout Example for Thin SOT Package

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Voltage Reference Design Tips For Data Converters*
- Texas Instruments, *Voltage Reference Selection Basics*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

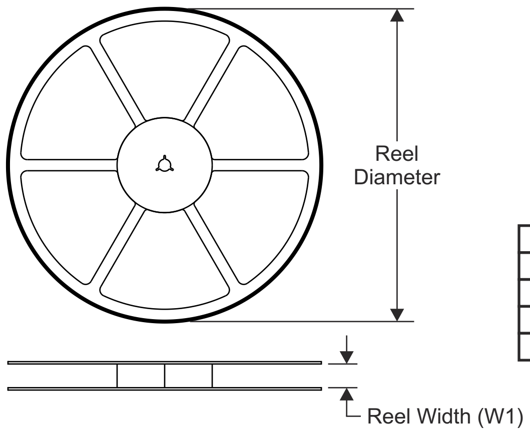
DATE	REVISION	NOTES
August 2026	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

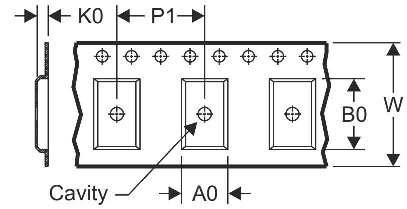
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Tape and Reel Information

REEL DIMENSIONS

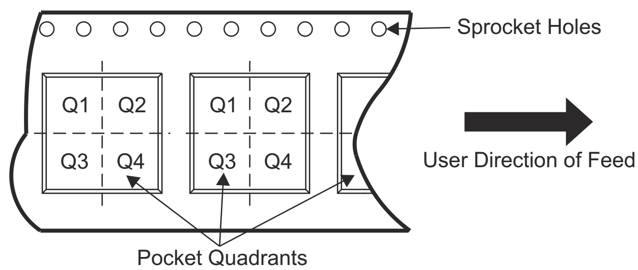


TAPE DIMENSIONS



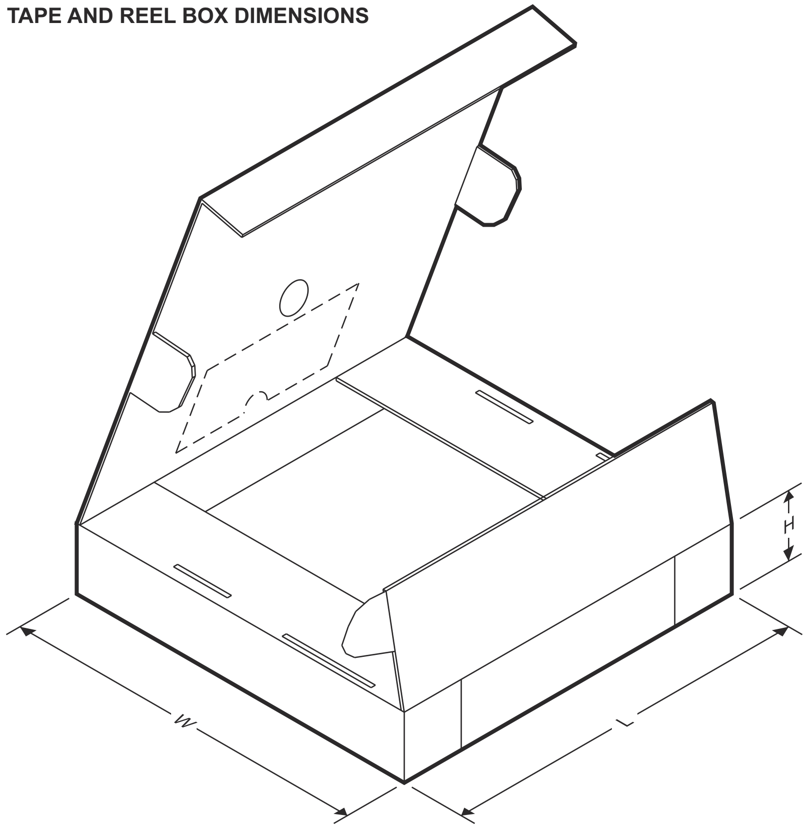
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF53-Q1	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

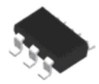


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF53-Q1	SOT-23- THIN	DDC	6	3000	213.0	191.0	35.0

ADVANCE INFORMATION

12.2 Mechanical Data

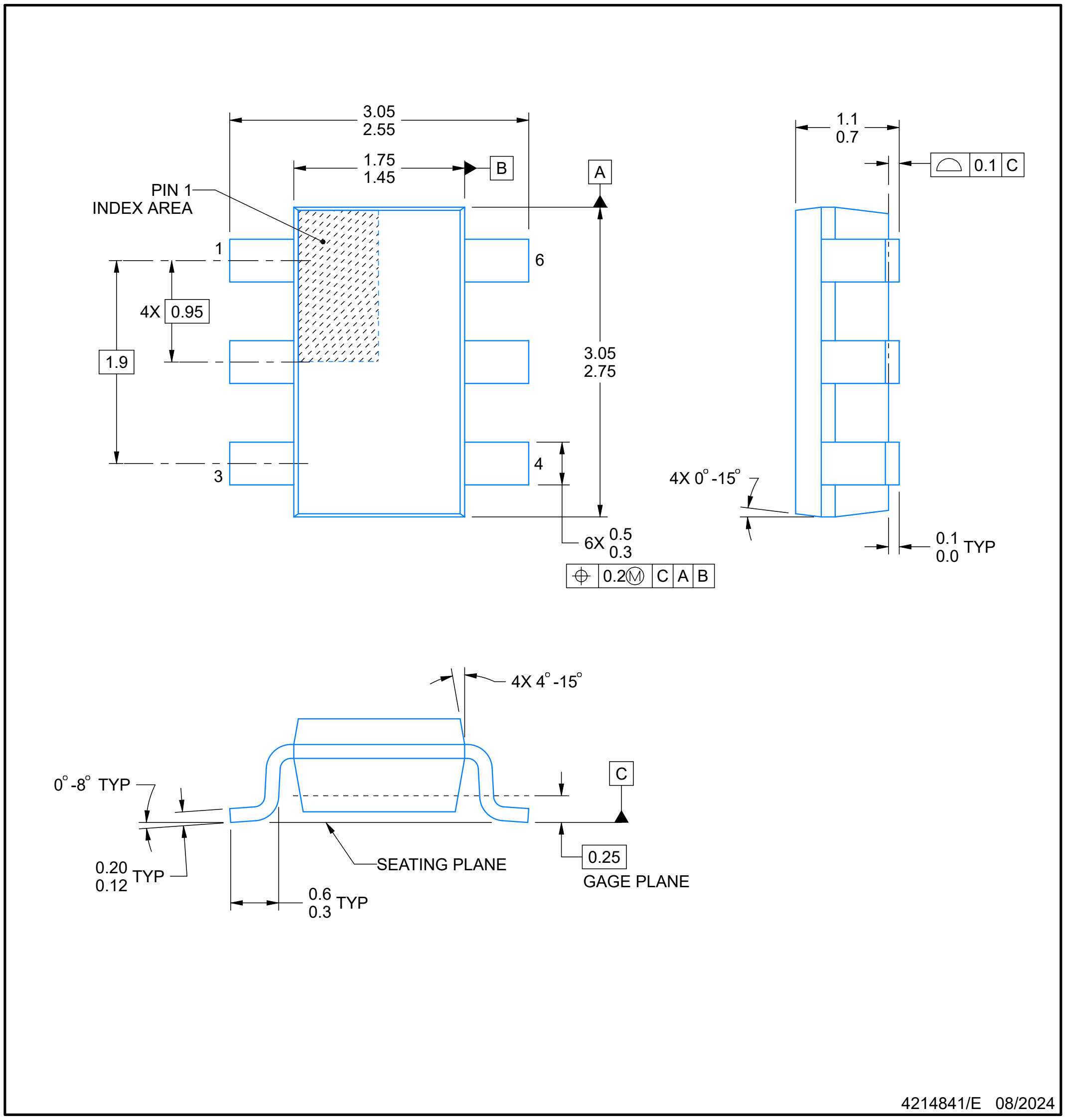
DDC0006A



PACKAGE OUTLINE

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.

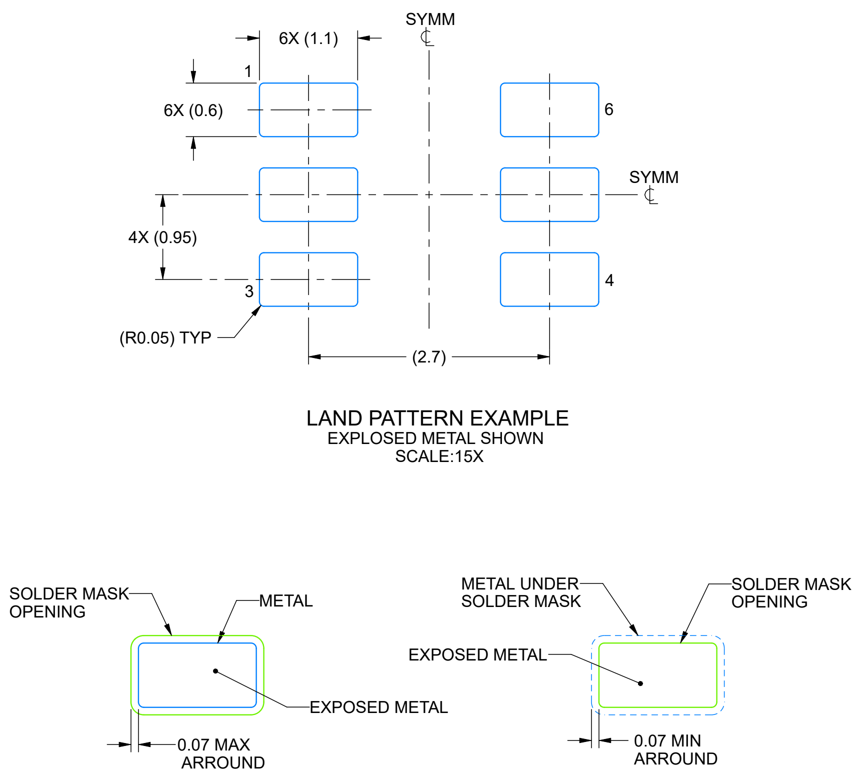
www.ti.com

EXAMPLE BOARD LAYOUT

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

ADVANCE INFORMATION

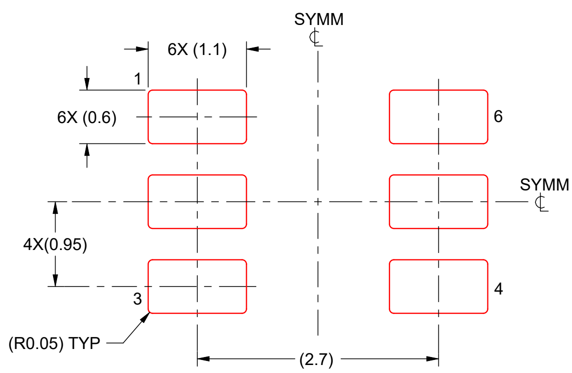
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

www.ti.com

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PREF53125AQDDCRQ1	Active	Preproduction	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE AND DISCLAIMER