QML CLASS V PRECISION TIMER

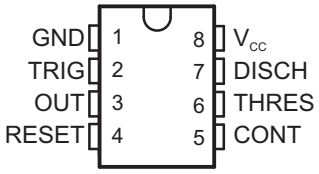
Check for Samples: SE555-SP

FEATURES

- **Timing From Microseconds to Hours**
- **Astable or Monostable Operation**
- **Adjustable Duty Cycle**
- **TTL-Compatible Output Can Sink or Source up to 100 mA**
- **QML-V Qualified, SMD 5962-98555**
- **Military Temperature Range (-55°C to 125°C)**
- **Rad-Tolerant: 25 kRad (Si) TID** (1)

(1) Radiation tolerance is a typical value based upon initial device qualification with dose rate = 10 mrad/sec. Radiation Lot Acceptance Testing is available - contact factory for details.

JG PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SE555 is a precision timing circuit capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

The threshold and trigger levels normally are two-thirds and one-third, respectively, of V_{CC}. These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set, and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset, and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

The output circuit is capable of sinking or sourcing current up to 100 mA. Operation is specified for supplies of 4.5 V to 16.5 V. With a 5-V supply, output levels are compatible with TTL inputs.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	CDIP - JG	Tube of 50	5962-9855501VPA	5962-9855501VPA

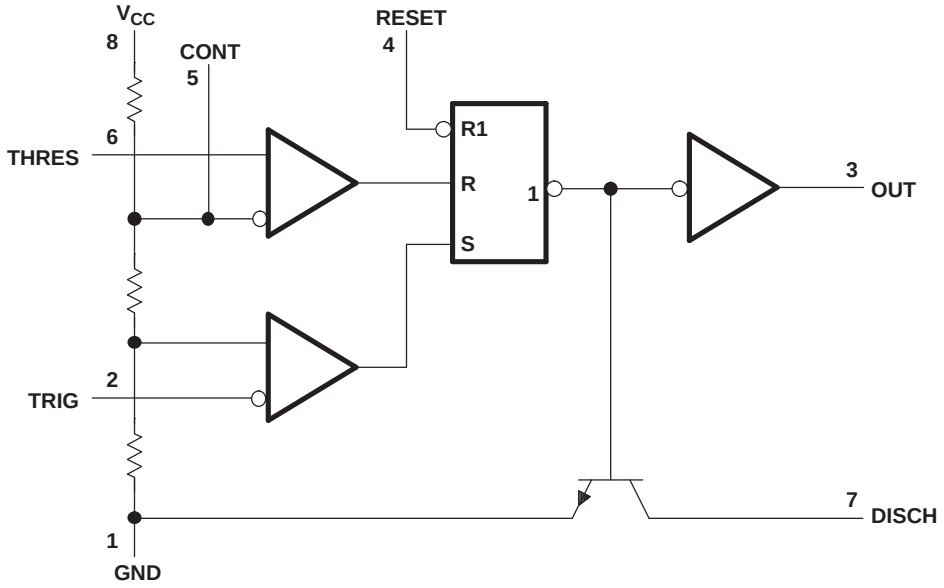
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Table 1. FUNCTION TABLE

RESET	TRIGGER VOLTAGE(1)	THRESHOLD VOLTAGE(1)	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	<1/3 V_{CC}	Irrelevant	High	Off
High	>1/3 V_{CC}	>2/3 V_{CC}	Low	On
High	>1/3 V_{CC}	<2/3 V_{CC}	As previously established	

(1) Voltage levels shown are nominal.

FUNCTIONAL BLOCK DIAGRAM



A. RESET can override TRIG, which can override THRES.

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Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)			18	V
V_I	Input voltage	CONT, RESET, THRES, TRIG		V_{CC}	V
I_O	Output current			±200	mA
θ_{JC}	Package thermal impedance(3) (4)			45	°C/W
T_J	Operating virtual junction temperature			150	°C
	Lead temperature 1, 6 mm (1/16 in) from case for 60 s			300	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Maximum power dissipation is a function of $T_J(max)$, θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(max) - T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with MIL-STD-883.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	16.5	V
V_I	Input voltage	CONT, RESET, THRES, and TRIG		V_{CC}	V
I_O	Output current			±100	mA
T_A	Operating free-air temperature		–55	125	°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5 V to 16.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Power supply current	V_{CC} = 4.5 V, RL = ∞	T_A = 25°C, 125°C, –55°C			5	mA
		V_{CC} = 16.5 V, RL = ∞	T_A = 25°C, 125°C, –55°C			20	
V_{TR}	Trigger voltage	V_{CC} = 4.5 V	T_A = 25°C	1.30		1.80	V
			T_A = 125°C	1.30		2.10	
			T_A = –55°C	1.15		1.80	
		V_{CC} = 16.5 V	T_A = 25°C	5.20		5.80	
			T_A = 125°C	5.20		6.10	
			T_A = –55°C	5		5.80	
I_{TR}	Trigger current	V_{CC} = 16.5 V for V_{TR} = 5 V	T_A = 25°C, 125°C, –55°C	–5			µA
V_{TH}	Threshold voltage	V_{CC} = 4.5 V	T_A = 25°C	2.70		3.30	V
			T_A = 125°C, –55°C	2.60		3.40	
		V_{CC} = 16.5 V	T_A = 25°C	10.70		11.30	
			T_A = 125°C, –55°C	10.60		11.40	
I_{TH}	Threshold current	V_{CC} = 16.5 V	T_A = 25°C, 125°C			250	nA
			T_A = –55°C			2.5	µA

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ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 4.5 V to 16.5 V, over operating free-air temperature range (unless otherwise noted)

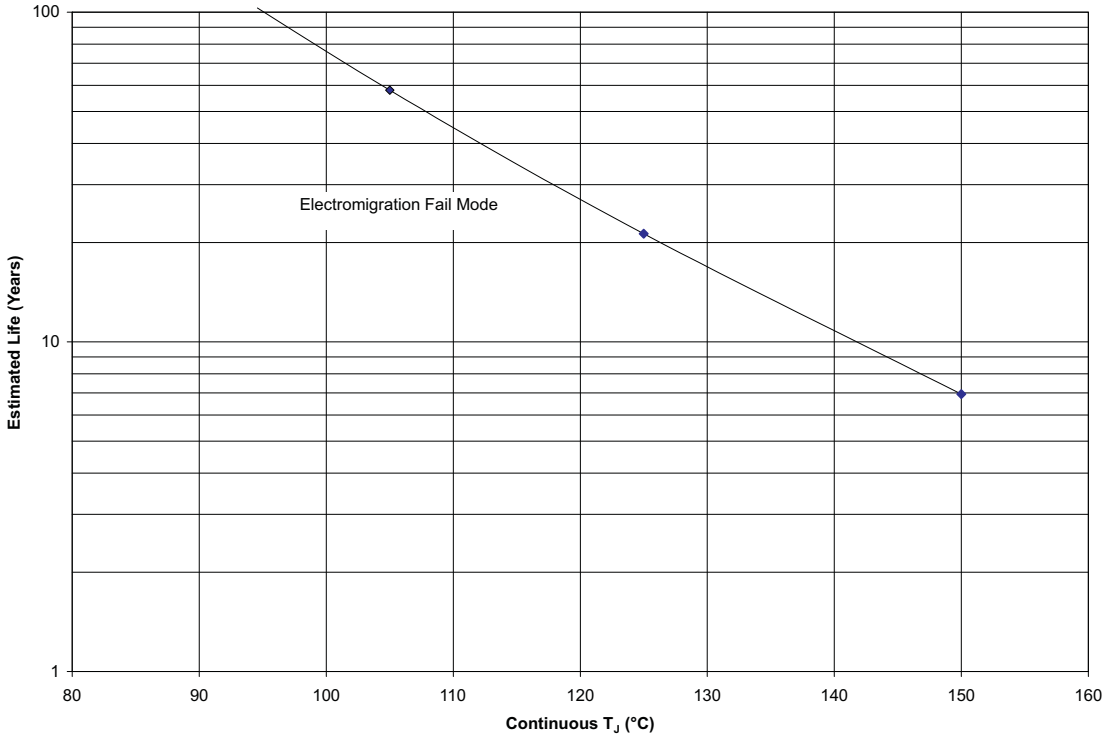
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OL}	Low level output voltage	V_{CC} = 4.5 V, I_{SINK} = 5 mA	T_A = 25°C			0.25	V
			T_A = 125°C, –55°C			0.35	
		V_{CC} = 4.5 V, I_{SINK} = 50 mA	T_A = 25°C, 125°C			2.20	
			T_A = –55°C			2.60	
		V_{CC} = 16.5 V, I_{SINK} = 10 mA	T_A = 25°C, –55°C			0.15	
			T_A = 125°C			0.25	
		V_{CC} = 16.5 V, I_{SINK} = 50 mA	T_A = 25°C, –55°C			0.50	
			T_A = 125°C			0.70	
		V_{CC} = 16.5 V, I_{SINK} = 100 mA	T_A = 25°C			2.20	
			T_A = 125°C, –55°C			2.80	
V_{OH}	High level output voltage	V_{CC} = 4.5 V, I_{SOURCE} = –100 mA	T_A = 25°C, 125°C	2.60			V
			T_A = –55°C	2.20			
		V_{CC} = 16.5 V, I_{SOURCE} = –100 mA	T_A = 25°C, 125°C	14.60			
			T_A = –55°C	14			
I_{CEX}	Discharge transistor leakage current	V_{CC} = 16.5 V	T_A = 25°C, –55°C			100	nA
			T_A = 125°C			3	µA
V_{SAT}	Discharge transistor saturation voltage	V_{CC} = 16.5 V, I_D = 50 mA	T_A = 25°C, –55°C			0.80	V
			T_A = 125°C			1	
V_R	Reset voltage	V_{CC} = 16.5 V	T_A = 25°C, 125°C, –55°C	0.10		1.30	V
I_R	Reset current	V_{CC} = 16.5 V, V_R = 0 V	T_A = 25°C, 125°C, –55°C	–1.60		0	mA
t_{PLH}	Propgation delay time, low to high level output (monostable)	4.5 V ≤ V_{CC} ≤ 16.5 V, R_T = 1 kΩ, C_T = 0.1 µF	T_A = 25°C, –55°C			800	ns
			T_A = 125°C			900	
t_{TLH}	Transition time, low to high level output (monostable)	4.5 V ≤ V_{CC} ≤ 16.5 V, R_T = 1 kΩ, C_T = 0.1 µF	T_A = 25°C, 125°C, –55°C			300	ns
t_{THL}	Transition time, high to low level output (monostable)	4.5 V ≤ V_{CC} ≤ 16.5 V, R_T = 1 kΩ, C_T = 0.1 µF	T_A = 25°C, 125°C, –55°C			300	ns
$t_{D(OH)}$	Time delay, output high (monostable)	4.5 V ≤ V_{CC} ≤ 16.5 V, R_T = 1 kΩ, C_T = 0.1 µF	T_A = 25°C, 125°C, –55°C	106.70		113.30	µs
		4.5 V ≤ V_{CC} ≤ 16.5 V, R_T = 100 kΩ, C_T = 0.1 µF		10.67		11.33	ms
$\Delta t_{D(OH)}$ / ΔV_{CC}	Drift in time delay versus change in supply voltage (monostable)	ΔV_{CC} = 12 V, R_T = 1 kΩ, C_T = 0.1 µF	T_A = 25°C	–220		220	ns/V
t_{PHL}	Propogation delay time, threshold to output	4.5 V ≤ V_{CC} ≤ 16.5 V, R_T = 1 kΩ	T_A = 25°C, 125°C, –55°C			12	µs
$\Delta t_{D(OH)}$ / ΔT	Temperature coefficient of time delay (monostable)	V_{CC} = 16.5 V, R_T = 1 kΩ, C_T = 0.1 µF	T_A = 125°C, –55°C	–11		11	ns/°C
t_{ch}	Capacitor charge time (astable)	4.5 V ≤ V_{CC} ≤ 16.5 V, R_{TA} = R_{TB} = 1 kΩ, C_T = 0.1 µF	T_A = 25°C, 125°C, –55°C	120		156	µs
		4.5 V ≤ V_{CC} ≤ 16.5 V, R_{TA} = R_{TB} = 100 kΩ, C_T = 0.1 µF		11.30		15	ms
t_{dis}	Capacitor discharge time (astable)	4.5 V ≤ V_{CC} ≤ 16.5 V, R_{TA} = R_{TB} = 1 kΩ, C_T = 0.1 µF	T_A = 25°C, 125°C, –55°C	57.50		80	µs
		4.5 V ≤ V_{CC} ≤ 16.5 V, R_{TA} = R_{TB} = 100 kΩ, C_T = 0.1 µF		5.40		7.70	ms

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ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 4.5 V to 16.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\Delta t_{ch} / \Delta V_{CC}$	Drift in capacitor charge time versus change in supply voltage (astable)	ΔV_{CC} = 12 V, $R_{TA} = R_{TB}$ = 1 kΩ, C_T = 0.1 μF	T_A = 25°C	–820		820	ns/V
$\Delta t_{ch} / \Delta T$	Temperature coefficient of capacitor charge time (astable)	ΔV_{CC} = 16.5 V, $R_{TA} = R_{TB}$ = 1 kΩ, C_T = 0.1 μF	T_A = 125°C, –55°C	–68		68	ns/°C
t_{res}	Reset time	V_{CC} = 16.5 V	T_A = 25°C, –55°C			1.50	μs
			T_A = 125°C			2	



A. See datasheet for absolute maximum and minimum recommended operating conditions.

B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

Figure 1. SE555 8/JG Package Operating Life Derating Chart

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TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

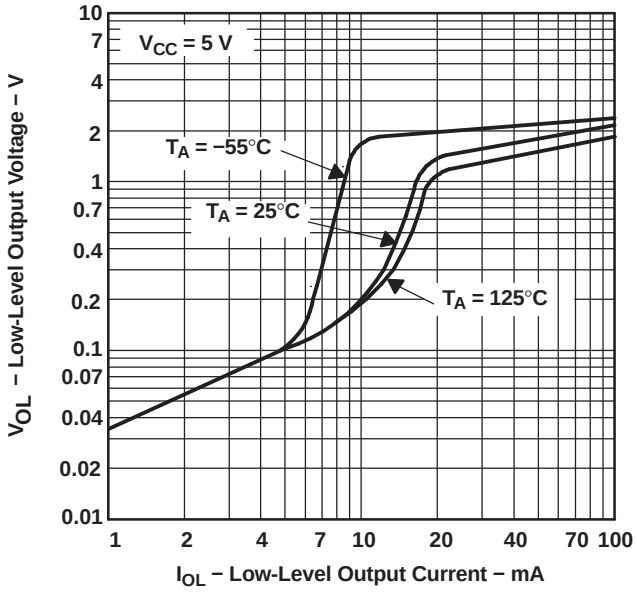


Figure 2.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

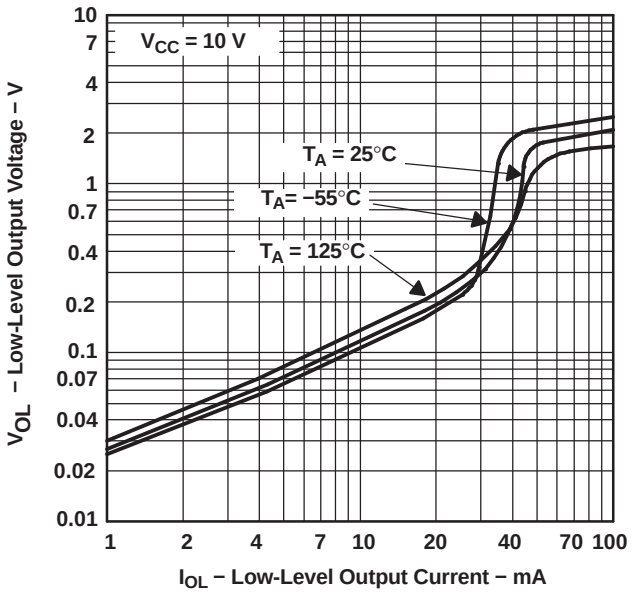


Figure 3.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

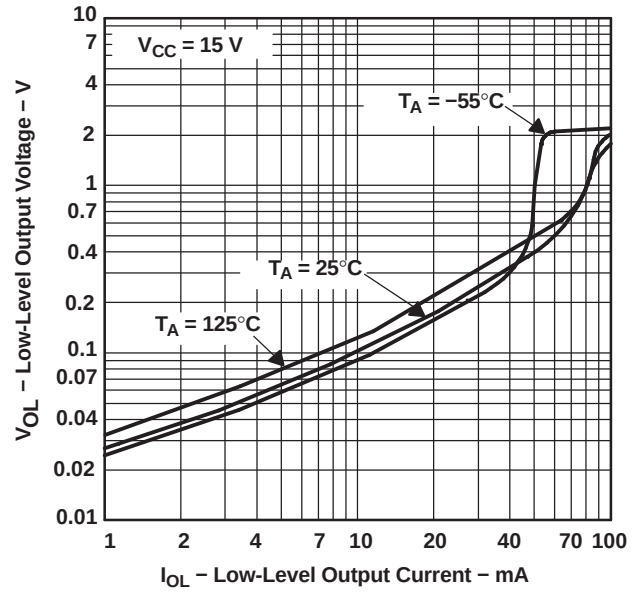


Figure 4.

DROP BETWEEN SUPPLY VOLTAGE AND OUTPUT
vs
HIGH-LEVEL OUTPUT CURRENT

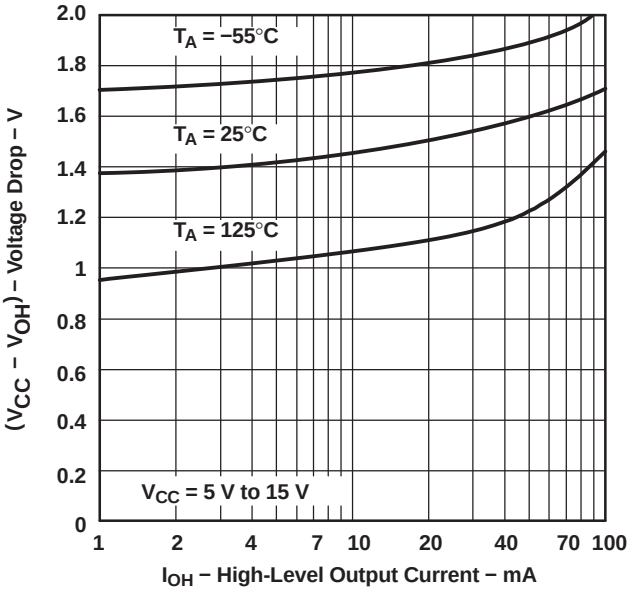


Figure 5.

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TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

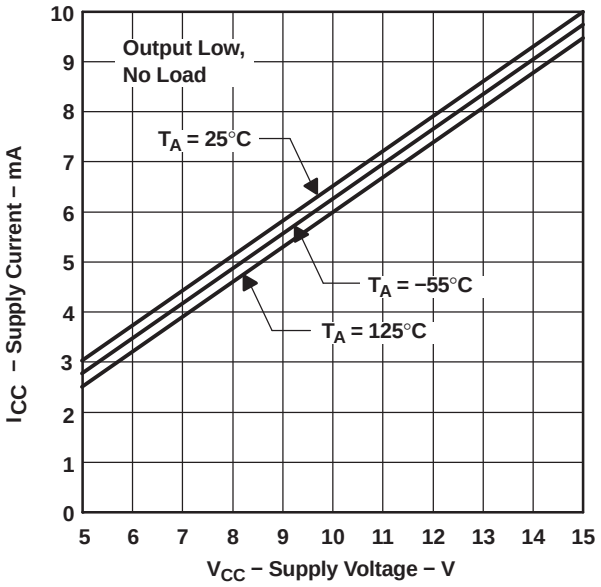


Figure 6.

NORMALIZED OUTPUT PULSE DURATION
(MONOSTABLE OPERATION)
vs
SUPPLY VOLTAGE

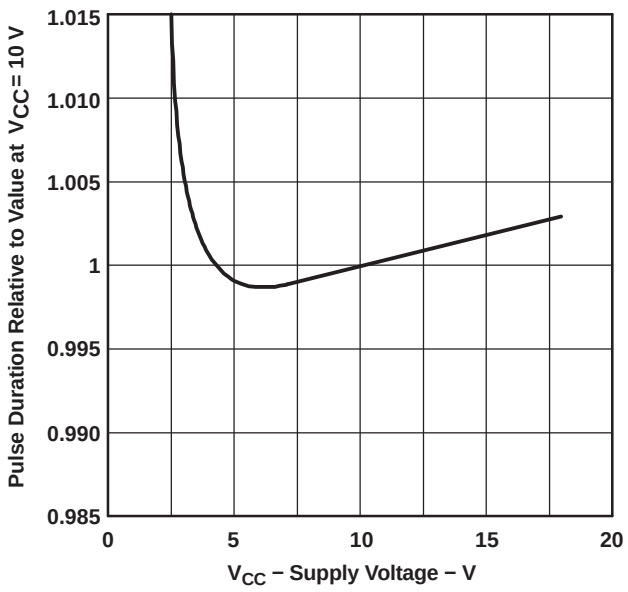


Figure 7.

NORMALIZED OUTPUT PULSE DURATION
(MONOSTABLE OPERATION)
vs
FREE-AIR TEMPERATURE

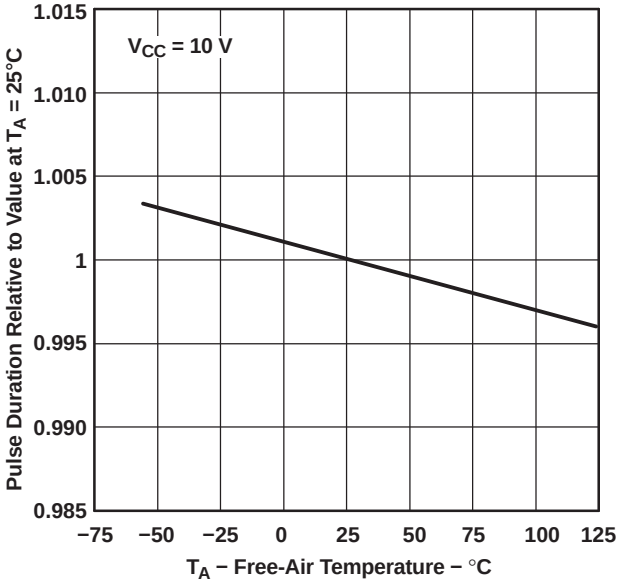


Figure 8.

PROPAGATION DELAY TIME
vs
LOWEST VOLTAGE LEVEL
OF TRIGGER PULSE

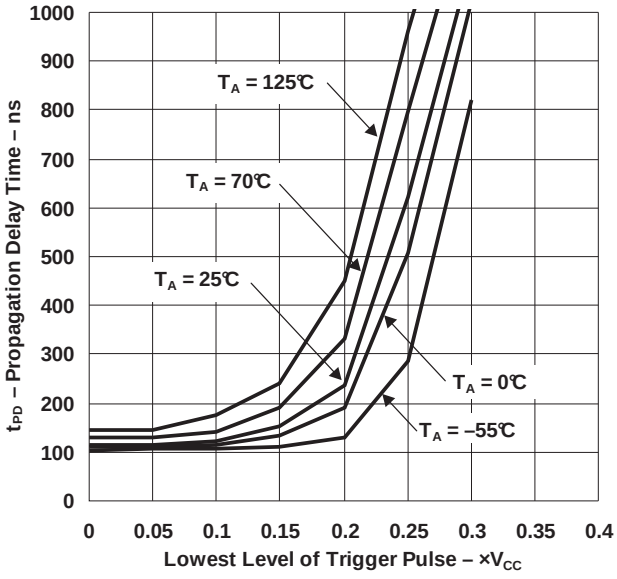


Figure 9.

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APPLICATION INFORMATION

Monostable Operation

For monostable operation, any of these timers can be connected as shown in Figure 10. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the flip-flop ($\overline{Q}$ goes low), drives the output high, and turns off Q1. Capacitor C then is charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the flip-flop ($\overline{Q}$ goes high), drives the output low, and discharges C through Q1.

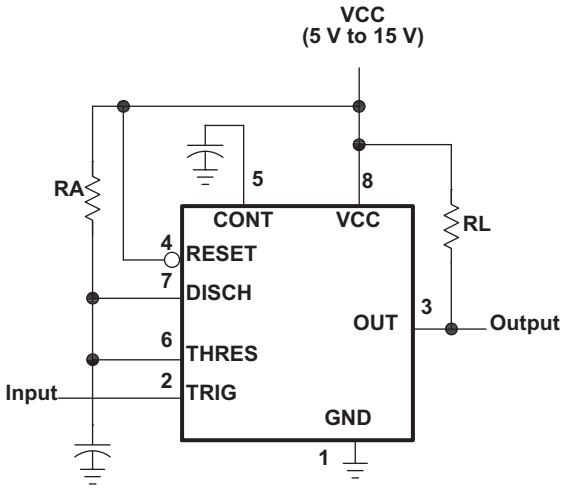


Figure 10. Circuit for Monostable Operation

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high at the end of the timing interval. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_w = 1.1R_AC$. Figure 12 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates both are directly proportional to the supply voltage, V_{CC}. The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used, it should be connected to V_{CC}.

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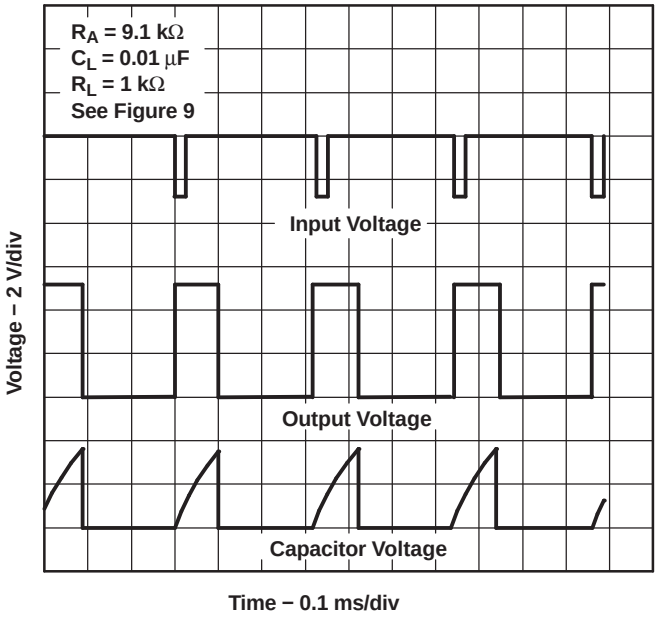


Figure 11. Typical Monostable Waveforms

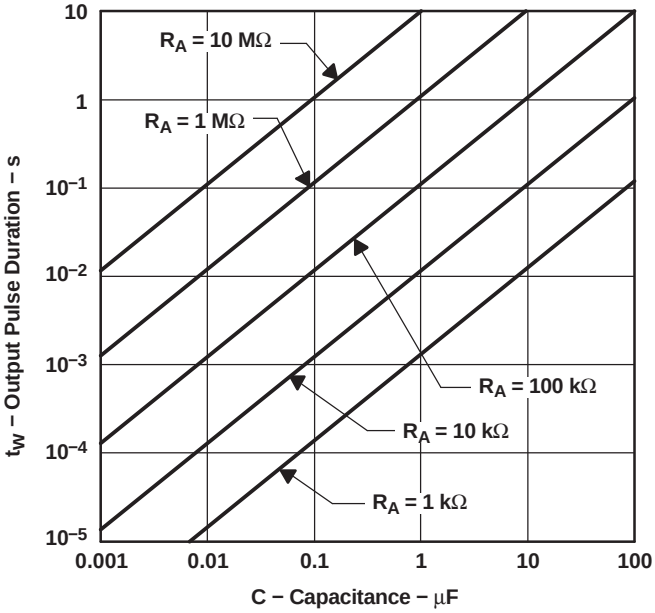
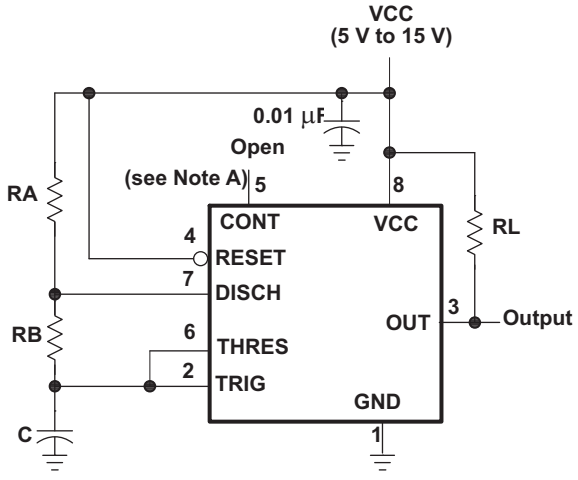


Figure 12. Output Pulse Duration vs Capacitance

Astable Operation

As shown in Figure 13, adding a second resistor, R_B, to the circuit of Figure 10 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level (X0.67 × V_{CC}) and the trigger-voltage level (X0.33 × V_{CC}). As in the monostable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.



NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

Figure 13. Circuit for Astable Operation

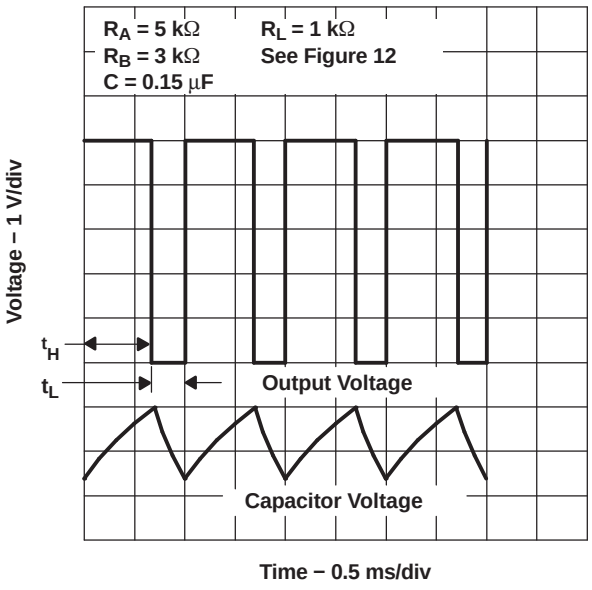


Figure 14. Typical Astable Waveforms

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Figure 13 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L can be calculated as follows:

$$t_H = 0.693\ (R_A + R_B)\ C \quad (1)$$

$$t_L = 0.693\ (R_B)\ C \quad (2)$$

Other useful relationships are shown in the following equations.

$$period = t_H + t_L = 0.693\ (R_A + 2R_B)\ C \quad (3)$$

$$frequency \approx \frac{1.44}{(R_A + 2R_B)\ C} \quad (4)$$

$$Output\ driver\ duty\ cycle = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B} \quad (5)$$

$$Output\ waveform\ duty\ cycle = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B} \quad (6)$$

$$Low\text{-}to\text{-}high\ ratio = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B} \quad (7)$$

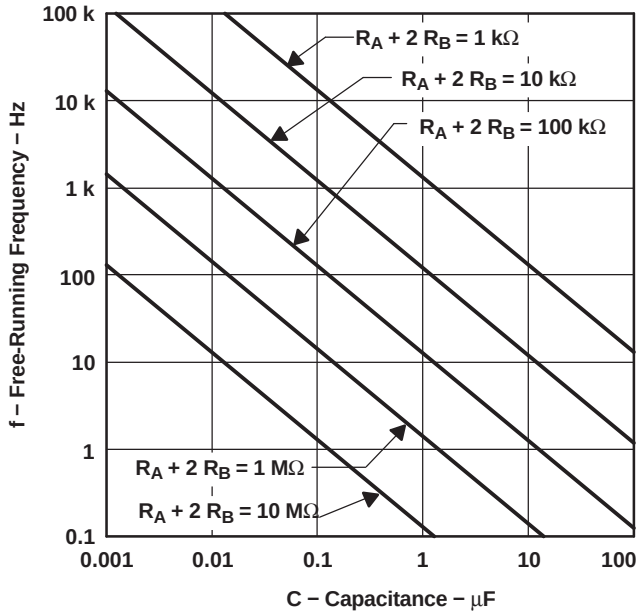


Figure 15. Free-Running Frequency

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Missing-Pulse Detector

The circuit shown in Figure 16 can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is retriggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in Figure 17.

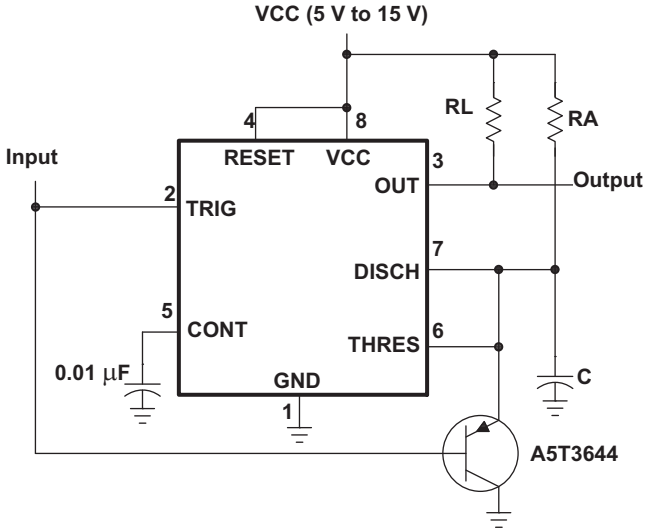


Figure 16. Circuit for Missing-Pulse Detector

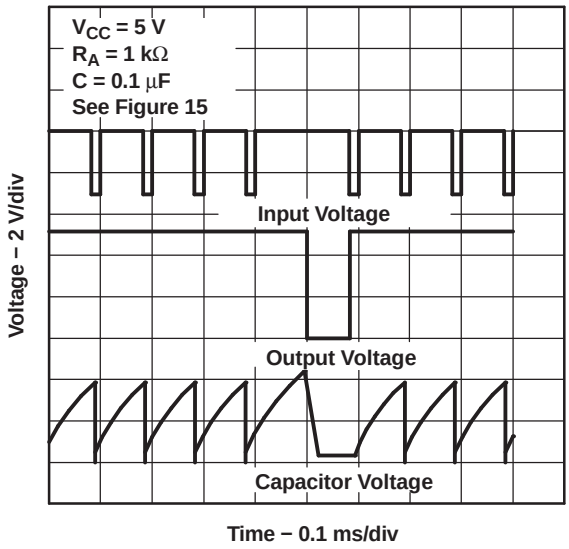


Figure 17. Completed Timing Waveforms for Missing-Pulse Detector

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Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of Figure 10 can be made to operate as a frequency divider. Figure 18 shows a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

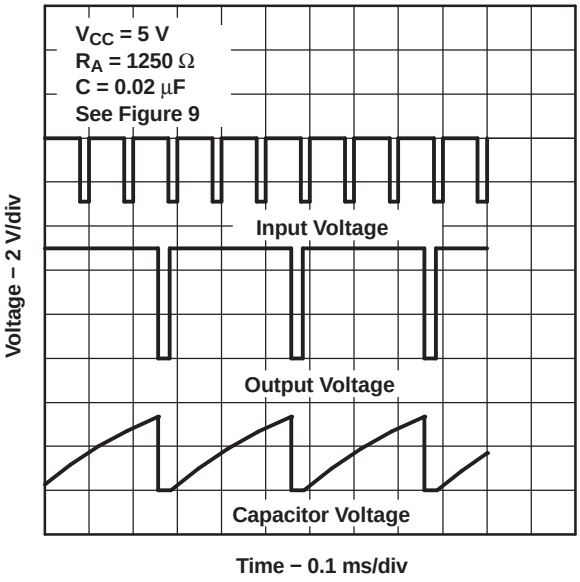
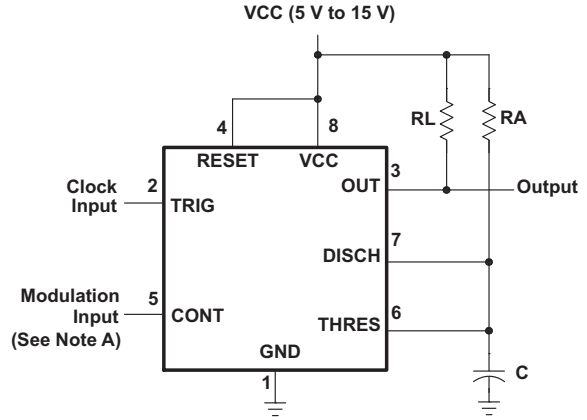


Figure 18. Divide-by-Three Circuit Waveforms

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Pulse-Width Modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 19 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 20 shows the resulting output pulse-width modulation. While a sine-wave modulation signal is shown, any wave shape could be used.



NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 19. Circuit for Pulse-Width Modulation

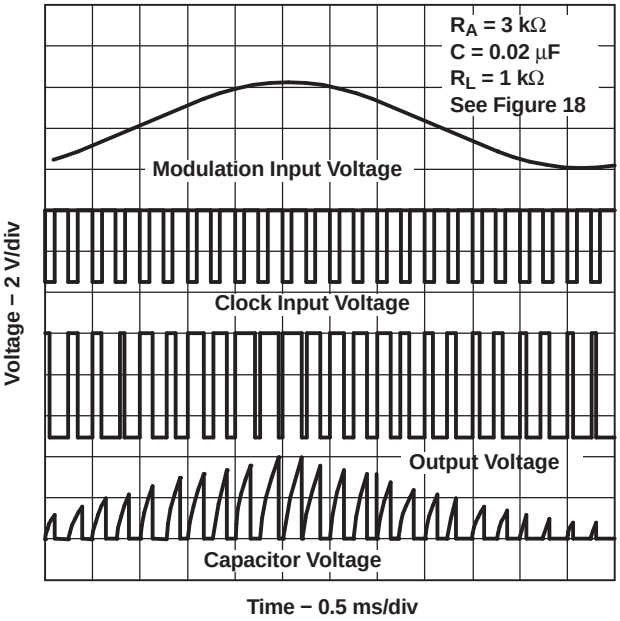
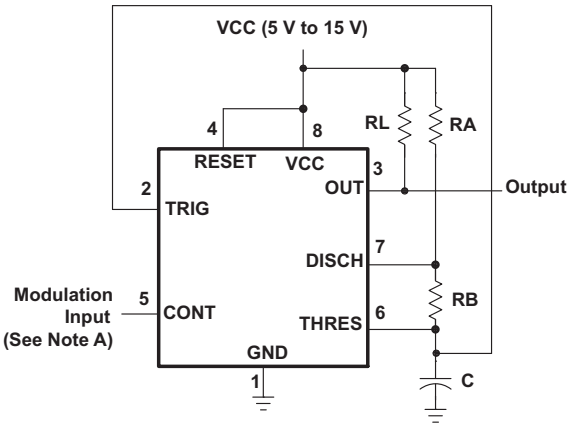


Figure 20. Pulse-Width-Modulation Waveforms

Pulse-Position Modulation

As shown in Figure 21, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and, thereby, the time delay, of a free-running oscillator. Figure 22 shows a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.



NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 21. Circuit for Pulse-Position Modulation

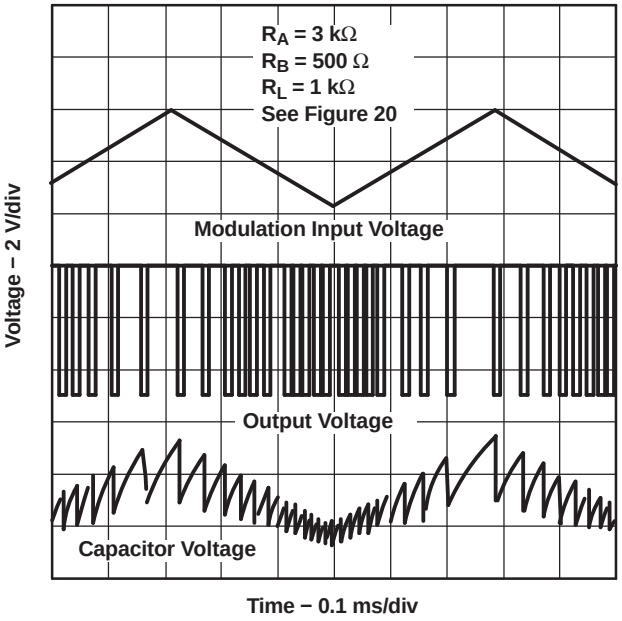
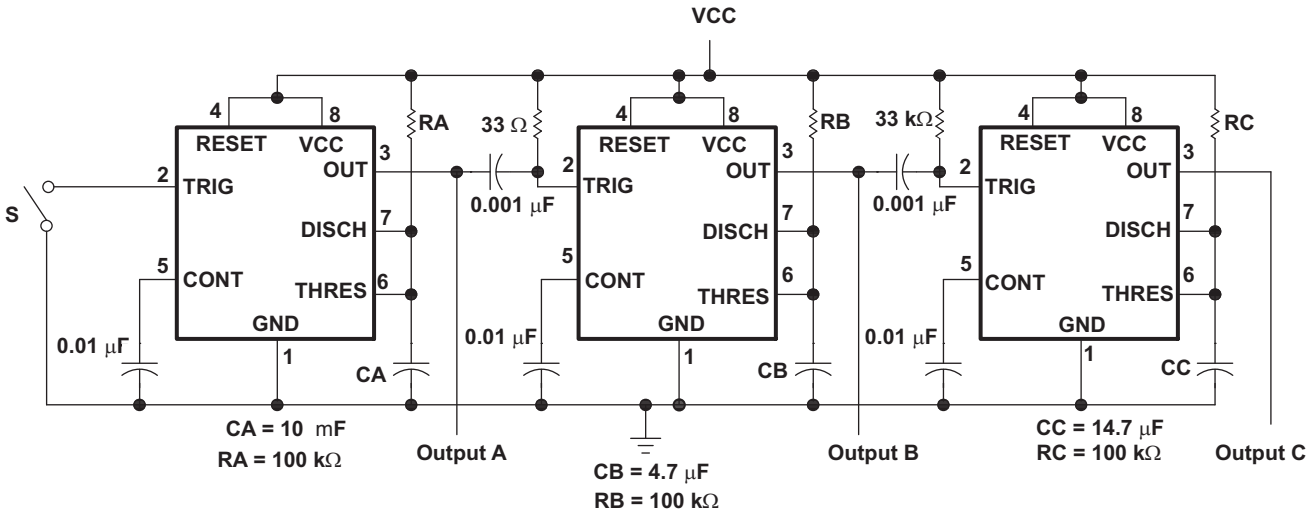


Figure 22. Pulse-Position-Modulation Waveforms

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Sequential Timer

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 23 shows a sequencer circuit with possible applications in many systems, and Figure 24 shows the output waveforms.



NOTE A: S closes momentarily at t = 0.

Figure 23. Sequential Timer Circuit

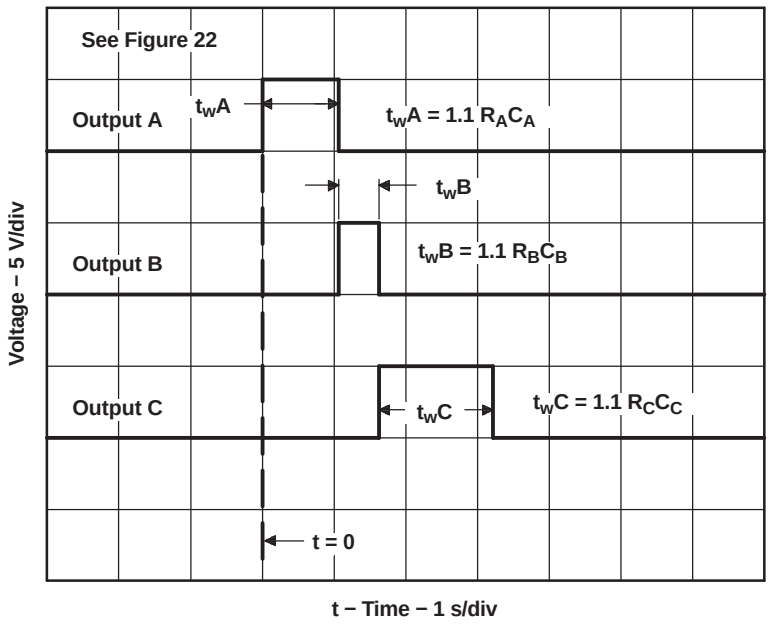


Figure 24. Sequential Timer Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9855501VPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9855501VPA
5962-9855501VPA.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9855501VPA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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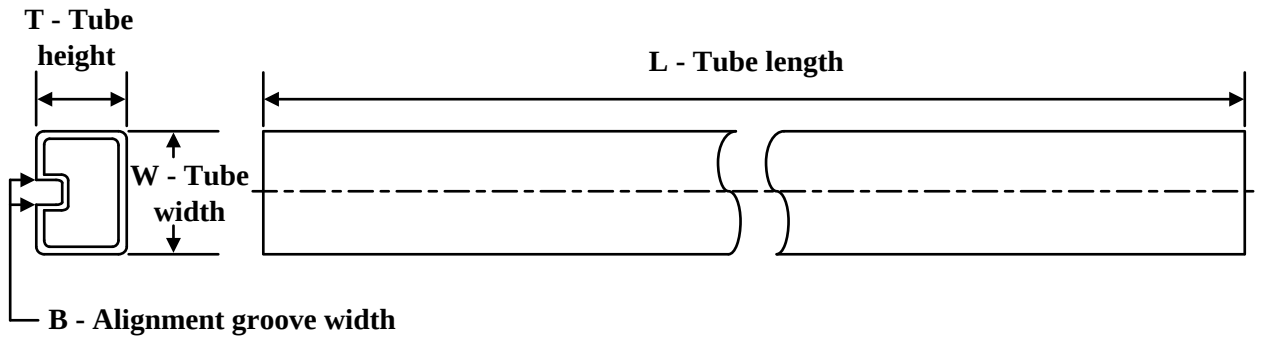
OTHER QUALIFIED VERSIONS OF SE555-SP :

- Catalog : SE555
- Military : SE555M

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE



*All dimensions are nominal

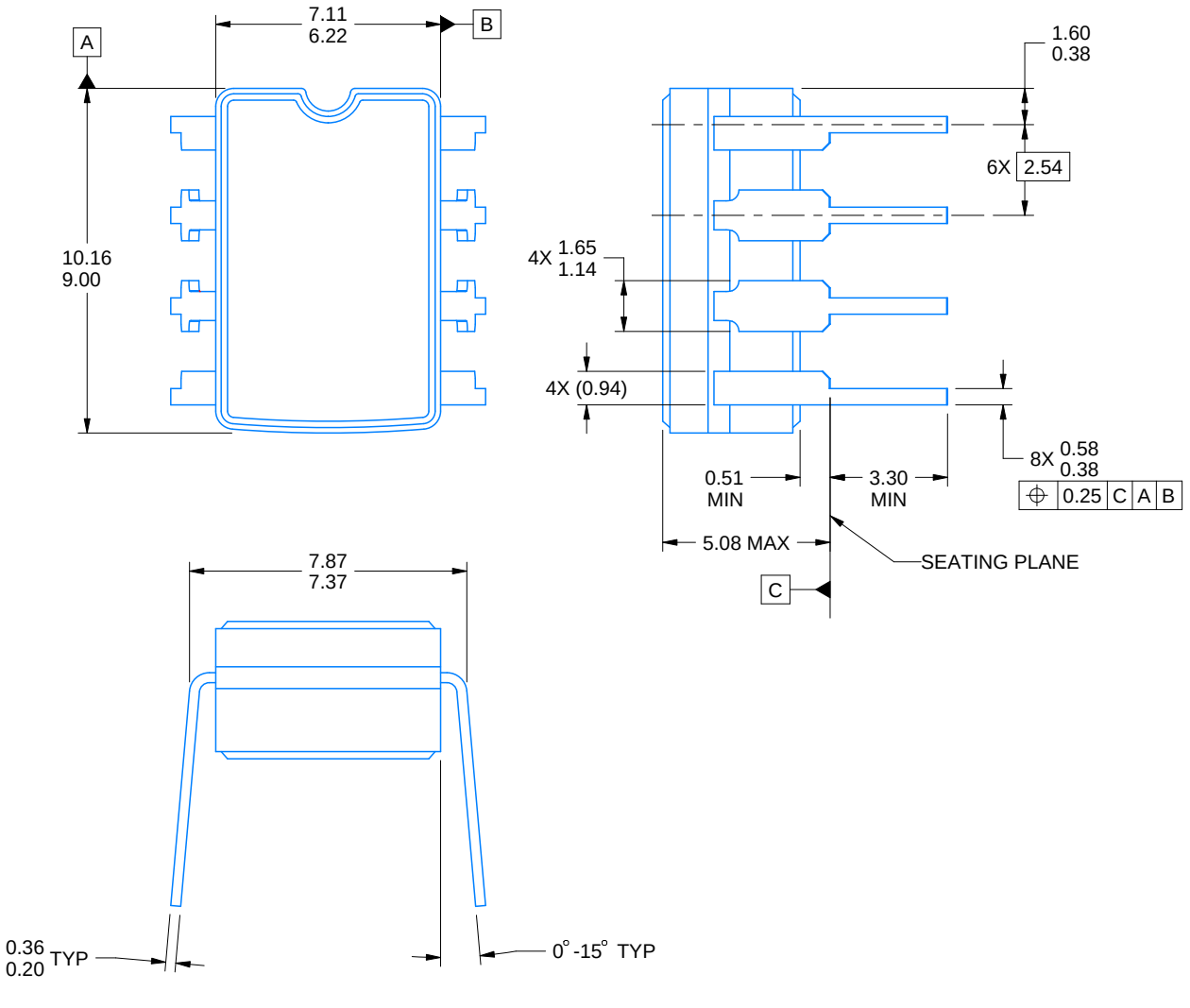
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9855501VPA	JG	CDIP	8	50	506.98	15.24	13440	NA
5962-9855501VPA.A	JG	CDIP	8	50	506.98	15.24	13440	NA

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



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NOTES:

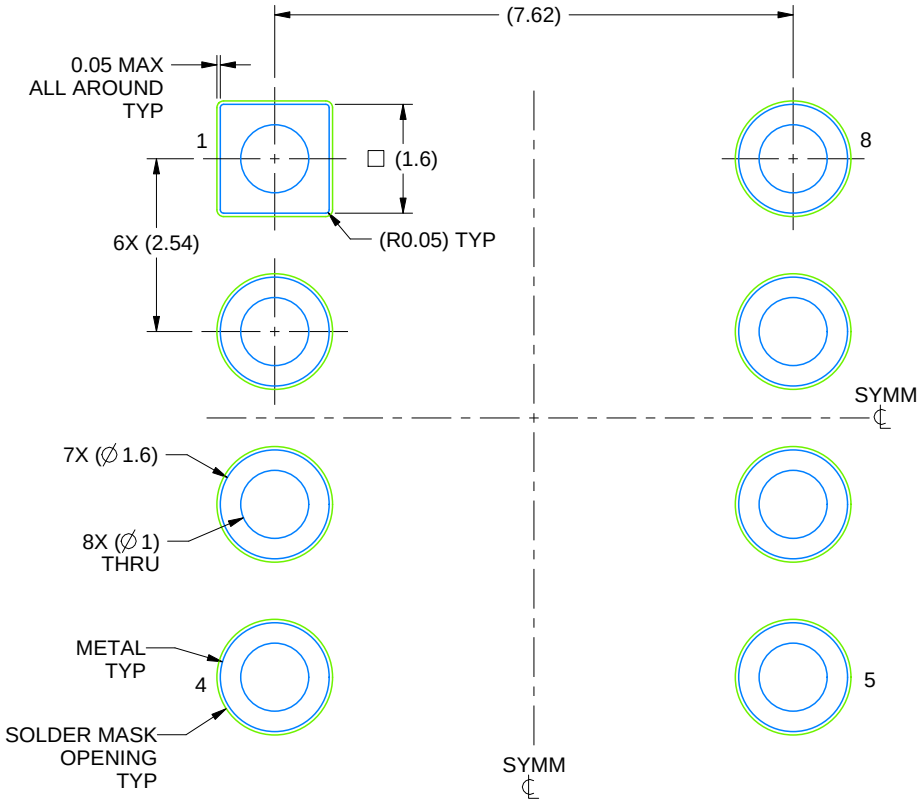
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

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Last updated 10/2025