

SN54ABT16543, SN74ABT16543 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS087C – FEBRUARY 1991 – REVISED JANUARY 1997

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

description

The 'ABT16543 16-bit registered transceivers contain two sets of D-type latches for temporary storage of data flowing in either direction. The 'ABT16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16543 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16543 is characterized for operation from -40°C to 85°C .

SN54ABT16543 . . . WD PACKAGE
SN74ABT16543 . . . DGG OR DL PACKAGE
(TOP VIEW)

$\overline{1OEAB}$	1	56	$\overline{1OEBA}$
$\overline{1LEAB}$	2	55	$\overline{1LEBA}$
$\overline{1CEAB}$	3	54	$\overline{1CEBA}$
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
$\overline{2CEAB}$	26	31	$\overline{2CEBA}$
$\overline{2LEAB}$	27	30	$\overline{2LEBA}$
$\overline{2OEAB}$	28	29	$\overline{2OEBA}$



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**TEXAS
INSTRUMENTS**

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SN54ABT16543, SN74ABT16543

16-BIT REGISTERED TRANSCEIVERS

WITH 3-STATE OUTPUTS

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FUNCTION TABLE[†]
(each 8-bit section)

INPUTS				OUTPUT B
<u>CEAB</u>	<u>LEAB</u>	<u>OEAB</u>	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B ₀ [‡]
L	L	L	L	L
L	L	L	H	H

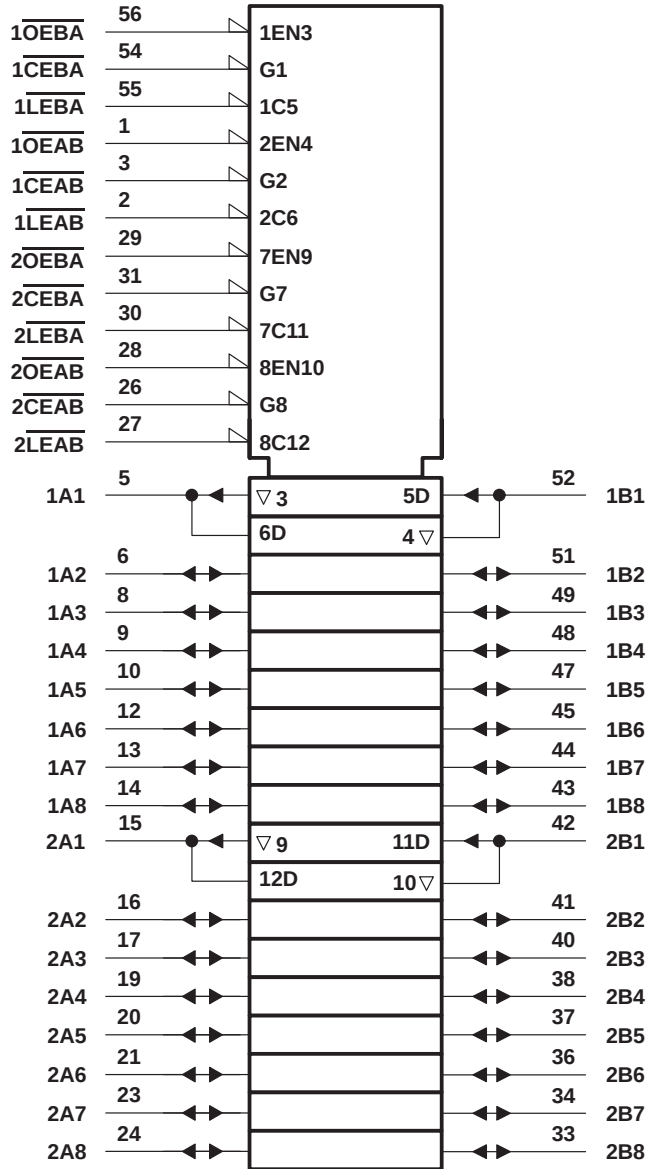
[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

[‡] Output level before the indicated steady-state input conditions were established

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logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

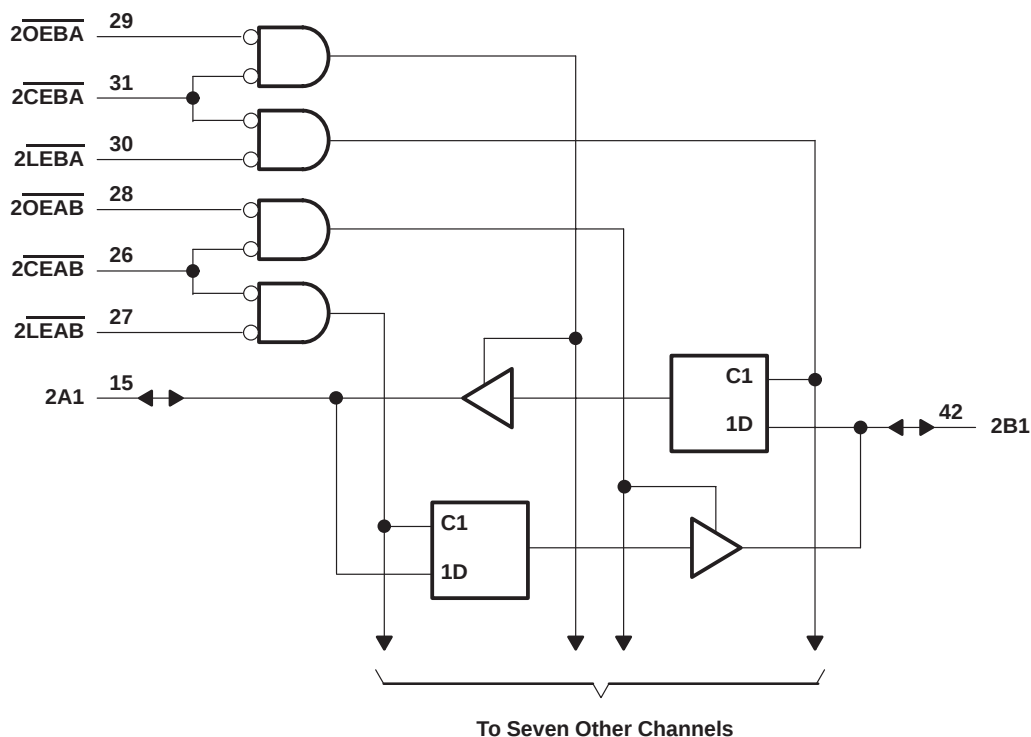
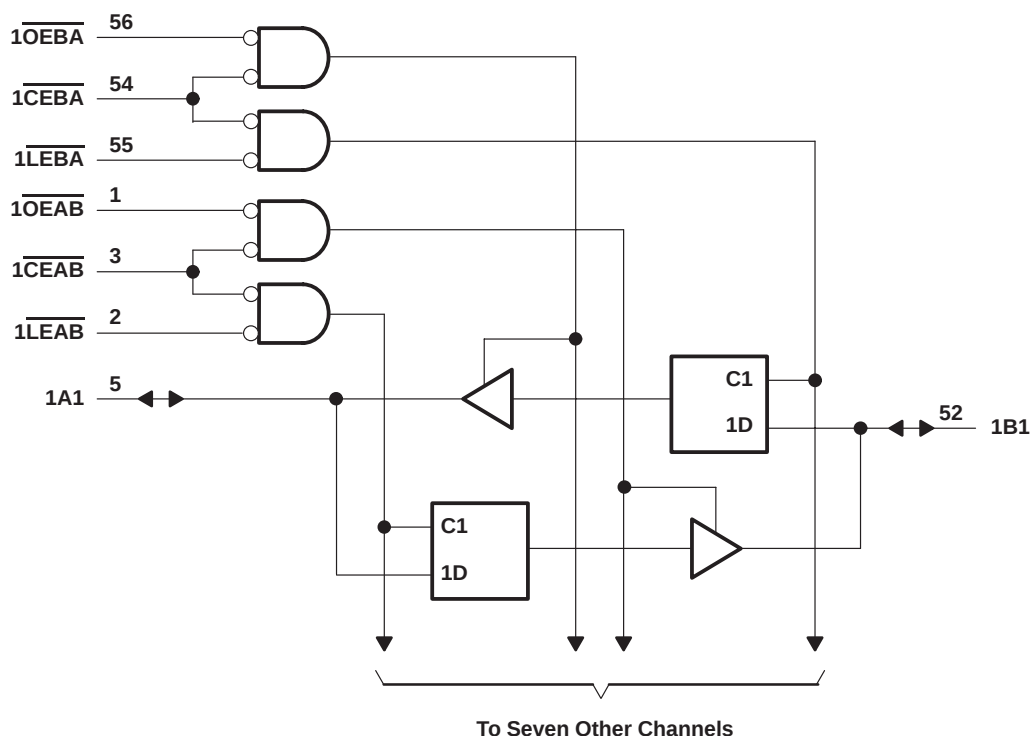
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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16543	96 mA
SN74ABT16543	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

		SN54ABT16543		SN74ABT16543		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.



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16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A = 25°C			SN54ABT16543		SN74ABT16543		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = –18 mA		–1.2			–1.2		–1.2		V
V _{OH}		V _{CC} = 4.5 V, I _{OH} = –3 mA		2.5			2.5		2.5		V
		V _{CC} = 5 V, I _{OH} = –3 mA		3			3		3		
		V _{CC} = 4.5 V	I _{OH} = –24 mA	2			2				
			I _{OH} = –32 mA	2*					2		
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 48 mA	0.55			0.55				V
			I _{OL} = 64 mA	0.55*					0.55		
V _{hys}				100							mV
I _I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND		±1			±1		±1		μA
	A or B ports			±100			±100		±100		
I _{OZH} ‡		V _{CC} = 5.5 V, V _O = 2.7 V		50**			10		50		μA
I _{OZL} ‡		V _{CC} = 5.5 V, V _O = 0.5 V		–50**			–10		–50		μA
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V		±100					±100		μA
I _{CEX}		V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high	50			50		50		μA
I _O §		V _{CC} = 5.5 V, V _O = 2.5 V		–50	–100	–200	–50	–200	–50	–200	mA
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	2			2		2		mA
			Outputs low	35			35		35		
			Outputs disabled	2			2		2		
ΔI _{CC} ¶		V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		0.5			0.5		0.5		mA
C _i	Control inputs	V _I = 2.5 V or 0.5 V		3							pF
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V		8.5							pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

** These limits apply only to the SN74ABT16543.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V _{CC} = 5 V, T _A = 25°C		SN54ABT16543		SN74ABT16543		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$ low		4		4		4		ns
t _{su}	Setup time, data before $\overline{\text{LEAB}}\uparrow$ or $\overline{\text{LEBA}}\uparrow$	High	1.5		1.5		1.5		ns
		Low	3.5		3.5		3.5		
t _h	Hold time, data after $\overline{\text{LEAB}}\uparrow$ or $\overline{\text{LEBA}}\uparrow$	High	1.5		1.5		1.5		ns
		Low	2		2		2		



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT16543					UNIT
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t _{PLH}	A or B	B or A	0.8	2.5	3.3	0.8	3.9	ns
t _{PHL}			0.9	2.7	4.4	0.9	5.2	
t _{PLH}	$\overline{LE}$	A or B	1	3.1	4.3	1	5.3	ns
t _{PHL}			1.2	3.3	4.8	1.2	5.7	
t _{PZH}	$\overline{OE}$	A or B	0.8	3.4	4.3	0.8	5.3	ns
t _{PZL}			1.1	3.8	7	1.1	7.9	
t _{PHZ}	$\overline{OE}$	A or B	1.9	4	6.3	1.9	7.2	ns
t _{PLZ}			1.6	3.3	4.6	1.6	5	
t _{PZH}	$\overline{CE}$	A or B	0.9	3.8	4.9	0.9	6.3	ns
t _{PZL}			1.2	4.2	6.8	1.2	7.9	
t _{PHZ}	$\overline{CE}$	A or B	2	4.5	6.4	2	7.3	ns
t _{PLZ}			1.7	3.9	5.1	1.7	5.6	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT16543					UNIT
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t _{PLH}	A or B	B or A	1	2.5	3.3	1	3.8	ns
t _{PHL}			1	2.7	4.4	1	5.1	
t _{PLH}	$\overline{LE}$	A or B	1	3.1	4.3	1	5.2	ns
t _{PHL}			1.2	3.3	4.8	1.2	5.6	
t _{PZH}	$\overline{OE}$	A or B	1	3.4	4.3	1	5.2	ns
t _{PZL}			1.1	3.8	5.9	1.1	7	
t _{PHZ}	$\overline{OE}$	A or B	1.9	4	5	1.9	5.7	ns
t _{PLZ}			1.6	3.3	4.2	1.6	4.6	
t _{PZH}	$\overline{CE}$	A or B	1	3.8	4.9	1	6.2	ns
t _{PZL}			1.2	4.2	6.5	1.2	7.8	
t _{PHZ}	$\overline{CE}$	A or B	2	4.5	5.6	2	6.6	ns
t _{PLZ}			1.7	3.9	5.1	1.7	5.4	

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PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



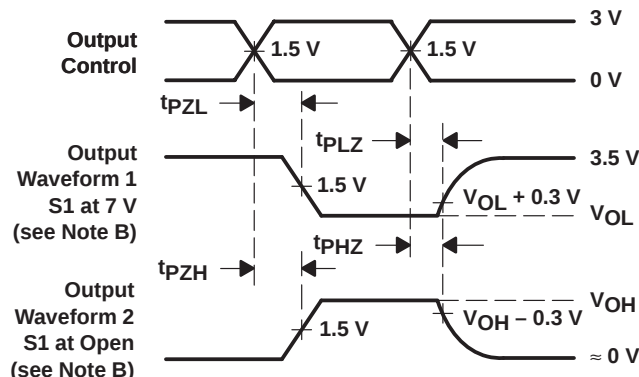
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9324101MXA	Active	Production	CFP (WD) 56	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9324101MX A SNJ54ABT16543W D
SN74ABT16543DGGR	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16543
SN74ABT16543DGGR.B	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16543
SN74ABT16543DGGRG4	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16543
SN74ABT16543DGGRG4.B	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16543
SN74ABT16543DL	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16543
SN74ABT16543DL.B	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16543
SN74ABT16543DLR	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16543
SN74ABT16543DLR.B	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16543
SN74ABT16543DLRG4	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16543
SN74ABT16543DLRG4.B	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16543
SNJ54ABT16543WD	Active	Production	CFP (WD) 56	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9324101MX A SNJ54ABT16543W D

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54ABT16543, SN74ABT16543 :

- Catalog : [SN74ABT16543](#)
- Military : [SN54ABT16543](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16543DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74ABT16543DGGRG4	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74ABT16543DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN74ABT16543DLRG4	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16543DGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74ABT16543DGGRG4	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74ABT16543DLR	SSOP	DL	56	1000	356.0	356.0	53.0
SN74ABT16543DLRG4	SSOP	DL	56	1000	356.0	356.0	53.0

TUBE

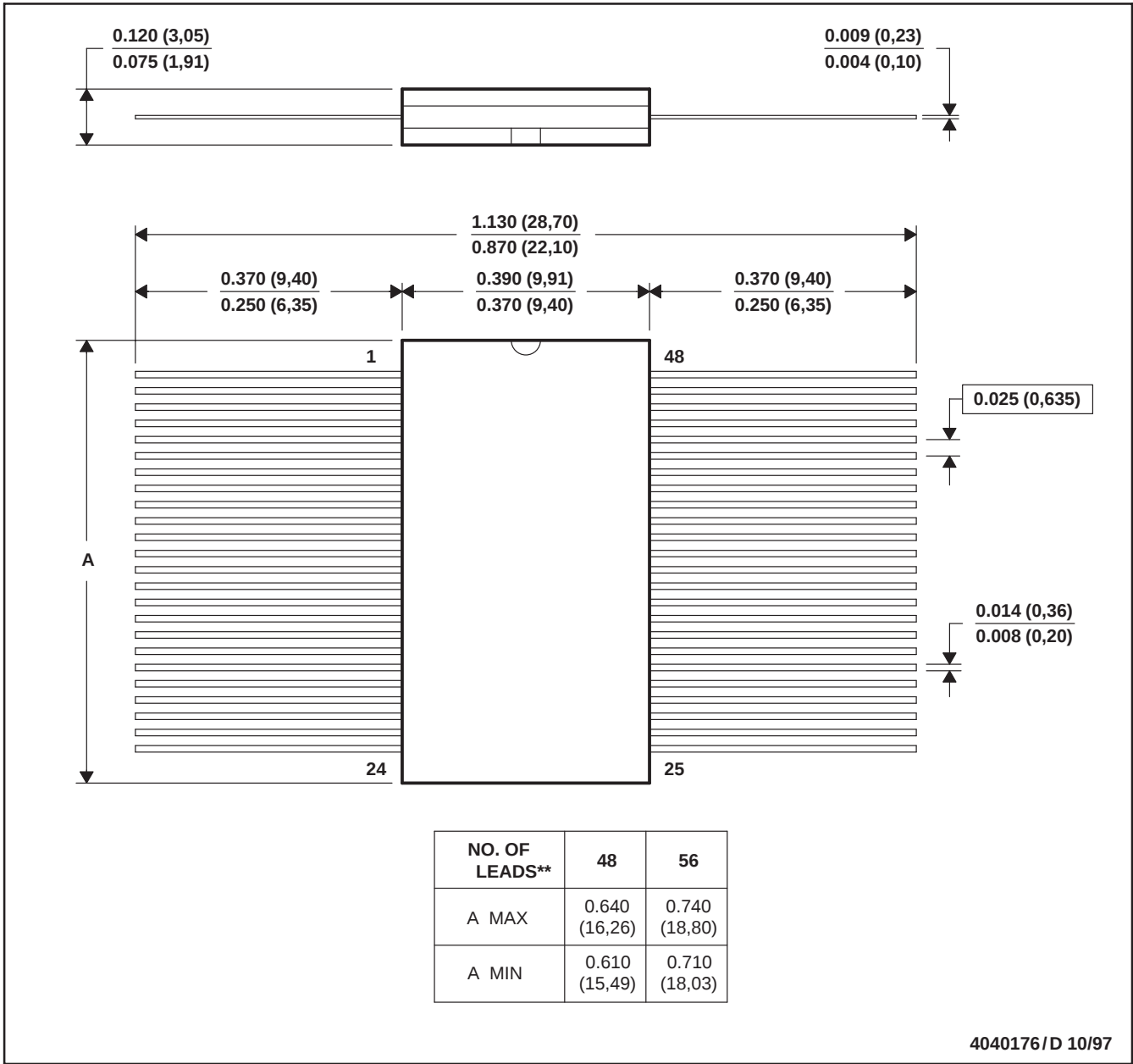


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABT16543DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74ABT16543DL.B	DL	SSOP	56	20	473.7	14.24	5110	7.87

WD (R-GDFP-F**)
48 LEADS SHOWN

CERAMIC DUAL FLATPACK



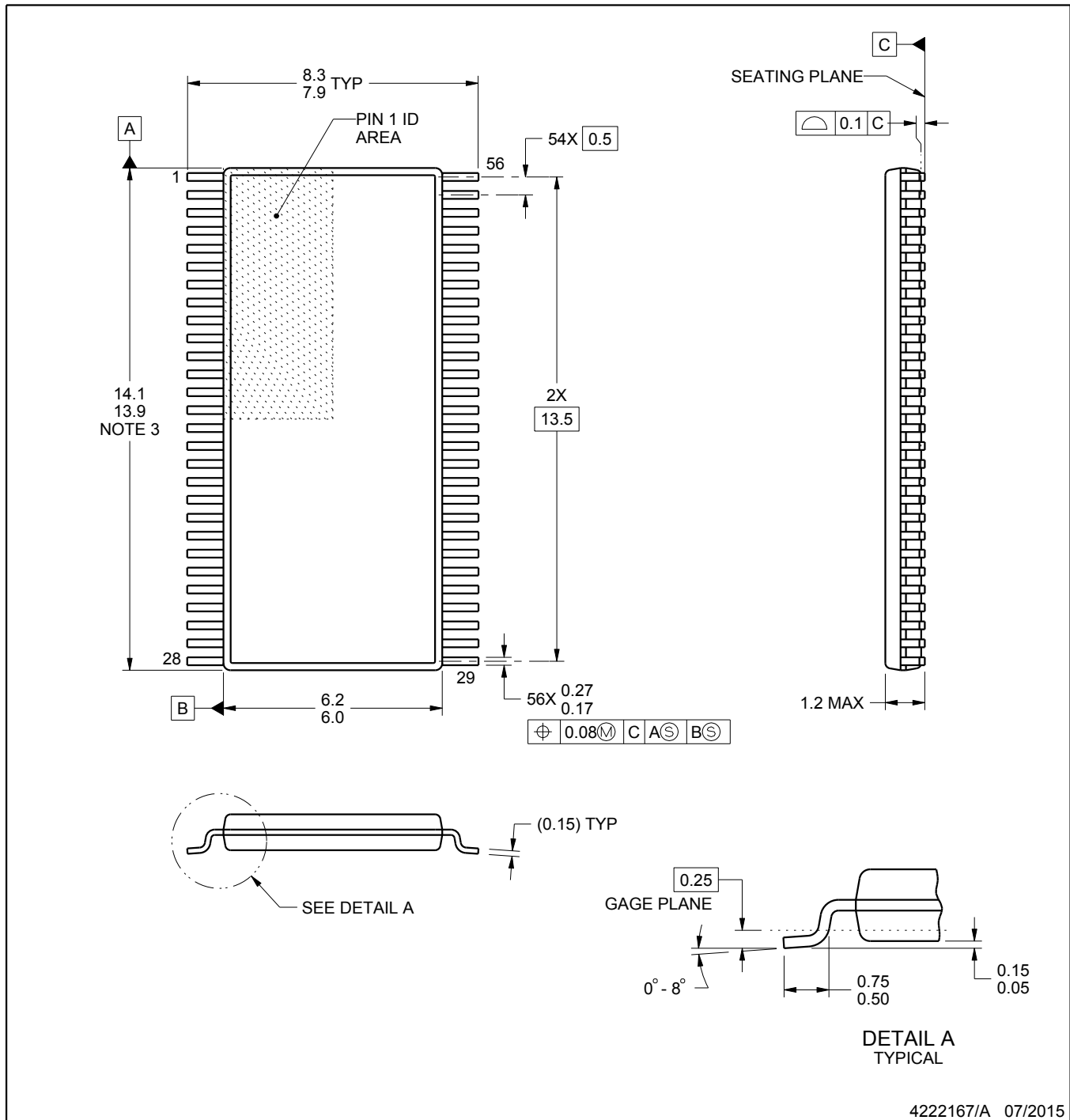
- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only
E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
GDFP1-F56 and JEDEC MO-146AB

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118



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NOTES:

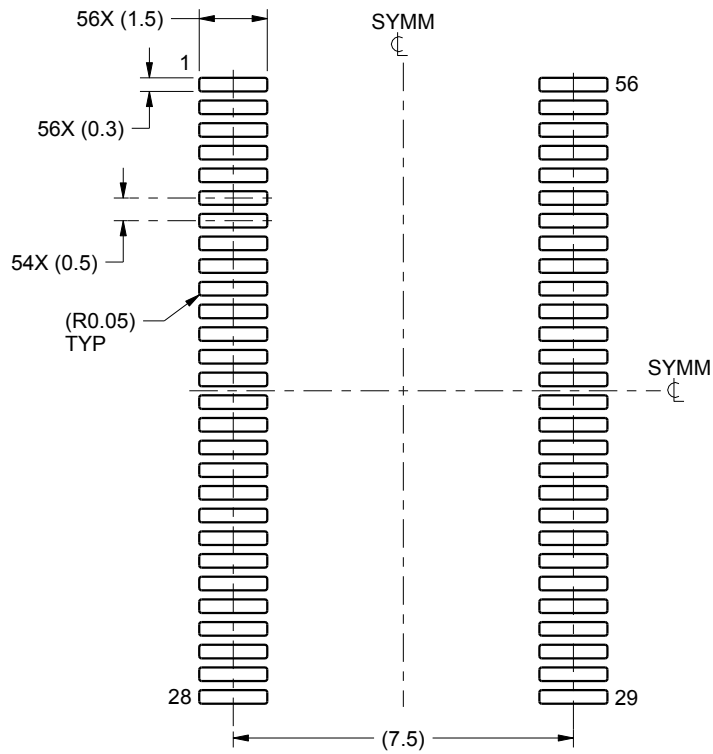
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

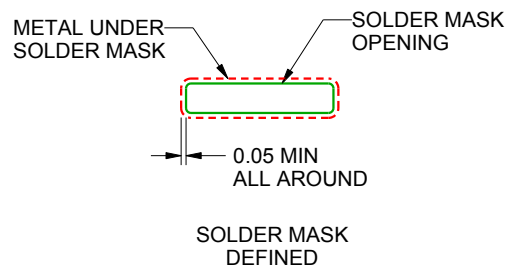
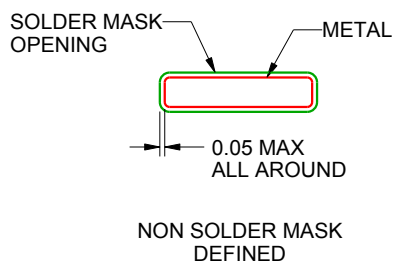
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

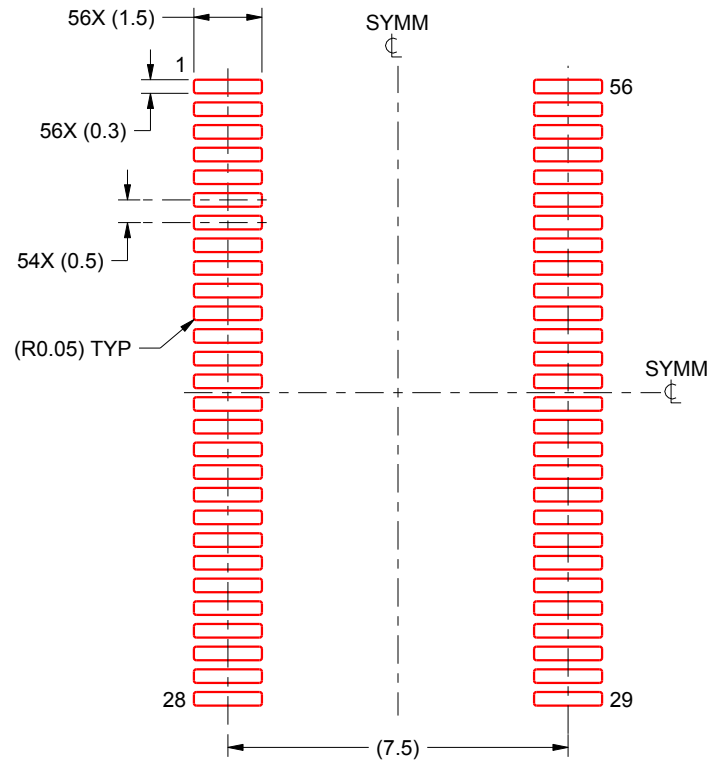
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025