

# SN54ABTH245, SN74ABTH245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS663D – APRIL 1996 – REVISED SEPTEMBER 1999

- State-of-the-Art *EPIC-II<sup>TM</sup>* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- High-Drive Outputs (–32-mA  $I_{OH}$ , 64-mA  $I_{OL}$ )
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Thin Very Small-Outline (DGV) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package

## description

These octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

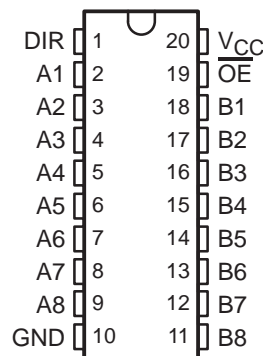
When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

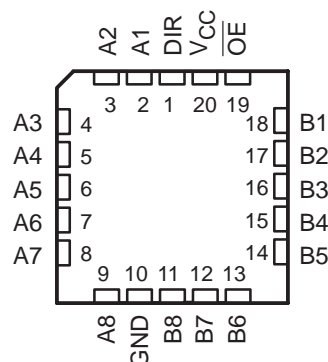
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABTH245 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABTH245 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABTH245 . . . J OR W PACKAGE  
SN74ABTH245 . . . DB, DGV, DW, N, OR PW PACKAGE  
(TOP VIEW)



SN54ABTH245 . . . FK PACKAGE  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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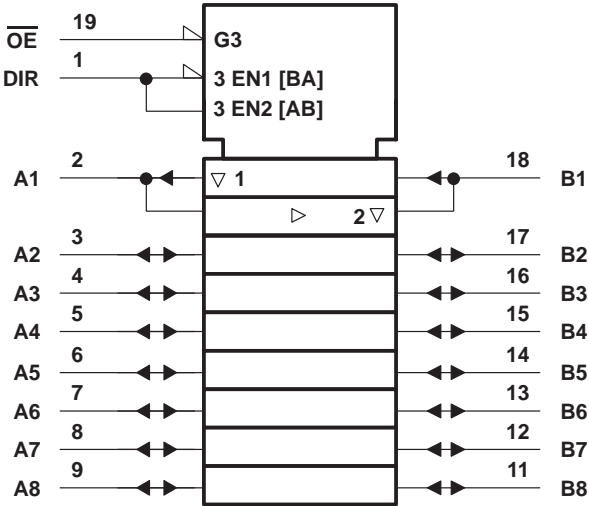
SN54ABTH245, SN74ABTH245  
OCTAL BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS

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FUNCTION TABLE

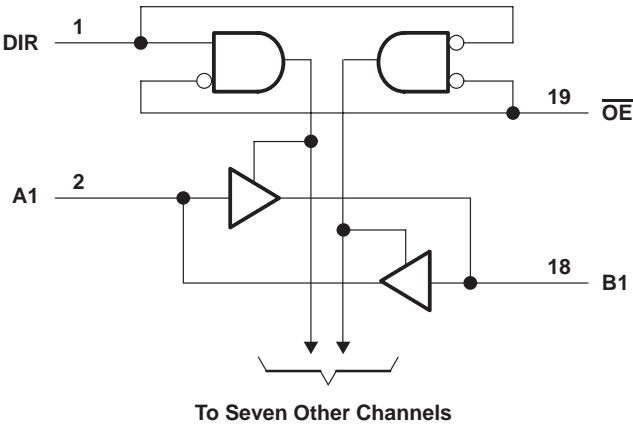
| INPUTS |     | OPERATION       |
|--------|-----|-----------------|
| OE     | DIR |                 |
| L      | L   | B data to A bus |
| L      | H   | A data to B bus |
| H      | X   | Isolation       |

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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|   |       |                 |
|---|-------|-----------------|
| Supply voltage range, $V_{CC}$  | ..... | –0.5 V to 7 V   |
| Input voltage range, $V_I$ (except I/O ports) (see Note 1)                | ..... | –0.5 V to 7 V   |
| Voltage range applied to any output in the high or power-off state, $V_O$ | ..... | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$ : SN54ABTH245             | ..... | 96 mA           |
| SN74ABTH245   | ..... | 128 mA          |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                               | ..... | –18 mA          |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ )                              | ..... | –50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package         | ..... | 70°C/W          |
| DGV package   | ..... | 92°C/W          |
| DW package  | ..... | 58°C/W          |
| N package   | ..... | 69°C/W          |
| PW package  | ..... | 83°C/W          |
| Storage temperature range, $T_{Stg}$                                      | ..... | –65°C to 150°C  |

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JEDEC 51.

|                     |                                    | SN54ABTH245 |                 | SN74ABTH245 |                 | UNIT |
|---------------------|------------------------------------|-------------|-----------------|-------------|-----------------|------|
|                     |                                    | MIN         | MAX             | MIN         | MAX             |      |
| V <sub>CC</sub>     | Supply voltage                     | 4.5         | 5.5             | 4.5         | 5.5             | V    |
| V <sub>IH</sub>     | High-level input voltage           | 2           |                 | 2           |                 | V    |
| V <sub>IL</sub>     | Low-level input voltage            |             | 0.8             |             | 0.8             | V    |
| V <sub>I</sub>      | Input voltage                      | 0           | V <sub>CC</sub> | 0           | V <sub>CC</sub> | V    |
| I <sub>OH</sub>     | High-level output current          |             | −24             |             | −32             | mA   |
| I <sub>OL</sub>     | Low-level output current           |             | 48              |             | 64              | mA   |
| Δt/Δv               | Input transition rise or fall rate |             | 5               |             | 5               | ns/V |
| Δt/ΔV <sub>CC</sub> | Power-up ramp rate                 |             |                 | 200         |                 | μs/V |
| T <sub>A</sub>      | Operating free-air temperature     | −55         | 125             | −40         | 85              | °C   |



# SN54ABTH245, SN74ABTH245

## OCTAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER            |                | TEST CONDITIONS  |                          | T <sub>A</sub> = 25°C |      |       | SN54ABTH245 |       | SN74ABTH245 |      | UNIT |
|----------------------|----------------|--|--------------------------|-----------------------|------|-------|-------------|-------|-------------|------|------|
|                      |                |  |                          | MIN                   | TYP† | MAX   | MIN         | MAX   | MIN         | MAX  |      |
| V <sub>IK</sub>      |                | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA                                     |                          |                       |      | -1.2  |             | -1.2  |             | -1.2 | V    |
| V <sub>OH</sub>      |                | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA                                     |                          | 2.5                   |      |       | 2.5         |       | 2.5         |      | V    |
|                      |                | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA                                       |                          | 3                     |      |       | 3           |       | 3           |      |      |
|                      |                | V <sub>CC</sub> = 4.5 V  | I <sub>OH</sub> = -24 mA | 2                     |      |       | 2           |       |             |      |      |
|                      |                |  | I <sub>OH</sub> = -32 mA | 2*                    |      |       |             |       | 2           |      |      |
| V <sub>OL</sub>      |                | V <sub>CC</sub> = 4.5 V  | I <sub>OL</sub> = 48 mA  |                       |      | 0.55  |             | 0.55  |             |      | V    |
|                      |                |  | I <sub>OL</sub> = 64 mA  |                       |      | 0.55* |             |       |             | 0.55 |      |
| V <sub>hys</sub>     |                |  |                          |                       | 100  |       |             |       |             |      | mV   |
| I <sub>I</sub>       | Control inputs | V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND                |                          |                       |      | ±1    |             | ±1    |             | ±1   | μA   |
|                      | A or B ports   | V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND            |                          |                       |      | ±20   |             | ±100  |             | ±20  |      |
| I <sub>I(hold)</sub> |                | V <sub>CC</sub> = 4.5 V  | V <sub>I</sub> = 0.8 V   | 100                   |      |       | 100         |       | 100         |      | μA   |
|                      |                |  | V <sub>I</sub> = 2 V     | -100                  |      |       | -100        |       | -100        |      |      |
| I <sub>OZPU</sub>    |                | V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$   |                          |                       |      | ±50** |             | ±50** |             | ±50  | μA   |
| I <sub>OZPD</sub>    |                | V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$   |                          |                       |      | ±50** |             | ±50** |             | ±50  | μA   |
| I <sub>off</sub>     |                | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V                        |                          |                       |      | ±100  |             |       |             | ±100 | μA   |
| I <sub>CEX</sub>     |                | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V                                      | Outputs high             |                       |      | 50    |             | 50    |             | 50   | μA   |
| I <sub>O‡</sub>      |                | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V                                      |                          | -50                   | -140 | -180  | -50         | -180  | -50         | -180 | mA   |
| I <sub>CC</sub>      | A or B ports   | V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND | Outputs high             |                       | 5    | 250   |             | 250   |             | 250  | μA   |
|                      |                |  | Outputs low              |                       | 22   | 30    |             | 30    |             | 30   | mA   |
|                      |                |  | Outputs disabled         |                       | 1    | 250   |             | 250   |             | 250  | μA   |
| ΔI <sub>CC</sub> §   | Data inputs    | V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND  | Outputs enabled          |                       |      | 1.5   |             | 1.5   |             | 1.5  | mA   |
|                      |                |  | Outputs disabled         |                       |      | 1.5   |             | 1.5   |             | 1.5  | mA   |
|                      | Control inputs | V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND  |                          |                       |      | 1.5   |             | 1.5   |             | 1.5  | mA   |
| C <sub>i</sub>       | Control inputs | V <sub>I</sub> = 2.5 V or 0.5 V  |                          |                       | 4    |       |             |       |             |      | pF   |
| C <sub>io</sub>      | A or B ports   | V <sub>O</sub> = 2.5 V or 0.5 V  |                          |                       | 8    |       |             |       |             |      | pF   |

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

\*\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



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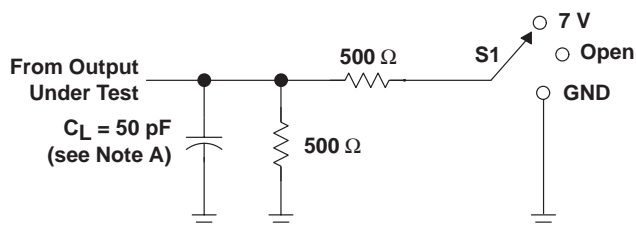
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

| PARAMETER   | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC} = 5$ V,<br>$T_A = 25^\circ\text{C}$ |     |     | SN54ABTH245 |     | SN74ABTH245 |     | UNIT |
|-------------|-----------------|----------------|---|-----|-----|-------------|-----|-------------|-----|------|
|             |                 |                | MIN   | TYP | MAX | MIN         | MAX | MIN         | MAX |      |
| $t_{PLH}$   | A or B          | B or A         | 1   | 2   | 3.2 | 0.8         | 3.8 | 1           | 3.6 | ns   |
| $t_{PHL}$   |                 |                | 1   | 2.6 | 3.5 | 0.8         | 4.2 | 1           | 3.9 |      |
| $t_{PZH}$   | $\overline{OE}$ | A or B         | 2   | 3.5 | 4.5 | 1.2         | 6.2 | 2           | 5.6 | ns   |
| $t_{PZL}$   |                 |                | 1.9   | 4   | 5.3 | 1.3         | 7   | 1.9         | 6.2 |      |
| $t_{PHZ}$   | $\overline{OE}$ | A or B         | 2.2   | 4.4 | 5.4 | 2.2         | 6.1 | 2.2         | 5.9 | ns   |
| $t_{PLZ}$   |                 |                | 1.5   | 3   | 4   | 1           | 4.9 | 1.5         | 4.5 |      |
| $t_{sk(o)}$ |                 |                |   |     | 0.5 |             |     |             | 0.5 | ns   |

# SN54ABTH245, SN74ABTH245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

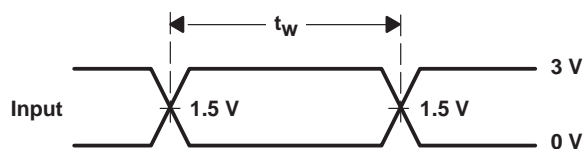
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## PARAMETER MEASUREMENT INFORMATION

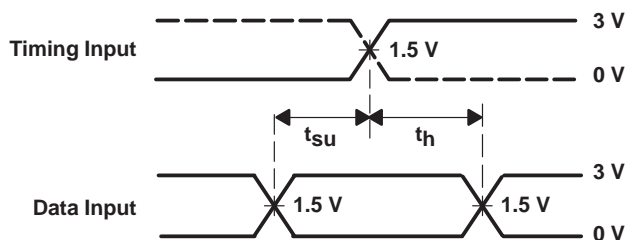


LOAD CIRCUIT

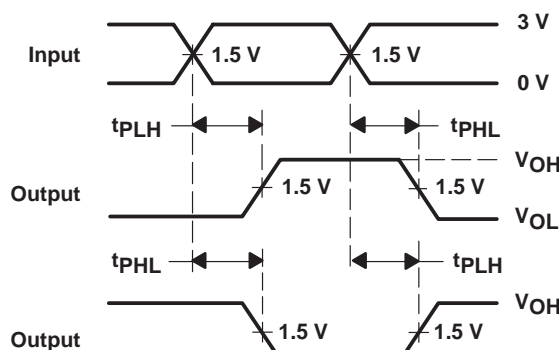
| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



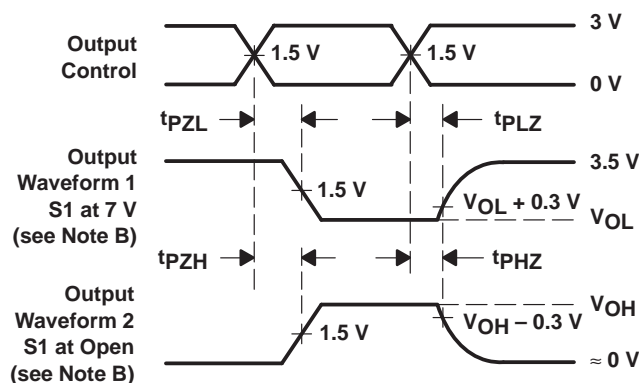
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                       |
|---------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---|
| <a href="#">5962-9762301Q2A</a> | Active        | Production           | LCCC (FK)   20  | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>9762301Q2A<br>SNJ54ABTH<br>245FK |
| <a href="#">5962-9762301QSA</a> | Active        | Production           | CFP (W)   20    | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9762301QS<br>A<br>SNJ54ABTH245W      |
| <a href="#">SN74ABTH245DBR</a>  | Active        | Production           | SSOP (DB)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABH245                                    |
| SN74ABTH245DBR.B                | Active        | Production           | SSOP (DB)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABH245                                    |
| <a href="#">SN74ABTH245DW</a>   | Active        | Production           | SOIC (DW)   20  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABTH245                                   |
| SN74ABTH245DW.B                 | Active        | Production           | SOIC (DW)   20  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABTH245                                   |
| SN74ABTH245DWE4                 | Active        | Production           | SOIC (DW)   20  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABTH245                                   |
| <a href="#">SN74ABTH245DWR</a>  | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABTH245                                   |
| SN74ABTH245DWR.B                | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABTH245                                   |
| <a href="#">SN74ABTH245N</a>    | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74ABTH245N                              |
| SN74ABTH245N.B                  | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74ABTH245N                              |
| <a href="#">SN74ABTH245PWR</a>  | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABH245                                    |
| SN74ABTH245PWR.B                | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABH245                                    |
| SN74ABTH245PWRG4                | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABH245                                    |
| SN74ABTH245PWRG4.B              | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABH245                                    |
| <a href="#">SNJ54ABTH245FK</a>  | Active        | Production           | LCCC (FK)   20  | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>9762301Q2A<br>SNJ54ABTH<br>245FK |
| <a href="#">SNJ54ABTH245W</a>   | Active        | Production           | CFP (W)   20    | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9762301QS<br>A<br>SNJ54ABTH245W      |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54ABTH245, SN74ABTH245 :**

● Catalog : [SN74ABTH245](#)

● Military : [SN54ABTH245](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications



## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABTH245DBR   | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74ABTH245DWR   | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74ABTH245PWR   | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| SN74ABTH245PWRG4 | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABTH245DBR   | SSOP         | DB              | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74ABTH245DWR   | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| SN74ABTH245PWR   | TSSOP        | PW              | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74ABTH245PWRG4 | TSSOP        | PW              | 20   | 2000 | 353.0       | 353.0      | 32.0        |

## TUBE



\*All dimensions are nominal

| Device          | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9762301Q2A | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| 5962-9762301QSA | W            | CFP          | 20   | 25  | 506.98 | 26.16  | 6220   | NA     |
| SN74ABTH245DW   | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74ABTH245DW.B | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74ABTH245DWE4 | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74ABTH245N    | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| SN74ABTH245N.B  | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| SNJ54ABTH245FK  | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SNJ54ABTH245W   | W            | CFP          | 20   | 25  | 506.98 | 26.16  | 6220   | NA     |

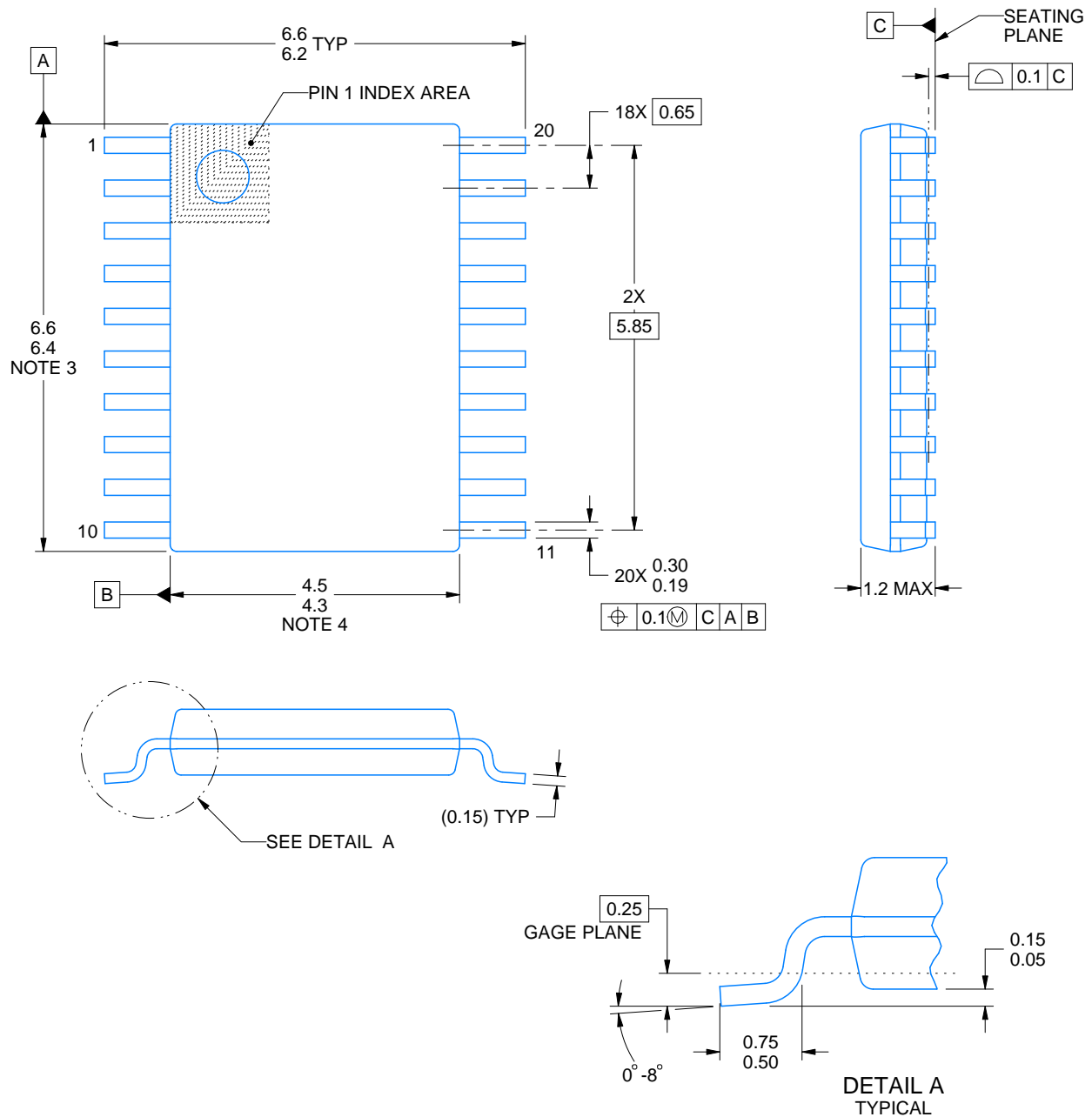
W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



4220206/A 02/2017

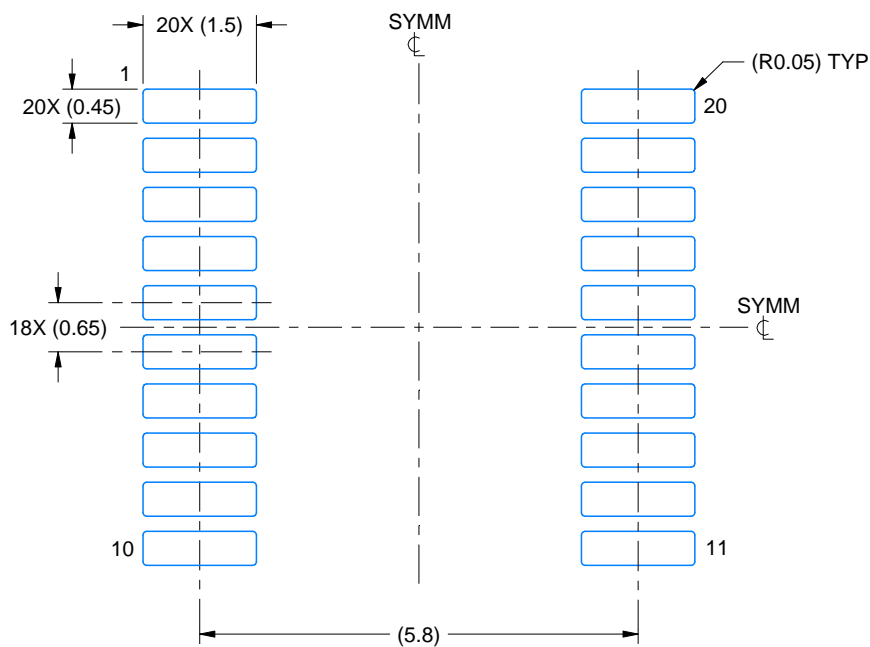
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

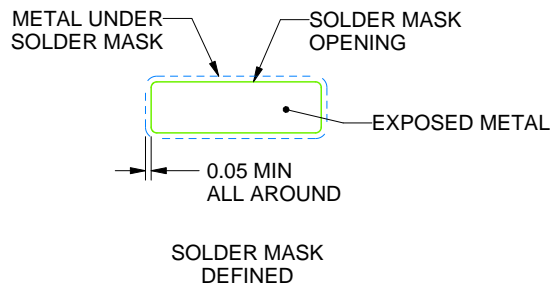
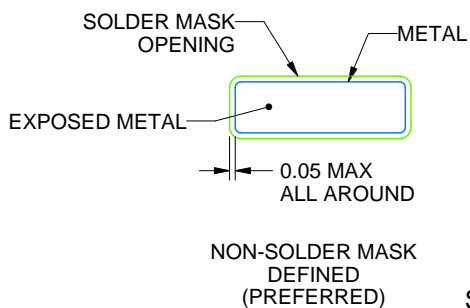
**PW0020A**

## TSSOP - 1.2 mm max height

## SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



## SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

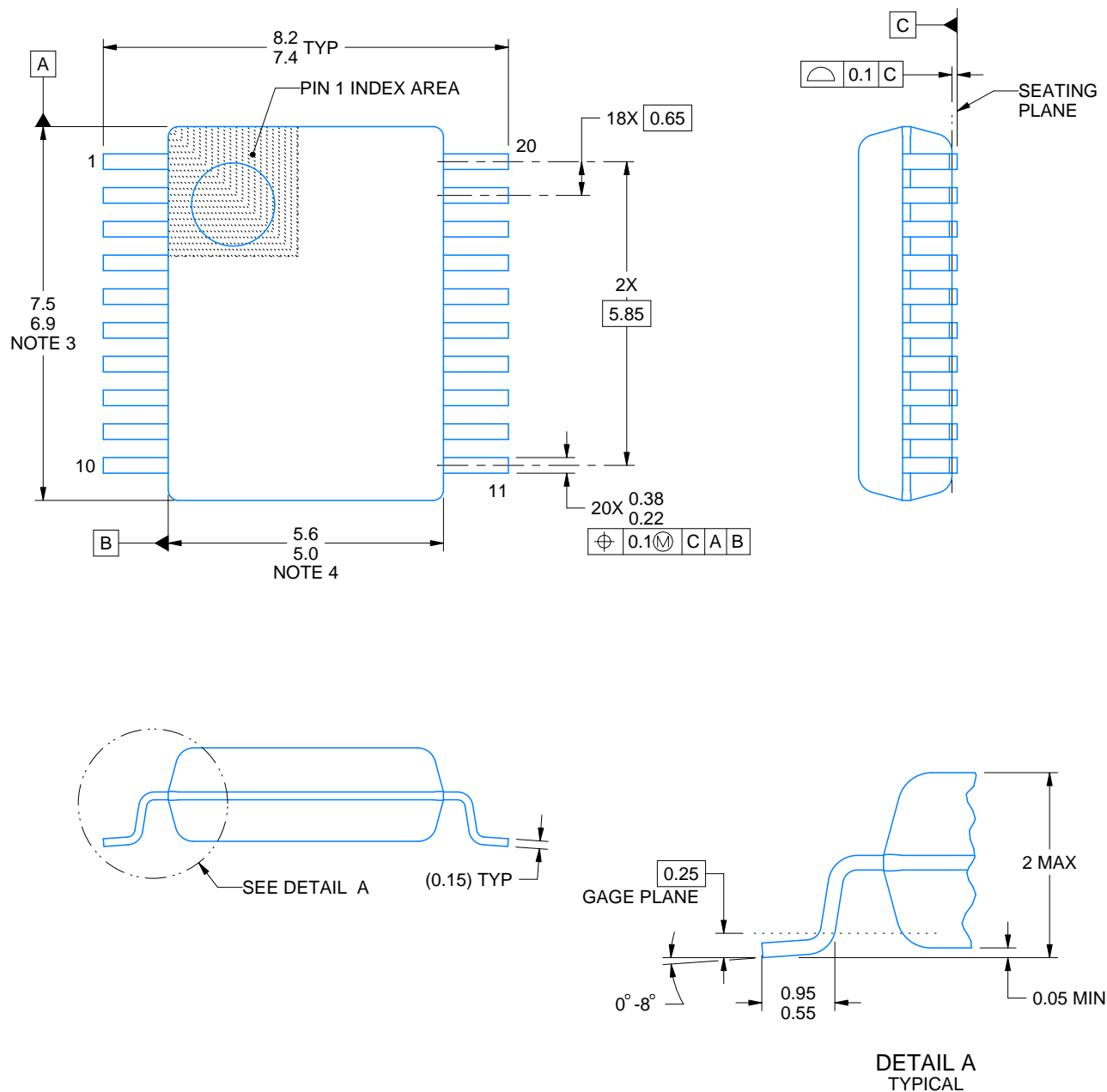
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



## SSOP - 2 mm max height

## SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



# EXAMPLE BOARD LAYOUT

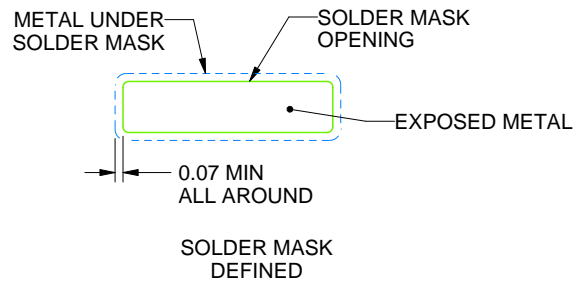
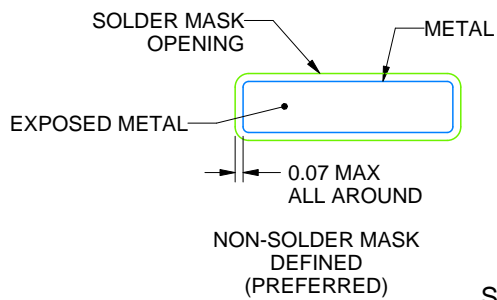
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



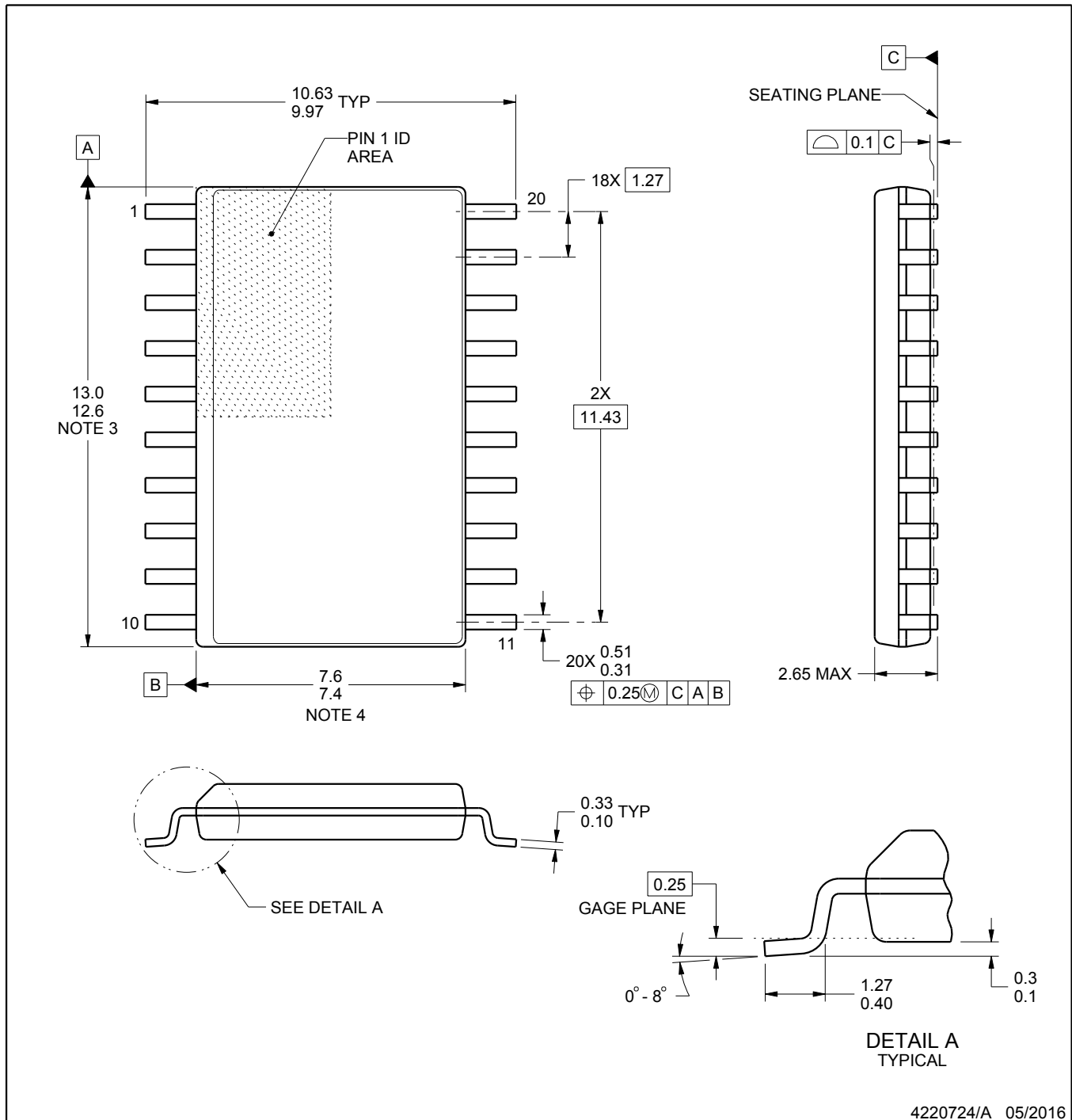
| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220724/A 05/2016

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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