

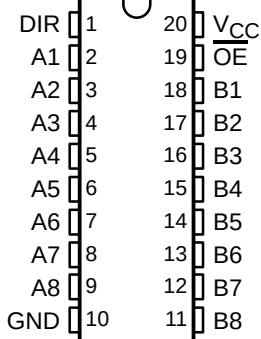
SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDAS272A – NOVEMBER 1994 – REVISED JANUARY 2003

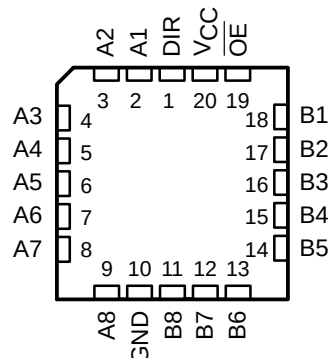
- 4.5-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 5.5 ns at 5 V

- 3-State Outputs Drive Bus Lines Directly
- pnp Inputs Reduce dc Loading

SN54ALS245A . . . J OR W PACKAGE
SN54AS245 . . . J PACKAGE
SN74ALS245A . . . DB, DW, N, OR NS PACKAGE
SN74AS245 . . . DW, N, OR NS PACKAGE
(TOP VIEW)



SN54ALS245A, SN54AS245 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74ALS245A-1N	SN74ALS245A-1N
			SN74ALS245AN	SN74ALS245AN
			SN74AS245N	SN74AS245N
	SOIC – DW	Tube	SN74ALS245ADW	ALS245A
		Tape and reel	SN74ALS245ADWR	
		Tube	SN74ALS245A-1DW	ALS245A-1
		Tape and reel	SN74ALS245A-1DWR	
		Tube	SN74AS245DW	AS245
		Tape and reel	SN74AS245DWR	
	SOP – NS	Tape and reel	SN74ALS245ANSR	ALS245A
		Tape and reel	SN74ALS245A-1NSR	ALS245A-1
		Tape and reel	SN74AS245NSR	74AS245
–55°C to 125°C	SSOP – DB	Tape and reel	SN74ALS245ADBR	G245A
	CDIP – J	Tube	SNJ54ALS245AJ	SNJ54ALS245AJ
			SNJ54AS245J	SNJ54AS245J
	CFP – W	Tube	SNJ54ALS245AW	SNJ54ALS245AW
	LCCC – FK	Tube	SNJ54ALS245AFK	SNJ54ALS245AFK
			SNJ54AS245FK	SNJ54AS245FK



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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The -1 version of the SN74ALS245A is identical to the standard version, except that the recommended maximum I_{OL} is increased to 48 mA. There is no -1 version of the SN54ALS245A.

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

The logic diagram of the 74VHC147 decoder shows the following components and connections:

- Inputs:**
 - DIR (1):** Connected to the top input of the first AND gate and the top input of the second AND gate.
 - A1 (2):** Connected to the bottom input of the first AND gate and the top input of the first inverter.
 - B1 (18):** Connected to the bottom input of the second AND gate and the top input of the second inverter.
- Logic Gates:**
 - AND Gate 1:** Inputs are DIR and A1. Its output is one of the three outputs shown.
 - AND Gate 2:** Inputs are DIR and B1. Its output is one of the three outputs shown.
 - Inverter 1:** Input is A1. Its output is one of the three outputs shown.
 - Inverter 2:** Input is B1. Its output is one of the three outputs shown.
- Outputs:**
 - 18:** Output of the first inverter (A1).
 - 19:** Output of the second inverter (B1).
 - OE:** Output of the first AND gate (DIR and A1).
- Other Connections:**
 - The output of the second AND gate (DIR and B1) is connected to the OE input of the second AND gate.
 - The output of the first inverter (A1) is connected to the input of the second inverter (B1).
 - The output of the second inverter (B1) is connected to the input of the first inverter (A1).

Supply voltage, V_{CC}	7 V
Input voltage, V_I : All inputs	7 V
I/O ports	5.5 V
Package thermal impedance, θ_{JA} (see Note 1): DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range	–65°C to 150°C

NOTE 1: The package thermal impedance is calculated in accordance with JEDEC 51-7.

SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245

OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 2)

		SN54ALS245A			SN74ALS245A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-12			-15	mA
I_{OL}	Low-level output current			12			24	mA
							48 [†]	
T_A	Operating free-air temperature	-55		125	0		70	°C

[†] Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS245A			SN74ALS245A			UNIT
				MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			-1.5			-1.5	V
V_{OH}		$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -0.4$ mA	$V_{CC} - 2$			$V_{CC} - 2$			V
		$V_{CC} = 4.5$ V	$I_{OH} = -3$ mA	2.4	3.2		2.4	3.2		
			$I_{OH} = -12$ mA	2						
			$I_{OH} = -15$ mA				2			
V_{OL}		$V_{CC} = 4.5$ V	$I_{OL} = 12$ mA		0.25	0.4		0.25	0.4	V
			$I_{OL} = 24$ mA					0.35	0.5	
			$I_{OL} = 48$ mA [†]					0.35	0.5	
I_I	Control inputs	$V_{CC} = 5.5$ V	$V_I = 7$ V			0.1			0.1	mA
	A or B ports		$V_I = 5.5$ V			0.1			0.1	
I_{IH}	Control inputs	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			20			20	μA
	A or B ports [§]					20			20	
I_{IL}	Control inputs	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			-0.1			-0.1	mA
	A or B ports [§]					-0.1			-0.1	
$I_O^{\parallel}$		$V_{CC} = 5.5$ V,	$V_O = 2.25$ V	-20		-112	-30		-112	mA
I_{CC}		$V_{CC} = 5.5$ V	Outputs high		30	48		30	45	mA
			Outputs low		36	60		36	55	
			Outputs disabled		38	63		38	58	

[†] Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

[‡] All typical values are $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

[§] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

^{||} The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245

OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54ALS245A		SN74ALS245A		
			MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	1	19	3	10	ns
t _{PHL}			1	14	3	10	
t _{PZH}	$\overline{\text{OE}}$	A or B	2	30	5	20	ns
t _{PZL}			2	29	5	20	
t _{PHZ}	$\overline{\text{OE}}$	A or B	2	14	2	10	ns
t _{PLZ}			2	30	4	15	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (SN54AS245, SN74AS245) (unless otherwise noted)†

Supply voltage, V _{CC}	7 V
Input voltage, V _I : All inputs	7 V
I/O ports	5.5 V
Package thermal impedance, θ _{JA} (see Note 1): DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

		SN54AS245			SN74AS245			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			–12			–15	mA
I _{OL}	Low-level output current			48			64	mA
T _A	Operating free-air temperature	–55		125	0		70	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245

OCTAL BUS TRANSCEIVERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS245			SN74AS245			UNIT	
				MIN	TYP†	MAX	MIN	TYP†	MAX		
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA		−1.2			−1.2			V	
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = −2 mA		V _{CC} − 2			V _{CC} − 2			V	
		V _{CC} = 4.5 V	I _{OH} = −3 mA		2.4	3.2	2.4	3.2			
			I _{OH} = −12 mA		2						
			I _{OH} = −15 mA				2				
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 48 mA		0.3	0.55				V	
			I _{OL} = 64 mA					0.35	0.55		
I _I	Control inputs	V _{CC} = 5.5 V	V _I = 7 V		0.1			0.1			mA
	A or B ports		V _I = 5.5 V		0.1			0.1			
I _{IH}	Control inputs	V _{CC} = 5.5 V, V _I = 2.7 V		50			20			μA	
	A or B ports‡			70			70				
I _{IL}	Control inputs	V _{CC} = 5.5 V, V _I = 0.4 V		−0.5			−0.5			mA	
	A or B ports‡			−0.75			−0.75				
I _O §		V _{CC} = 5.5 V, V _O = 2.25 V		−50 −150			−50 −150			mA	
I _{CC}		V _{CC} = 5.5 V	Outputs high		62	97	62	97	mA		
			Outputs low		95	143	95	143			
			Outputs disabled		79	123	79	123			

[†] All typical values are $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX ^{††}				UNIT
			SN54AS245		SN74AS245		
			MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	2	9.5	2	7.5	ns
t _{PHL}			2	9	2	7	
t _{PZH}	$\overline{\text{OE}}$	A or B	2	11	2	9	ns
t _{PZL}			2	10.5	2	8.5	
t _{PHZ}	$\overline{\text{OE}}$	A or B	2	7.5	2	5.5	ns
t _{PLZ}			2	12	2	9.5	

^{††} For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245

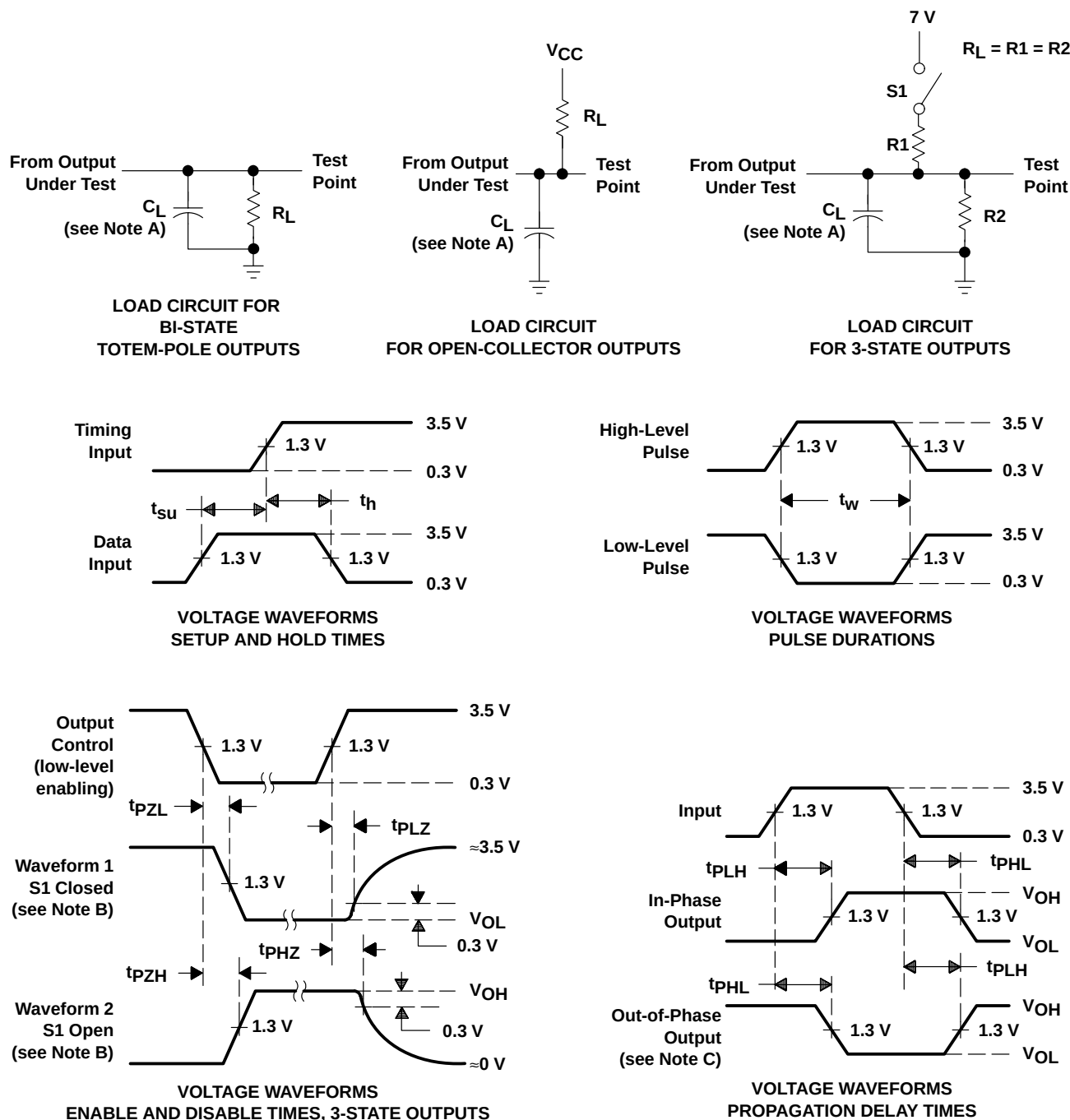
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WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION

SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 - D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 - E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
84030012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84030012A SNJ54ALS 245AFK
8403001RA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8403001RA SNJ54ALS245AJ
8403001SA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8403001SA SNJ54ALS245AW
SN54ALS245AJ	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS245AJ
SN54ALS245AJ.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS245AJ
SN54AS245J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54AS245J
SN54AS245J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54AS245J
SN74ALS245A-1DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	0 to 70	ALS245A-1
SN74ALS245A-1DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS245A-1
SN74ALS245A-1DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS245A-1
SN74ALS245A-1N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS245A-1N
SN74ALS245A-1N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS245A-1N
SN74ALS245A-1NSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS245A-1
SN74ALS245A-1NSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS245A-1
SN74ALS245ADBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	G245A
SN74ALS245ADBR.A	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	G245A
SN74ALS245ADW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	0 to 70	ALS245A
SN74ALS245ADWR	NRND	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS245A
SN74ALS245ADWR.A	NRND	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS245A
SN74ALS245ADWRG4	NRND	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS245A
SN74ALS245AN	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS245AN
SN74ALS245AN.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS245AN
SN74ALS245ANSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS245A
SN74ALS245ANSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS245A
SN74ALS245ANSRG4	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS245A
SN74AS245DW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS245

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AS245DW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS245
SN74AS245N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS245N
SN74AS245N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS245N
SN74AS245NSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74AS245
SN74AS245NSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74AS245
SNJ54ALS245AFK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84030012A SNJ54ALS 245AFK
SNJ54ALS245AFK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84030012A SNJ54ALS 245AFK
SNJ54ALS245AJ	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8403001RA SNJ54ALS245AJ
SNJ54ALS245AJ.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8403001RA SNJ54ALS245AJ
SNJ54ALS245AW	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8403001SA SNJ54ALS245AW
SNJ54ALS245AW.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8403001SA SNJ54ALS245AW
SNJ54AS245FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54AS 245FK
SNJ54AS245FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54AS 245FK
SNJ54AS245J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54AS245J
SNJ54AS245J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54AS245J

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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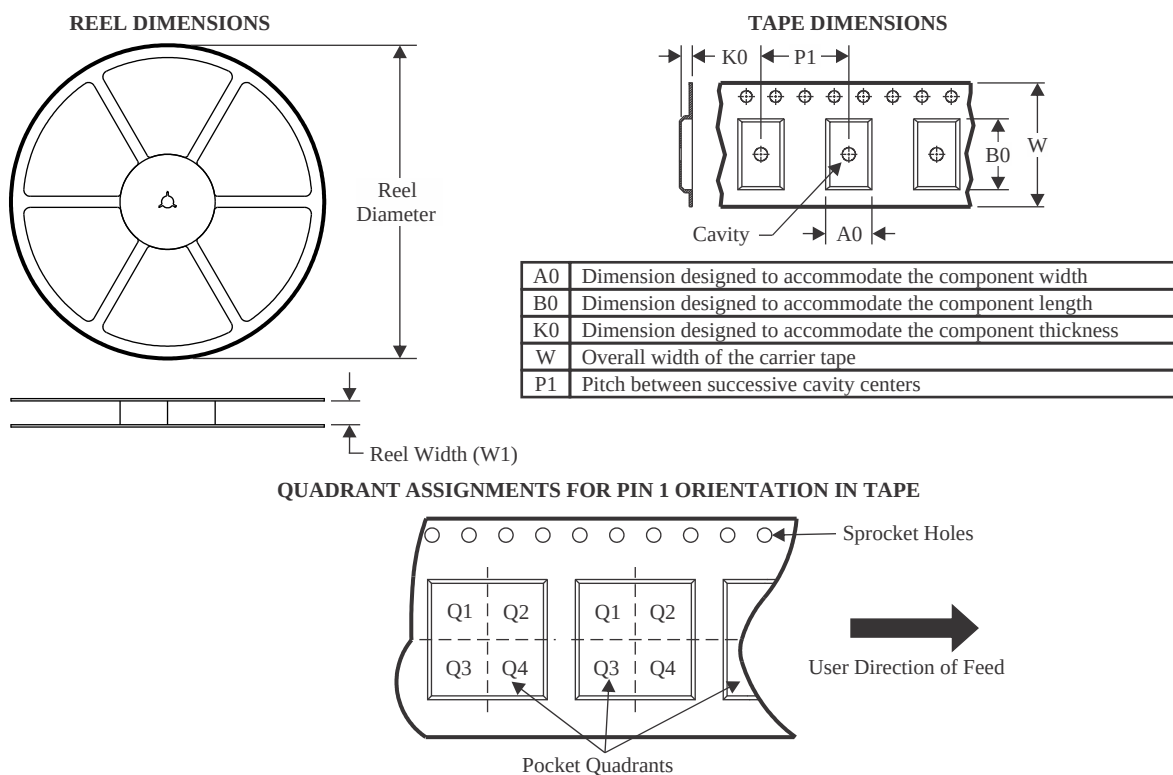
OTHER QUALIFIED VERSIONS OF SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245 :

- Catalog : [SN74ALS245A](#), [SN74AS245](#)
- Military : [SN54ALS245A](#), [SN54AS245](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

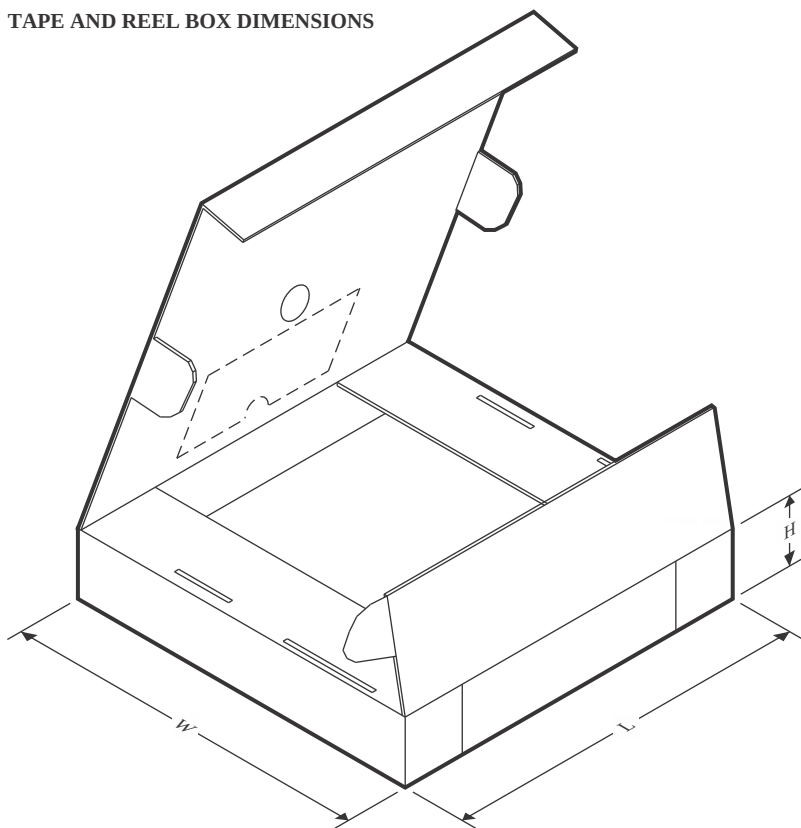
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS245A-1DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS245A-1NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ALS245ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ALS245ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS245ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AS245NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

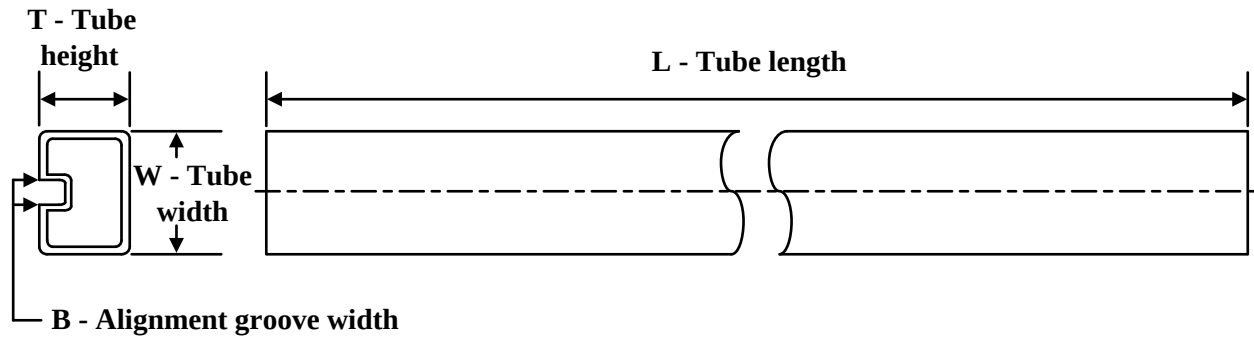
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS245A-1DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ALS245A-1NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74ALS245ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74ALS245ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ALS245ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74AS245NSR	SOP	NS	20	2000	356.0	356.0	45.0

TUBE

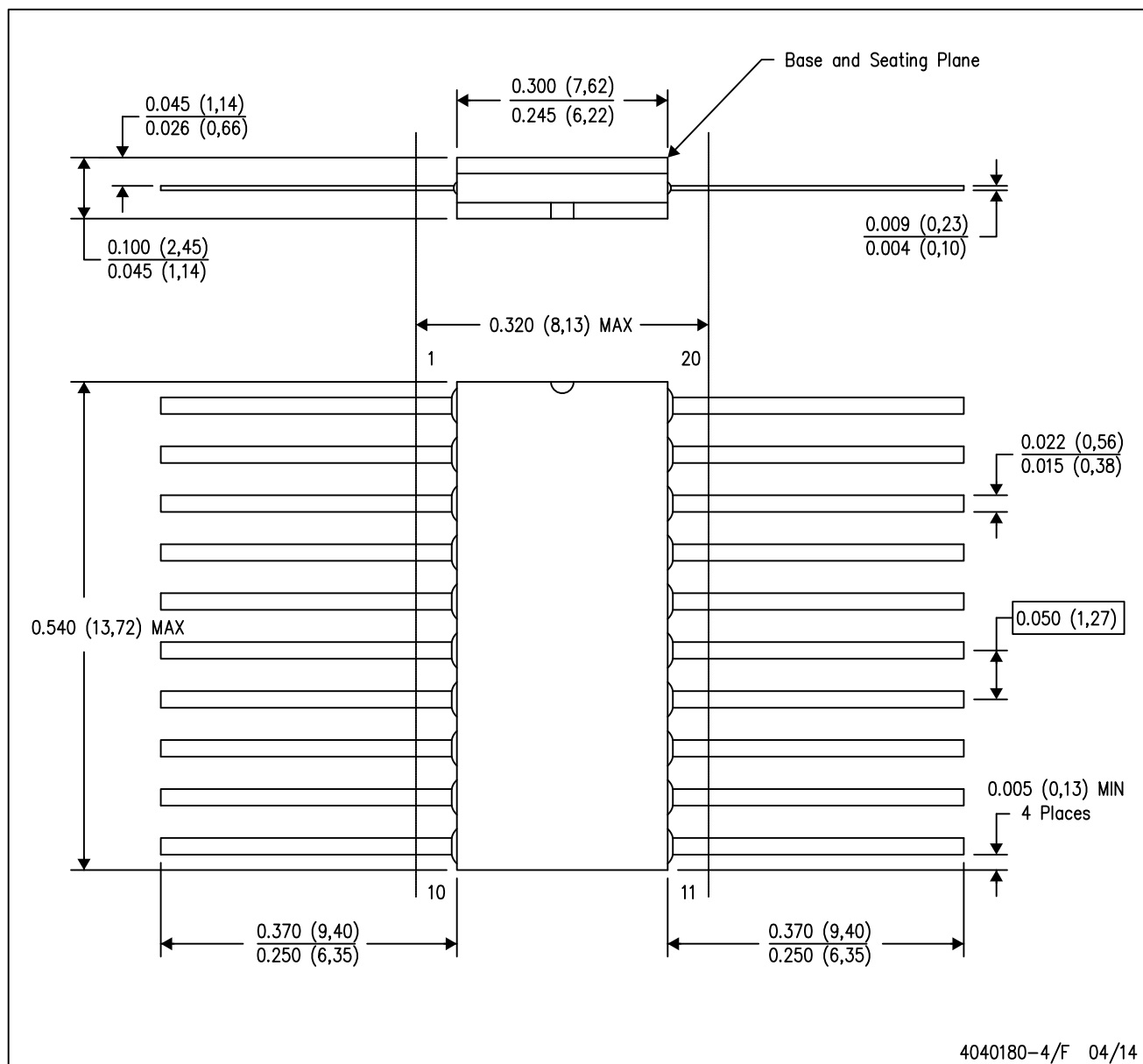


*All dimensions are nominal

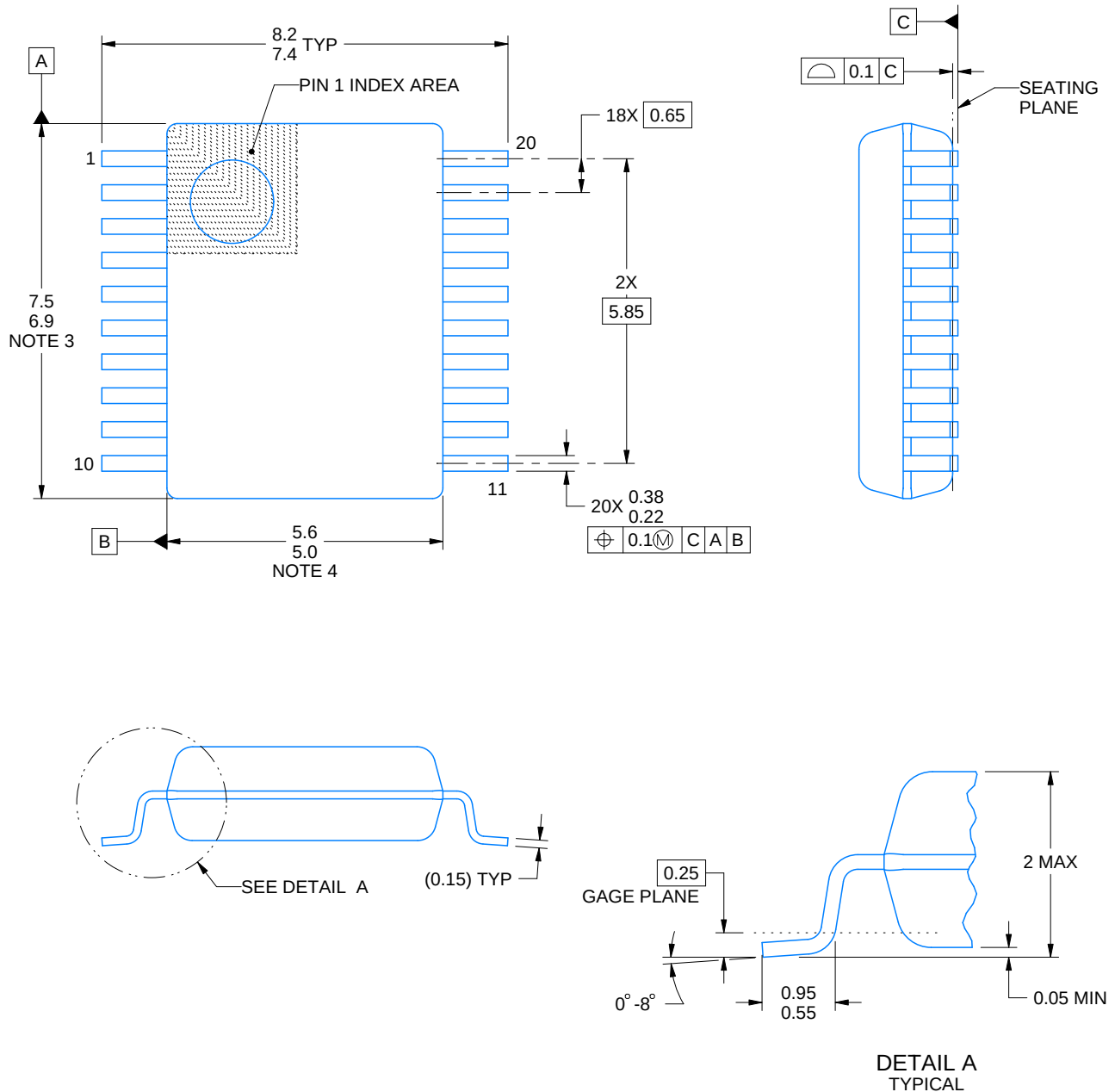
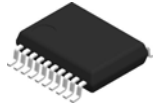
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
84030012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8403001SA	W	CFP	20	25	506.98	26.16	6220	NA
SN74ALS245A-1N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS245A-1N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS245AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS245AN.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74AS245DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74AS245DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74AS245N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AS245N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ALS245AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS245AFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS245AW	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54ALS245AW.A	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54AS245FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AS245FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20



4214851/B 08/2019

NOTES:

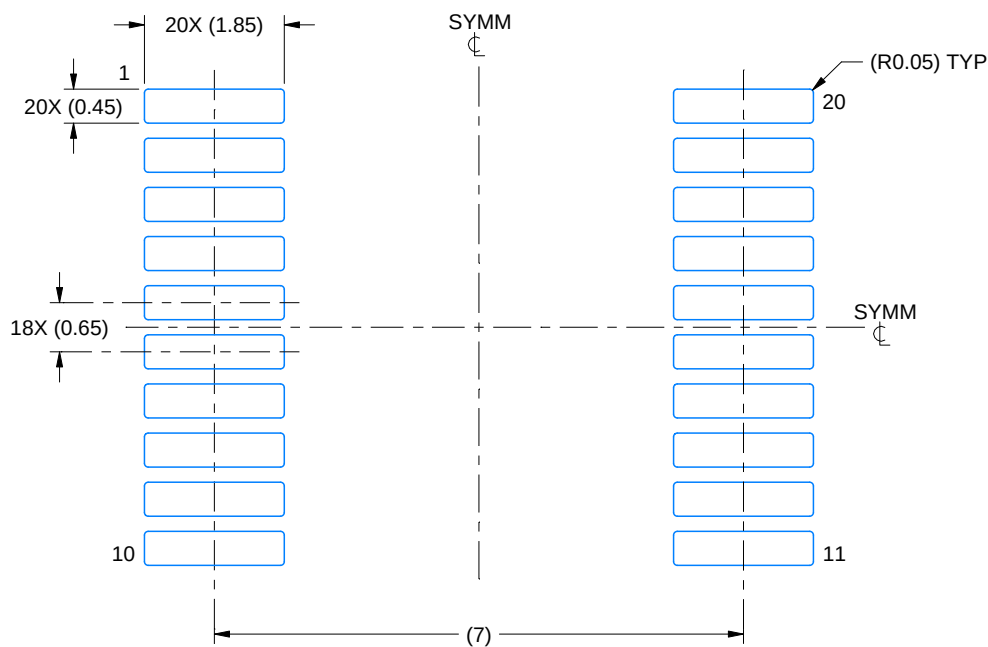
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

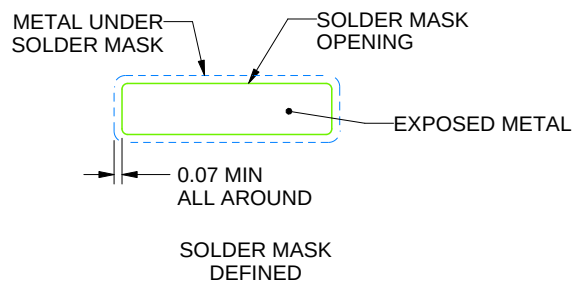
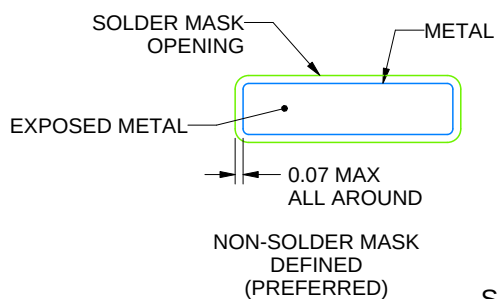
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

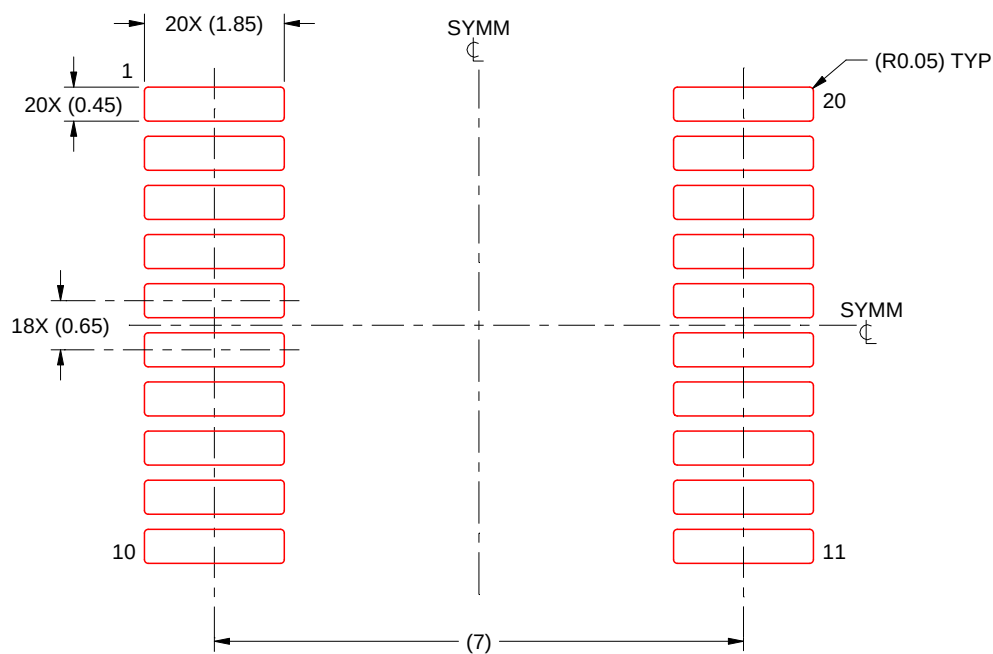
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

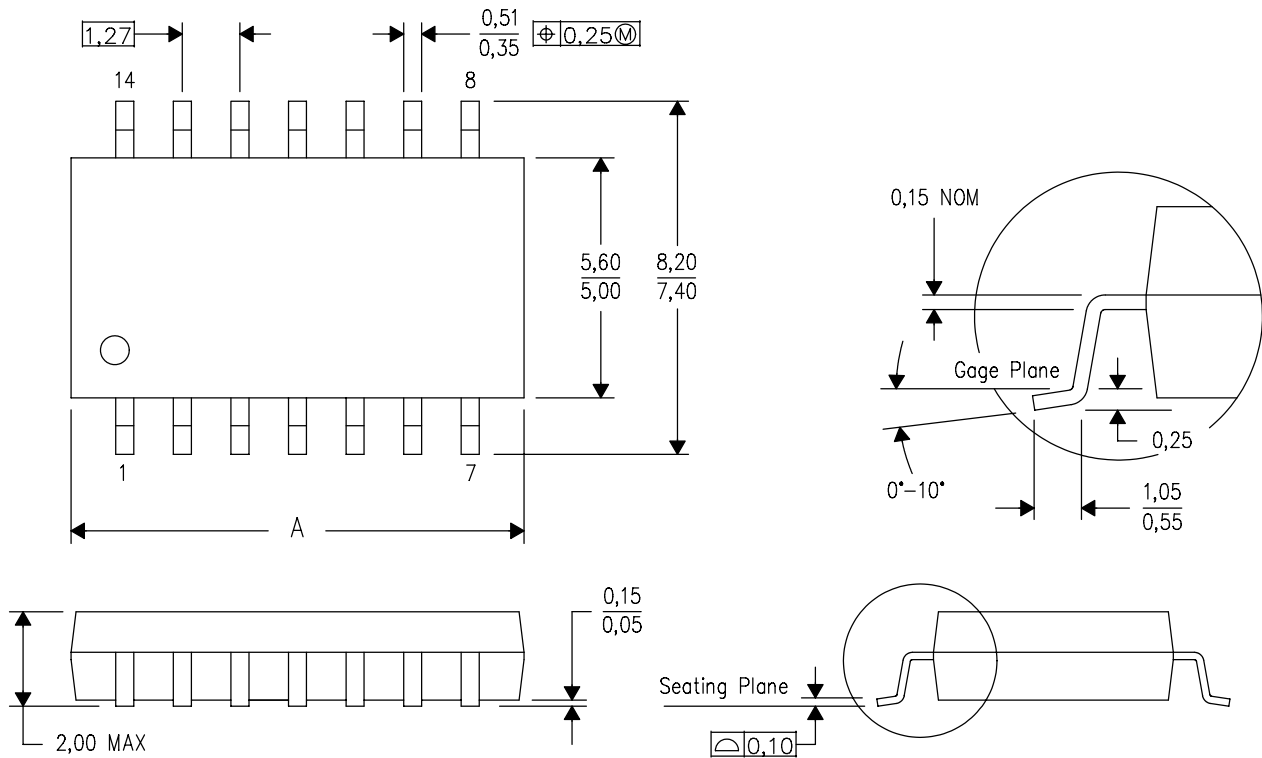
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

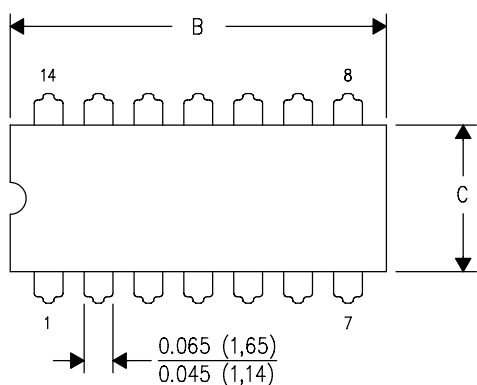
4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

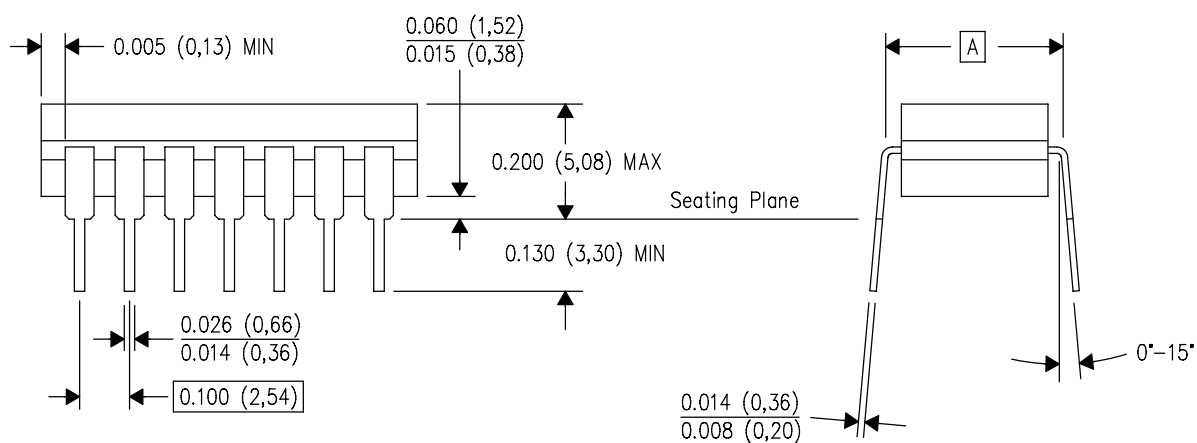
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

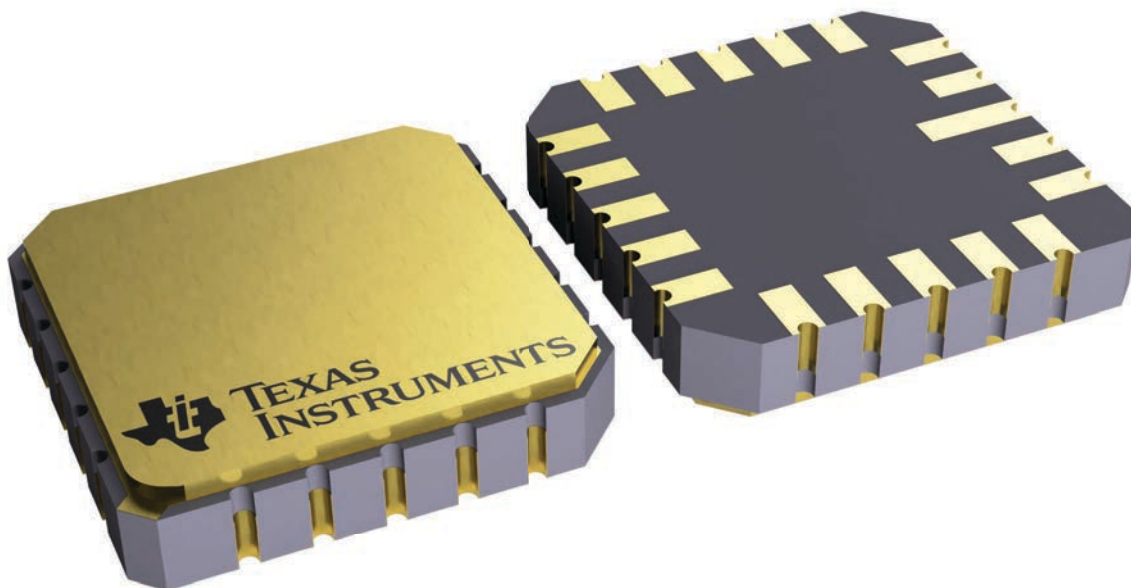
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

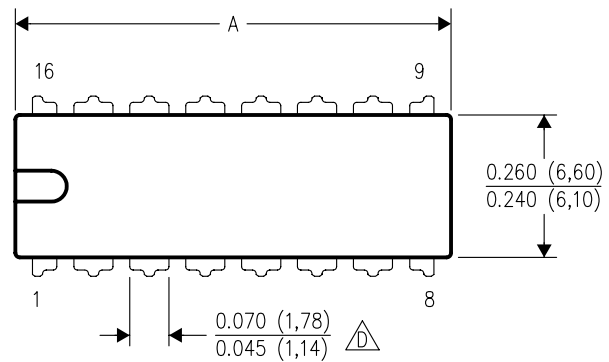


4229370VA\

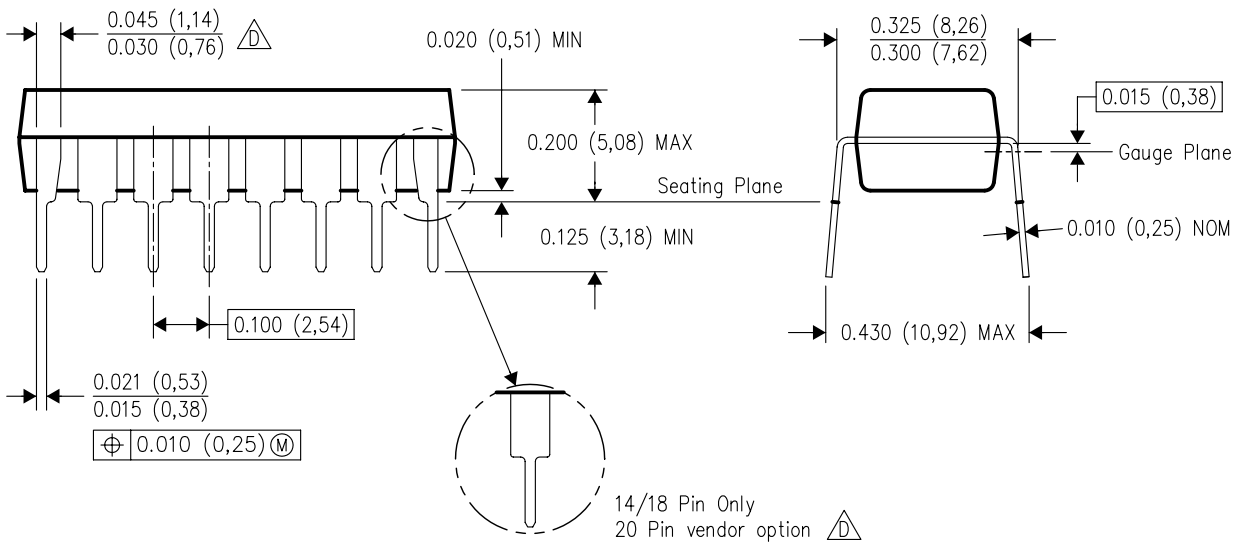
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

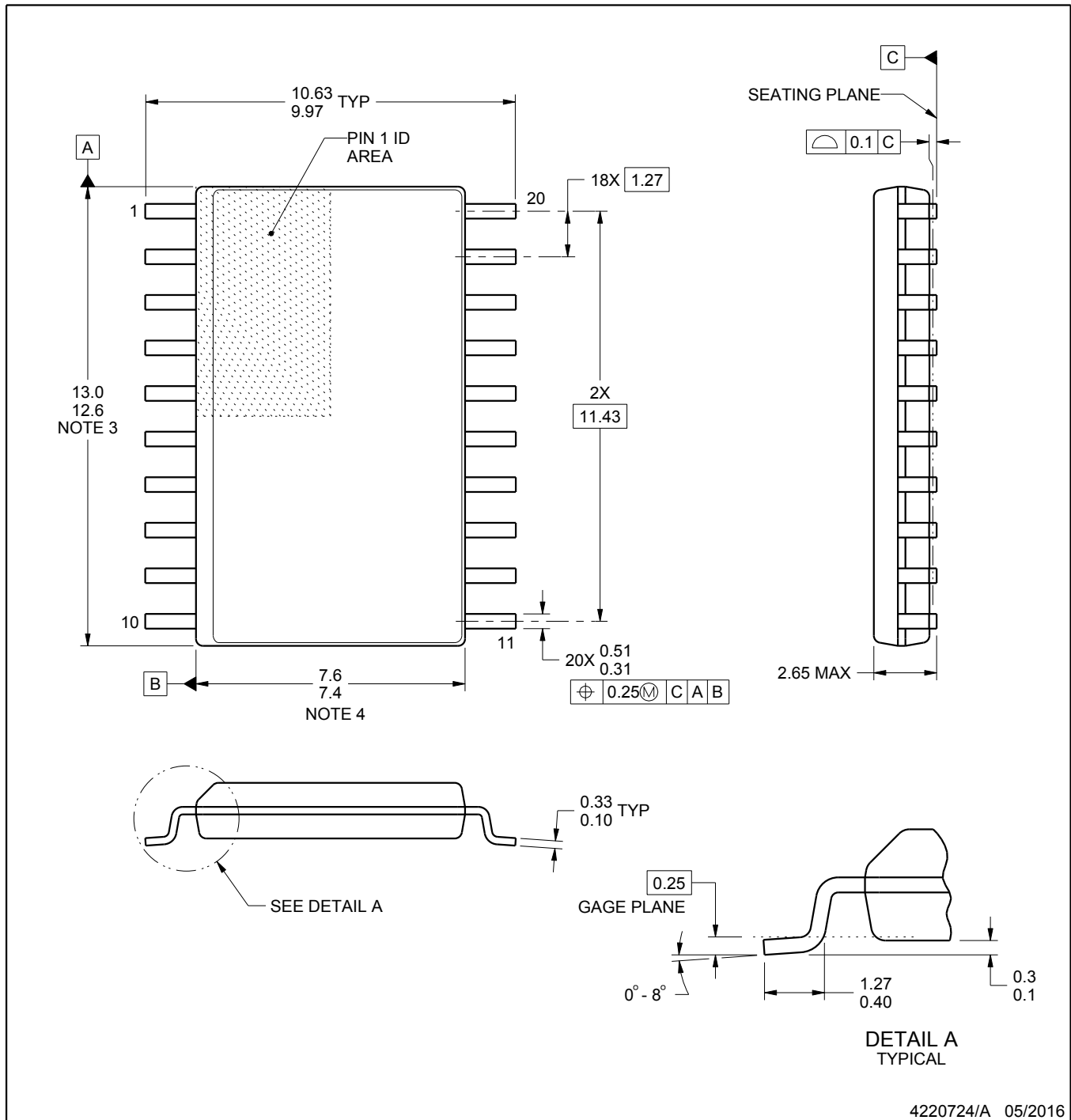
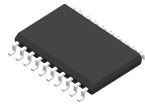


PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220724/A 05/2016

NOTES:

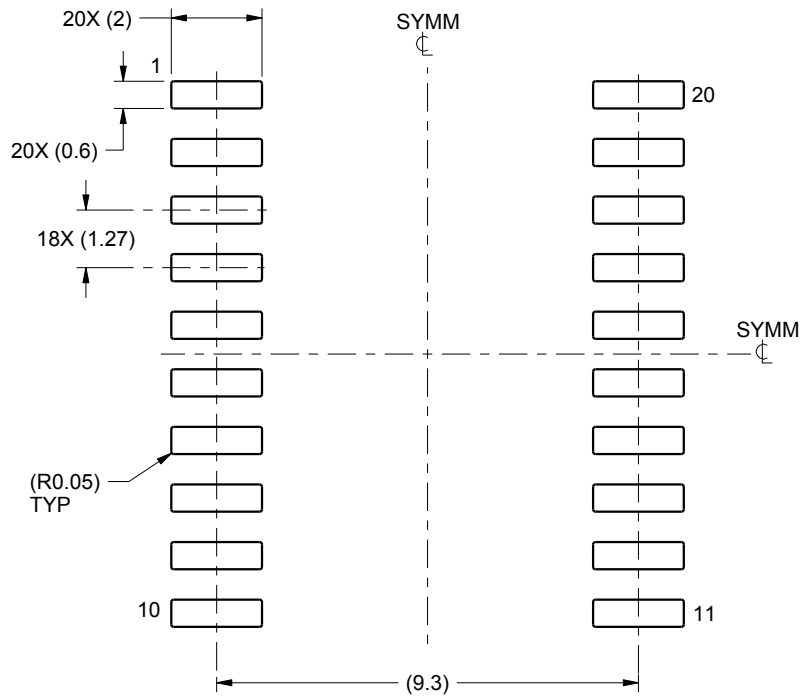
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

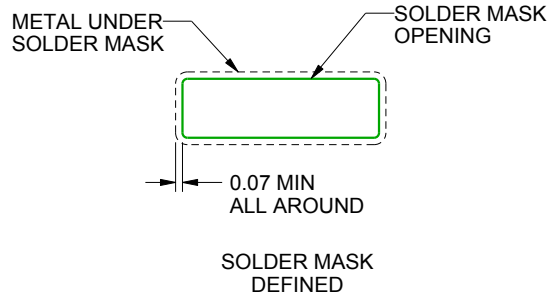
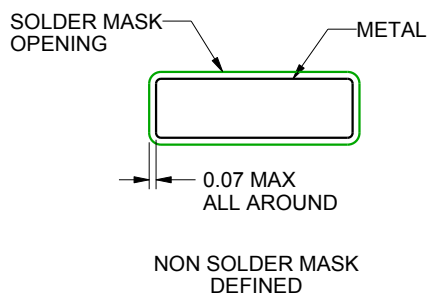
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

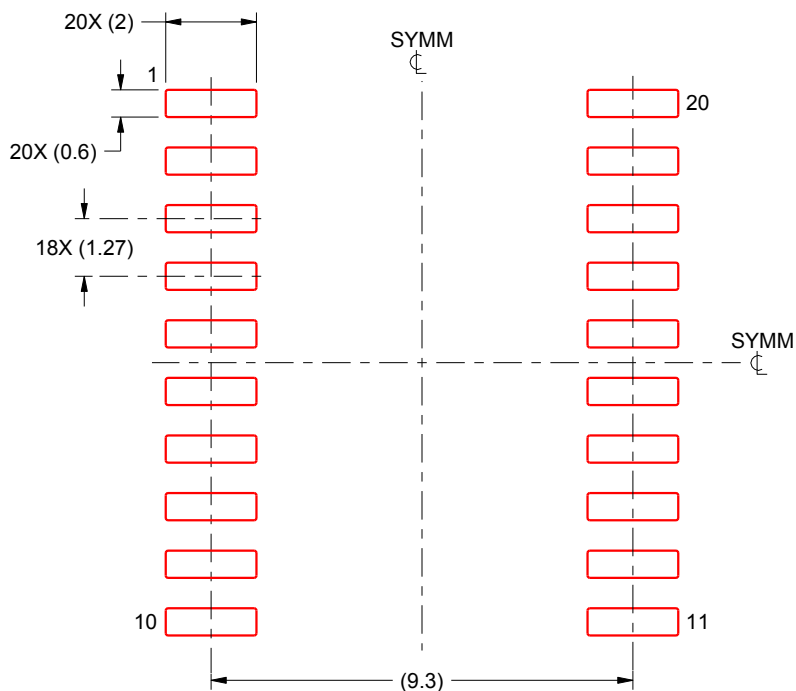
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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