

SN54AS756, SN74AS756, SN74AS757 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

SDAS040B – DECEMBER 1983 – REVISED JANUARY 1995

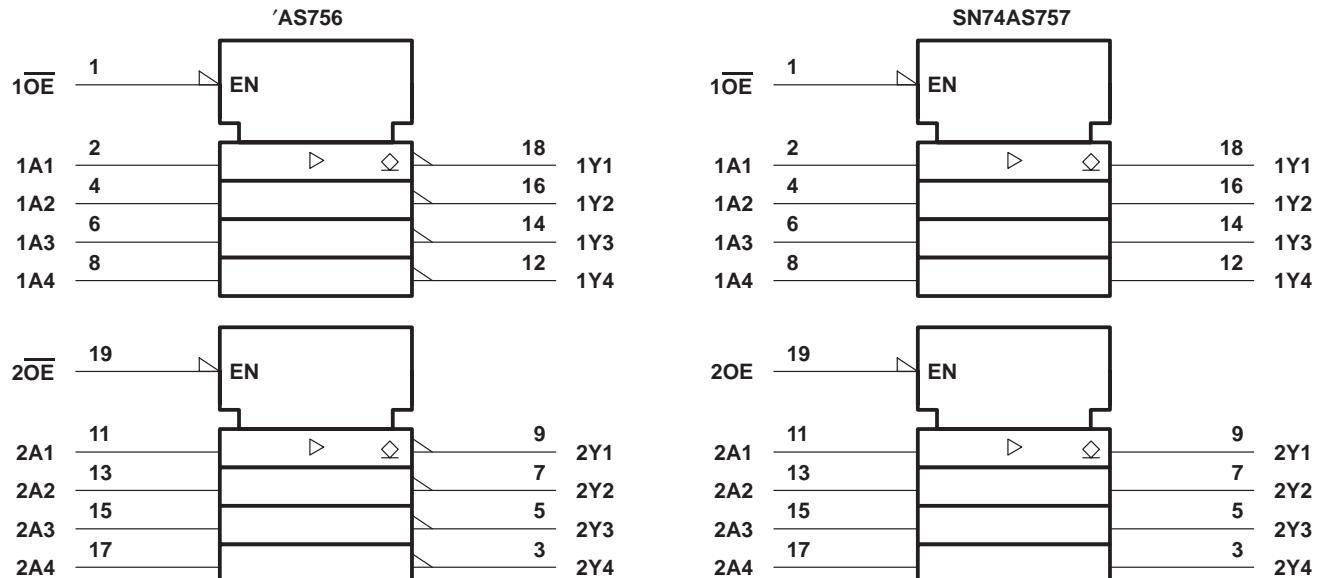
- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- Eliminate the Need for 3-State Overlap Protection
- pnp Inputs Reduce dc Loading
- Open-Collector Versions of 'AS240A and 'AS241
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

These octal buffers and line drivers are designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for 3-state overlap protection. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable (\overline{OE}) inputs, and complementary OE and \overline{OE} inputs. These devices feature high fan-out and improved fan-in.

The SN54AS756 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS756 and SN74AS757 are characterized for operation from 0°C to 70°C .

logic symbols[‡]



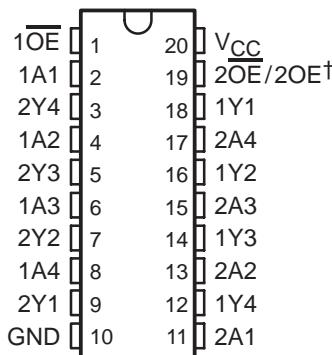
[‡] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

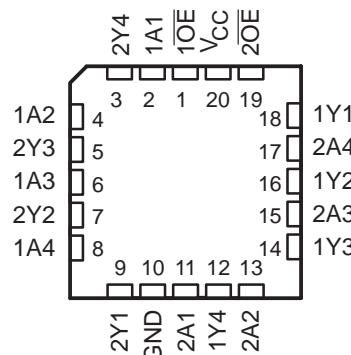


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SN54AS756 . . . J PACKAGE SN74AS756, SN74AS757 . . . DW OR N PACKAGE (TOP VIEW)



SN54AS756 . . . FK PACKAGE (TOP VIEW)

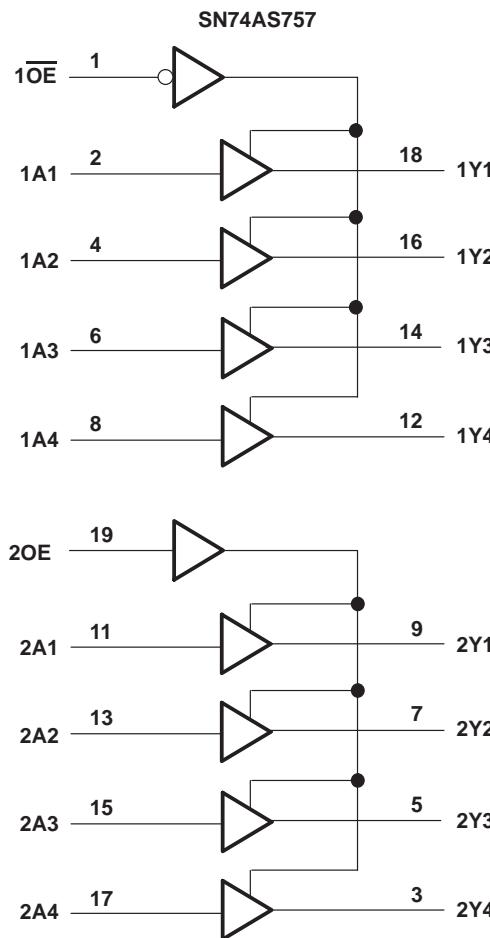
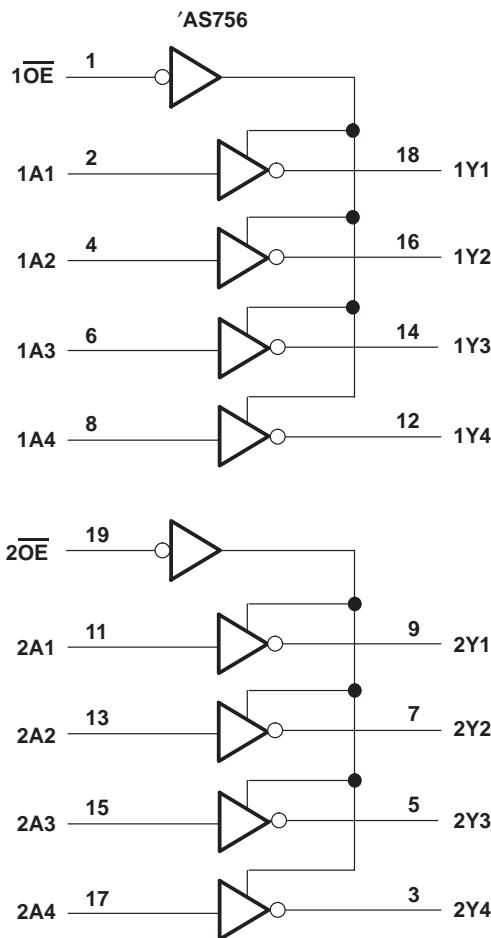


[†] 2OE for 'AS756 or 2OE for SN74AS757

SN54AS756, SN74AS756, SN74AS757 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

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logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**SN54AS756, SN74AS756, SN74AS757
OCTAL BUFFERS AND LINE DRIVERS
WITH OPEN-COLLECTOR OUTPUTS**

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recommended operating conditions

		SN54AS756			SN74AS756 SN74AS757			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
V _{OH}	High-level output voltage			5.5			5.5	V
I _{OL}	Low-level output current			48			64	mA
T _A	Operating free-air temperature	-55	125	0	0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS756			SN74AS756 SN74AS757			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2			-1.2	V
I _{OH}	V _{CC} = 4.5 V, V _{OH} = 5.5 V			0.1			0.1	mA
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 48 mA		0.55				V
		I _{OL} = 64 mA					0.55	
I _I	V _{CC} = 5.5 V, V _I = 7 V			0.1			0.1	mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V			20			20	μA
I _{IL}	A inputs of SN74AS757 only	V _{CC} = 5.5 V, V _I = 0.4 V			-1		-1	mA
	All other inputs				-0.5		-0.5	
I _{CC}	'AS756	V _{CC} = 5.5 V	Outputs high	9	15	9	15	mA
			Outputs low	51	80	51	80	
	SN74AS757	V _{CC} = 5.5 V	Outputs high	21	33	21	33	
			Outputs low	61	95	61	95	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

**SN54AS756, SN74AS756, SN74AS757
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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, $T_A = \text{MIN to MAX}^\dagger$				UNIT	
			SN54AS756		SN74AS756			
			MIN	MAX	MIN	MAX		
t_{PLH}	A	Y	3	20	3	19	ns	
t_{PHL}			1	7	1	6		
t_{PLH}	\overline{OE}	Y	3	22	3	19.5	ns	
t_{PHL}			1	8.5	1	7.5		

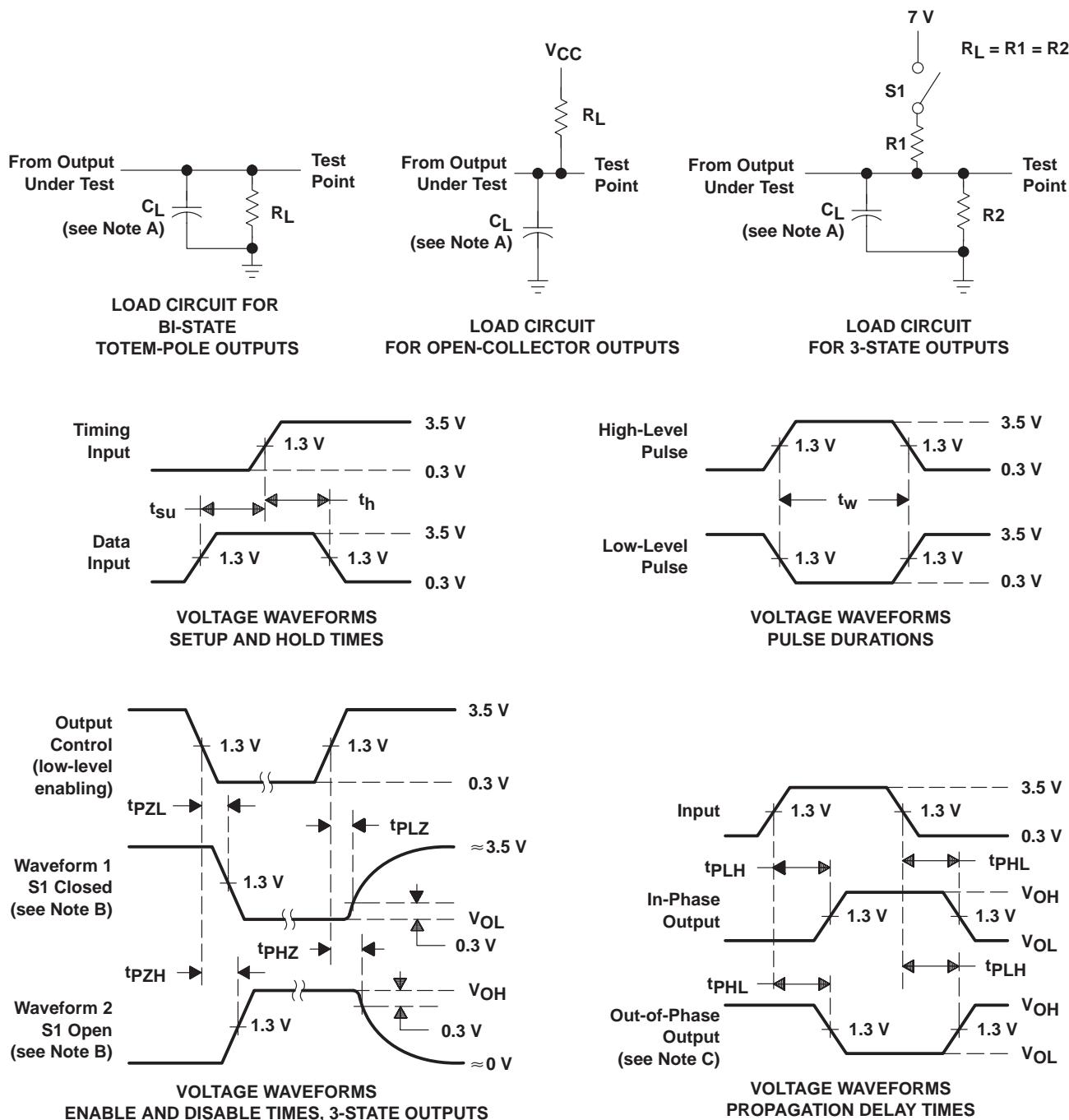
[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, $T_A = \text{MIN to MAX}^\dagger$				UNIT	
			SN74AS757					
			MIN	MAX				
t_{PLH}	A	Y	3	18.5			ns	
t_{PHL}			1	6				
t_{PLH}	$1\overline{OE}$	1Y	3	20			ns	
t_{PHL}			1	7				
t_{PLH}	2OE	2Y	3	21			ns	
t_{PHL}			1	7.5				

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-90563012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-90563012A SNJ54AS756FK
5962-9056301RA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9056301RA SNJ54AS756J
5962-9056301SA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9056301SA SNJ54AS756W
SN54AS756J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54AS756J
SN54AS756J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54AS756J
SN74AS756DW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS756
SN74AS756DW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS756
SN74AS756N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS756N
SN74AS756N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS756N
SN74AS757DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	0 to 70	AS757
SN74AS757DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS757
SN74AS757DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS757
SN74AS757N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS757N
SN74AS757N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS757N
SNJ54AS756FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-90563012A SNJ54AS756FK
SNJ54AS756FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-90563012A SNJ54AS756FK
SNJ54AS756J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9056301RA SNJ54AS756J
SNJ54AS756J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9056301RA SNJ54AS756J
SNJ54AS756W	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9056301SA SNJ54AS756W

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54AS756W.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9056301SA SNJ54AS756W

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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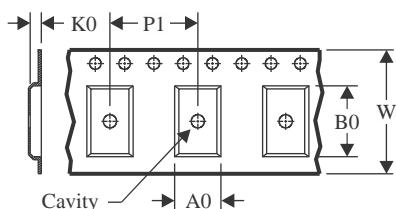
OTHER QUALIFIED VERSIONS OF SN54AS756, SN74AS756 :

- Catalog : [SN74AS756](#)
- Military : [SN54AS756](#)

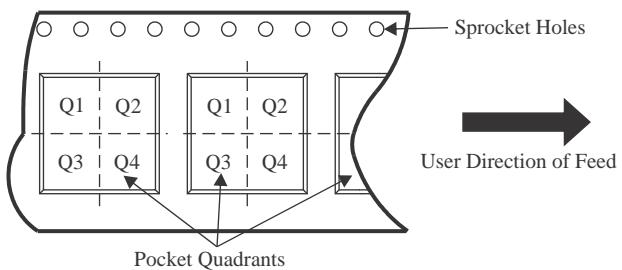
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


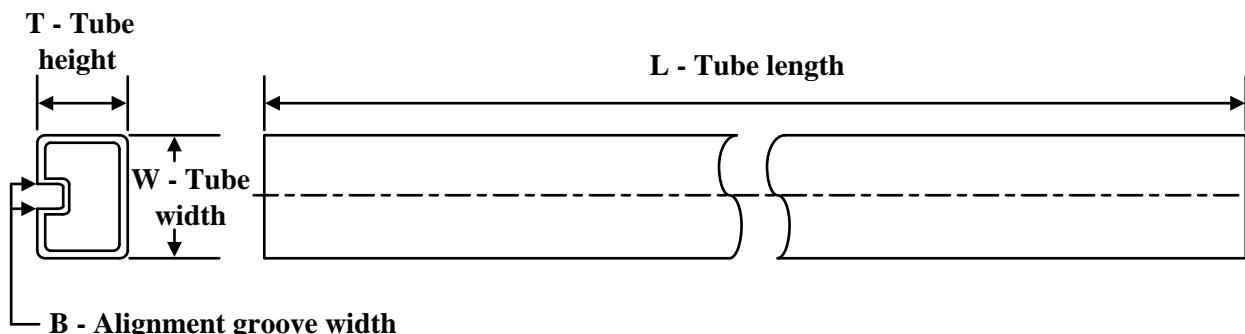
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AS757DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AS757DWR	SOIC	DW	20	2000	356.0	356.0	45.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
5962-90563012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9056301SA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AS756DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74AS756DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74AS756N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AS756N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74AS757N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AS757N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AS756FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AS756FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AS756W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54AS756W.A	W	CFP	20	25	506.98	26.16	6220	NA

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

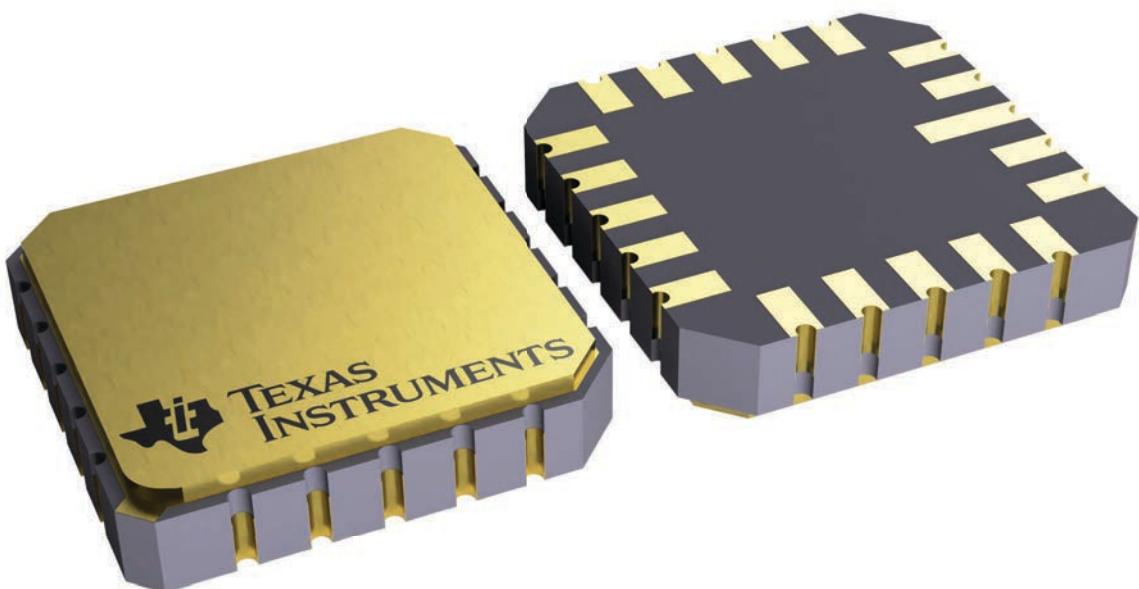
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

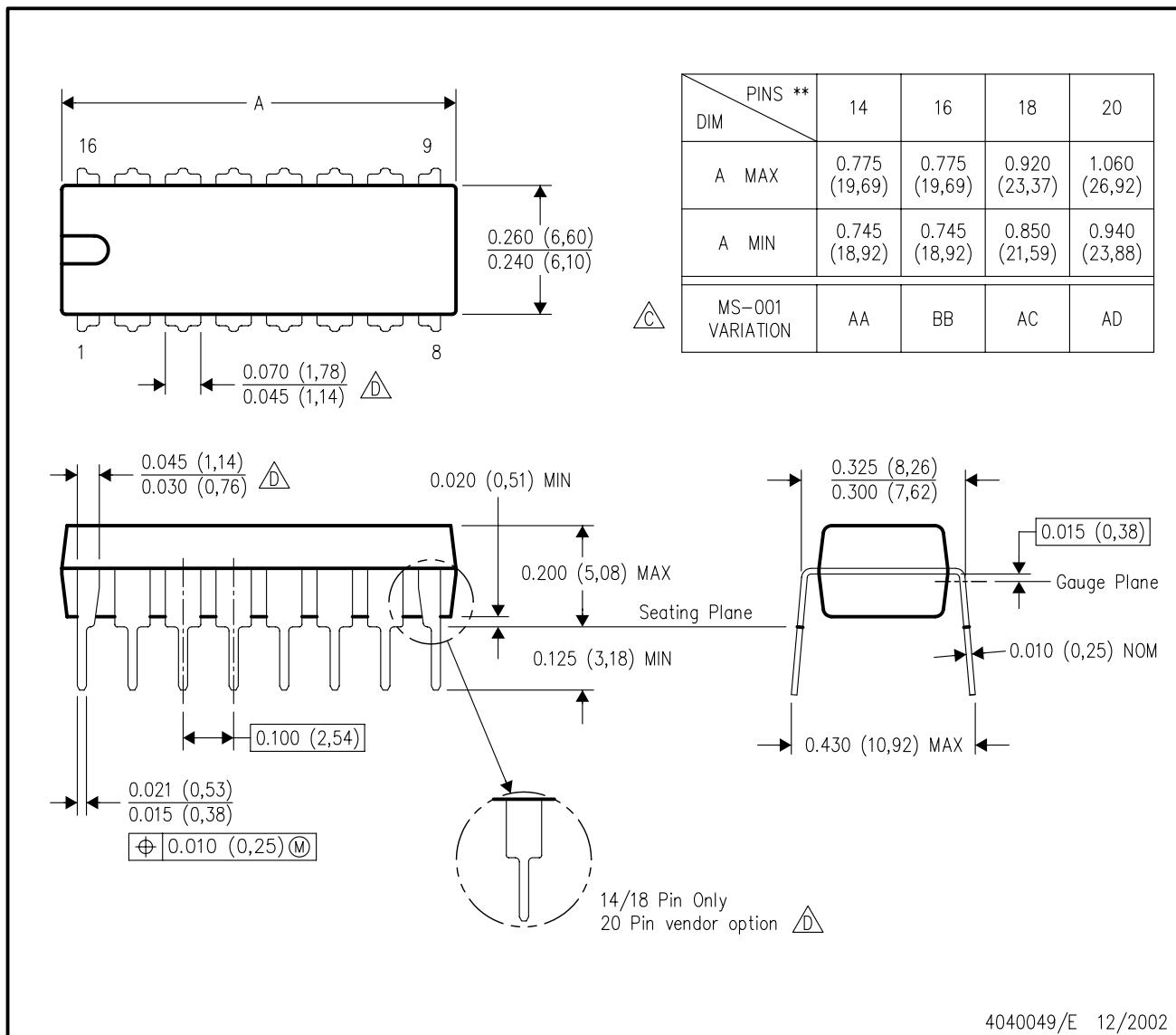


4229370VA\

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

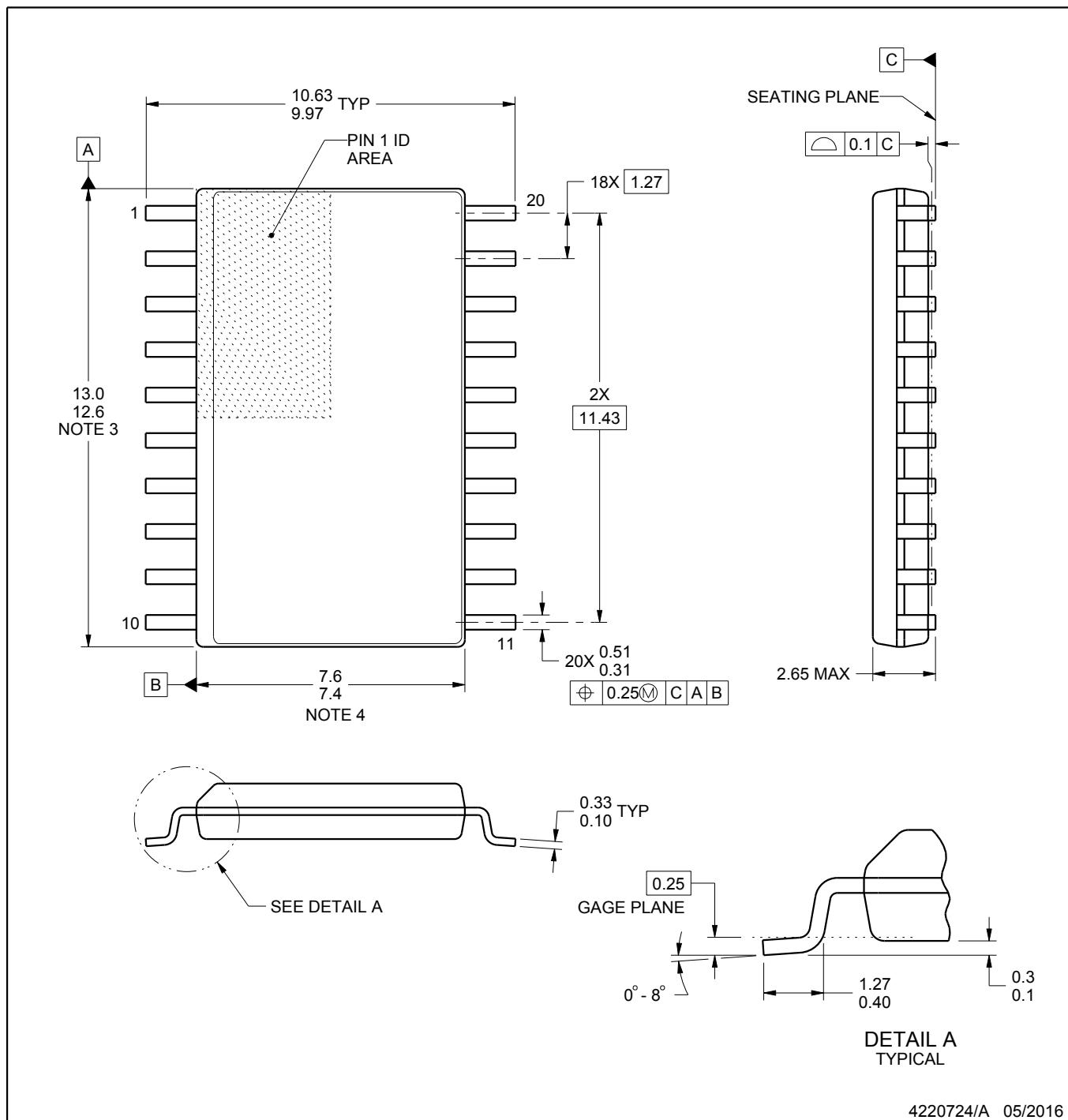


PACKAGE OUTLINE

DW0020A

SOIC - 2.65 mm max height

SOIC



NOTES:

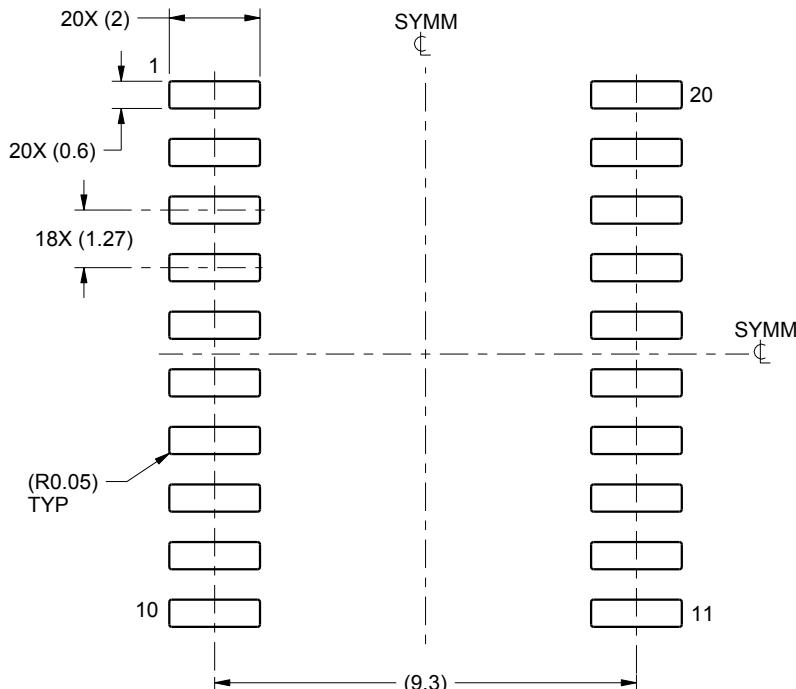
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

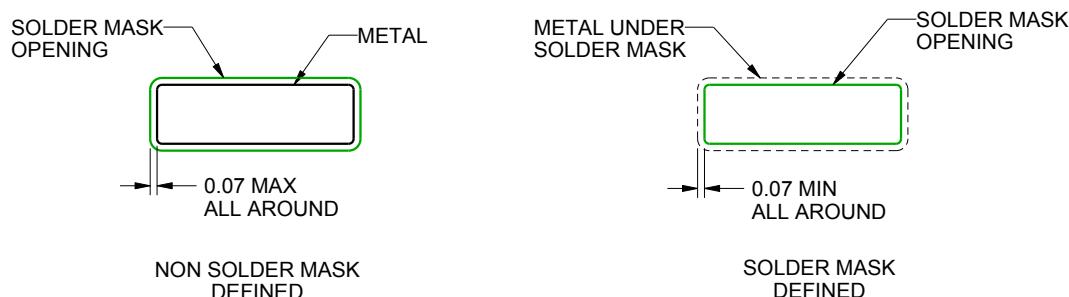
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

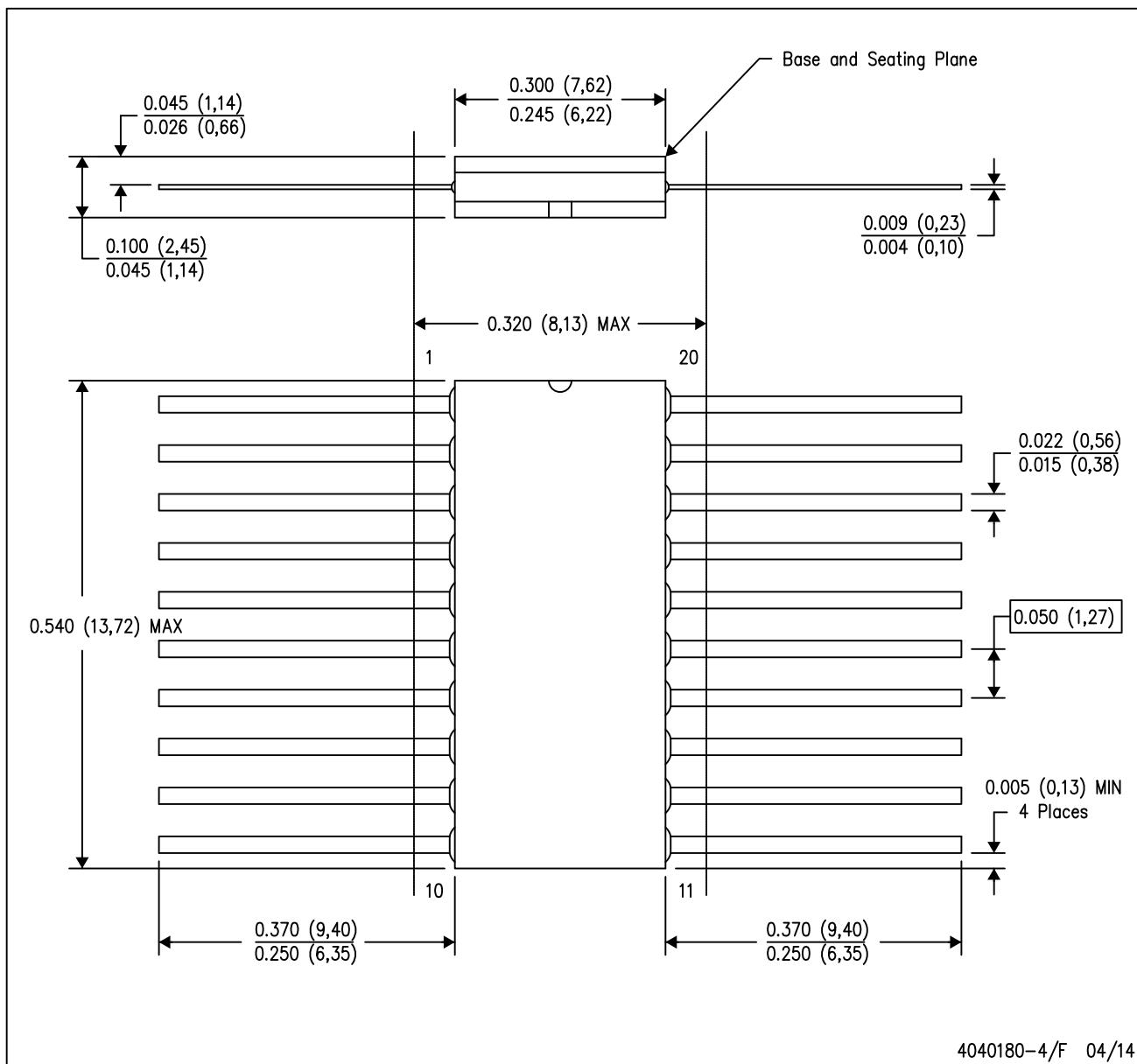
4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

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