

- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

### description

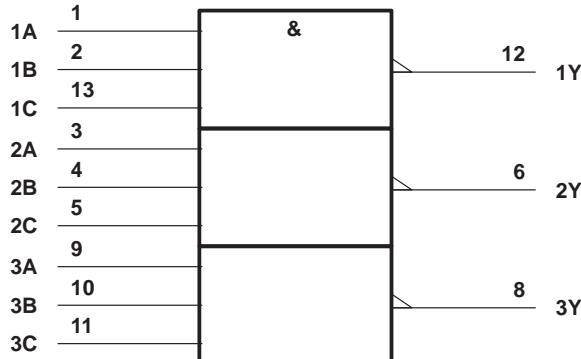
These devices contain three independent 3-input NAND gates. They perform the Boolean functions  $Y = \overline{A} \bullet \overline{B} \bullet \overline{C}$  or  $Y = \overline{A} + \overline{B} + \overline{C}$  in positive logic.

The SN54F10 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74F10 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE  
(each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

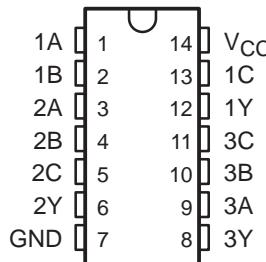
### logic symbol<sup>†</sup>



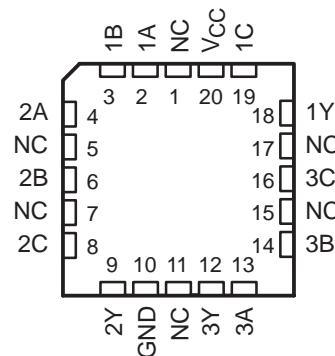
<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.

SN54F10 . . . J PACKAGE  
SN74F10 . . . D OR N PACKAGE  
(TOP VIEW)

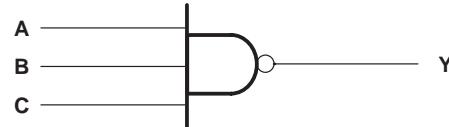


SN54F10 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

### logic diagram, each gate (positive logic)



# SN54F10, SN74F10 TRIPLE 3-INPUT POSITIVE-NAND GATES

SDFS039A – MARCH 1987 – REVISED OCTOBER 1993

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V		
Input voltage range, $V_I$ (see Note 1) .....	–1.2 V to 7 V		
Input current range .....	–30 mA to 5 mA		
Voltage range applied to any output in the high state .....	–0.5 V to $V_{CC}$		
Current into any output in the low state .....	40 mA		
Operating free-air temperature range: SN54F10 .....	–55°C to 125°C		
SN74F10 .....	0°C to 70°C		
Storage temperature range .....	–65°C to 150°C		

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

		SN54F10			SN74F10			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage		2		2			V
$V_{IL}$	Low-level input voltage			0.8		0.8		V
$I_{IK}$	Input clamp current			–18		–18		mA
$I_{OH}$	High-level output current			–1		–1		mA
$I_{OL}$	Low-level output current			20		20		mA
$T_A$	Operating free-air temperature	–55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54F10			SN74F10			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IK}$	$V_{CC} = 4.5$ V, $I_J = –18$ mA		–1.2			–1.2		V
$V_{OH}$	$V_{CC} = 4.5$ V, $I_{OH} = –1$ mA	2.5	3.4		2.5	3.4		V
	$V_{CC} = 4.75$ V, $I_{OH} = –1$ mA			2.7				
$V_{OL}$	$V_{CC} = 4.5$ V, $I_{OL} = 20$ mA	0.3	0.5		0.3	0.5		V
$I_I$	$V_{CC} = 5.5$ V, $V_I = 7$ V		0.1			0.1		mA
$I_{IH}$	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20		20		μA
$I_{IL}$	$V_{CC} = 5.5$ V, $V_I = 0.5$ V			–0.6		–0.6		mA
$I_{OS}^§$	$V_{CC} = 5.5$ V, $V_O = 0$	–60	–150		–60	–150		mA
$I_{CCH}$	$V_{CC} = 5.5$ V, $V_I = 0$	1.4	2.1		1.4	2.1		mA
$I_{CCL}$	$V_{CC} = 5.5$ V, $V_I = 4.5$ V	5.1	7.7		5.1	7.7		mA

<sup>‡</sup>All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

<sup>§</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V}$ , $C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$ , $T_A = 25^\circ\text{C}$	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ , $C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$ , $T_A = \text{MIN to MAX}^\dagger$			UNIT	
			'F10			SN54F10		
			MIN	TYP	MAX	MIN	MAX	
$t_{PLH}$	A, B, or C	Y	1.6	3.3	5	1.2	7	1.6 6
			1	2.8	4.3	1	6.5	1 5.3

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and waveforms are shown in Section 1.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9757901Q2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9757901Q2A SNJ54F10FK
5962-9757901QCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9757901QC A SNJ54F10J
JM38510/33003B2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/33003B2A
JM38510/33003B2A.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/33003B2A
JM38510/33003BCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/33003BCA
JM38510/33003BCA.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/33003BCA
JM38510/33003BDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/33003BDA
JM38510/33003BDA.A	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/33003BDA
M38510/33003B2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/33003B2A
M38510/33003BCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/33003BCA
M38510/33003BDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/33003BDA
SN54F10J	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54F10J
SN54F10J.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54F10J
SN74F10D	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	0 to 70	F10
SN74F10DR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F10
SN74F10DR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F10
SN74F10N	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F10N
SN74F10N.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F10N
SN74F10NSR	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74F10

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74F10NSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74F10
<a href="#">SNJ54F10FK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9757901Q2A SNJ54F 10FK
SNJ54F10FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9757901Q2A SNJ54F 10FK
<a href="#">SNJ54F10J</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9757901QC A SNJ54F10J
SNJ54F10J.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9757901QC A SNJ54F10J

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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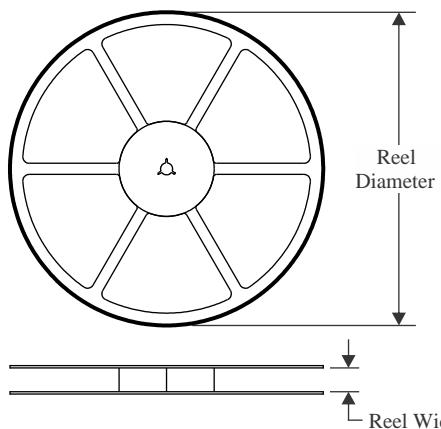
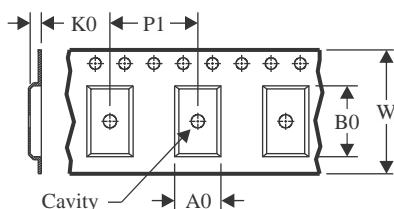
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54F10, SN74F10 :**

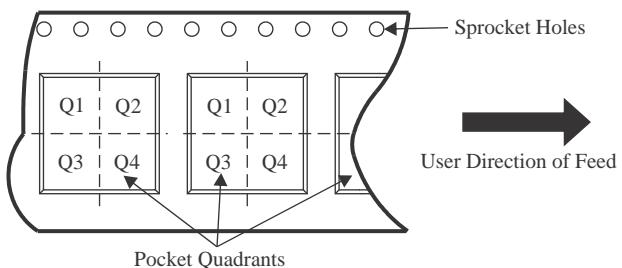
- Catalog : [SN74F10](#)
- Military : [SN54F10](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

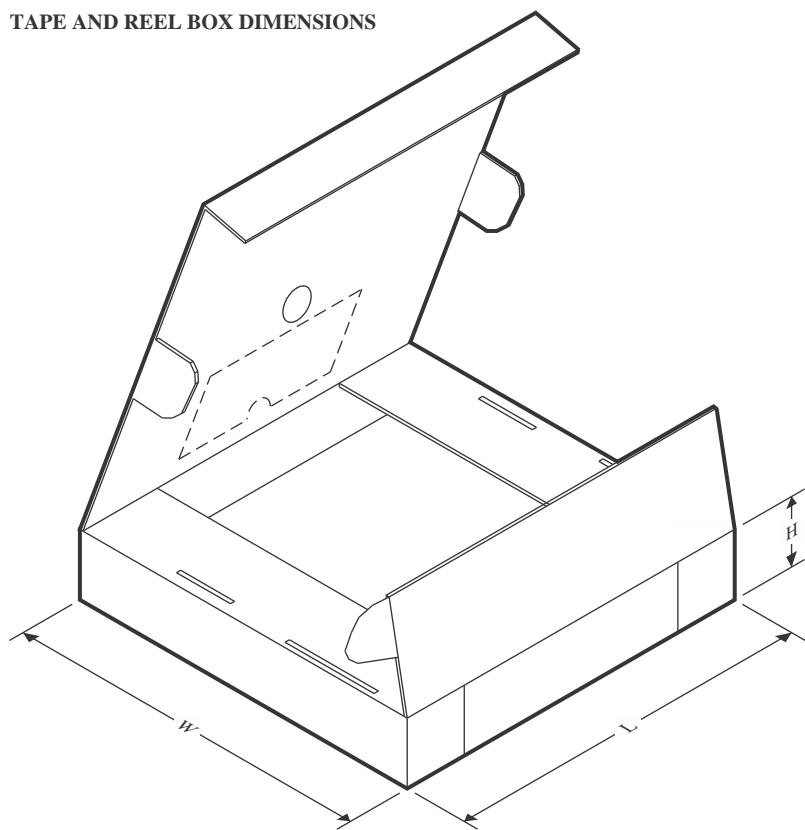
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


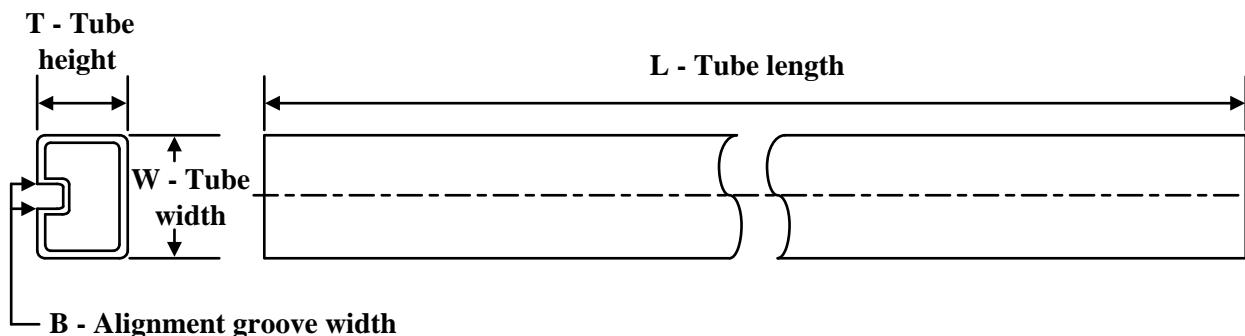
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F10DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74F10NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F10DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74F10NSR	SOP	NS	14	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

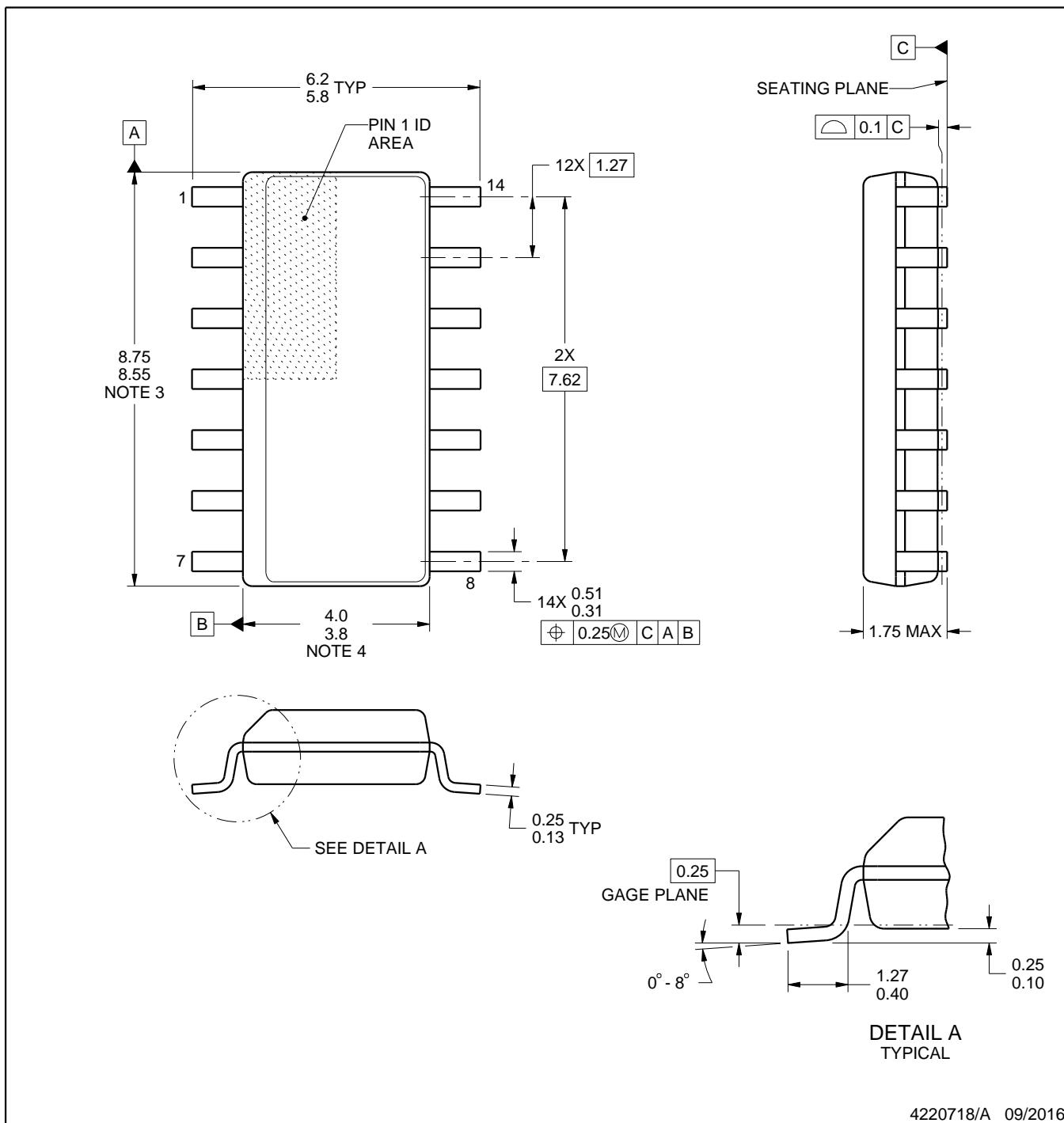
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9757901Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/33003B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/33003B2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/33003BDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/33003BDA.A	W	CFP	14	25	506.98	26.16	6220	NA
M38510/33003B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/33003BDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74F10N	N	PDIP	14	25	506	13.97	11230	4.32
SN74F10N	N	PDIP	14	25	506	13.97	11230	4.32
SN74F10N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74F10N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54F10FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54F10FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

# PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



## NOTES:

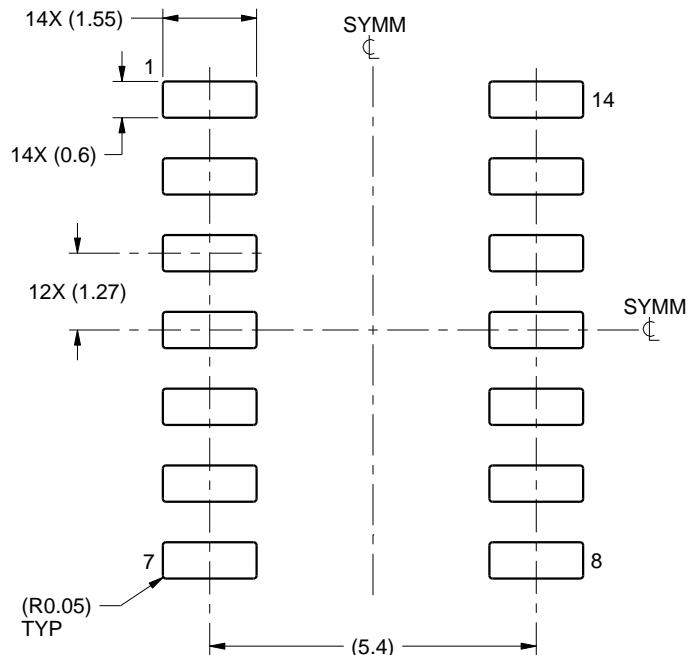
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

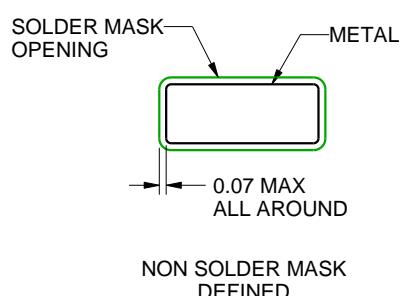
D0014A

SOIC - 1.75 mm max height

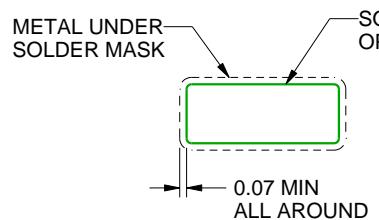
SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

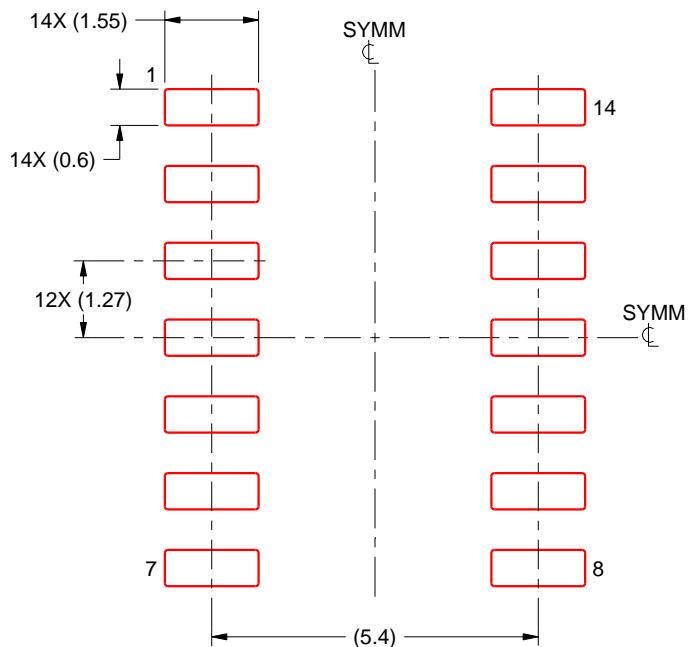
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

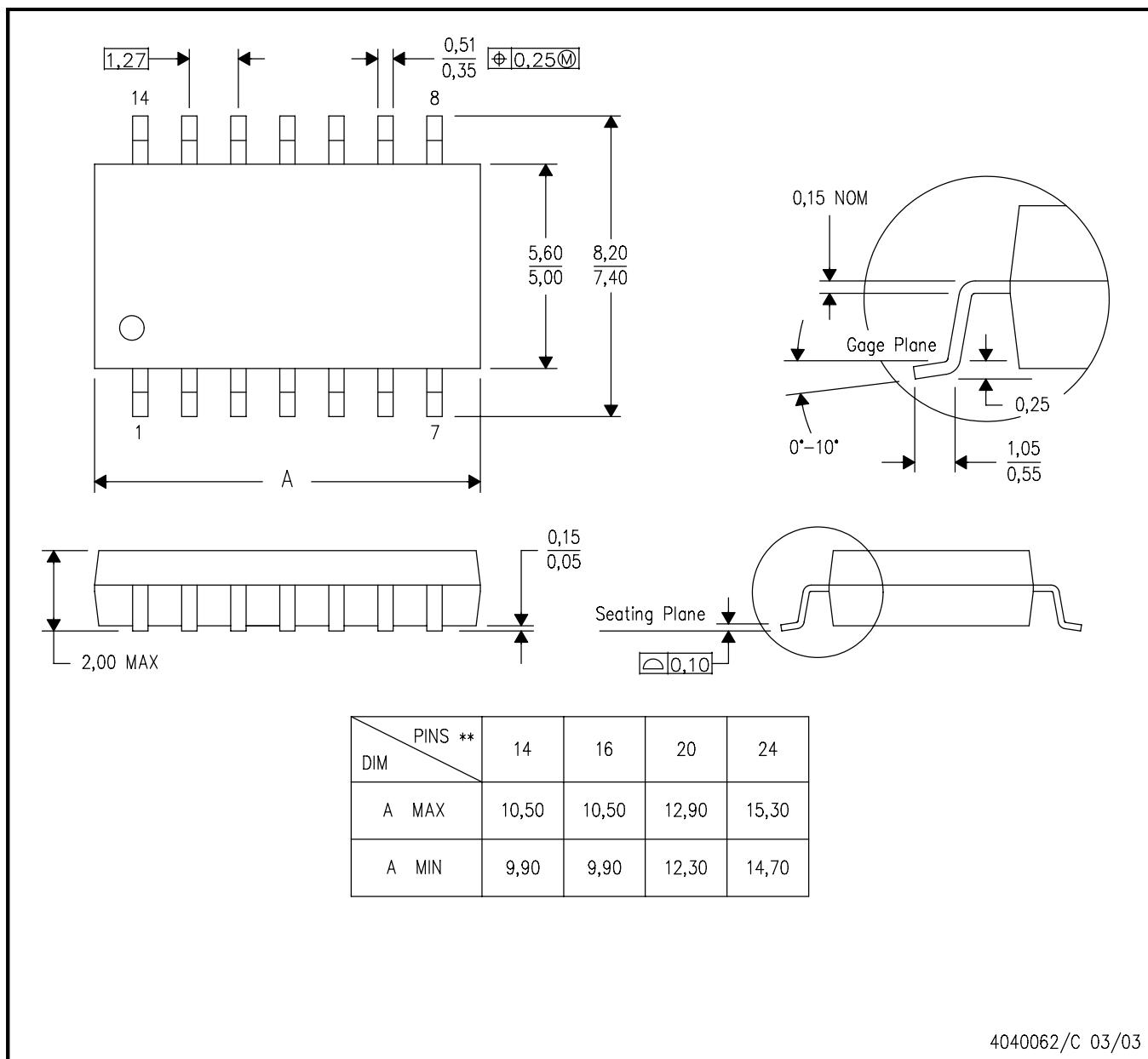
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

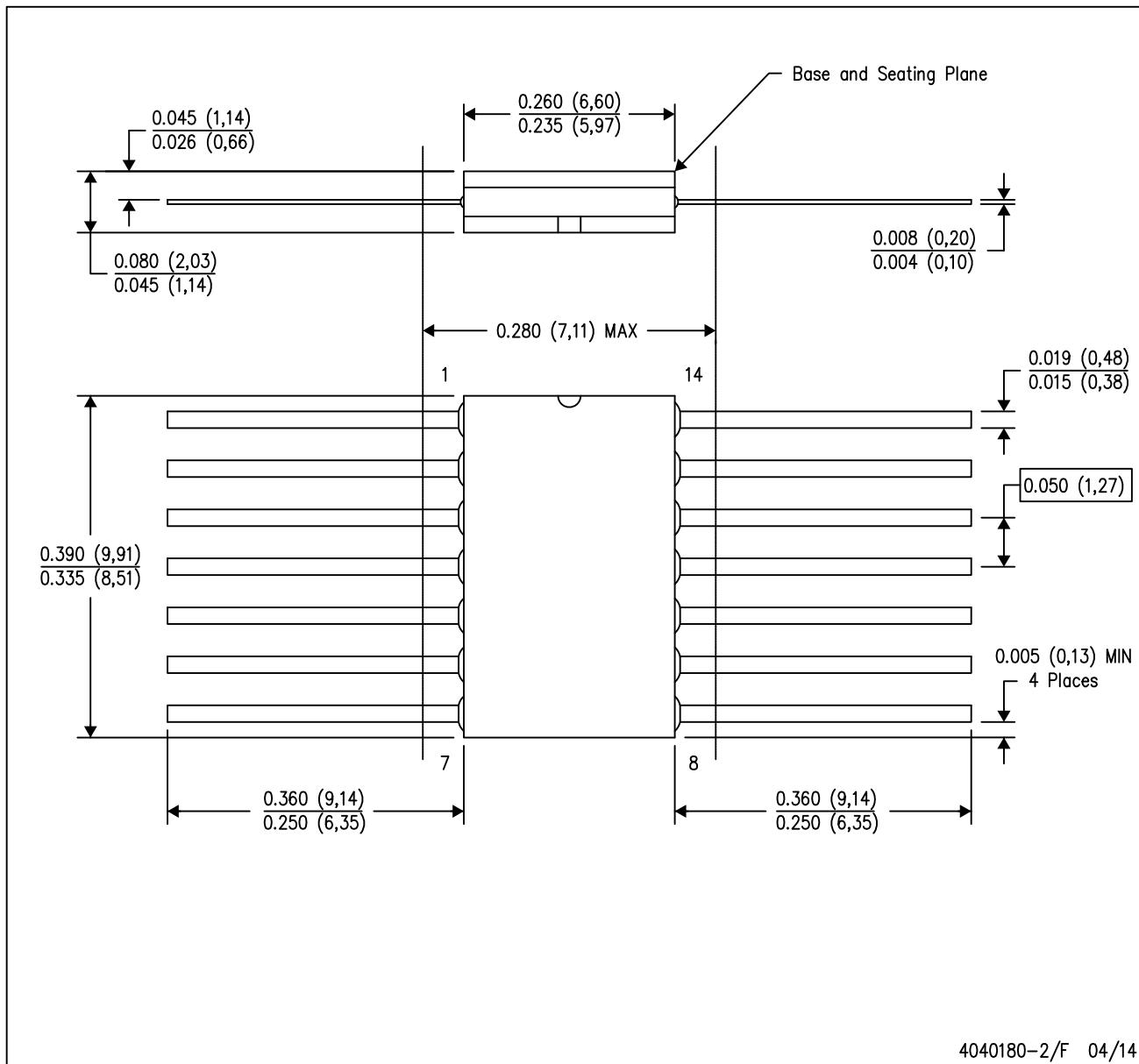


NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

4040062/C 03/03

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL-STD 1835 GDFP1-F14

# GENERIC PACKAGE VIEW

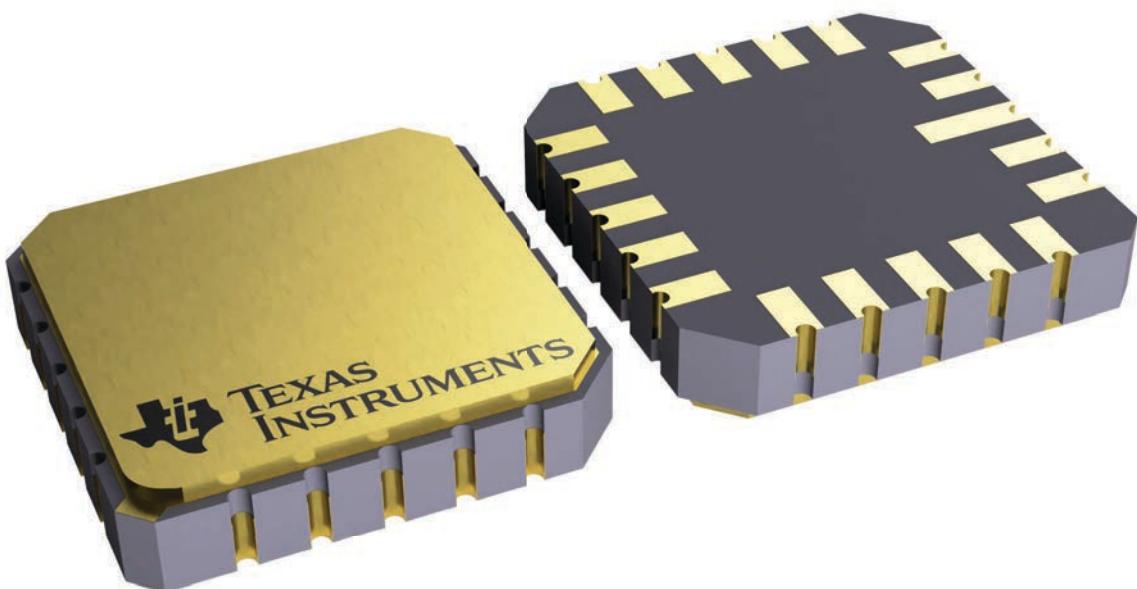
**FK 20**

**LCCC - 2.03 mm max height**

**8.89 x 8.89, 1.27 mm pitch**

**LEADLESS CERAMIC CHIP CARRIER**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



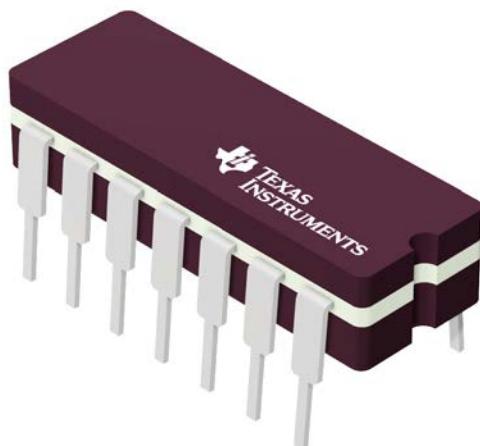
4229370VA\

# GENERIC PACKAGE VIEW

**J 14**

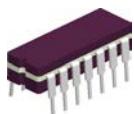
**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

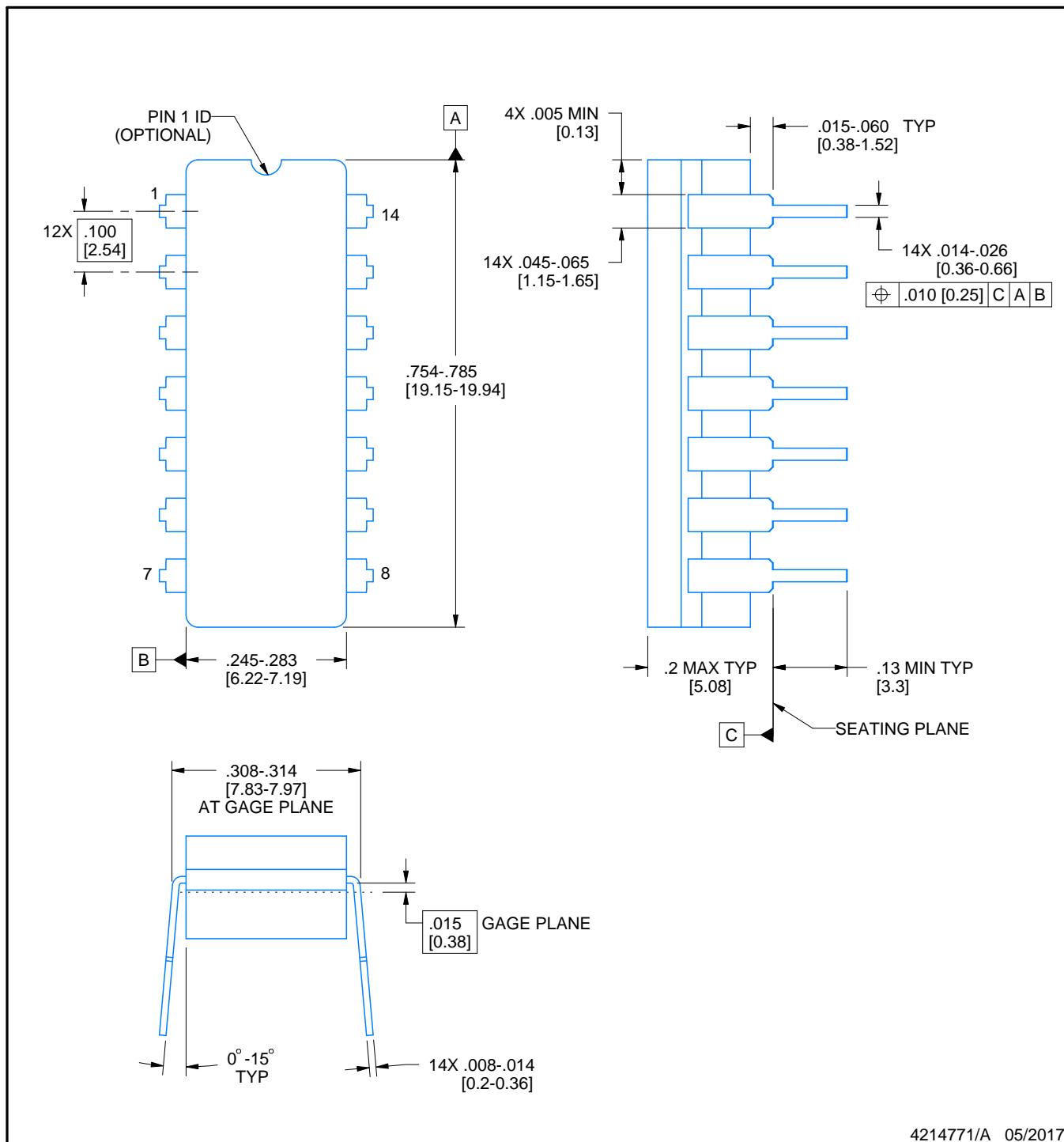


# PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

## NOTES:

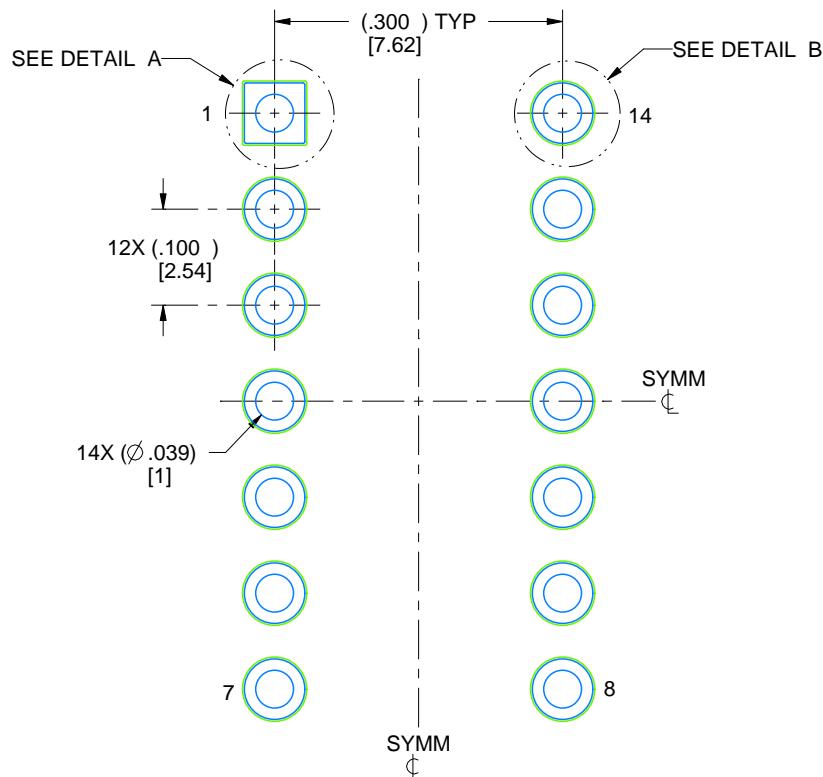
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

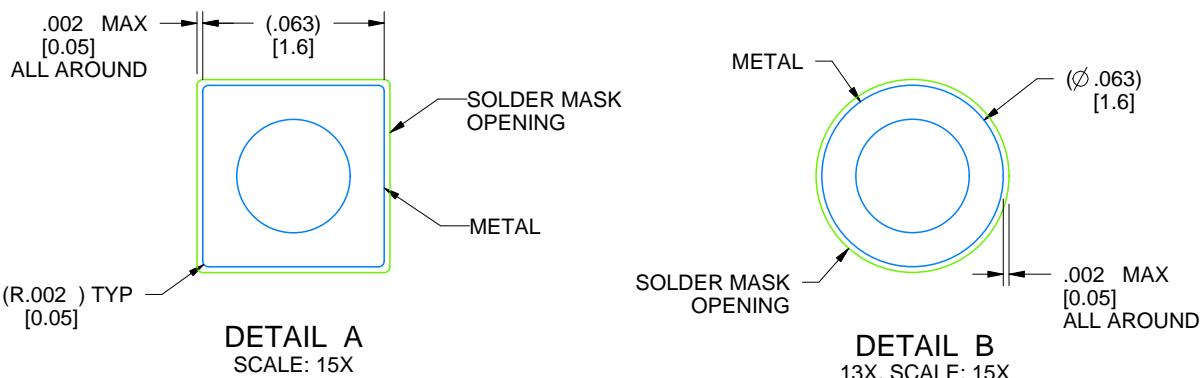
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X

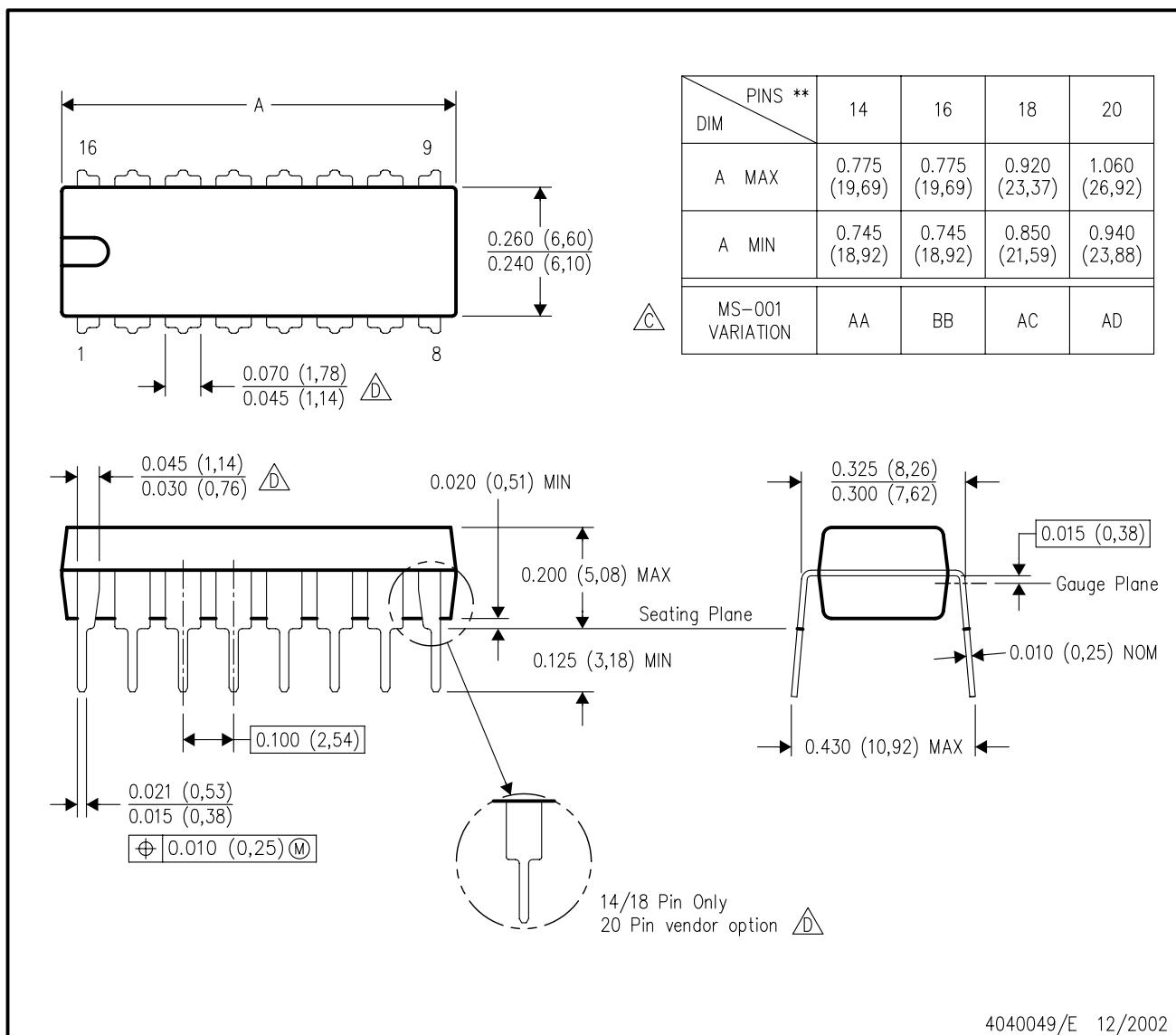


4214771/A 05/2017

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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