

SDLS048

SN54136, SN54LS136, SN74136, SN74LS136 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES WITH OPEN-COLLECTOR OUTPUTS

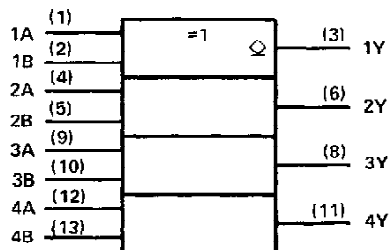
DECEMBER 1972 - REVISED MARCH 1988

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

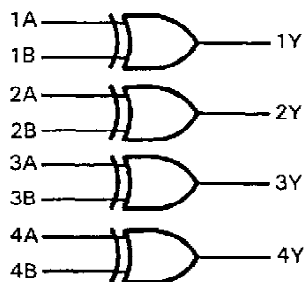
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

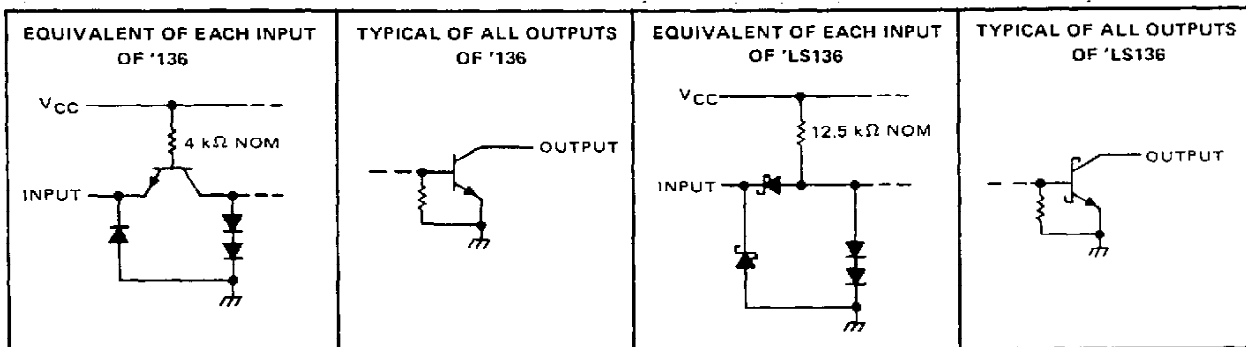
logic diagram (each gate)



positive logic

$$Y = A \oplus B = \bar{A} \cdot B + A \cdot \bar{B}$$

schematics of inputs and outputs



Resistor values shown are nominal.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54136, SN74136

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54136	-55°C to 125°C
SN74136	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54136			SN74136			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54136			SN74136			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -8 \text{ mA}$			-1.5			-1.5	V
I_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$						0.25	mA
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.7 \text{ V}, V_{OH} = 5.5 \text{ V}$			0.25				
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$			0.2			0.2	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{CC}	$V_{CC} = \text{MAX}, \text{ See Note 2}$			30			30	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with one input of each gate at 4.5 V, the other inputs grounded, and the outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	$C_L = 15 \text{ pF}, R_L = 400 \Omega,$ See Note 3	12	18		ns
t_{PHL}				39	50		
t_{PLH}	A or B	Other input high	See Note 3	14	22		ns
t_{PHL}				42	55		

¶ t_{PLH} propagation delay time, low-to-high-level output

t_{PHL} propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TEXAS
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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54LS136, SN74LS136

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS136	-55°C to 125°C
SN74LS136	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS136			SN74LS136			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS136			SN74LS136			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{OH} = 5.5 \text{ V}$			100			100	μA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$	0.25	0.4		0.25	0.4		V
	$I_{OL} = 8 \text{ mA}$				0.35	0.5		
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.2			0.2		mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		40			40		μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.8			-0.8		mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	6.1	10		6.1	10		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with one input of each gate at 4.5 V, the other inputs grounded, and the outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega, \text{ (See Note 3)}$	18	30		ns
t_{PHL}				18	30		
t_{PLH}	A or B	Other input high	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega, \text{ (See Note 3)}$	18	30		ns
t_{PHL}				18	30		

¶ t_{PLH} propagation delay time, low-to-high-level output

¶ t_{PHL} propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9231901MCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9231901MC A SNJ54LS136J
SN54LS136J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS136J
SN54LS136J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS136J
SN74LS136DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS136
SN74LS136DR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS136
SN74LS136N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS136N
SN74LS136N.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS136N
SN74LS136NE4	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS136N
SN74LS136NSR	NRND	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS136
SN74LS136NSR.A	NRND	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS136
SNJ54LS136J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9231901MC A SNJ54LS136J
SNJ54LS136J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9231901MC A SNJ54LS136J

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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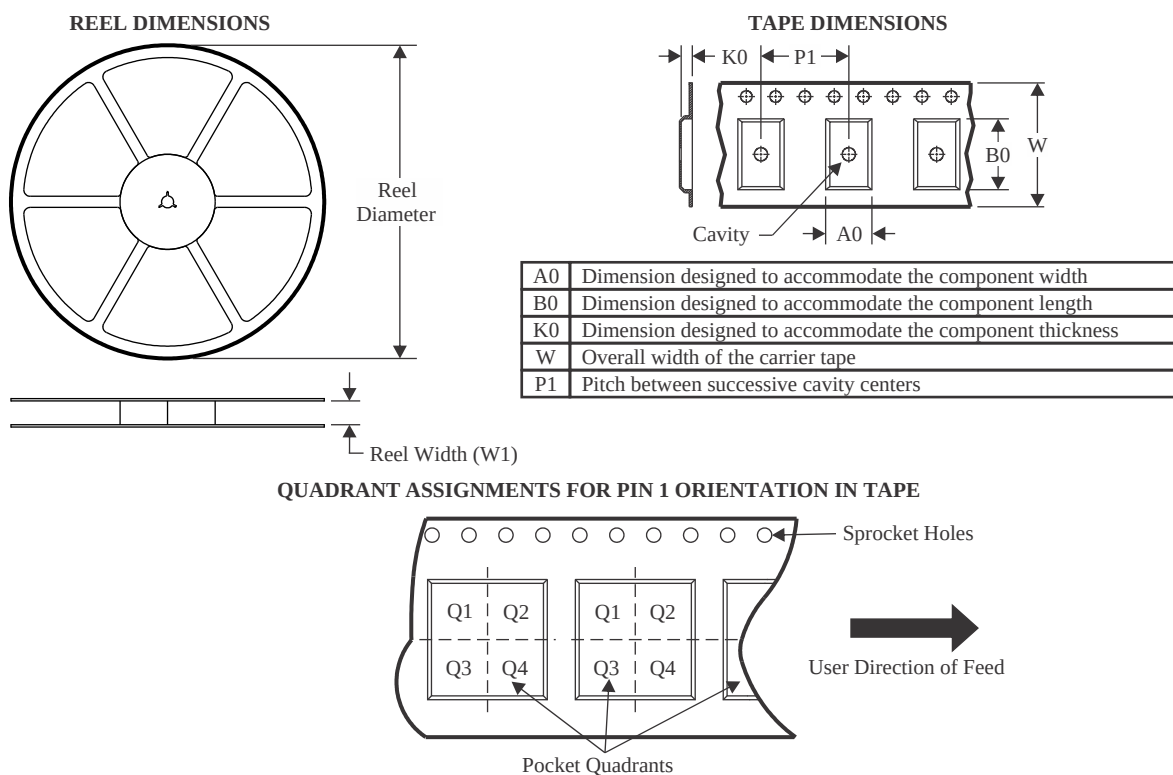
OTHER QUALIFIED VERSIONS OF SN54LS136, SN74LS136 :

- Catalog : [SN74LS136](#)
- Military : [SN54LS136](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

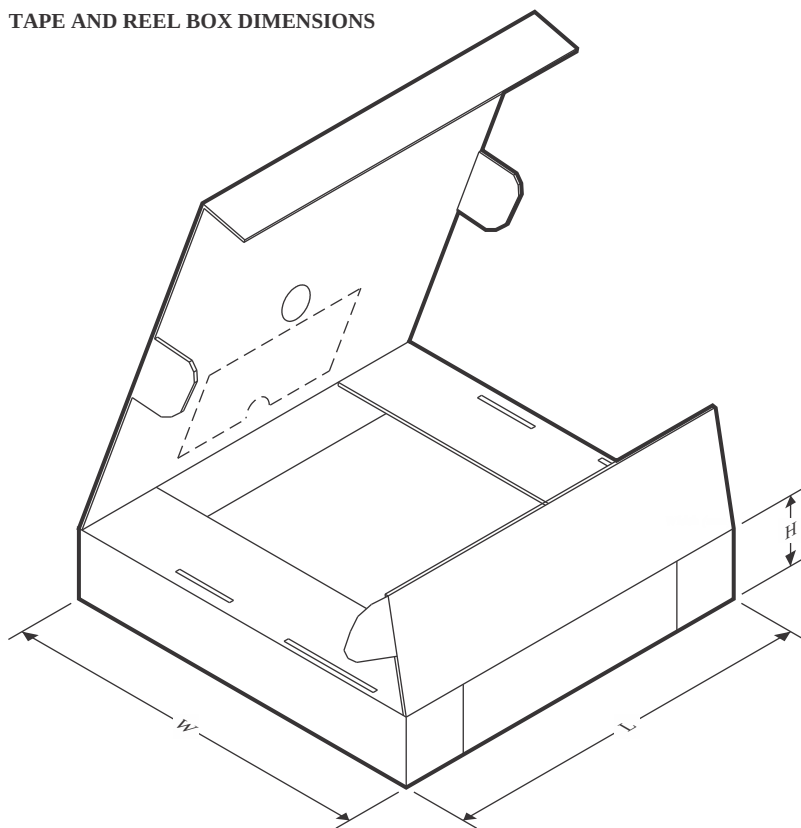
TAPE AND REEL INFORMATION



*All dimensions are nominal

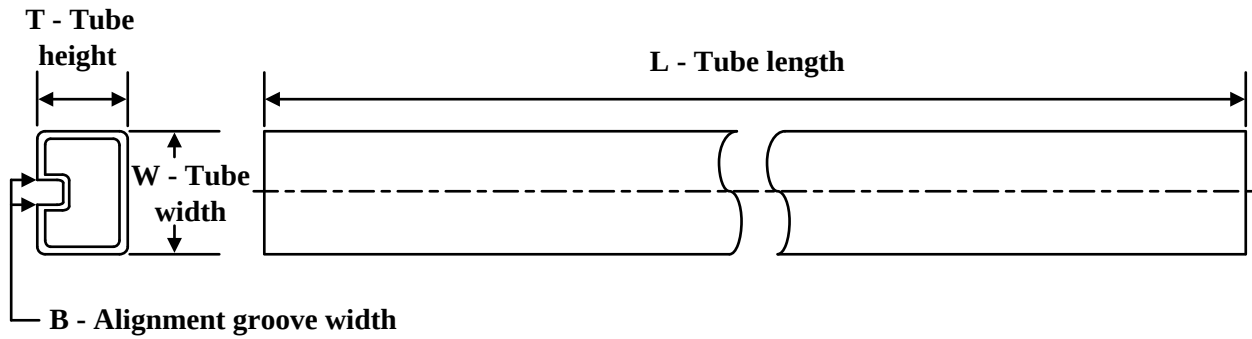
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS136DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS136NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



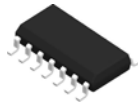
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS136DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LS136NSR	SOP	NS	14	2000	353.0	353.0	32.0

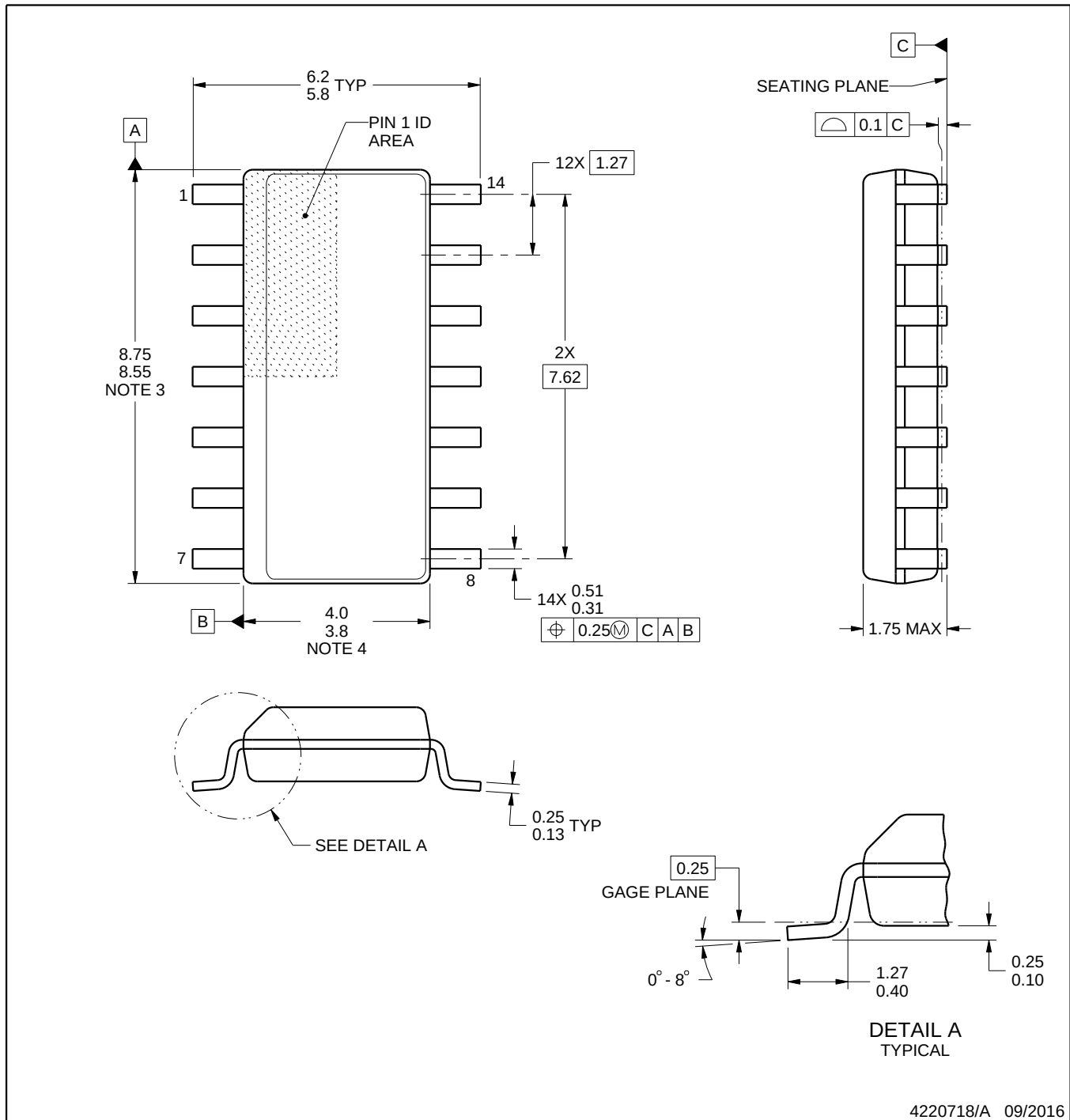
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LS136N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS136N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS136N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS136N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS136NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS136NE4	N	PDIP	14	25	506	13.97	11230	4.32

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

**NOTES:**

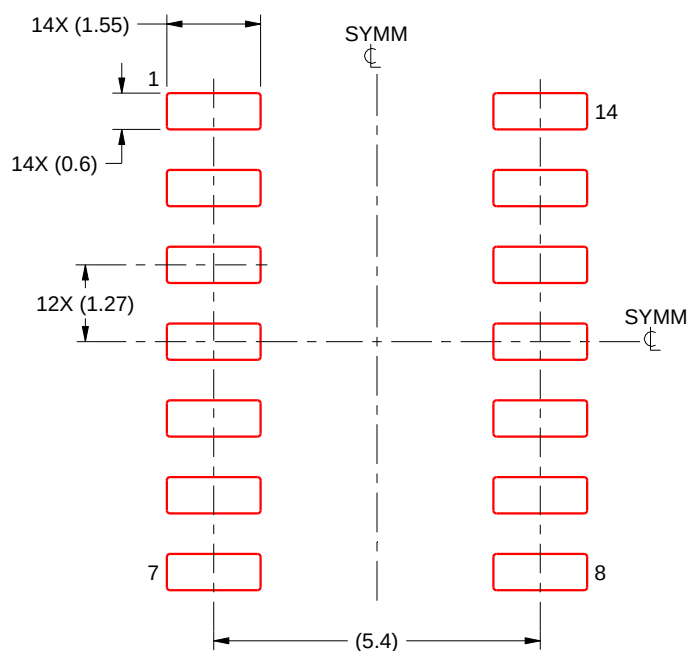
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

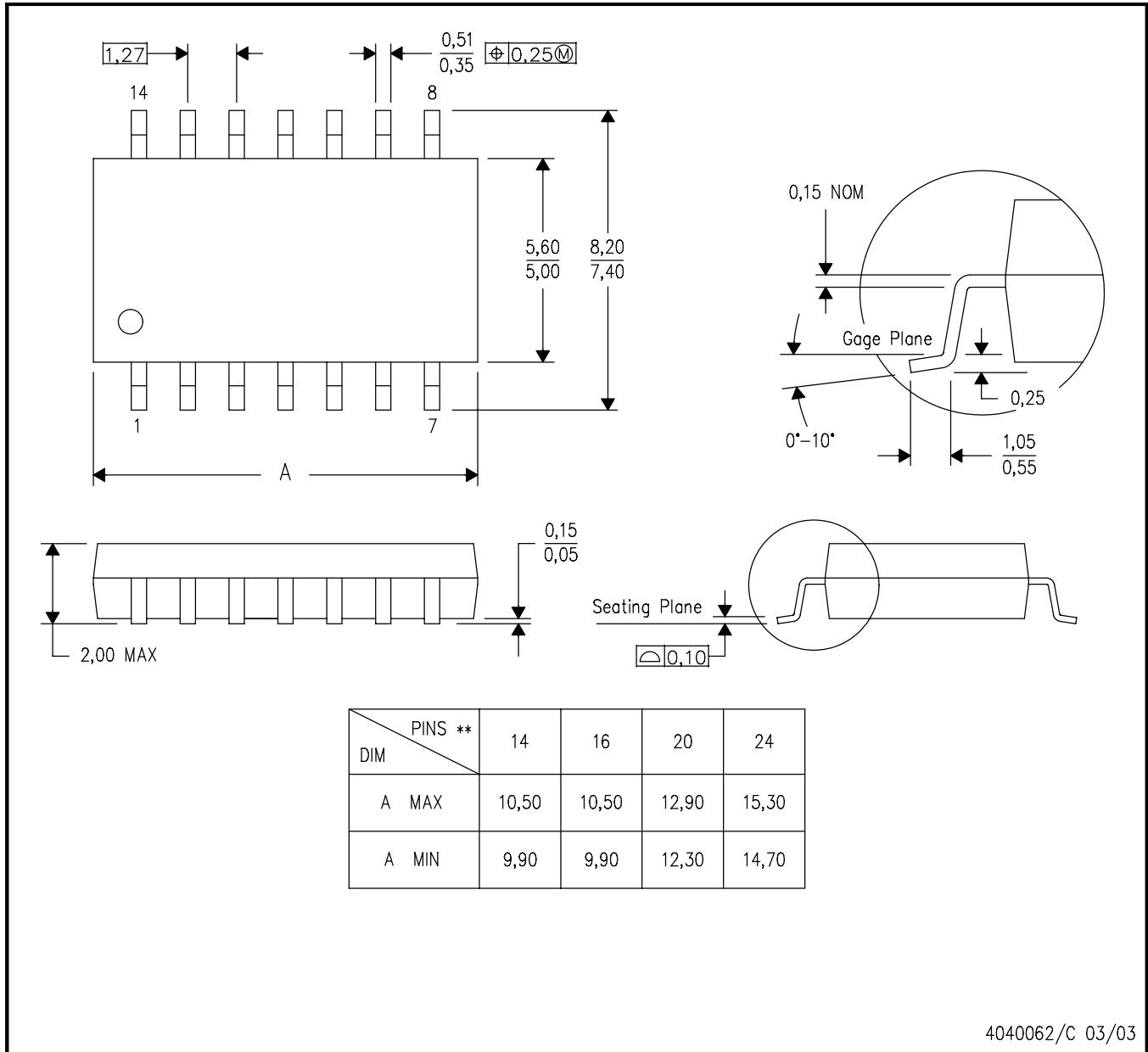
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



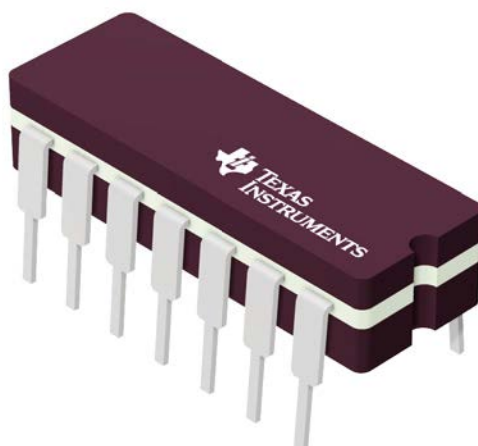
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J 14

GENERIC PACKAGE VIEW

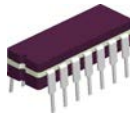
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

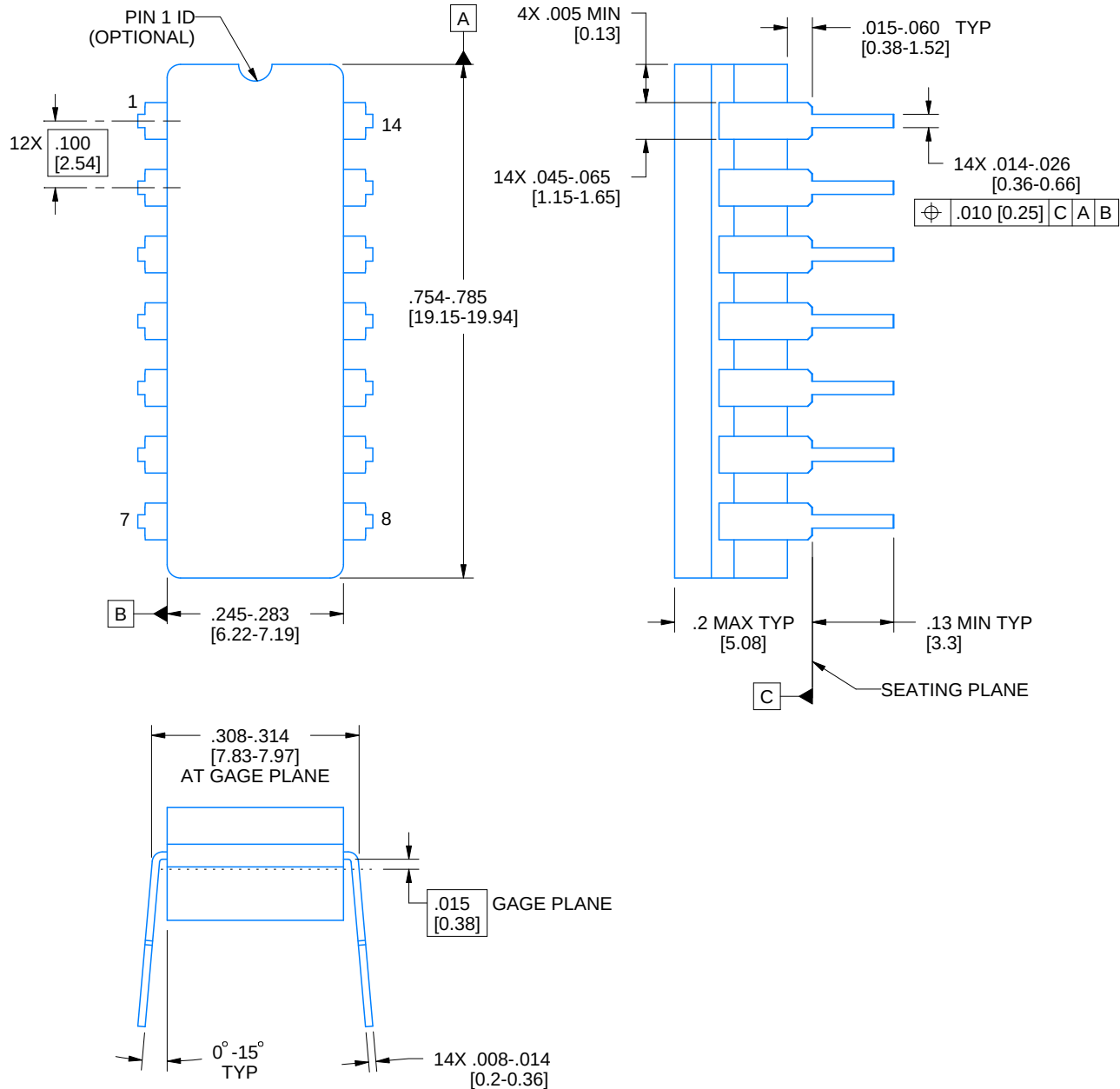


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A**PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



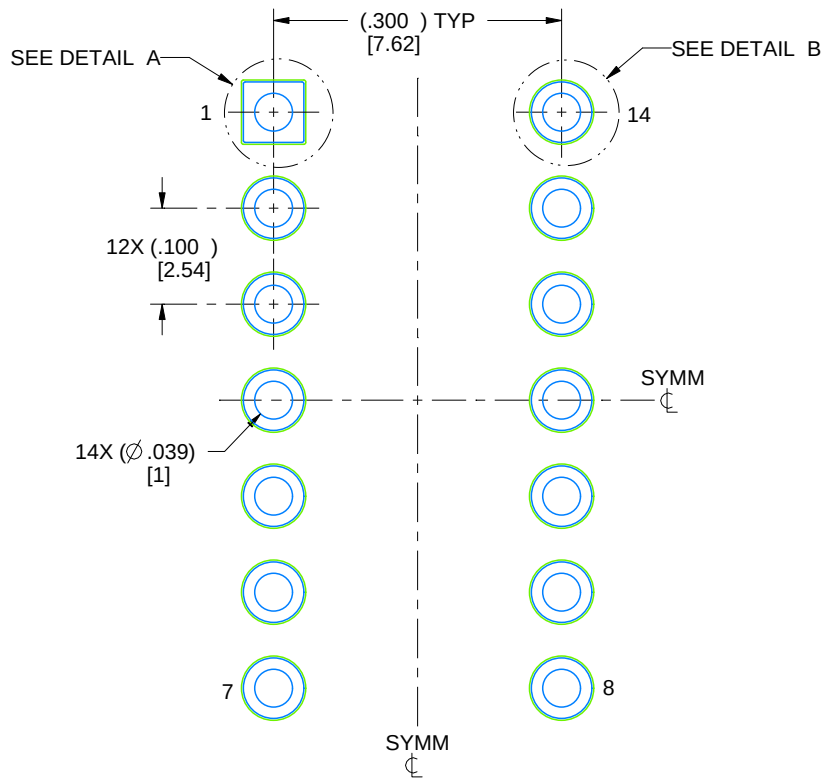
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EXAMPLE BOARD LAYOUT

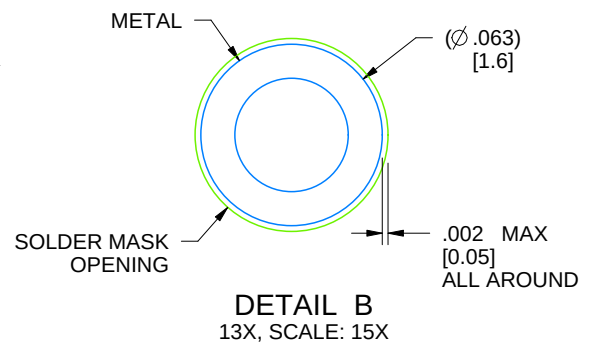
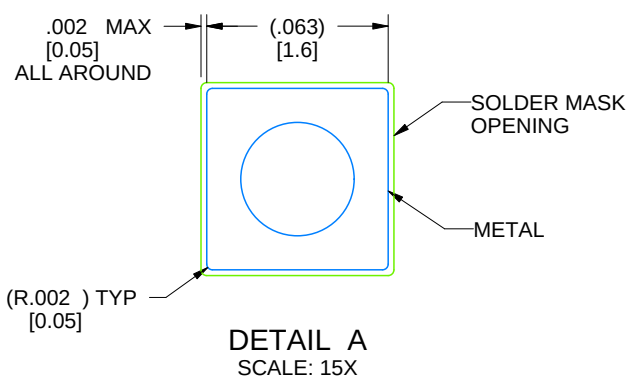
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

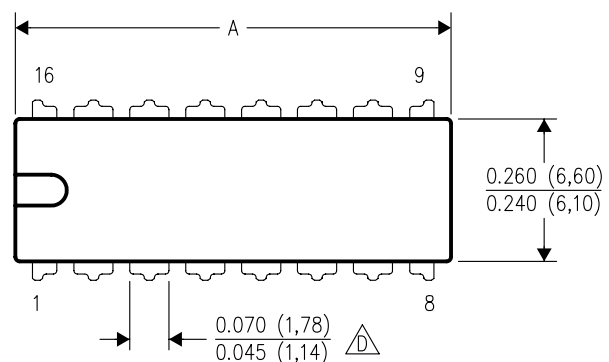


4214771/A 05/2017

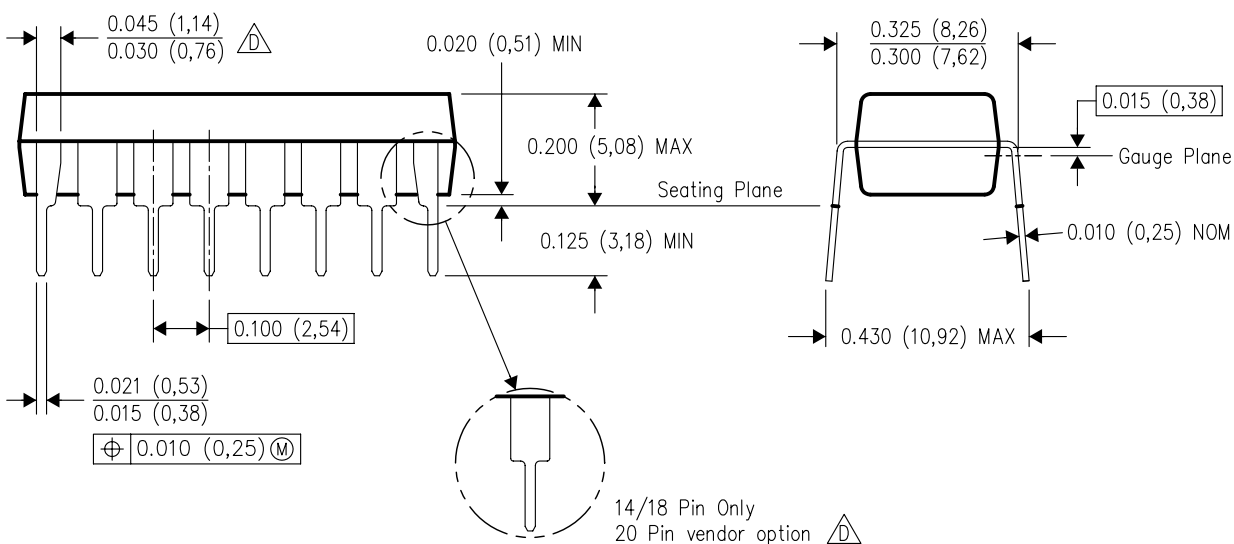
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

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