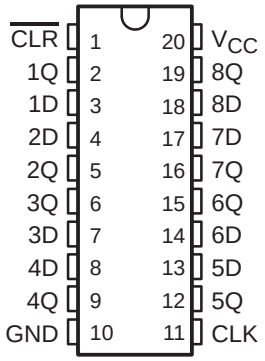
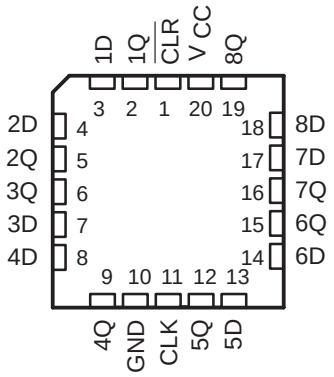
SDLS090 – OCTOBER 1976 – REVISED MARCH 1988

- **Contains Eight Flip-Flops With Single-Rail Outputs**
- **Buffered Clock and Direct Clear Inputs**
- **Individual Data Input to Each Flip-Flop**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**

**SN54273, SN74LS273 . . . J OR W PACKAGE**
**SN74273 . . . N PACKAGE**
**SN74LS273 . . . DW OR N PACKAGE**
**(TOP VIEW)**




**SN54LS273 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

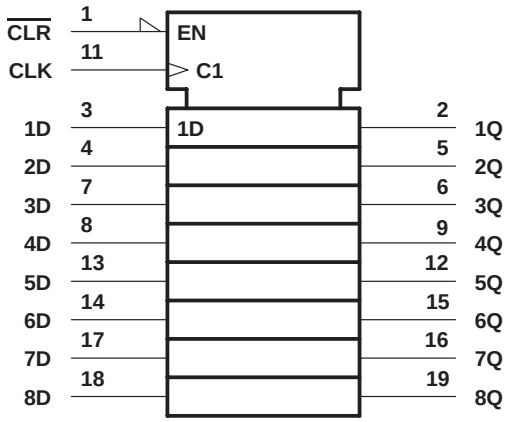
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect ar the output.

These flip-flops are guaranteed to respond to clock frequencies ranging form 0 to 30 megahertz while maximum clock frequency is typically 40 megahertz. Typical power dissipation is 39 milliwatts per flip-flop for the ′273 and 10 milliwatts for the ′LS273.

**FUNCTION TABLE**
**(each flip-flop)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| CLEAR | CLOCK | D | Q |
| L | X | X | L |
| H | ↑ | H | H |
| H | ↑ | L | L |
| H | L | X | $Q_0$ |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, J, N, and W packages.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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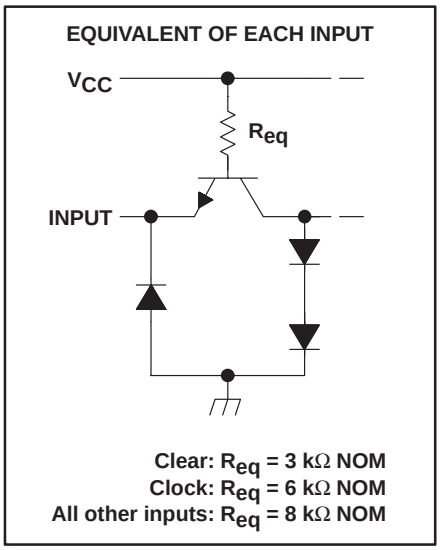
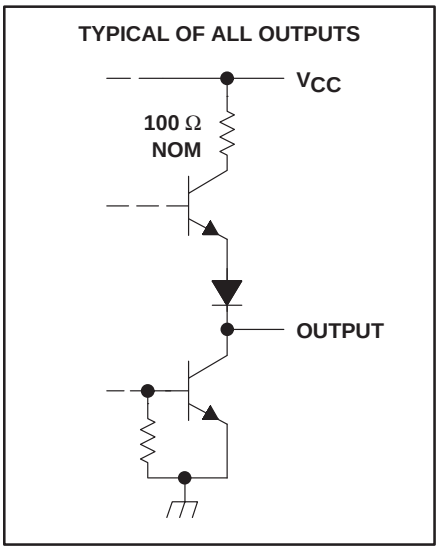
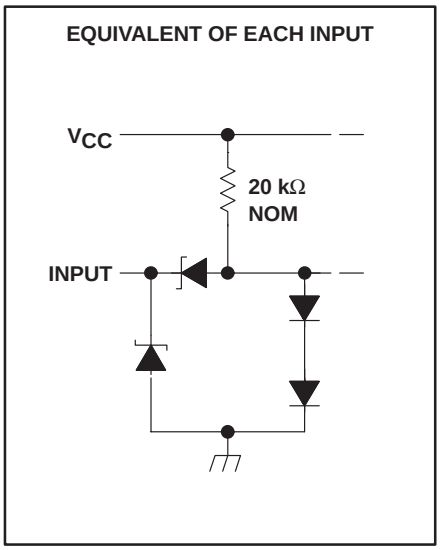
## schematics of inputs and outputs

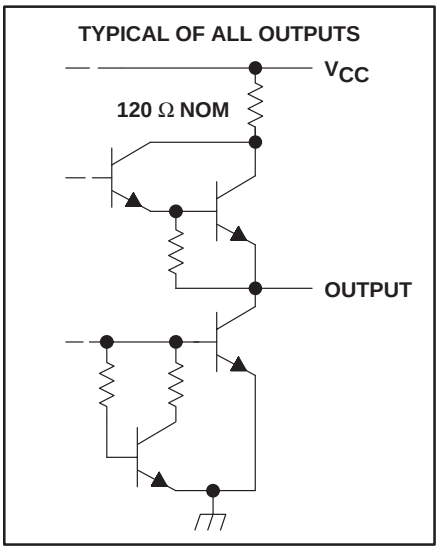
′273



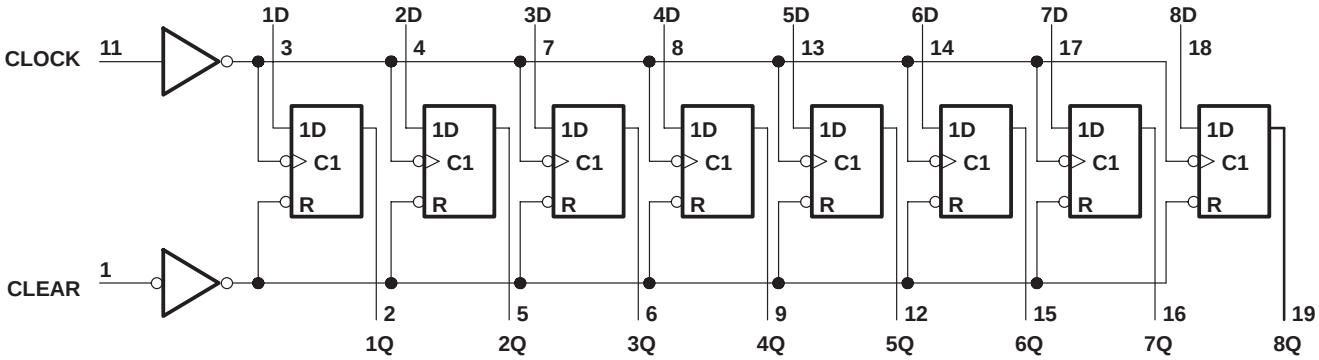




′LS273




## logic diagram (positive logic)




Pin numbers shown are for the DW, J, N, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range, $T_A$: SN54273 . . . . . –55°C to 125°C
SN74273 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

| | | SN54273 | | | SN74273 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | | –800 | | | –800 | µA |
| Low-level output current, $I_{OL}$ | | | | 16 | | | 16 | mA |
| Clock frequency, $f_{clock}$ | | 0 | | 30 | 0 | | 30 | MHz |
| Width of clock or clear pulse, $t_w$ | | 16.5 | | | 16.5 | | | ns |
| Setup time, $t_{su}$ | Data input | 20↑ | | | 20↑ | | | ns |
| | Clear inactive state | 25↑ | | | 25↑ | | | |
| Data hold time, $t_h$ | | 5↑ | | | 5↑ | | | ns |
| Operating free-air temperature, $T_A$ | | –55 | | 125 | 0 | | 70 | °C |

↑ The arrow indicates that the rising edge of the clock pulse is used for reference.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS† | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, | $I_I$ = –12 mA | | | –1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, | $V_{IH}$ = 2 V, $I_{OH}$ = –800 µA | 2.4 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, | $V_{IH}$ = 2 V, $I_{OH}$ = 16 mA | | | 0.4 | V |
| $I_I$ | Input current at maximum input voltage | | $V_{CC}$ = MAX, | $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High-level input current | Clear | $V_{CC}$ = MAX, | $V_I$ = 2.4 V | | | 80 | µA |
| | | Clock or D | | | | | 40 | |
| $I_{IL}$ | Low-level input current | Clear | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | –3.2 | mA |
| | | Clock or D | | | | | –1.6 | |
| $I_{OS}$ | Short-circuit output current§ | | $V_{CC}$ = MAX | | –18 | | –57 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX, | See Note 2 | | 62 | 94 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, $I_{CC}$ is measured after a momentary ground, then 4.5 V, is applied to clock.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | $C_L$ = 15 pF, $R_L$ = 400 Ω, See Note 3 | 30 | 40 | | MHz |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output from clear | | | 18 | 27 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output from clock | | | 17 | 27 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output from clock | | | 18 | 27 | ns |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range, $T_A$: SN54LS273 . . . . . –55°C to 125°C
SN74LS273 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

| | | SN54LS273 | | | SN74LS273 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | | –400 | | | –400 | μA |
| Low-level output current, $I_{OL}$ | | | | 4 | | | 8 | mA |
| Clock frequency, $f_{clock}$ | | 0 | | 30 | 0 | | 30 | MHz |
| Width of clock or clear pulse, $t_w$ | | 20 | | | 20 | | | ns |
| Setup time, $t_{su}$ | Data input | 20↑ | | | 20↑ | | | ns |
| | Clear inactive state | 25↑ | | | 25↑ | | | |
| Data hold time, $t_h$ | | 5↑ | | | 5↑ | | | ns |
| Operating free-air temperature, $T_A$ | | –55 | | 125 | 0 | | 70 | °C |

↑ The arrow indicates that the rising edge of the clock pulse is used for reference.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | | SN54LS273 | | | SN74LS273 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | 0.7 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, | $I_I$ = –18 mA | | | | –1.5 | | | –1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = $V_{IL}$max, | $V_{IH}$ = 2 V, $I_{OH}$ = –400 µA | | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = $V_{IL}$max, | $V_{IH}$ = 2 V, | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, | $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | | 20 | | | 20 | µA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | | –0.4 | | | –0.4 | mA |
| $I_{OS}$ | Short-circuit output current§ | $V_{CC}$ = MAX | | | –20 | | –100 | –20 | | –100 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, | See Note 2 | | | 17 | 27 | | 17 | 27 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time and duration of short circuit should not exceed one second.
NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, $I_{CC}$ is measured after a momentary ground, then 4.5 V, is applied to clock.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | $C_L$ = 15 pF, $R_L$ = 2 kΩ, See Note 3 | 30 | 40 | | MHz |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output from clear | | | 18 | 27 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output from clock | | | 17 | 27 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output from clock | | | 18 | 27 | ns |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-7801001VRA | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-7801001VR A SNV54LS273J |
| 5962-7801001VRA.A | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-7801001VR A SNV54LS273J |
| 78010012A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 78010012A SNJ54LS 273FK |
| 7801001RA | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 7801001RA SNJ54LS273J |
| 7801001SA | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 7801001SA SNJ54LS273W |
| JM38510/32501B2A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 32501B2A |
| JM38510/32501B2A.A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 32501B2A |
| JM38510/32501BRA | Last Time Buy | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 32501BRA |
| JM38510/32501BRA.A | Last Time Buy | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 32501BRA |
| JM38510/32501BSA | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 32501BSA |
| JM38510/32501BSA.A | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 32501BSA |
| M38510/32501B2A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 32501B2A |
| M38510/32501BRA | Last Time Buy | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 32501BRA |
| M38510/32501BSA | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 32501BSA |
| SN54LS273J | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54LS273J |
| SN54LS273J.A | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54LS273J |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LS273DW | Obsolete | Production | SOIC (DW) \| 20 | - | - | Call TI | Call TI | 0 to 70 | LS273 |
| SN74LS273DWR | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS273 |
| SN74LS273DWR.A | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS273 |
| SN74LS273N | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS273N |
| SN74LS273N.A | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS273N |
| SN74LS273NE4 | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS273N |
| SN74LS273NSR | Active | Production | SOP (NS) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS273 |
| SN74LS273NSR.A | Active | Production | SOP (NS) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS273 |
| SNJ54LS273FK | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 78010012A SNJ54LS 273FK |
| SNJ54LS273FK.A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 78010012A SNJ54LS 273FK |
| SNJ54LS273J | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 7801001RA SNJ54LS273J |
| SNJ54LS273J.A | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 7801001RA SNJ54LS273J |
| SNJ54LS273W | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 7801001SA SNJ54LS273W |
| SNJ54LS273W.A | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 7801001SA SNJ54LS273W |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS273, SN54LS273-SP, SN74LS273 :**

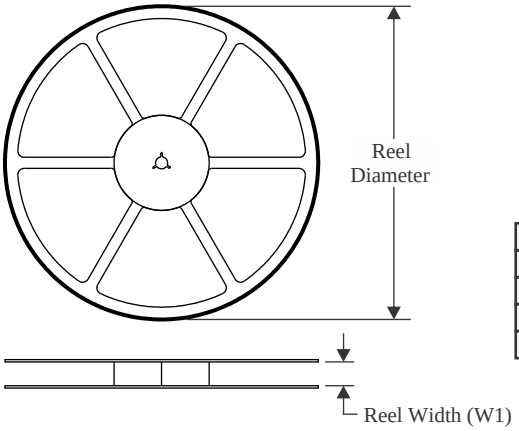
- Catalog : SN74LS273, SN54LS273
- Military : SN54LS273
- Space : SN54LS273-SP

NOTE: Qualified Version Definitions:

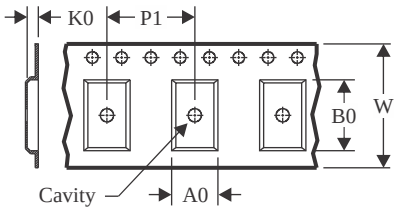
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

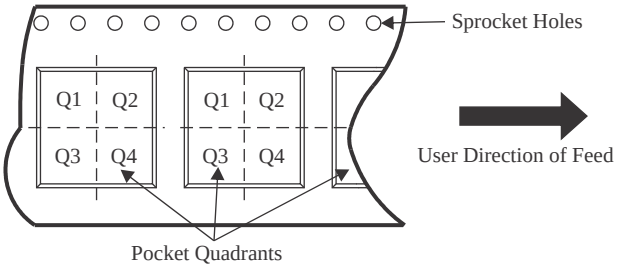



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

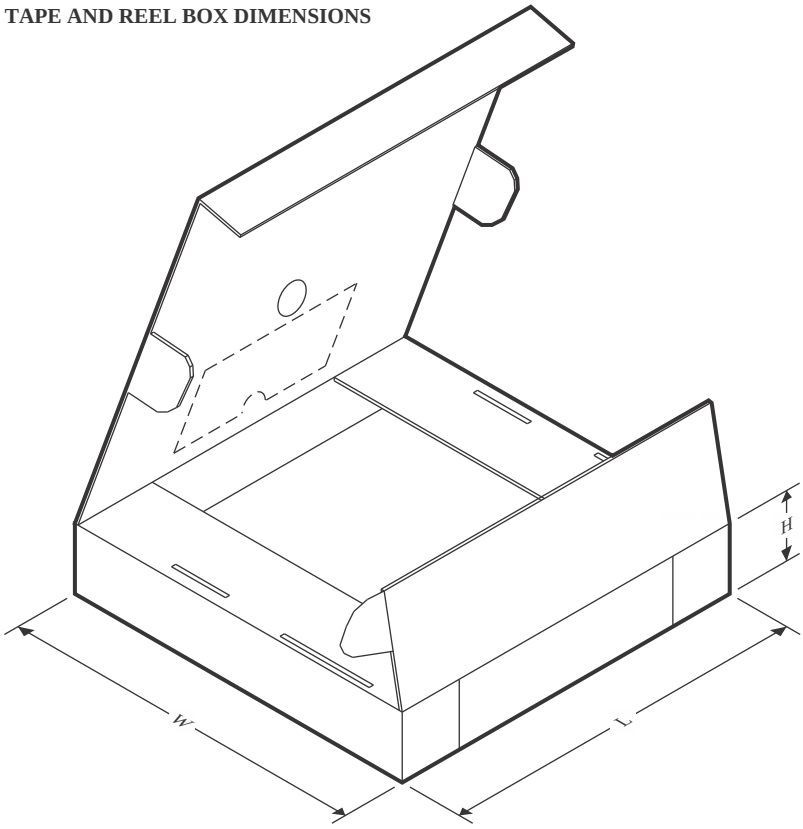
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS273DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LS273DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LS273NSR | SOP | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |

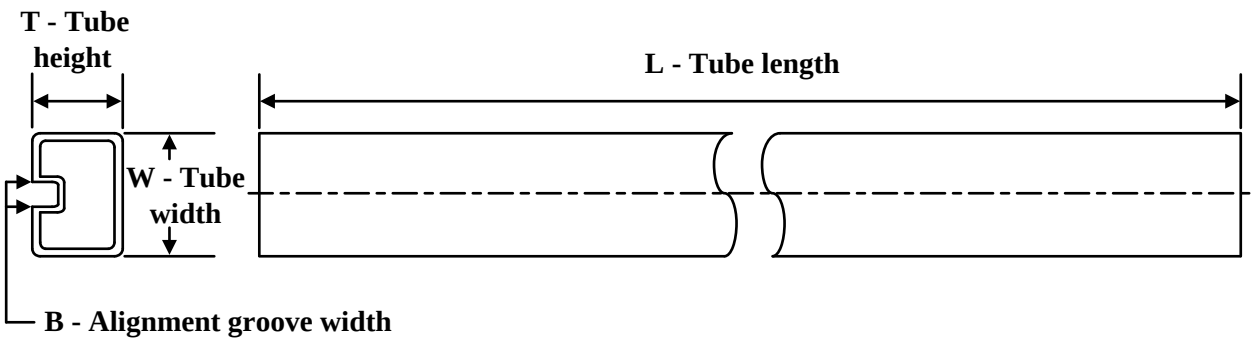
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LS273DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LS273DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74LS273NSR | SOP | NS | 20 | 2000 | 356.0 | 356.0 | 45.0 |

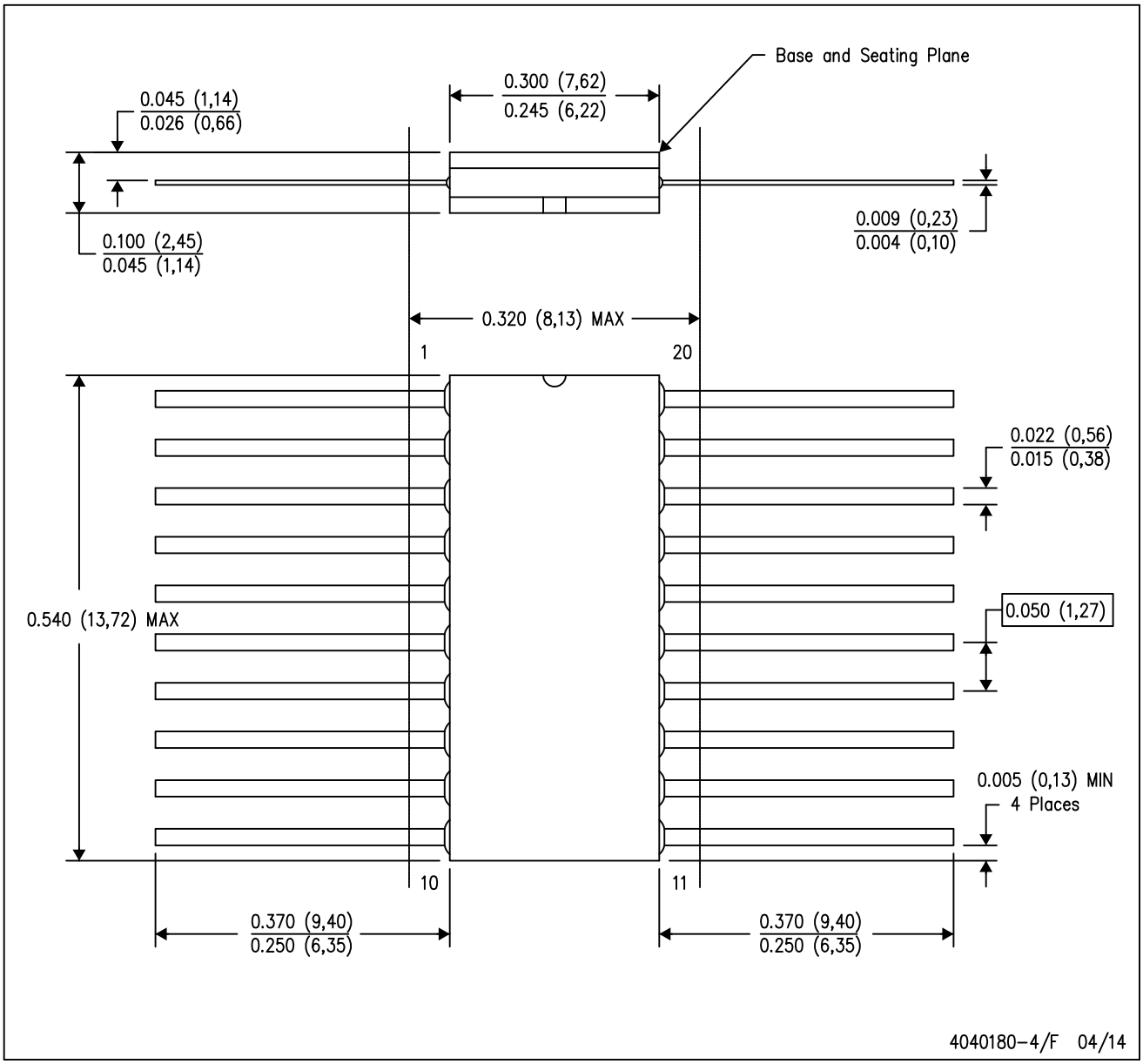
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 78010012A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 7801001SA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| JM38510/32501B2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| JM38510/32501B2A.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| JM38510/32501BSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| JM38510/32501BSA.A | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| M38510/32501B2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| M38510/32501BSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74LS273N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS273N.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS273NE4 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54LS273FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54LS273FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54LS273W | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54LS273W.A | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |

W (R–GDFP–F20) CERAMIC DUAL FLATPACK

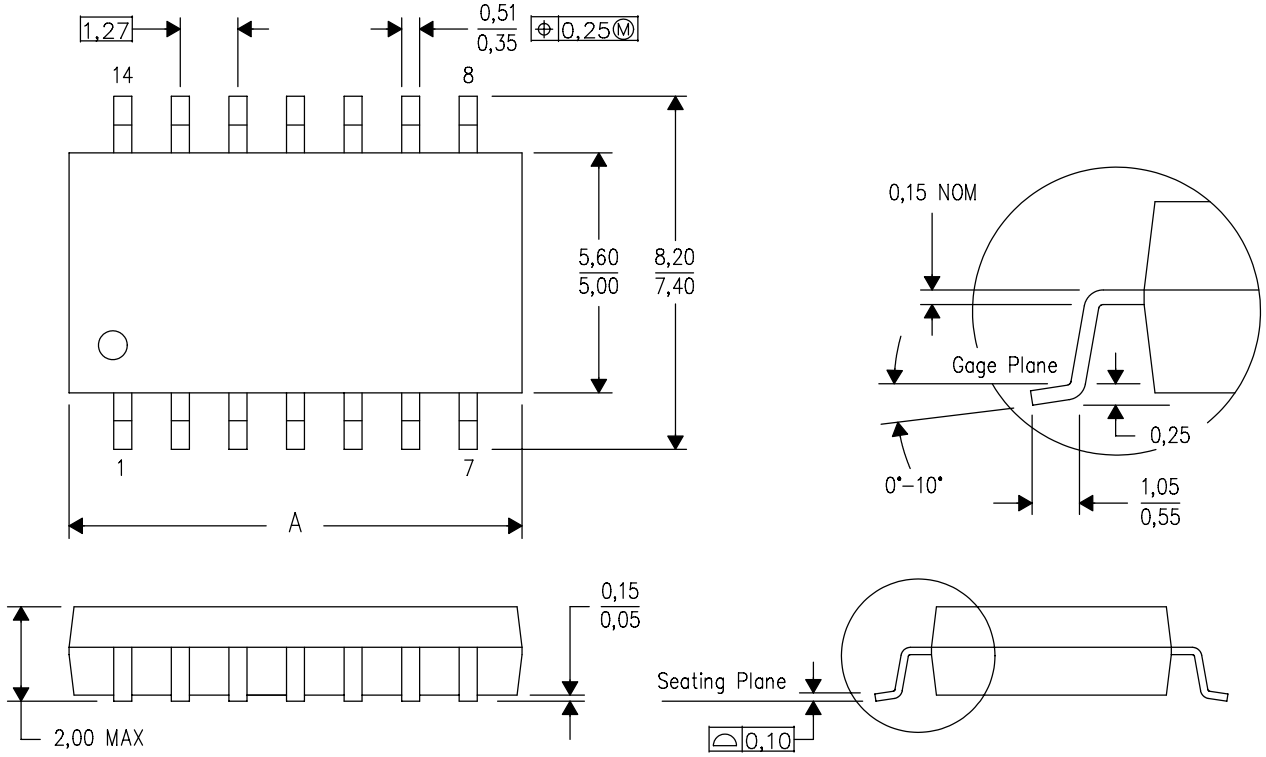



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



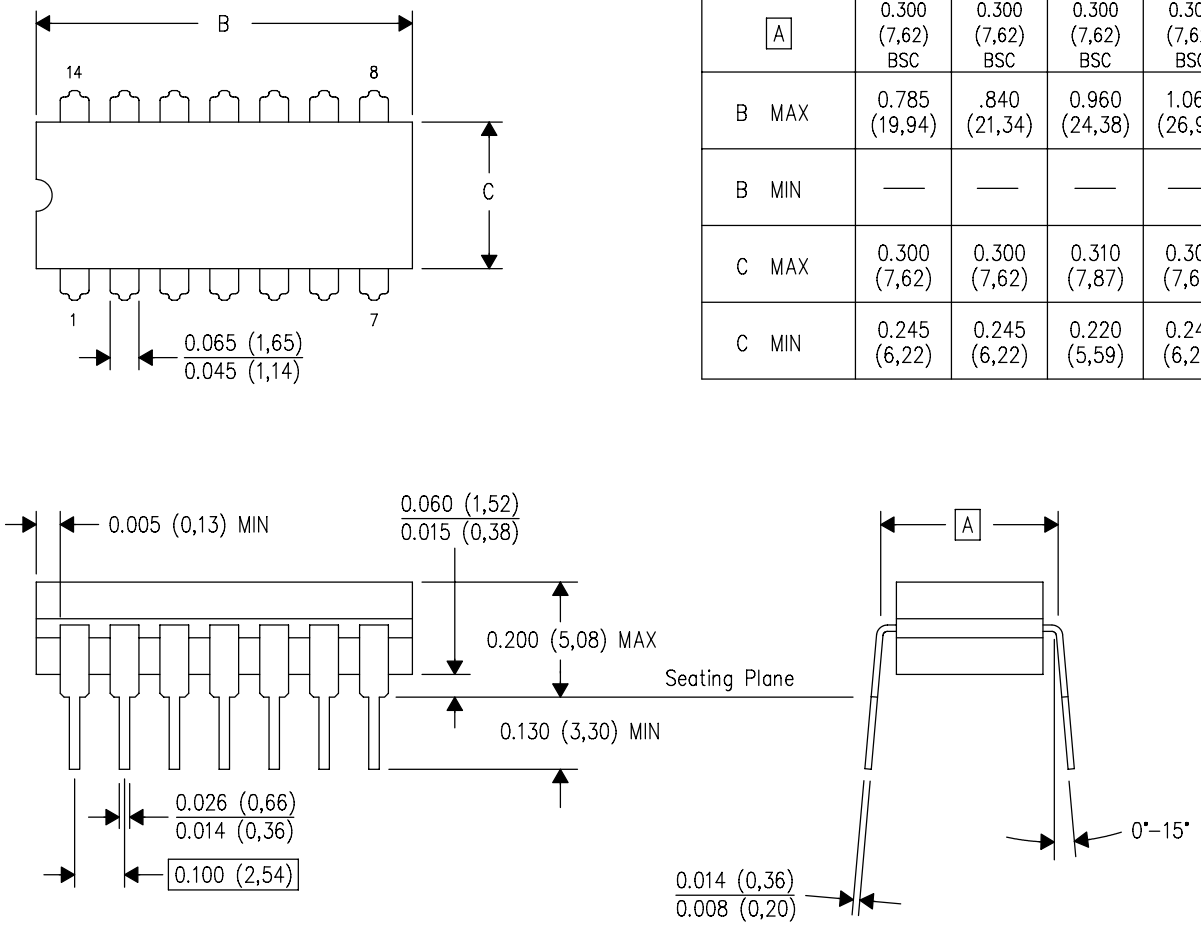

| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

# GENERIC PACKAGE VIEW

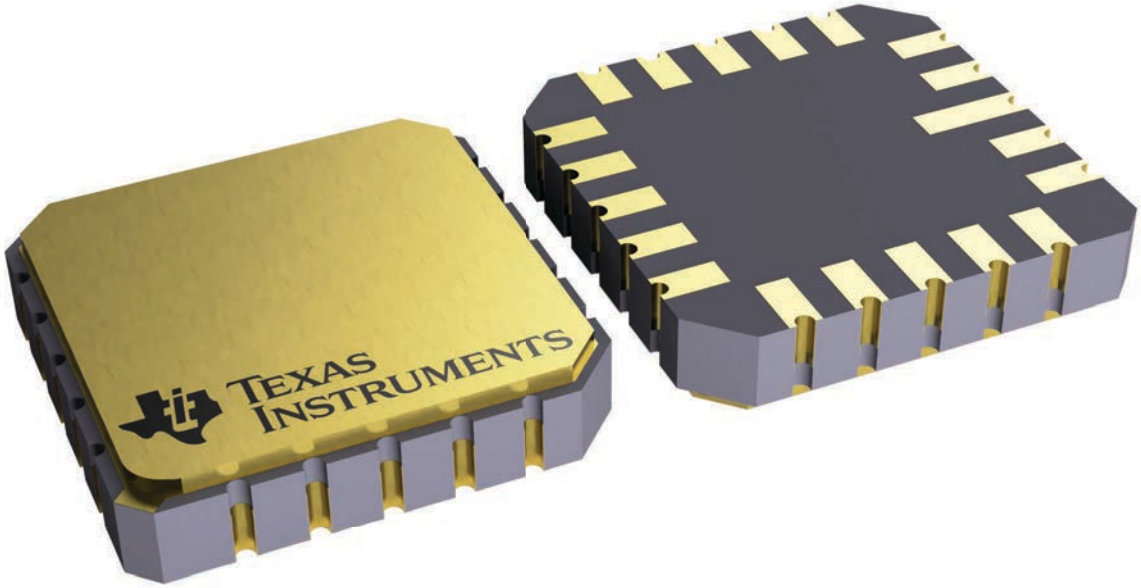
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

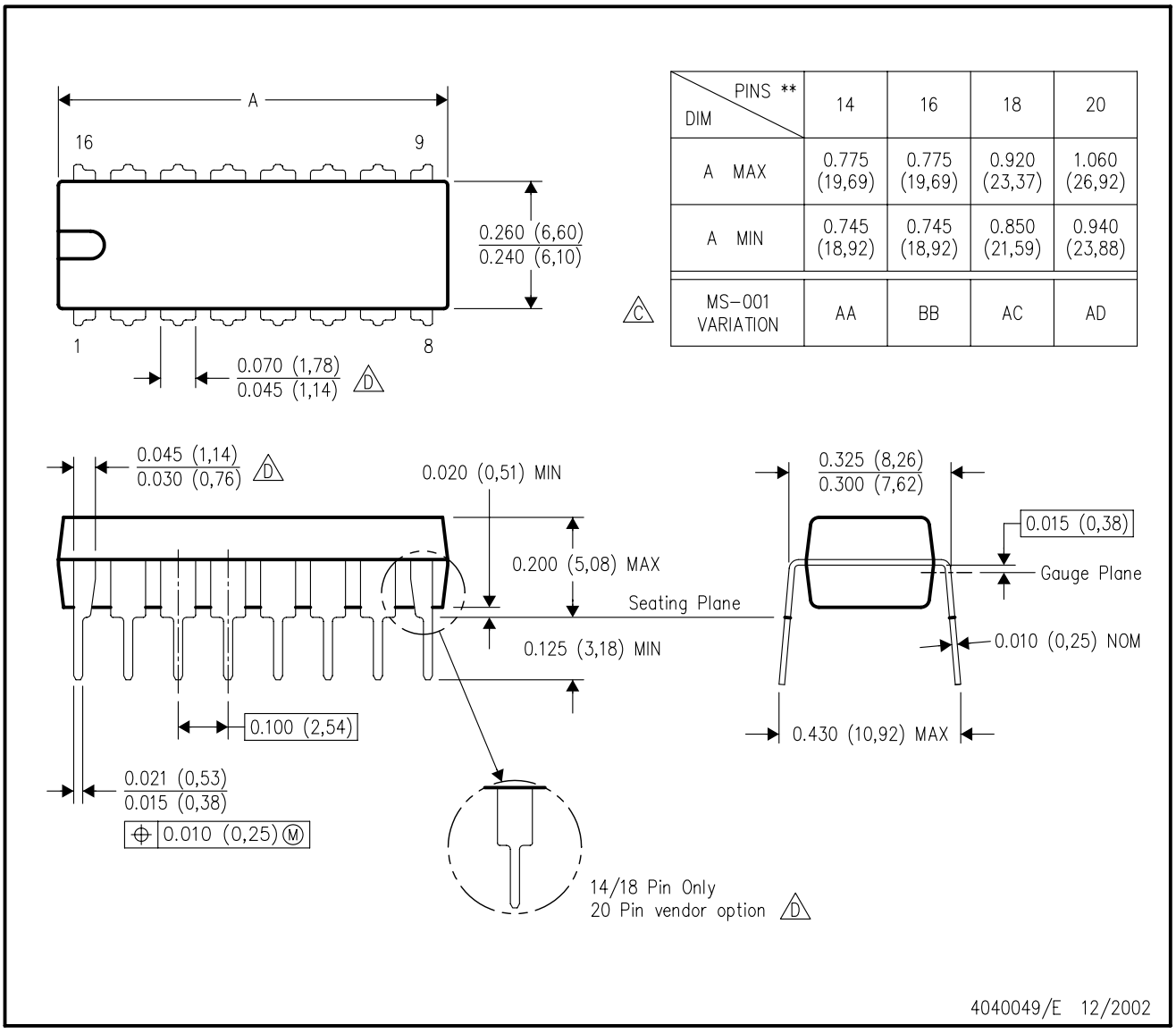
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4229370VA\

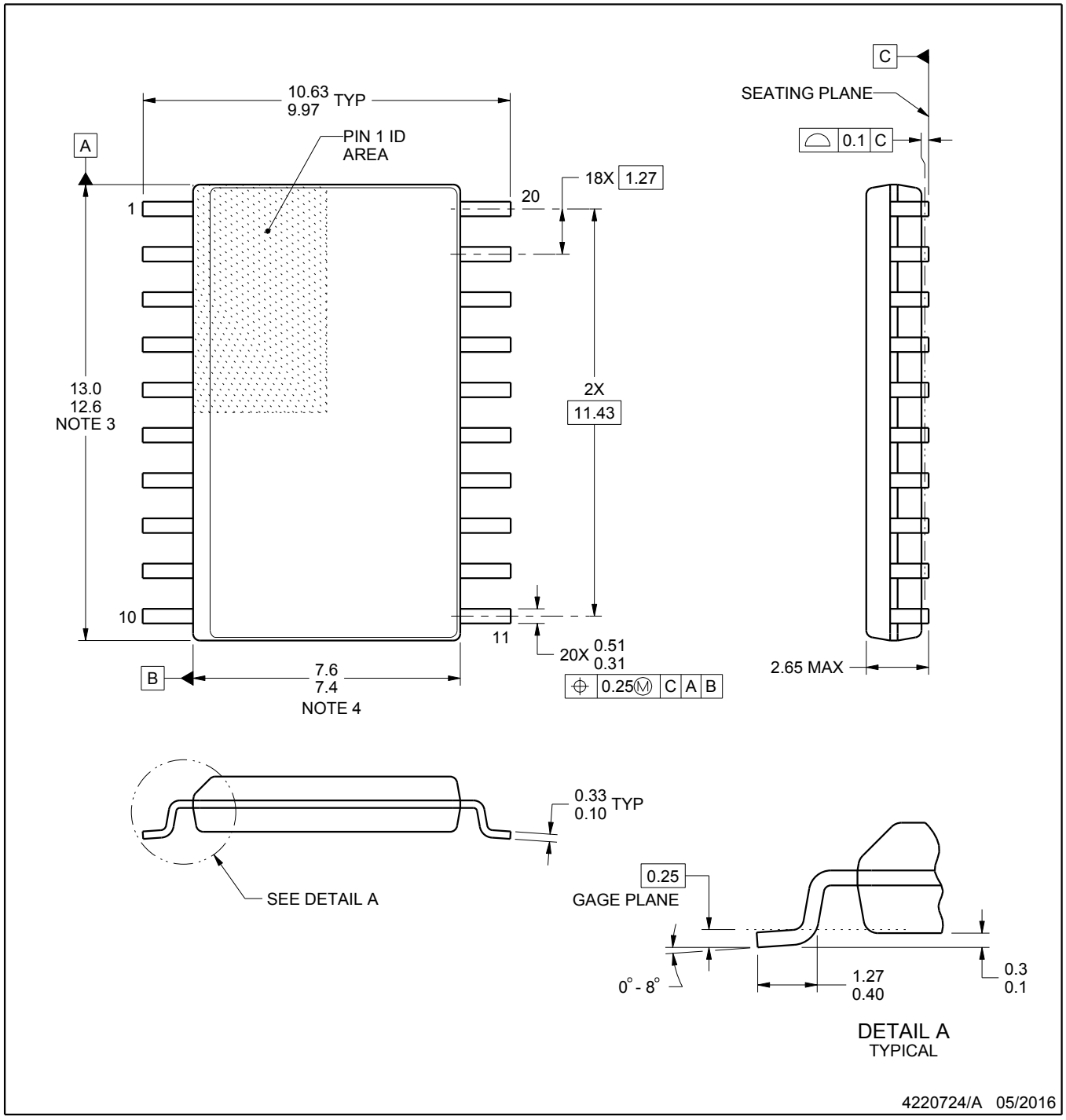
## N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



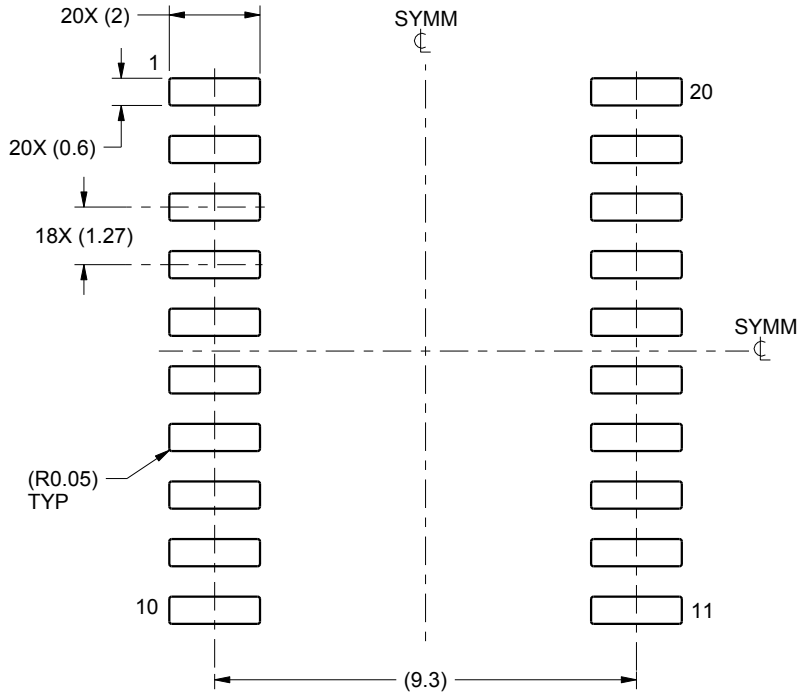

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

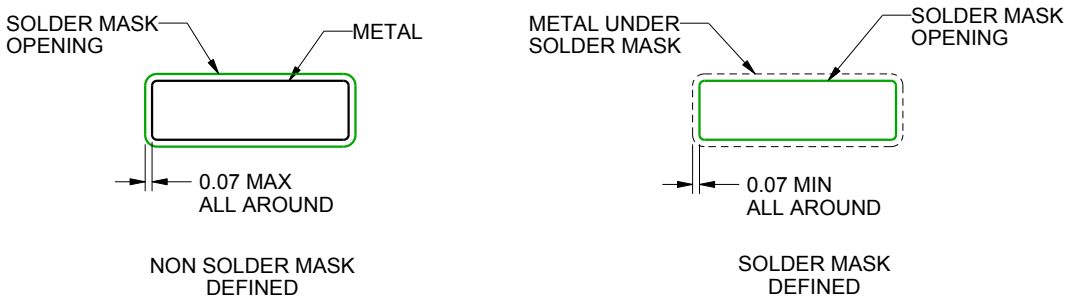



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

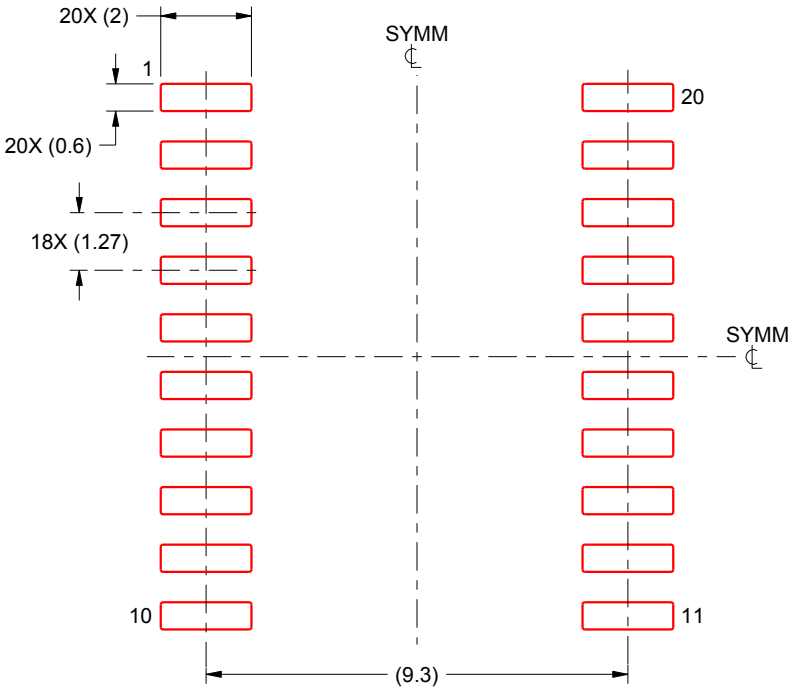



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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