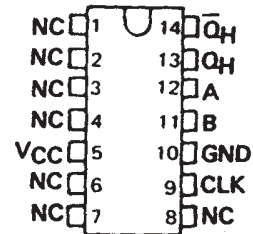


SN5491A, SN54LS91, SN7491A, SN74LS91 8-BIT SHIFT REGISTERS

SDLS126 – MARCH 1974 – REVISED MARCH 1988

- For applications in:
Digital Computer Systems
Data-Handling Systems
Control Systems

SN5491A, SN54LS91 . . . J PACKAGE
SN7491A . . . N PACKAGE
SN74LS91 . . . D OR N PACKAGE
(TOP VIEW)

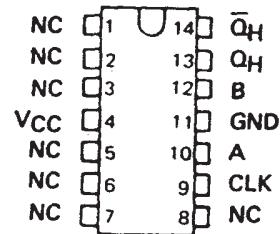


TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'91A	18 MHz	175 mW
'LS91	18 MHz	60 mW

description

These monolithic serial-in, serial-out, 8-bit shift registers utilize transistor-transistor logic (TTL) circuits and are composed of eight R-S master-slave flip-flops, input gating, and a clock driver. Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. This clock pulse inverter/driver causes these circuits to shift information one bit on the positive edge of an input clock pulse.

SN5491A, SN54LS91 . . . W PACKAGE
(TOP VIEW)



NC – No internal connection

schematics of inputs and outputs

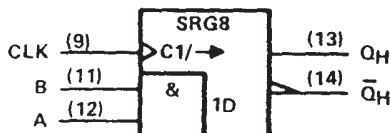
FUNCTION TABLE

INPUTS AT t_n		OUTPUTS AT $t_n + 8$	
A	B	Q_H	$\bar{Q}_H$
H	H	H	L
L	X	L	H
X	L	L	H

t_n = Reference bit time,
clock low

$t_n + 8$ = Bit time after 8
low-to-high
clock transitions.

logic symbol†



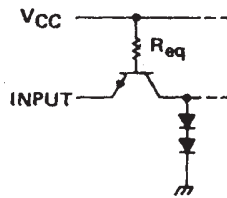
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'91A

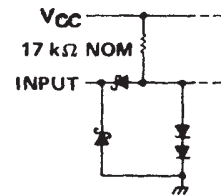
'LS91

EQUIVALENT OF EACH INPUT

EQUIVALENT OF EACH INPUT



'91A: $R_{eq} = 4 \text{ k}\Omega \text{ NOM}$

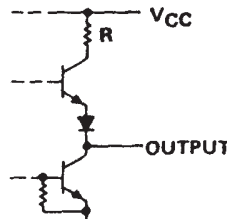


'91A

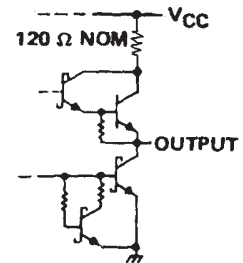
'LS91

TYPICAL OF BOTH OUTPUTS

TYPICAL OF BOTH OUTPUTS



'91A: $R = 130 \Omega \text{ NOM}$



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Pin numbers shown in () are for the D, J or N packages and pin numbers shown in [] are for the W package.

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN5491A	−55°C to 125°C
SN7491A	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. Input signals must be zero or positive with respect to network ground terminal.

	SN5491A			SN7491A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			16			16	mA
Width of clock input pulse, t_W	25			25			ns
Setup time, t_{SU} (see Figure 1)	25			25			ns
Hold time, t_H (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}C$

PARAMETER	TEST CONDITIONS†	SN5491A			SN7491A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage		0.8			0.8			V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -400 μA	2.4	3.5		2.4	3.5		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH} High-level input current	V _{CC} = MAX, V _I = 2.4 V			40			40	μA
I _{IL} Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-1.6			-1.6	mA
I _{OS} Short-circuit output current‡	V _{CC} = MAX	-20		-57	-18		-57	mA
I _{CC} Supply current	V _{CC} = MAX, See Note 3		35	50		35	58	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured after the eighth clock pulse with the output open and A and B inputs grounded.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\max}$	Maximum clock frequency	$C_L = 15 \text{ pF}$,	10	18		MHz
t_{PLH}	Propagation delay time, low-to-high-level output	$R_L = 400 \Omega$,		24	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output	See Figure 1		27	40	ns

SN5491A, SN54LS91, SN7491A, SN74LS91 8-BIT SHIFT REGISTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS91	–55°C to 125°C
SN74LS91	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS91			SN74LS91			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			–400			–400	μ A
Low-level output current, I_{OL}			4			8	mA
Width of clock input pulse, t_W	25			25			ns
Setup time, t_{SU} (see Figure 1)	25			25			ns
Hold time, t_H (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS91			SN74LS91			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			–1.5			–1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = V_{IL \text{ max}}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	$I_{OL} = 4 \text{ mA}$	0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$			$I_{OL} = 8 \text{ mA}$	0.35	0.5	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			–0.4			–0.4	mA
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	–20		–100	–20		–100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 3	12		20	12		20	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 3: I_{CC} is measured after the eighth clock pulse with the output open and A and B inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

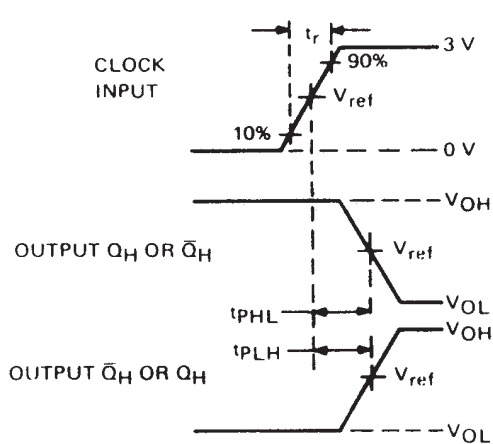
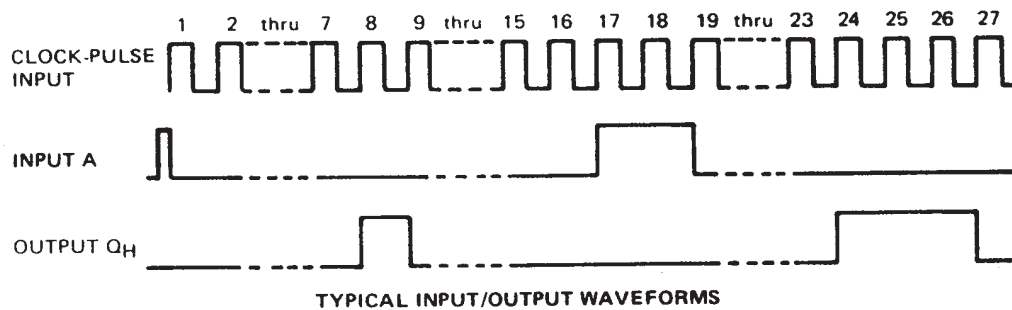
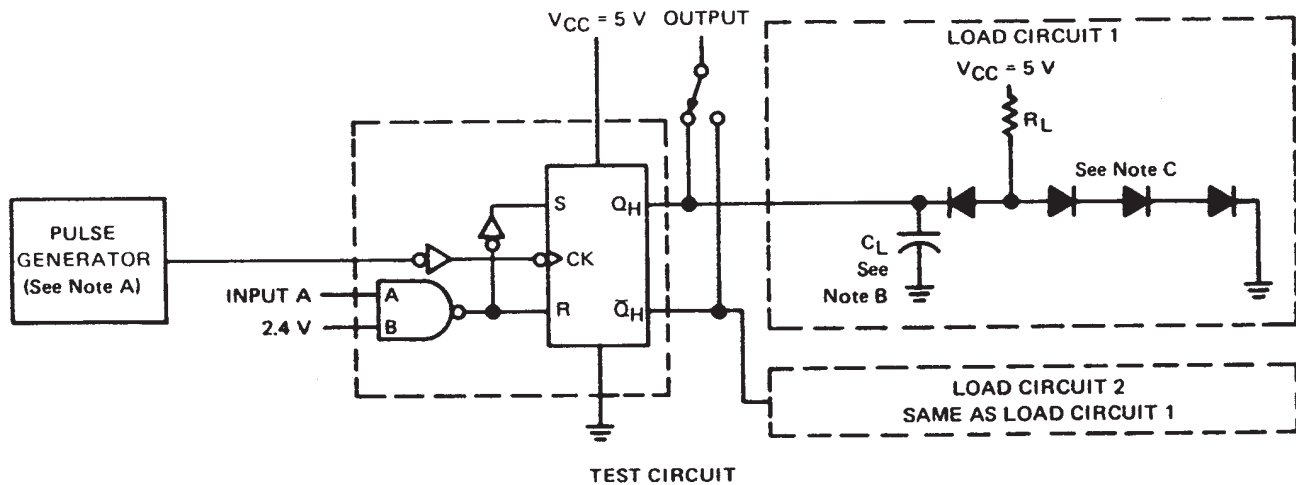
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF},$	10	18		MHz
t_{PLH} Propagation delay time, low-to-high-level output	$R_L = 2 \text{ k}\Omega,$		24	40	ns
t_{PHL} Propagation delay time, high-to-low-level output	See Figure 1		27	40	ns



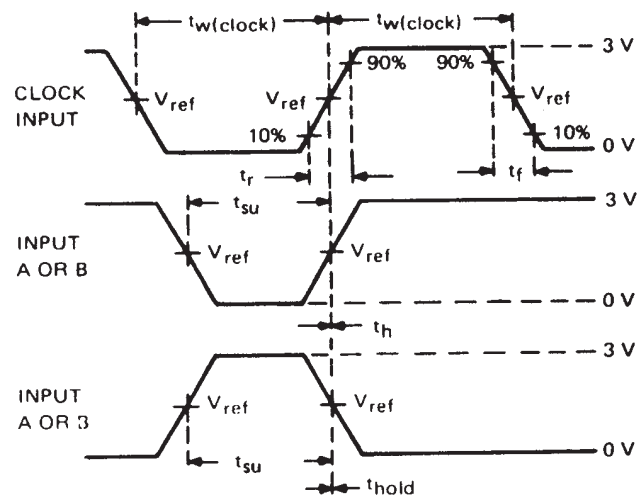
SN5491A, SN54LS91, SN7491A, SN74LS91 8-BIT SHIFT REGISTERS

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PARAMETER MEASUREMENT INFORMATION



PROPAGATION DELAY TIMES VOLTAGE WAVEFORMS



SWITCHING TIMES VOLTAGE WAVEFORMS

- NOTES: A. The generator has the following characteristics: $t_{w(\text{clock})} = 500 \text{ ns}$, $\text{PRR} \leq 1 \text{ MHz}$, $Z_{\text{out}} \approx 50 \Omega$. For SN5491A/SN7491A, $t_r \leq 10 \text{ ns}$ and $t_f \leq 10 \text{ ns}$; for SN54LS91, $t_r = 15 \text{ ns}$, and $t_f = 6 \text{ ns}$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. For SN5491A/SN7491A, $V_{\text{ref}} = 1.5 \text{ V}$; for SN54LS91/SN74LS91, $V_{\text{ref}} = 1.3 \text{ V}$.

FIGURE 1—SWITCHING TIMES

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN54LS91J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS91J
SN54LS91J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS91J

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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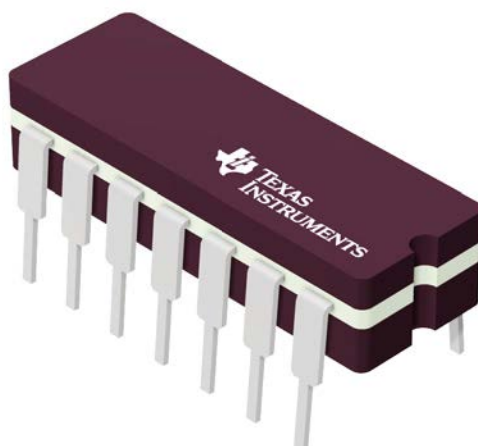
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J 14

GENERIC PACKAGE VIEW

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

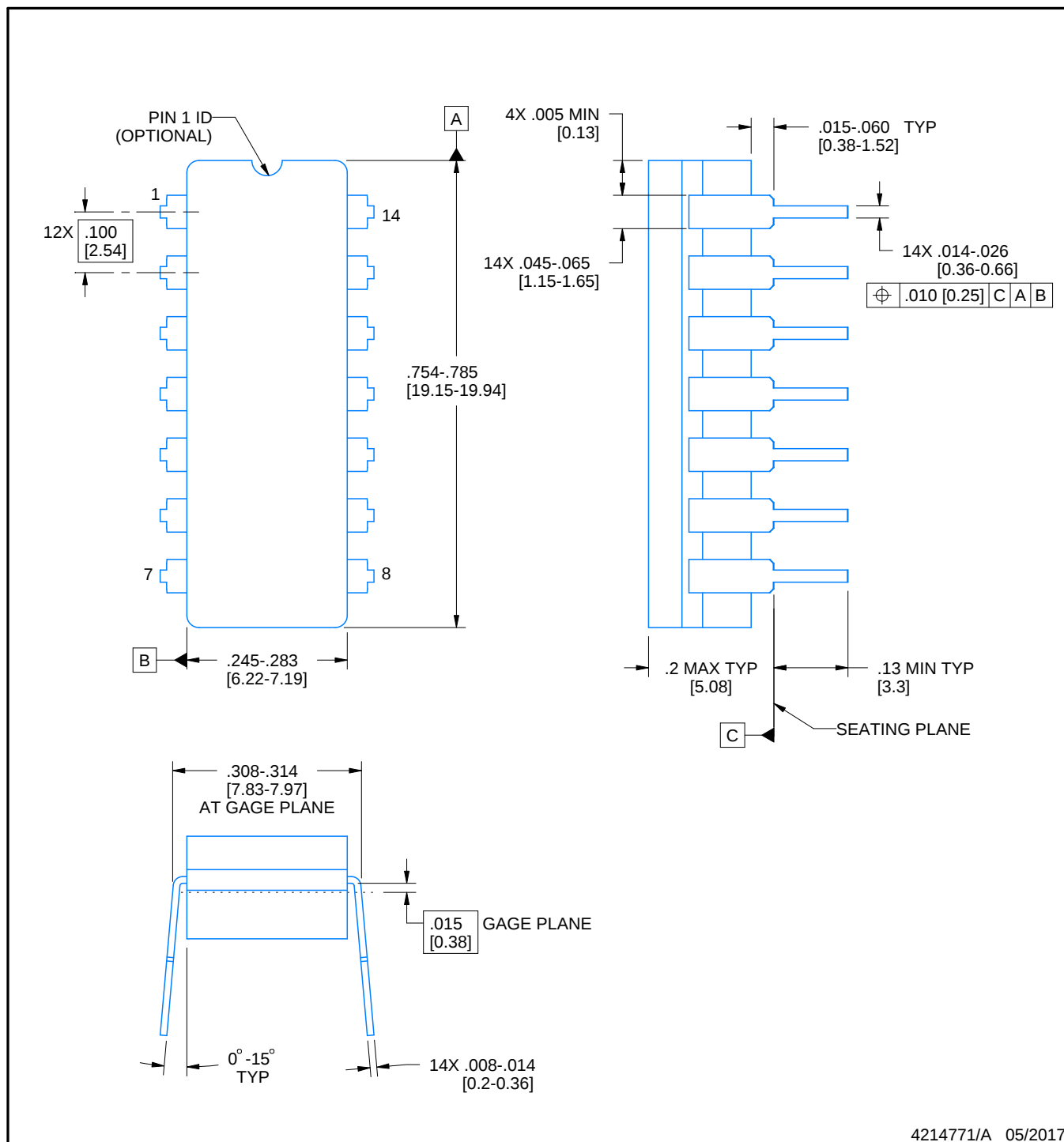


J0014A

PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

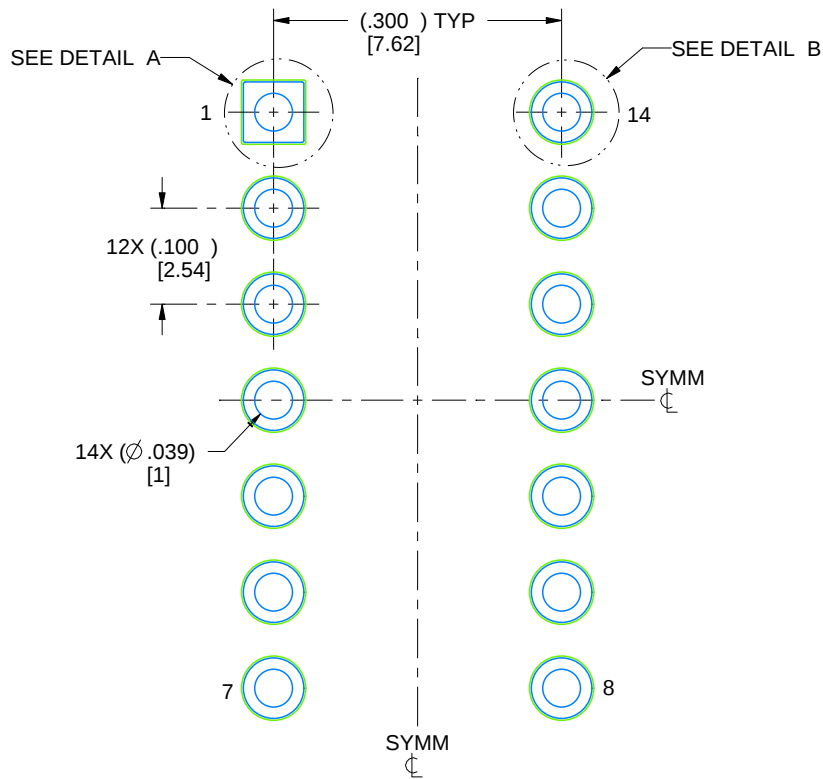
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

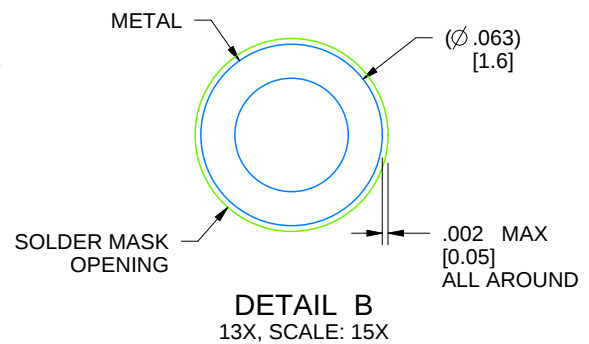
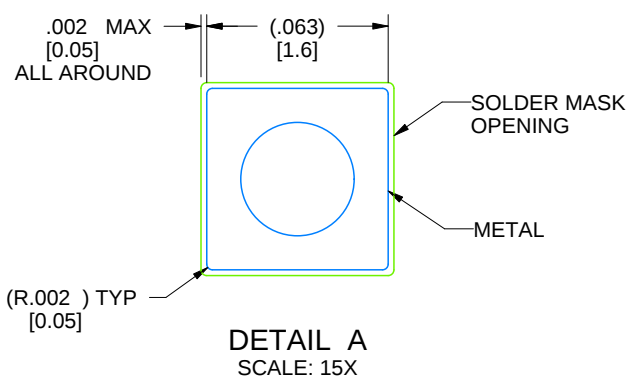
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

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