

# SN54LS112A, SN54S112, SN74LS112A, SN74S112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

D2661, APRIL 1982—REVISED MARCH 1988

SDLS011

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

## description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset and clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54LS112A and SN54S112 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LS112A and SN74S112A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

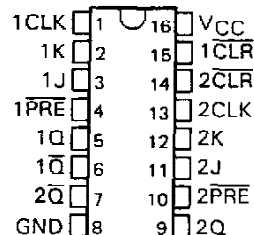
FUNCTION TABLE (each flip-flop)

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↓	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q <sub>0</sub>	$\bar{Q}_0$

<sup>†</sup> The output levels in this configuration are not guaranteed to meet the minimum levels for  $V_{OH}$  if the lows at preset and clear are near  $V_{IL}$  minimum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

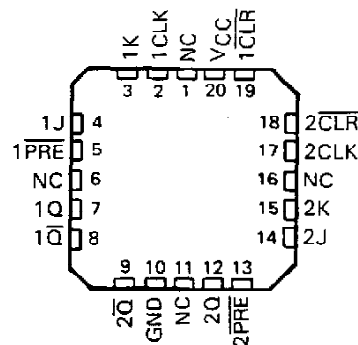
SN54LS112A, SN54S112 . . . J OR W PACKAGE  
SN74LS112A, SN74S112A . . . D OR N PACKAGE

(TOP VIEW)



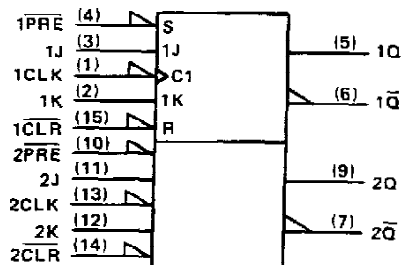
SN54LS112A, SN54S112 . . . FK PACKAGE

(TOP VIEW)



NC—No internal connection

## logic symbol<sup>†</sup>



<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

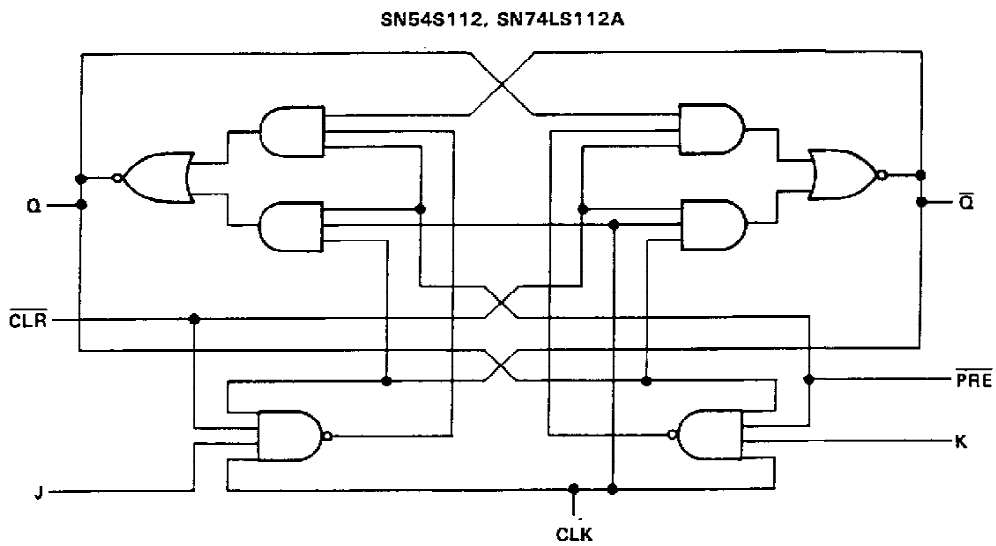
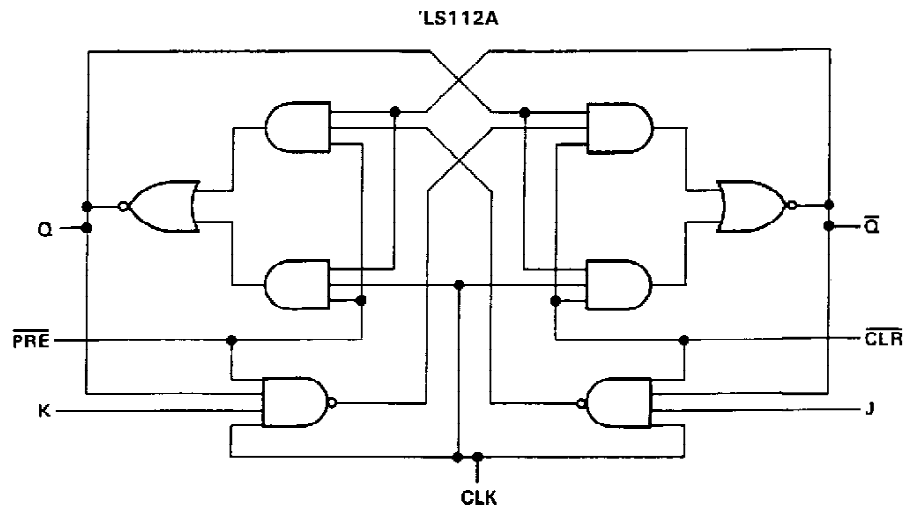
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**SN54LS112A, SN54S112, SN74LS112A, SN74S112A**  
**DUAL J-K NEGATIVE-EDGE-TRIGGERED**  
**FLIP-FLOPS WITH PRESET AND CLEAR**

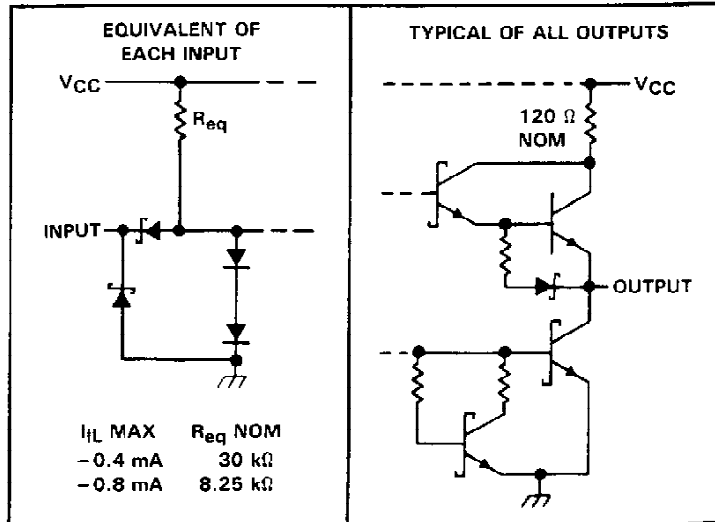
logic diagrams (positive logic)



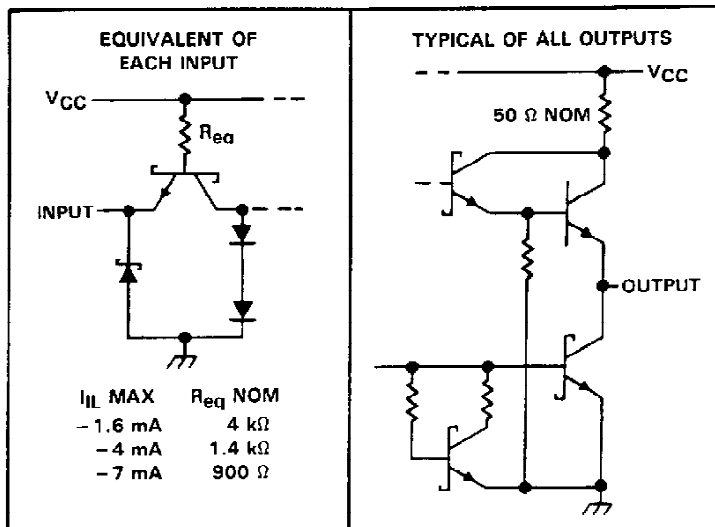
**SN54LS112A, SN54S112, SN74LS112A, SN74S112A**  
**DUAL J-K NEGATIVE-EDGE-TRIGGERED**  
**FLIP-FLOPS WITH PRESET AND CLEAR**

schematics of inputs and outputs

'LS112A



SN54S112, SN74S112A



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage: 'LS112A .....	7 V
SN54LS112, SN74LS112A .....	5.5 V
Operating free-air temperature range: SN54' .....	-55°C to 125°C
SN74' .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.



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# SN54LS112A, SN74LS112A

## DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

### recommended operating conditions

		SN54LS112A			SN74LS112A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			-0.4			-0.4	mA
$I_{OL}$	Low-level output current			4			8	mA
$f_{clock}$	Clock frequency	0		30	0		30	MHz
$t_w$	Pulse duration	CLK high		20			20	ns
		PRE or CLR low		25			25	
$t_{su}$	Set up time-before CLK↓	Data high or low		20			20	ns
		CLR inactive		25			25	
		PRE inactive		20			20	
$t_h$	Hold time-data after CLK↓	0			0			ns
$T_A$	Operating free-air temperature	-55		125	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS112A			SN74LS112A			UNIT	
			MIN	TYP‡	MAX	MIN	TYP‡	MAX		
$V_{IK}$		$V_{CC} = \text{MIN}$ , $I_I = -18 \text{ mA}$			-1.5			-1.5	V	
$V_{OH}$		$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = \text{MAX}$ , $I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V	
$V_{OL}$		$V_{CC} = \text{MIN}$ , $V_{IL} = \text{MAX}$ , $V_{IH} = 2 \text{ V}$ , $I_{OL} = 4 \text{ mA}$	0.25	0.4		0.25	0.4		V	
		$V_{CC} = \text{MIN}$ , $V_{IL} = \text{MAX}$ , $V_{IH} = 2 \text{ V}$ , $I_{OL} = 8 \text{ mA}$				0.35	0.5			
$I_I$	J or K	$V_{CC} = \text{MAX}$ , $V_I = 7 \text{ V}$			0.1			0.1	mA	
	CLR or PRE				0.3			0.3		
	CLK				0.4			0.4		
$I_{IH}$	J or K	$V_{CC} = \text{MAX}$ , $V_I = 2.7 \text{ V}$			20			20	$\mu\text{A}$	
	CLR or PRE				60			60		
	CLK				80			80		
$I_{IL}$	J or K	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$			-0.4			-0.4	mA	
	All other				-0.8			-0.8		
$I_{OS}^{\S}$		$V_{CC} = \text{MAX}$ , see Note 2	-20		-100			-20	-100	mA
$I_{CC}$ (Total)		$V_{CC} = \text{MAX}$ , see Note 3			4			4		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTES: 2. For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with  $V_O = 2.25 \text{ V}$  and  $2.125 \text{ V}$  for the '54 family and the '74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

3. With all outputs open,  $I_{CC}$  is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

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**SN54LS112A, SN74LS112A**  
**DUAL J-K NEGATIVE-EDGE-TRIGGERED**  
**FLIP-FLOPS WITH PRESET AND CLEAR**

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$f_{max}$			$R_L = 2\text{ k}\Omega$ , $C_L = 15\text{ pF}$	30	45		MHz	
$t_{PLH}$	$\overline{\text{CLR}}$ , $\overline{\text{PRE}}$ or CLK	Q or $\overline{\text{Q}}$			15	20		ns
$t_{PHL}$					15	20		ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

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**SN54S112, SN74S112A**  
**DUAL J-K NEGATIVE-EDGE-TRIGGERED**  
**FLIP-FLOPS WITH PRESET AND CLEAR**

**recommended operating conditions**

		SN54S112			SN74S112A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage				0.8			V
I <sub>OH</sub>	High-level output current				-1			mA
I <sub>OL</sub>	Low-level output current				20			mA
t <sub>w</sub>	Pulse duration	CLK high		6	6		ns	
		CLK low		6.5	6.5			
		PRE or CLR low		8	8			
t <sub>su</sub>	Set up time-before CLK↓	Data high or low		7	7		ns	
t <sub>h</sub>	Hold time-data after CLK↓	0			0			ns
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS†		SN54S112			SN74S112A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA		-1.2			-1.2			V
V <sub>OH</sub>		V <sub>CC</sub> = MIN, I <sub>OH</sub> = -1 mA, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX,		2.5	3.4		2.7	3.4		V
V <sub>OL</sub>		V <sub>CC</sub> = MIN, I <sub>OL</sub> = 20 mA, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V,		0.5			0.5			V
I <sub>I</sub>		V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V		1			1			mA
I <sub>IH</sub>	J or K	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V		50			50			μA
	All other			100			100			
I <sub>IL</sub>	J or K	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V		-1.6			-1.6			mA
	CLR‡			-7			-7			
	PRE‡			-7			-7			
	CLK			-4			-4			
I <sub>OS</sub> †		V <sub>CC</sub> = MAX		-40	-100		-40	-100	mA	
I <sub>CC</sub> #		V <sub>CC</sub> = MAX, see Note 3		15	25		15	25	mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Clear is tested with preset high and preset is tested with clear high.

¶ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

# Values are average per flip-flop.

NOTE 3: With all outputs open, I<sub>CC</sub> is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.



**SN54S112, SN74S112A**  
**DUAL J-K NEGATIVE-EDGE-TRIGGERED**  
**FLIP-FLOPS WITH PRESET AND CLEAR**

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{max}$			$R_L = 280\ \Omega, \quad C_L = 15\ \text{pF}$	80	125		MHz
$t_{PLH}$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	$Q$ or $\overline{Q}$			4	7	ns
$t_{PHL}$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ (CLK high)	$\overline{Q}$ or $Q$			5	7	ns
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ (CLK low)				5	7	
$t_{PLH}$	CLK	$Q$ or $\overline{Q}$			4	7	ns
$t_{PHL}$					5	7	ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">JM38510/07102BEA</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/07102B EA
JM38510/07102BEA.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/07102B EA
<a href="#">JM38510/07102BFA</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 07102BFA
JM38510/07102BFA.A	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 07102BFA
<a href="#">JM38510/30103B2A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30103B2A
JM38510/30103B2A.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30103B2A
<a href="#">JM38510/30103BEA</a>	NRND	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30103BEA
JM38510/30103BEA.A	NRND	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30103BEA
<a href="#">JM38510/30103BFA</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30103BFA
JM38510/30103BFA.A	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30103BFA
<a href="#">M38510/07102BEA</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/07102B EA
<a href="#">M38510/07102BFA</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 07102BFA
<a href="#">M38510/30103B2A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30103B2A
<a href="#">M38510/30103BEA</a>	NRND	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30103BEA
<a href="#">M38510/30103BFA</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30103BFA
<a href="#">SN54LS112AJ</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS112AJ
SN54LS112AJ.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS112AJ
<a href="#">SN54S112J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54S112J

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN54S112J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54S112J
<a href="#">SN74LS112AD</a>	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	0 to 70	LS112A
<a href="#">SN74LS112ADR</a>	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS112A
SN74LS112ADR.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS112A
<a href="#">SN74LS112AN</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS112AN
SN74LS112AN.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS112AN
<a href="#">SN74LS112ANSR</a>	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS112A
SN74LS112ANSR.A	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS112A
<a href="#">SN74S112AN</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74S112AN
SN74S112AN.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74S112AN
<a href="#">SNJ54LS112AFK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS 112AFK
SNJ54LS112AFK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS 112AFK
<a href="#">SNJ54LS112AJ</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS112AJ
SNJ54LS112AJ.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS112AJ
<a href="#">SNJ54LS112AW</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS112AW
SNJ54LS112AW.A	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS112AW
<a href="#">SNJ54S112FK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54S 112FK
SNJ54S112FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54S 112FK
<a href="#">SNJ54S112J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54S112J
SNJ54S112J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54S112J
<a href="#">SNJ54S112W</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54S112W
SNJ54S112W.A	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54S112W

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS112A, SN74LS112A :**

● Catalog : [SN74LS112A](#)

● Military : [SN54LS112A](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



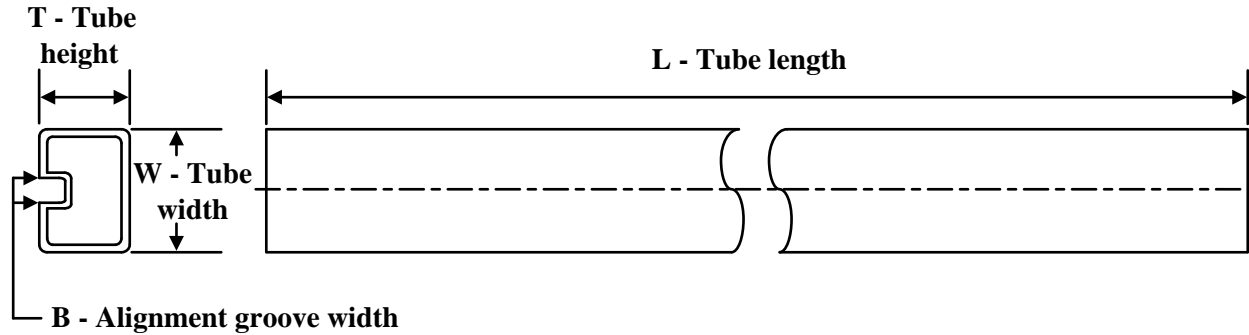
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS112ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS112ANSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS112ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LS112ANSR	SOP	NS	16	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal



Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
JM38510/07102BFA	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/07102BFA.A	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/30103B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/30103B2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/30103BFA	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/30103BFA.A	W	CFP	16	25	506.98	26.16	6220	NA
M38510/07102BFA	W	CFP	16	25	506.98	26.16	6220	NA
M38510/30103B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/30103BFA	W	CFP	16	25	506.98	26.16	6220	NA
SN74LS112AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS112AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS112AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS112AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74S112AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74S112AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74S112AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74S112AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54LS112AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS112AFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS112AW	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54LS112AW.A	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54S112FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54S112FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



4220735/A 12/2021

#### NOTES:

- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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