SN54SC8T574-SEP Radiation Tolerant Octal Edge-Triggered D-Type Flip-Flops with 3-State Outputs

1 Features

- Vendor item drawing available, VID V62/25629-01XE
- Radiation - Total Ionizing Dose (TID):
  - TID characterized up to 50krad(Si)
  - TID performance assurance up to 30krad(Si)
  - Radiation Lot Acceptance Testing (RLAT) for every wafer lot up to 30krad(Si)
- Radiation - Single-Event Effects (SEE):
  - Single Event Latch-Up (SEL) immune up to 50MeV-cm^2/mg at 125°C
  - Single Event Transient (SET) characterized up to LET = 50MeV-cm^2/mg
- Wide operating range of 1.2V to 5.5V
- Single-supply voltage translator:
  - Up translation:
    - 1.2V to 1.8V
    - 1.5V to 2.5V
    - 1.8V to 3.3V
    - 3.3V to 5.0V
  - Down translation:
    - 5.0V, 3.3V, 2.5V to 1.8V
    - 5.0V, 3.3V to 2.5V
    - 5.0V to 3.3V
- 5.5V tolerant input pins
- Supports standard pinouts
- Up to 150Mbps with 5V or 3.3V V_{CC}
- Latch-up performance exceeds 250mA per JESD 17
- Space enhanced plastic:
  - Supports defense and aerospace applications
  - Controlled baseline
  - Au bondwire and NiPdAu lead finish
  - Meets NASA ASTM E595 outgassing specification
  - One fabrication, assembly, and test site
  - Extended product life cycle
  - Product traceability

2 Applications

- Enable or disable a digital signal
- Controlling an indicator LED
- Translation between communication modules and system controllers

3 Description

The SN54SC8T574-SEP devices are octal edge-triggered D-type flip-flops..

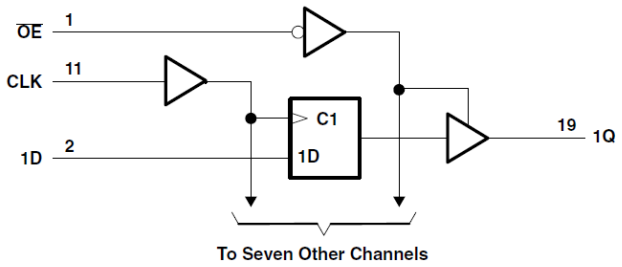
These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN54SC8T574-SEP	PW (TSSOP, 20)	6.5mm × 6.4mm	6.5mm × 4.4mm

(1) For more information, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

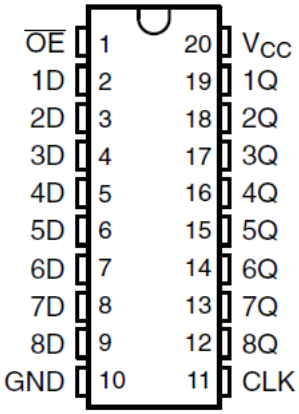


Figure 4-1. PW Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE	Description
NO.	NAME		
1	$\overline{OE}$	I	Clear all channels, active low
2	1D	I	Channel 1, D input
3	2D	I	Channel 2, D input
4	3D	I	Channel 3, D input
5	4D	I	Channel 4, D input
6	5D	I	Channel 5, D input
7	6D	I	Channel 6, D input
8	7D	I	Channel 7, D input
9	8D	I	Channel 8, D input
10	GND	—	Ground
11	CLK	I	Clock Pin
12	8Q	O	Channel 8, Q output
13	7Q	O	Channel 7, Q output
14	6Q	O	Channel 6, Q output
15	5Q	O	Channel 5, Q output
16	4Q	O	Channel 4, Q output
17	3Q	O	Channel 3, Q output
18	2Q	O	Channel 2, Q output
19	1Q	O	Channel 1, Q output
20	V_{CC}	—	Power Pin

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Output voltage range(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < -0.5V		-20	mA
I_{OK}	Output clamp current	V_O < -0.5V or V_O > V_{CC} + 0.5V		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous output current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specification	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		1.2	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
V_{IH}	High-level input voltage	V_{CC} = 1.2V to 1.3V	0.78		V
V_{IH}	High-level input voltage	V_{CC} = 1.65V to 2V	1.1		V
		V_{CC} = 2.25V to 2.75V	1.28		
		V_{CC} = 3V to 3.6V	1.45		
		V_{CC} = 4.5V to 5.5V	2		
V_{IL}	Low-Level input voltage	V_{CC} = 1.2V to 1.3V		0.18	V
V_{IL}	Low-Level input voltage	V_{CC} = 1.65V to 2V		0.5	V
		V_{CC} = 2.25V to 2.75V		0.65	
		V_{CC} = 3V to 3.6V		0.75	
		V_{CC} = 4.5V to 5.5V		0.85	
I_O	Output current	V_{CC} = 1.6V to 2V		±3	mA
		V_{CC} = 2.25V to 2.75V		±7	
		V_{CC} = 3.3V to 5.0V		±15	
I_O	Output Current	V_{CC} = 4.5V to 5.5V		±25	mA
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.6V to 5.0V		20	ns/V

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over operating free-air temperature range (unless otherwise noted)

Specification	Description	Condition	MIN	MAX	UNIT
T_A	Operating free-air temperature		-55	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
PW (TSSOP)	20	101.7	42.9	63.4	3.7	62.7	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range; typical ratings measured at T_A = 25°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = -50 uA	1.2V to 5.5V	V_{CC}-0.2			V
	I_{OH} = -1 mA	1.2V	0.8			
	I_{OH} = -2 mA	1.65V to 2V	1.21	1.7(1)		
	I_{OH} = -3 mA	2.25V to 2.75V	1.93	2.4(1)		
	I_{OH} = -5.5 mA	3V to 3.6V	2.49	3.08(1)		
	I_{OH} = -8 mA	4.5V to 5.5V	3.95	4.65(1)		
	I_{OH}= –24 mA	4.5V to 5.5V	3.15			
V_{OL}	I_{OL}= 50 µA	1.2V to 5.5V			0.1	V
	I_{OL} = 1 mA	1.2V			0.2	
	I_{OL} = 2 mA	1.65V to 2V		0.1(1)	0.25	
	I_{OL} = 3 mA	2.25V to 2.75V		0.1(1)	0.2	
	I_{OL} = 5.5 mA	3V to 3.6V		0.2(1)	0.25	
	I_{OL}= 8 mA	4.5V to 5.5V		0.3(1)	0.35	
	I_{OL}= 24 mA	4.5V to 5.5V			0.75	
I_I	V_I = 0 V or V_{CC}	0V to 5.5V		±0.1	±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	1.2V to 5.5V		2	220	µA
ΔI_{CC}	One input at 0.3 V or 3.4 V, other inputs at 0 or V_{CC}, I_O = 0	5.5V		1.35	1.5	mA
	One input at 0.3 V or 1.1 V, other inputs at 0 or V_{CC}, I_O = 0	1.8V			68	µA
C_I	V_I = V_{CC} or GND	5V		3	5	pF
C_O	V_O = V_{CC} or GND	5V		5	8	pF
I_{OZ}	V_O = V_{CC} or GND and V_{CC} = 5.5 V	5.5V			±26	µA
C_{PD} (2) (3)	C_L = 50 pF, F = 10 MHz	1.2V to 5.5V			200	pF

(1) Typical value at nearest nominal voltage (1.8V, 2.5V, 3.3V, and 5V)
(2) C_{PD} is used to determine the dynamic power consumption, per channel.
(3) P_D= V_{CC} ^{2}xF_Ix(C_{PD}+ C_L) where F_I= input frequency, C_L= output load capacitance, V_{CC}= supply voltage.

5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Load Capacitance	V_{CC}	-55°C to 125°C			UNIT
					MIN	TYP	MAX	
F_{MAX}	-	-	C_L = 15pF	1.2V ±0.2V			8	MHz
F_{MAX}	-	-	C_L = 50pF	1.2V ±0.2V			8	MHz

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over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Load Capacitance	V_{CC}	-55°C to 125°C			UNIT
					MIN	TYP	MAX	
T_{PHL}	CLK	Q	C_L = 15pF	1.2V ±0.2V	1		177.5	nS
T_{PHL}	CLK	Q	C_L = 50pF	1.2V ±0.2V	1		194.5	nS
T_{PLH}	CLK	Q	C_L = 15pF	1.2V ±0.2V	1		100.5	nS
T_{PLH}	CLK	Q	C_L = 50pF	1.2V ±0.2V	1		111.5	nS
T_{PZH}	OE	Q	C_L = 15pF	1.2V ±0.2V	1		90.7	nS
T_{PZH}	OE	Q	C_L = 50pF	1.2V ±0.2V	1		102.5	nS
T_{PZL}	OE	Q	C_L = 15pF	1.2V ±0.2V	1		97.3	nS
T_{PZL}	OE	Q	C_L = 50pF	1.2V ±0.2V	1		113.5	nS
T_{PHZ}	OE	Q	C_L = 15pF	1.2V ±0.2V	1.0		77.9	nS
T_{PHZ}	OE	Q	C_L = 50pF	1.2V ±0.2V	1		89.8	nS
T_{PLZ}	OE	Q	C_L = 15pF	1.2V ±0.2V	1.0		71.3	nS
T_{PLZ}	OE	Q	C_L = 50pF	1.2V ±0.2V	1		81	nS
F_{MAX}	-	-	C_L = 15pF	1.8V ±0.2V			26.5	MHz
F_{MAX}	-	-	C_L = 50pF	1.8V ±0.2V			26.5	MHz
T_{PHL}	CLK	Q	C_L = 15pF	1.8V ±0.2V	1		43.1	nS
T_{PHL}	CLK	Q	C_L = 50pF	1.8V ±0.2V	1		48.4	nS
T_{PLH}	CLK	Q	C_L = 15pF	1.8V ±0.2V	1		28.6	nS
T_{PLH}	CLK	Q	C_L = 50pF	1.8V ±0.2V	1		32.6	nS
T_{PZH}	OE	Q	C_L = 15pF	1.8V ±0.2V	1		28.8	nS
T_{PZH}	OE	Q	C_L = 50pF	1.8V ±0.2V	1		32.8	nS
T_{PZL}	OE	Q	C_L = 15pF	1.8V ±0.2V	1		29.2	nS
T_{PZL}	OE	Q	C_L = 50pF	1.8V ±0.2V	1		34.3	nS
T_{PHZ}	OE	Q	C_L = 15pF	1.8V ±0.2V	1.0		25.7	nS
T_{PHZ}	OE	Q	C_L = 50pF	1.8V ±0.2V	1		32.1	nS
T_{PLZ}	OE	Q	C_L = 15pF	1.8V ±0.2V	1.0		21.8	nS
T_{PLZ}	OE	Q	C_L = 50pF	1.8V ±0.2V	1		28.5	nS
F_{MAX}	-	-	C_L = 15pF	2.5V ±0.2V			40	MHz
F_{MAX}	-	-	C_L = 50pF	2.5V ±0.2V			41.9	MHz
T_{PHL}	CLK	Q	C_L = 15pF	2.5V ±0.2V	1		23.2	nS
T_{PHL}	CLK	Q	C_L = 50pF	2.5V ±0.2V	1		26.8	nS
T_{PLH}	CLK	Q	C_L = 15pF	2.5V ±0.2V	1		15.5	nS
T_{PLH}	CLK	Q	C_L = 50pF	2.5V ±0.2V	1		18.1	nS
T_{PZH}	OE	Q	C_L = 15pF	2.5V ±0.2V	1		17.5	nS
T_{PZH}	OE	Q	C_L = 50pF	2.5V ±0.2V	1		19.6	nS
T_{PZL}	OE	Q	C_L = 15pF	2.5V ±0.2V	1		17.3	nS
T_{PZL}	OE	Q	C_L = 50pF	2.5V ±0.2V	1		20.8	nS
T_{PHZ}	OE	Q	C_L = 15pF	2.5V ±0.2V	1.0		15.2	nS
T_{PHZ}	OE	Q	C_L = 50pF	2.5V ±0.2V	1		19.8	nS
T_{PLZ}	OE	Q	C_L = 15pF	2.5V ±0.2V	1.0		13.6	nS
T_{PLZ}	OE	Q	C_L = 50pF	2.5V ±0.2V	1		18	nS
F_{MAX}	-	-	C_L = 15pF	3.3V ±0.3V			51.7	MHz
F_{MAX}	-	-	C_L = 50pF	3.3V ±0.3V			52.5	MHz
T_{PHL}	CLK	Q	C_L = 15pF	3.3V ±0.3V	1		17.4	nS
T_{PHL}	CLK	Q	C_L = 50pF	3.3V ±0.3V	1		20.3	nS

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over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Load Capacitance	V_{CC}	-55°C to 125°C			UNIT
					MIN	TYP	MAX	
T_{PZH}	OE	Q	C_L = 15pF	3.3V ±0.3V	1		12.7	nS
T_{PZH}	OE	Q	C_L = 50pF	3.3V ±0.3V	1		14.9	nS
T_{PZL}	OE	Q	C_L = 15pF	3.3V ±0.3V	1		13.1	nS
T_{PZL}	OE	Q	C_L = 50pF	3.3V ±0.3V	1		16	nS
T_{PHZ}	OE	Q	C_L = 15pF	3.3V ±0.3V	1		11	nS
T_{PHZ}	OE	Q	C_L = 50pF	3.3V ±0.3V	1		14.5	nS
T_{PLZ}	OE	Q	C_L = 15pF	3.3V ±0.3V	1		9.9	nS
T_{PLZ}	OE	Q	C_L = 50pF	3.3V ±0.3V	1		13.4	nS
T_{PLH}	CLK	Q	C_L = 15pF	3.3V ±0.3V	1		12.3	nS
T_{PLH}	CLK	Q	C_L = 50pF	3.3V ±0.3V	1		14.3	nS
F_{MAX}	-	-	C_L = 15pF	5V ±0.5V			62.5	MHz
F_{MAX}	-	-	C_L = 50pF	5V ±0.5V			62.5	MHz
T_{PHL}	CLK	Q	C_L = 15pF	5V ±0.5V	1		12.7	nS
T_{PHL}	CLK	Q	C_L = 50pF	5V ±0.5V	1		14.9	nS
T_{PLH}	CLK	Q	C_L = 15pF	5V ±0.5V	1		9	nS
T_{PLH}	CLK	Q	C_L = 50pF	5V ±0.5V	1		10.9	nS
T_{PZH}	OE	Q	C_L = 15pF	5V ±0.5V	1		8.8	nS
T_{PZH}	OE	Q	C_L = 50pF	5V ±0.5V	1		10.7	nS
T_{PZL}	OE	Q	C_L = 15pF	5V ±0.5V	1		8.9	nS
T_{PZL}	OE	Q	C_L = 50pF	5V ±0.5V	1		11.3	nS
T_{PHZ}	OE	Q	C_L = 15pF	5V ±0.5V	1		8.2	nS
T_{PHZ}	OE	Q	C_L = 50pF	5V ±0.5V	1		10.2	nS
T_{PLZ}	OE	Q	C_L = 15pF	5V ±0.5V	1		7.1	nS
T_{PLZ}	OE	Q	C_L = 50pF	5V ±0.5V	1		9.8	nS

5.7 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	T_A = 25°C		-55°C to 125°C		UNIT
				MIN	MAX	MIN	MAX	
t_H	Hold time	Data after CLK↑	1.2V ±0.2V	0.5		2		nS
t_{SU}	Setup time	CLR inactive	1.2V ±0.2V	4		4.5		nS
t_{SU}	Setup time	Data before CLK↑	1.2V ±0.2V	51		89		nS
t_W	Pulse duration	CLK high or low	1.2V ±0.2V	42		53		nS
t_W	Pulse duration	CLR low	1.2V ±0.2V	6.5		7.5		nS
t_H	Hold time	Data after CLK↑	1.8V ±0.2V	1		2		nS
t_{SU}	Setup time	CLR inactive	1.8V ±0.2V	4		4.5		nS
t_{SU}	Setup time	Data before CLK↑	1.8V ±0.2V	13		20		nS
t_W	Pulse duration	CLK high or low	1.8V ±0.2V	13		15		nS
t_W	Pulse duration	CLR low	1.8V ±0.2V	6.5		7.5		nS
t_H	Hold time	Data after CLK↑	2.5V ±0.2V	0.5		2		nS
t_{SU}	Setup time	CLR inactive	2.5V ±0.2V	4		4.5		nS
t_{SU}	Setup time	Data before CLK↑	2.5V ±0.2V	10		13		nS
t_W	Pulse duration	CLK high or low	2.5V ±0.2V	9		10		nS
t_W	Pulse duration	CLR low	2.5V ±0.2V	6.5		7.5		nS

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over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	T_A = 25°C		-55°C to 125°C		UNIT
				MIN	MAX	MIN	MAX	
t_H	Hold time	Data after CLK↑	3.3V ±0.3V	1		1.5		nS
t_{SU}	Setup time	CLR inactive	3.3V ± 0.3V	2.5		3		nS
t_{SU}	Setup time	Data before CLK↑	3.3V ±0.3V	8		11		nS
t_W	Pulse duration	CLK high or low	3.3V ±0.3V	9		9		nS
t_W	Pulse duration	CLR low	3.3V ±0.3V	5		6.5		nS
t_H	Hold time	Data after CLK↑	5V ±0.5V	1		1.5		nS
t_{SU}	Setup time	CLR inactive	5V ±0.5V	2		2.5		nS
t_{SU}	Setup time	Data before CLK↑	5V ±0.5V	7		8		nS
t_W	Pulse duration	CLK high or low	5V ±0.5V	8		9		nS
t_W	Pulse duration	CLR low	5V ±0.5V	5		5.5		nS

5.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

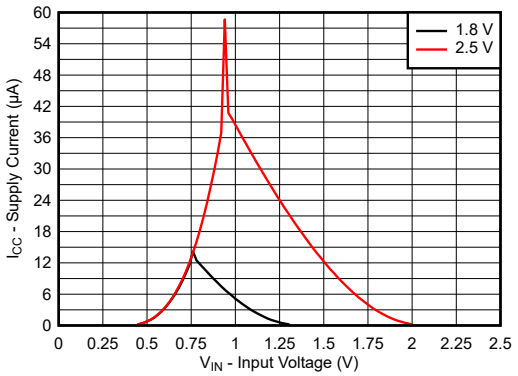


Figure 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply

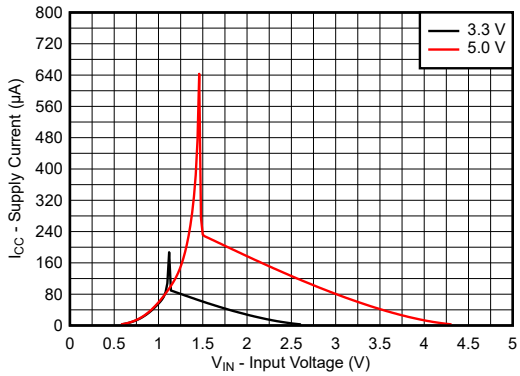


Figure 5-2. Supply Current Across Input Voltage 3.3V and 5.0V Supply

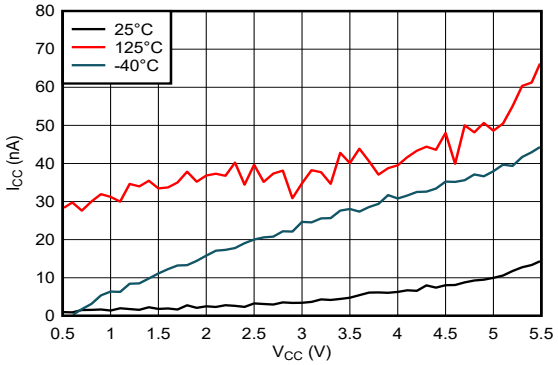


Figure 5-3. Supply Current Across Supply Voltage

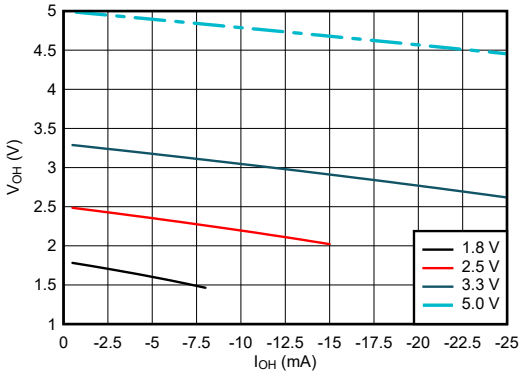


Figure 5-4. Output Voltage vs Current in HIGH State

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5.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

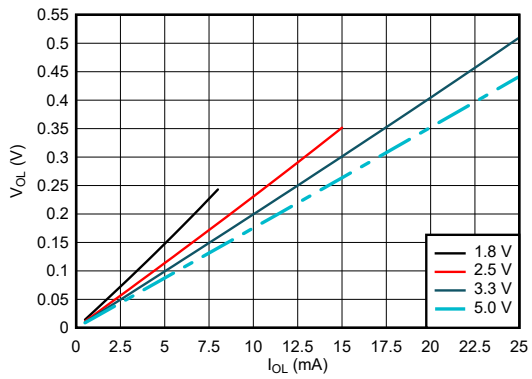


Figure 5-5. Output Voltage vs Current in LOW State

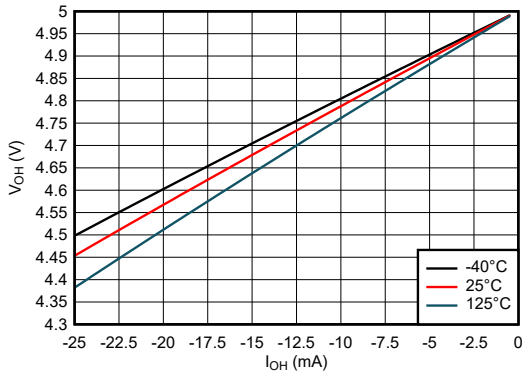


Figure 5-6. Output Voltage vs Current in HIGH State; 5V Supply

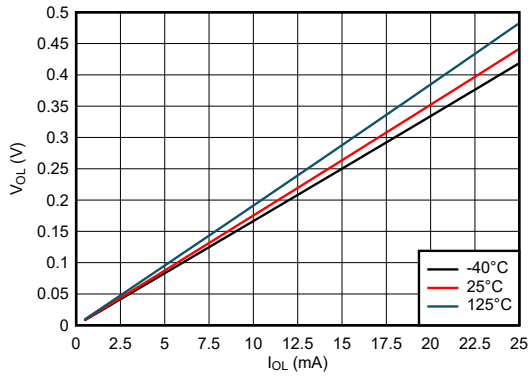


Figure 5-7. Output Voltage vs Current in LOW State; 5V Supply

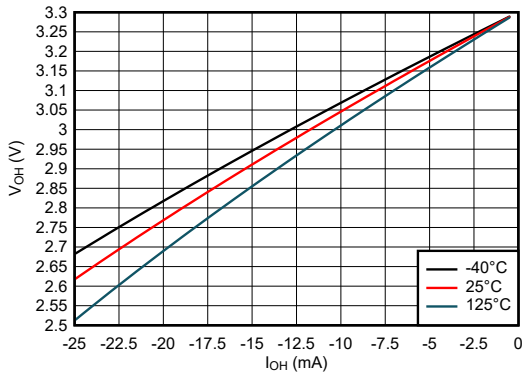


Figure 5-8. Output Voltage vs Current in HIGH State; 3.3V Supply

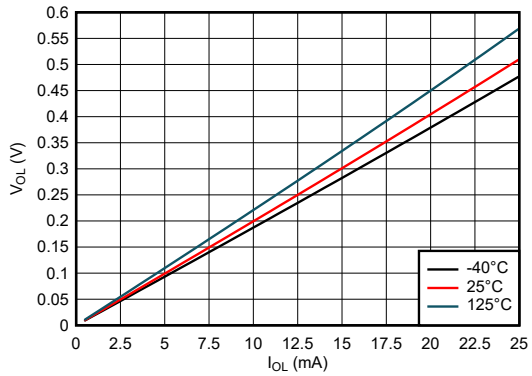


Figure 5-9. Output Voltage vs Current in LOW State; 3.3V Supply

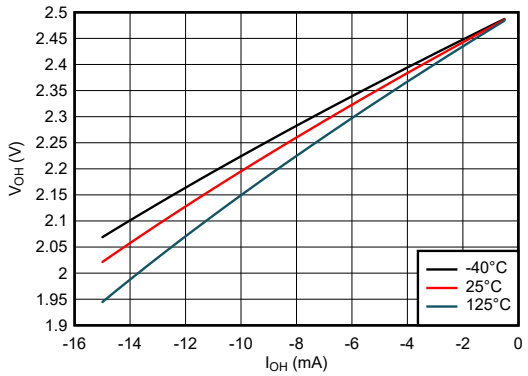


Figure 5-10. Output Voltage vs Current in HIGH State; 2.5V Supply

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5.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

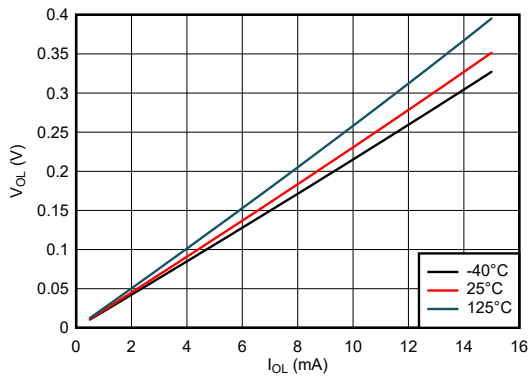


Figure 5-11. Output Voltage vs Current in LOW State; 2.5V Supply

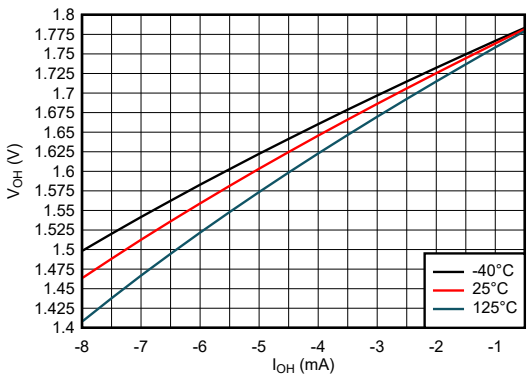


Figure 5-12. Output Voltage vs Current in HIGH State; 1.8V Supply

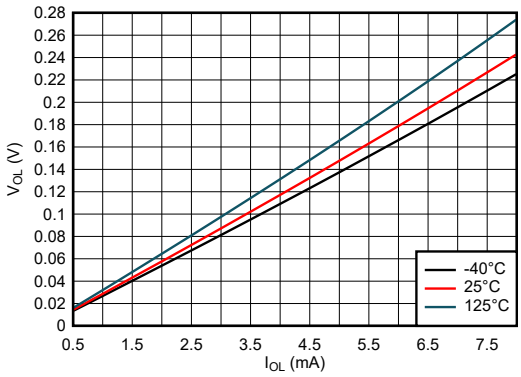


Figure 5-13. Output Voltage vs Current in LOW State; 1.8V Supply

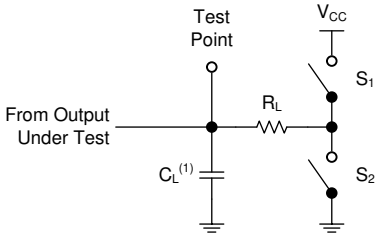
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6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω.

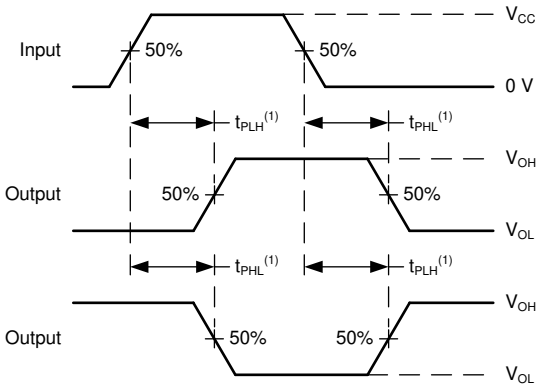
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



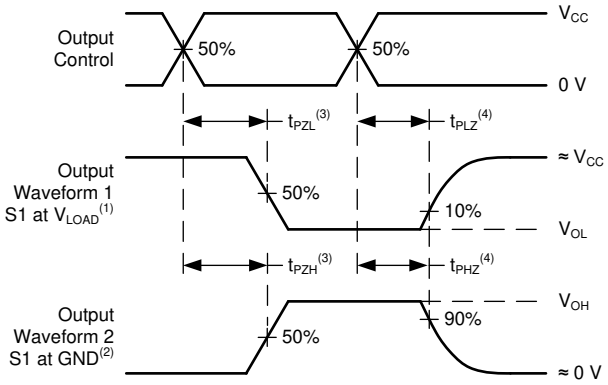
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-2. Voltage Waveforms Propagation Delays



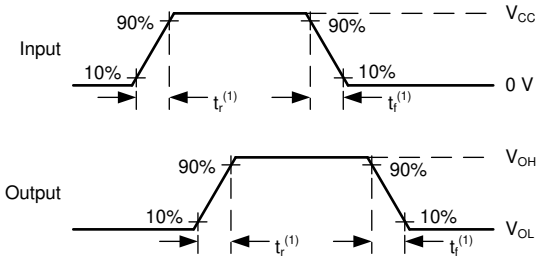
(1) S1 = CLOSED, S2 = OPEN.

(2) S1 = OPEN, S2 = CLOSED.

(3) The greater between t_{PZL} and t_{PZH} is the same as t_{en}.

(4) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis}.

Figure 6-3. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-4. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the SN54SC8T574-SEP devices are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

An output-enable ($\overline{OE}$) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Feature Description

7.2.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

7.2.2 SCxT Enhanced Input Voltage

The SN54SC8T574-SEP belongs to TI's SCxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5V levels to support down-translation. The output voltage will always be referenced to the supply voltage (V_{CC}), as described in the *Electrical Characteristics* table. For proper functionality, input signals must remain at or below the specified $V_{IH(MIN)}$ level for a HIGH input state, and at or below the specified $V_{IL(MAX)}$ for a LOW input state. Figure 7-1 shows the typical V_{IH} and V_{IL} levels for the SCxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

The inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification

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will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10-kΩ resistor is recommended and will typically meet all requirements.

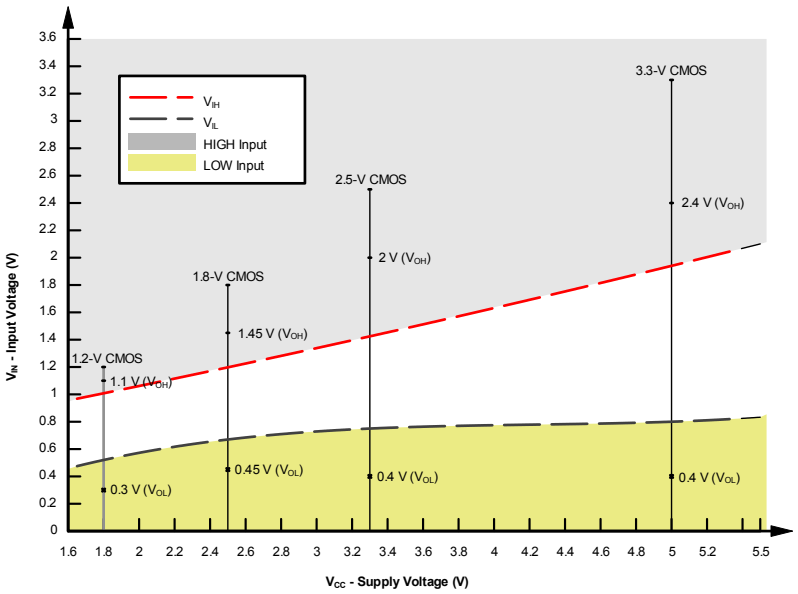


Figure 7-1. SCxT Input Voltage Levels

7.2.2.1 Up Translation

Input signals can be up translated using the SN54SC8T574-SEP. The voltage applied at V_{CC} will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables. When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5V supply will have a $V_{IH(MIN)}$ of 3.5V. For the SN54SC8T574-SEP, $V_{IH(MIN)}$ with a 5V supply is only 2V, which would allow for up-translation from a typical 2.5V to 5V signals.

As shown in Figure 7-2, ensure that the input signals in the HIGH state are above $V_{IH(MIN)}$ and input signals in the LOW state are lower than $V_{IL(MAX)}$.

Up Translation Combinations are as follows:

- 1.8V V_{CC} – Inputs from 1.2V
- 2.5V V_{CC} – Inputs from 1.8V
- 3.3V V_{CC} – Inputs from 1.8V and 2.5V
- 5.0-V V_{CC} – Inputs from 2.5V and 3.3V

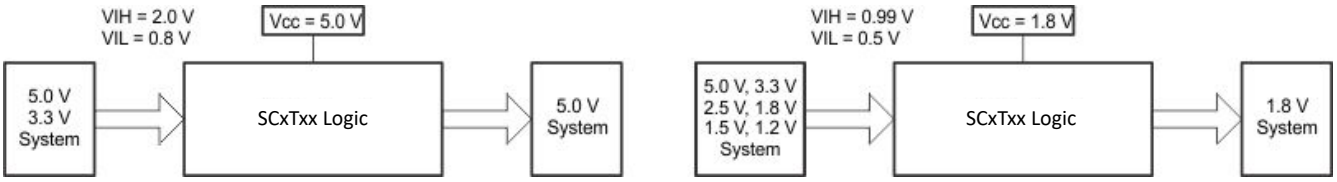


Figure 7-2. SCxT Up and Down Translation Example

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7.2.2.2 Down Translation

Signals can be translated down using the SN54SC8T574-SEP. The voltage applied at the V_{CC} will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0V in the LOW state. Ensure that the input signals in the HIGH state are between $V_{IH(MIN)}$ and 5.5V, and input signals in the LOW state are lower than $V_{IL(MAX)}$ as shown in Section 7.2.2.

For example, standard CMOS inputs for devices operating at 5.0V, 3.3V or 2.5V can be down-translated to match 1.8V CMOS signals when operating from 1.8V V_{CC}. See SCxT Up and Down Translation Example.

Down Translation Combinations are as follows:

- 1.8V V_{CC} – Inputs from 2.5V, 3.3V, and 5.0V
- 2.5V V_{CC} – Inputs from 3.3V and 5.0V
- 3.3V V_{CC} – Inputs from 5.0V

7.2.3 Clamp Diode Structure

As Figure 7-3 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

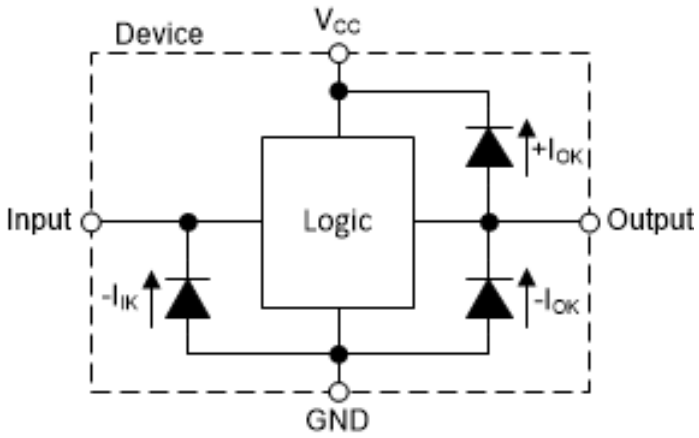


Figure 7-3. Electrical Placement of Clamping Diodes for Each Input and Output

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7.3 Functional Block Diagram

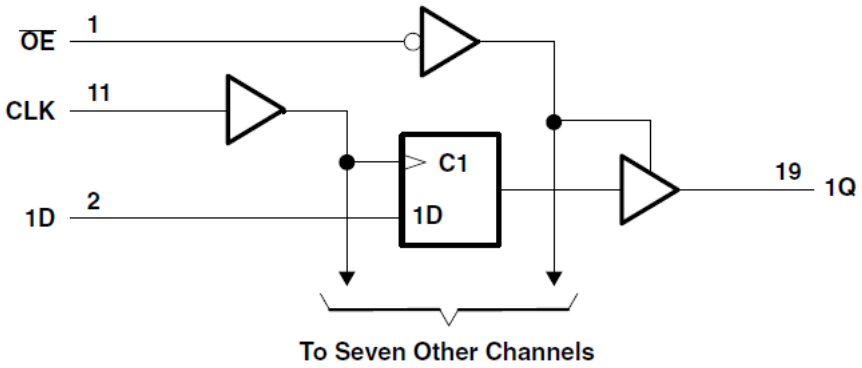


Figure 7-4. Logic Diagram (Positive Logic)

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS(1)			OUTPUT Q
$\overline{OE}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	L, H, ↓	X	Q_0
H	X	X	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Do not Care, Z = High Impedance

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN54SC8T574-SEP device is a high drive CMOS device that can be used for a multitude of bus-interface type applications where the data needs to be retained or latched. It can produce 24 mA of drive current at 3.3 V making it ideal for driving multiple outputs and also good for high-speed applications up to 100 Mhz. The inputs are 5.5 V tolerant allowing it to translate down to V_{CC}.

8.2 Typical Application

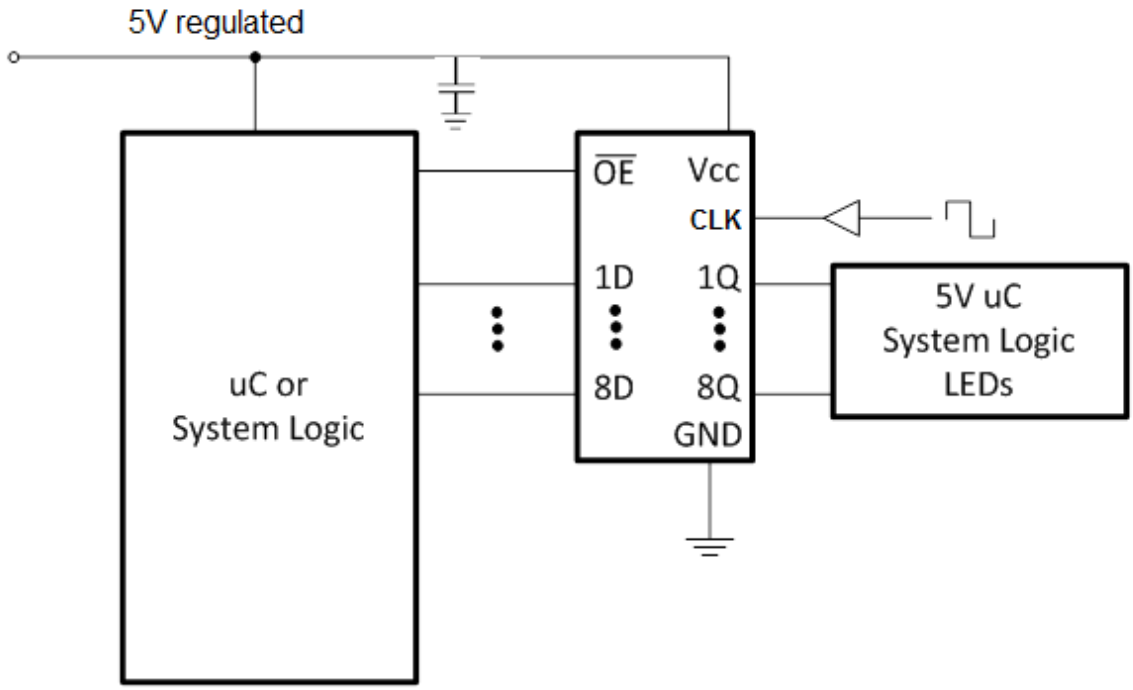


Figure 8-1. Typical Application Schematic

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8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN54SC8T574-SEP plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN54SC8T574-SEP plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN54SC8T574-SEP can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN54SC8T574-SEP can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

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8.2.1.2 Input Considerations

Input signals must cross to be considered a logic LOW, and to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN54SC8T574-SEP (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

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8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN54SC8T574-SEP to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

8.2.3 Application Curves

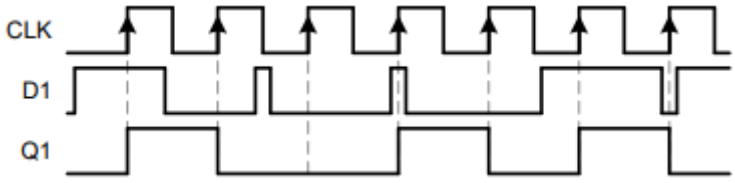


Figure 8-2. Simplified Functional Diagram Showing Clock Operation

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or VCC, whichever makes more sense for the logic function or is more convenient.

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8.4.2 Layout Example

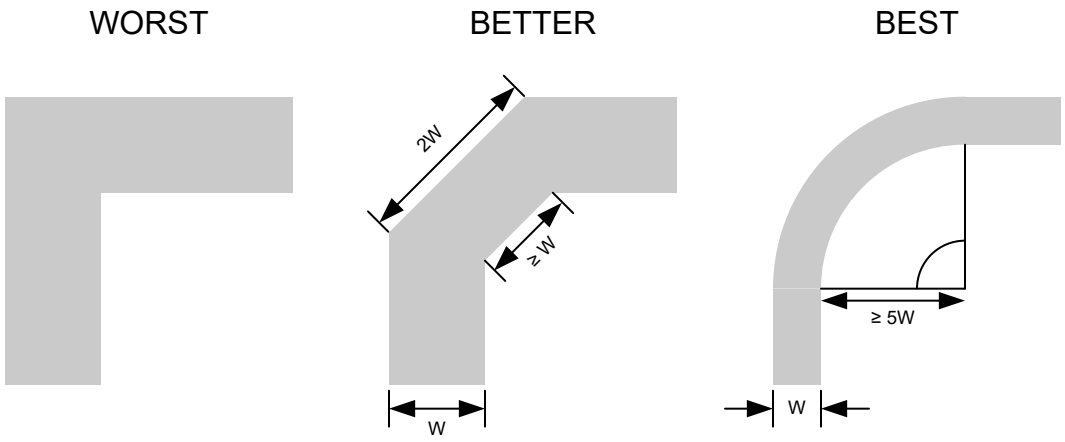


Figure 8-3. Example Trace Corners for Improved Signal Integrity

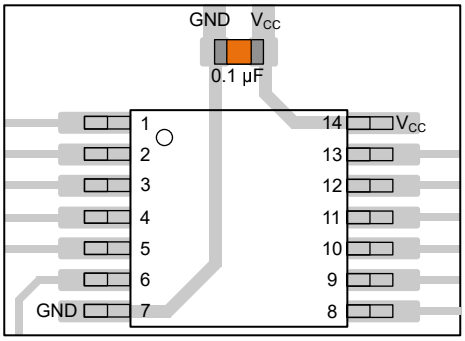


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

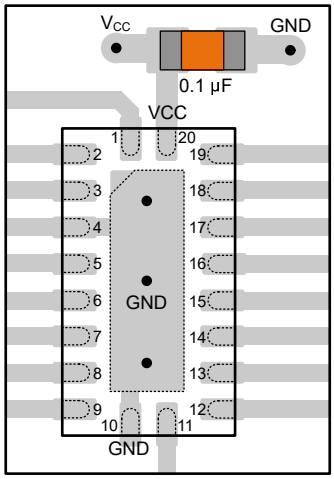


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

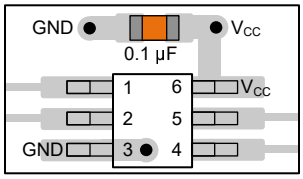


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

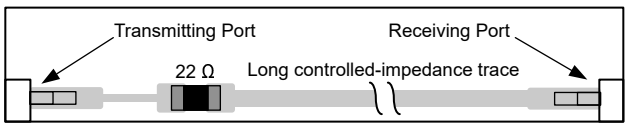


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
January 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN54SC8T574MPWTSEP	Active	Production	TSSOP (PW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	SC574SEP
SN54SC8T574MPWTSEP.A	Active	Production	TSSOP (PW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See SN54SC8T574MPWTSE	SC574SEP
V62/25629-01XE	Active	Production	TSSOP (PW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See SN54SC8T574MPWTSE	SC574SEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

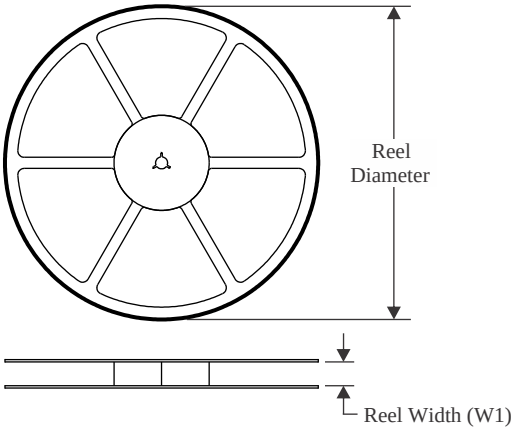
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

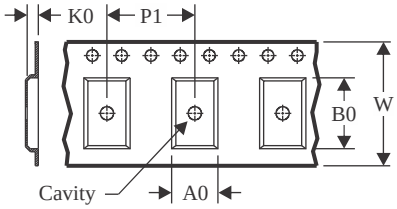
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

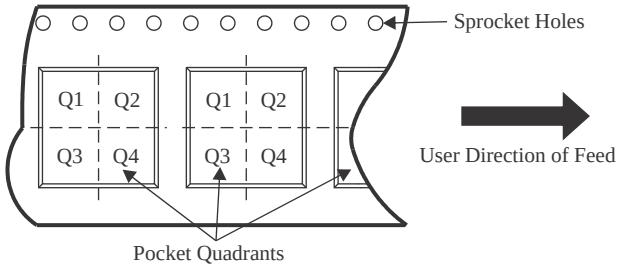


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

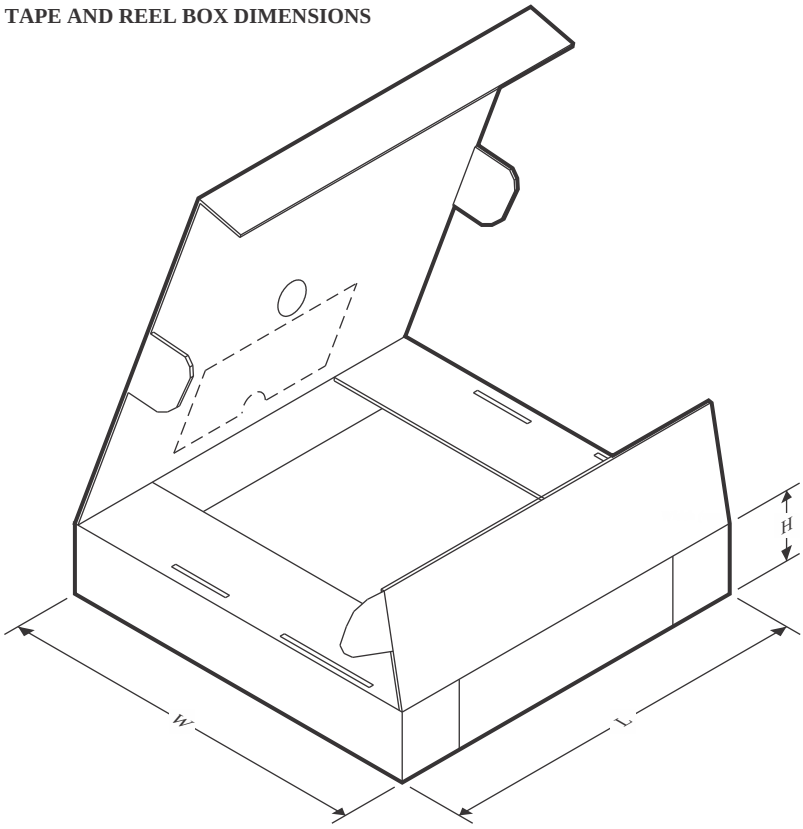
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN54SC8T574MPWTSEP	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

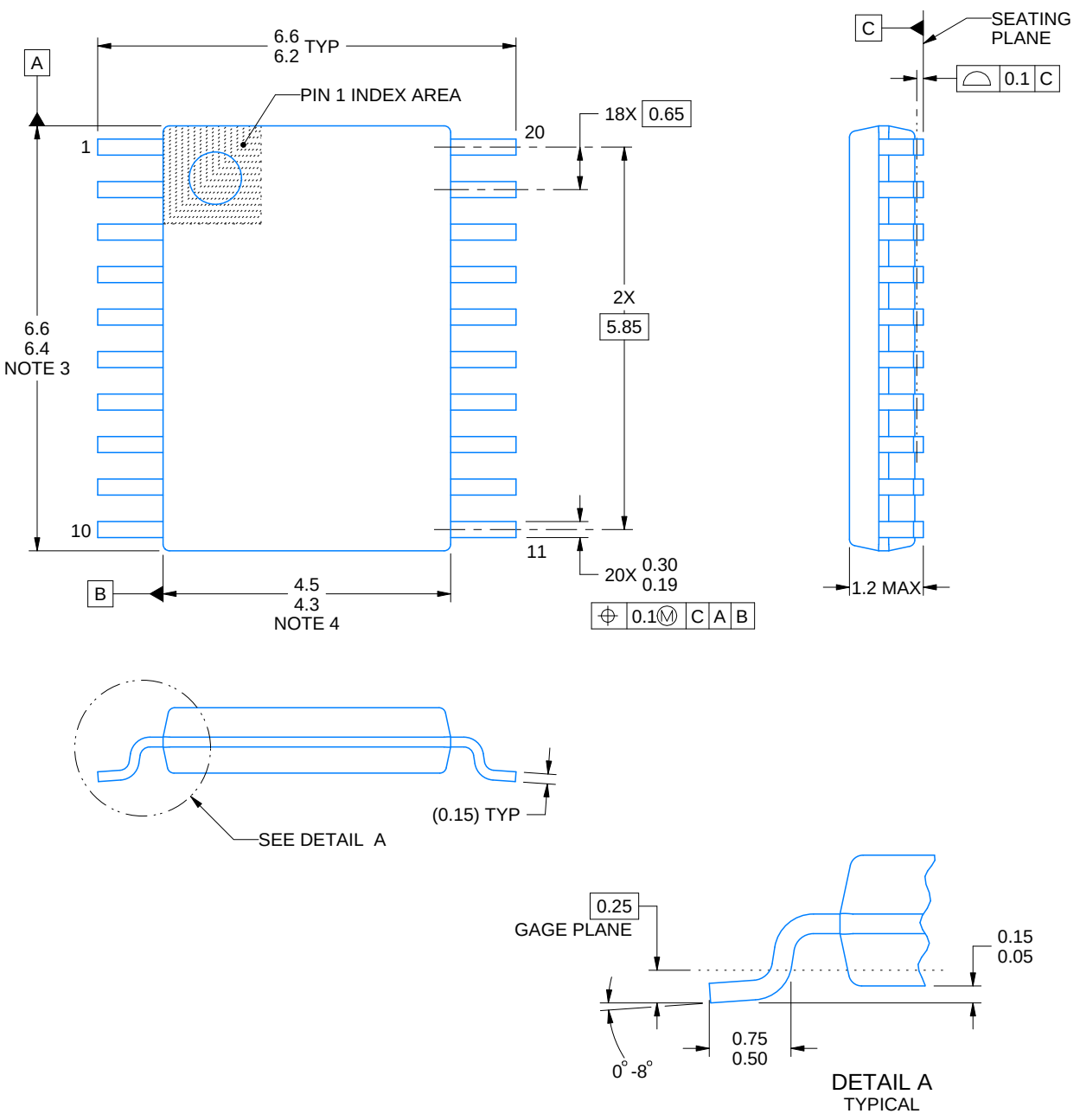
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN54SC8T574MPWTSEP	TSSOP	PW	20	250	353.0	353.0	32.0

PACKAGE OUTLINE

PW0020A

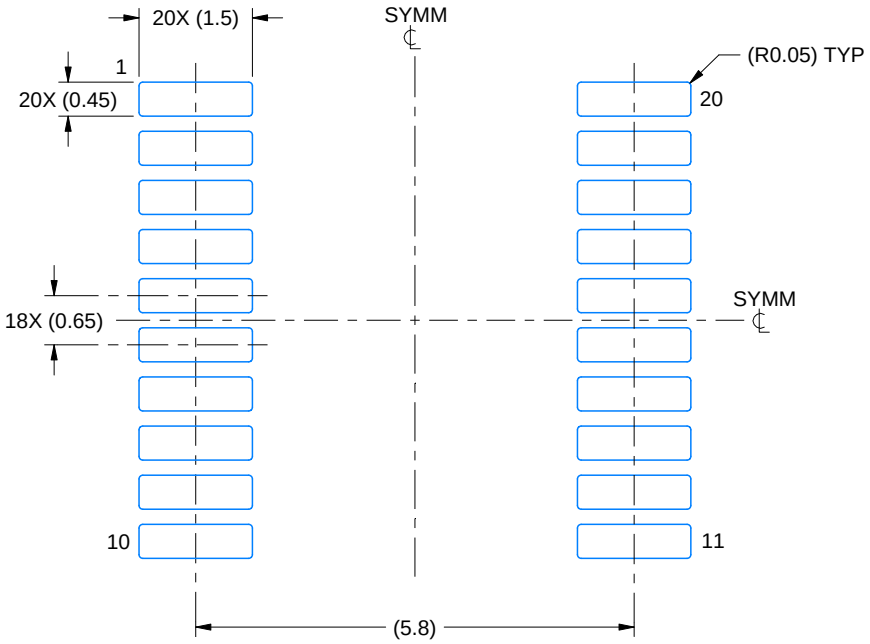
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

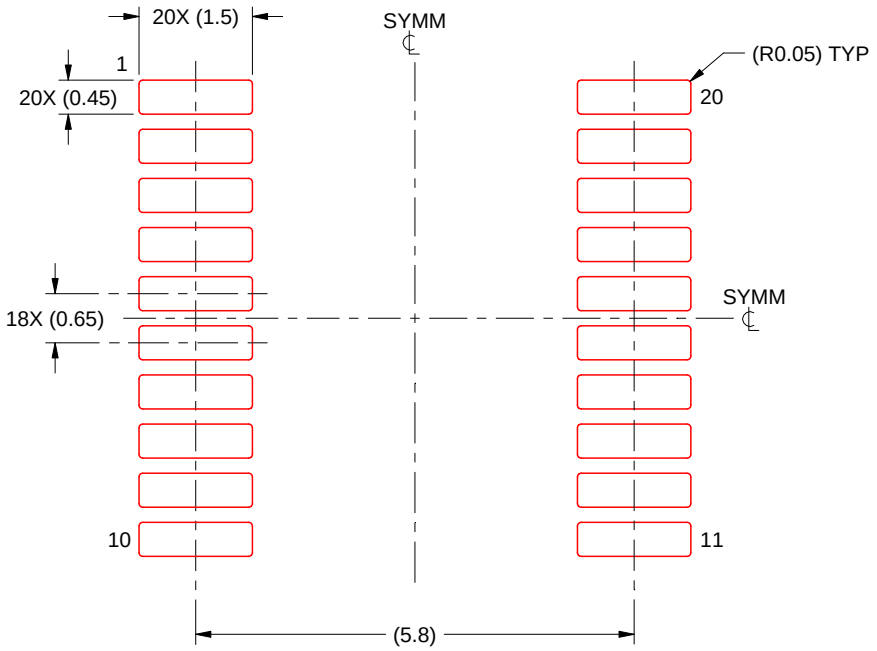


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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