HIGH-SPEED DIFFERENTIAL RECEIVER

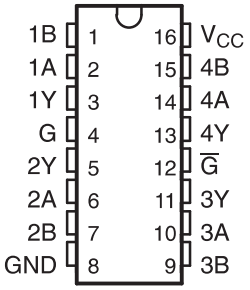
Check for Samples: SN55LVDS33-SP

FEATURES

- **400-Mbps Signaling Rate and 200-Mxfr/s Data Transfer Rate** (1)
- **Operates With a Single 3.3-V Supply**
- **–4 V to 5 V Common-Mode Input Voltage Range**
- **Differential Input Thresholds < ±50 mV With 50 mV of Hysteresis Over Entire Common-Mode Input Voltage Range**
- **Complies With TIA/EIA-644 (LVDS)**
- **Active Failsafe Assures a High-Level Output With No Input**
- **Bus-Pin ESD Protection Exceeds 15-kV HBM**
- **Input Remains High-Impedance On Power Down**
- **TTL Inputs Are 5-V Tolerant**
- **QML-V Qualified, SMD 5962-07248**
- **Military Temperature Range (–55°C to 125°C)**

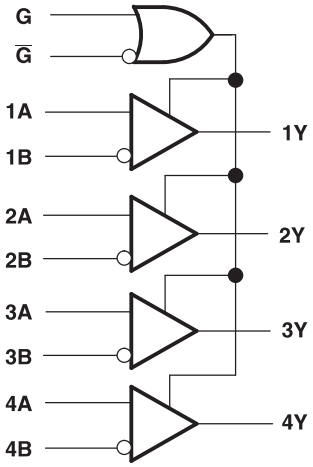
(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

W PACKAGE
(TOP VIEW)



SN55LVDS33W

logic diagram (positive logic)



DESCRIPTION/ORDERING INFORMATION

These LVDS data line receivers offers the widest common-mode input voltage range in the industry. These receivers provide an input voltage range specification compatible with a 5-V PECL signal as well as an overall increased ground-noise tolerance. They are in industry standard footprints with integrated termination as an option.

Precise control of the differential input voltage thresholds allows for inclusion of 50 mV of input voltage hysteresis to improve noise rejection on slowly changing input signals. The input thresholds are still no more than +50 mV over the full input common-mode voltage range.

The receivers can withstand ±15-kV Human-Body Model (HBM) and ±600-V Machine Model (MM) electrostatic discharges to the receiver input pins with respect to ground without damage. This provides reliability in cabled and other connections where potentially damaging noise is always a threat.

The receivers also include a (patent pending) failsafe circuit that provides a high-level output within 600 ns after loss of the input signal. The most common causes of signal loss are disconnected cables, shorted lines, or powered-down transmitters. The failsafe circuit prevents noise from being received as valid data under these fault conditions. This feature may also be used for wired-OR bus signaling. See *The Active Failsafe Feature of the SN65LVDS32B* application note.

The intended application and signaling technique of these devices is point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN55LVDS33 is characterized for operation from –55°C to 125°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	CFP - W	Tube	5962-0724801VFA	5962-0724801VFA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

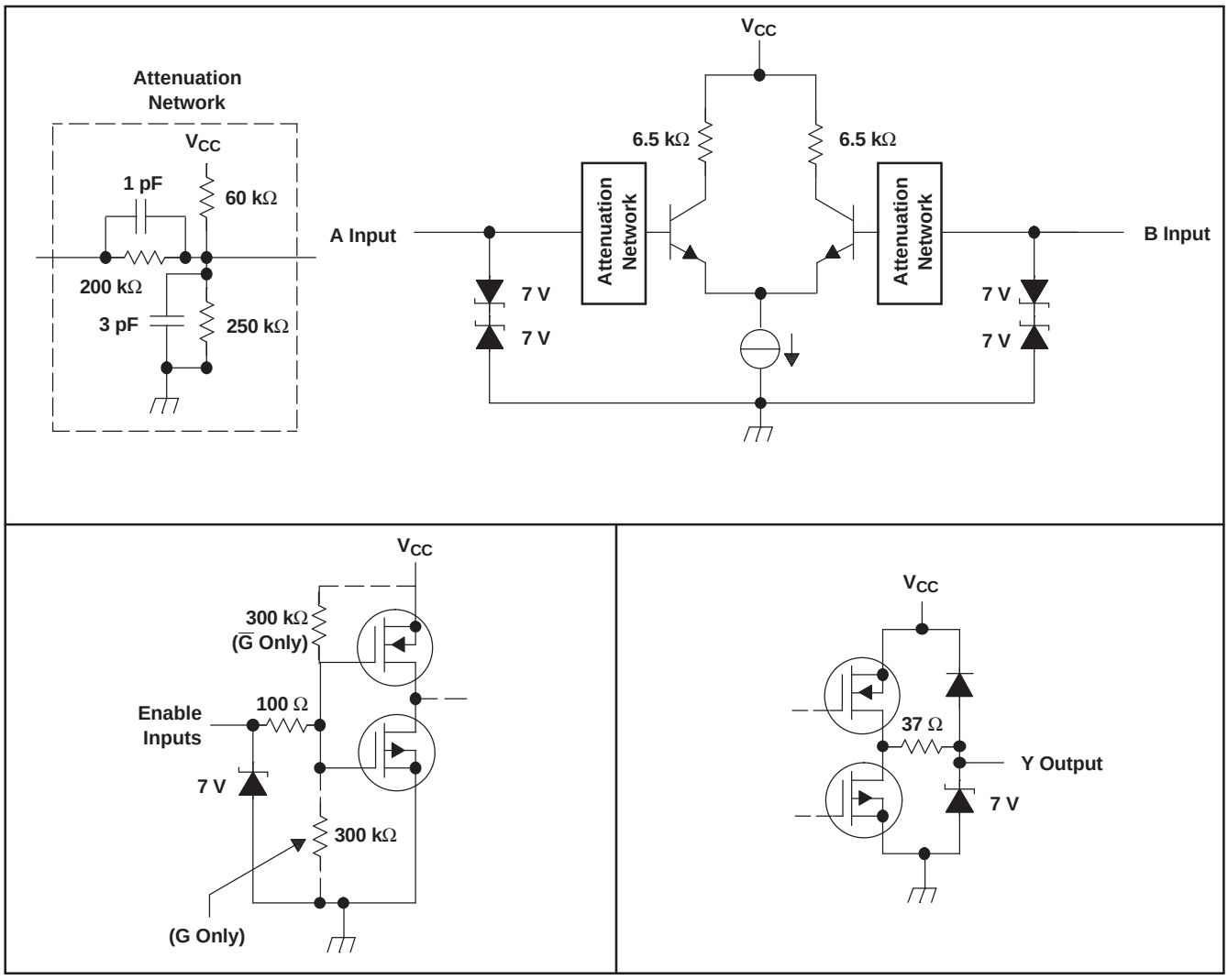
Table 1. FUNCTION TABLE(1)

SN55LVDS33			
DIFFERENTIAL INPUT	ENABLES		OUTPUT
$V_{ID} = V_A - V_B$	G	$\overline{G}$	Y
$V_{ID} \geq -32$ mV	H	X	H
	X	L	H
-100 mV $< V_{ID} \leq -32$ mV	H	X	?
	X	L	?
$V_{ID} \leq -100$ mV	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

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EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE
Supply voltage range, V_{CC} (2)		–0.5 V to +4 V
Voltage range	Enables or Y	–0.5 V to V_{CC} + 4 V
	A or B	–5 V to +6 V
Electrostatic discharge	A, B, and GND(3)	Class 3, A: 15 kV, B: 500 V
Charged-device mode	All pins(4)	±500 V
Storage temperature range		–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage	Enables	2		5	V
V_{IL}	Low-level input voltage	Enables	0		0.8	V
$\|V_{ID}\|$	Magnitude of differential input voltage		0.1		3	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common-mode)		–4		5	°C
T_A	Operating free-air temperature		–55		125	

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ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT1}	Positive-going differential input voltage threshold(2)	V_{IB} = –4 V or 5 V, See Figure 2				50	mV
V_{IT2}	Negative-going differential input voltage threshold(2)			–50			
V_{IT3}	Differential input failsafe voltage threshold(2)	See Table 2 and Figure 5		–32		–100	mV
$V_{ID(HYS)}$	Differential input voltage hysteresis, $V_{IT1} – V_{IT2}$				50		V
V_{OH}	High-level output voltage	I_{OH} = –4 mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA				0.4	V
I_{CC}	Supply current	G at V_{CC}, No load,	Steady state		16	25	mA
		G at GND			1.1	6	
I_I	Input current (A or B inputs)	V_I = 0 V,	Other input open			±25	µA
		V_I = 2.4 V,	Other input open			±25	
		V_I = –4 V,	Other input open			±80	
		V_I = 5 V,	Other input open			±45	
I_{IO}	Differential input current ($I_{IA} – I_{IB}$)	V_{ID} = 100 mV,	V_{IC}= –4 V or 5 V			±5	µA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	V_A or V_B = 0 V or 2.4 V, V_{CC} = 0 V				±25	µA
		V_A or V_B = –4 or 5 V, V_{CC} = 0 V				±60	
I_{IH}	High-level input current (enables)	V_{IH} = 2 V				12	µA
I_{IL}	Low-level input current (enables)	V_{IL} = 0.8 V				12	µA
I_{OZ}	High-impedance output current			–10		12	µA
C_I	Input capacitance, A or B input to GND	V_I = 0.4 sin (4E6πt) + 0.5 V			5		pF

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) Not production tested but guaranteed to the limit.

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SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{PLH(1)}$	Propagation delay time, low-to-high level output	See Figure 3	1.8	4	8	ns
$t_{PHL(1)}$	Propagation delay time, high-to-low level output		1.8	4	8	ns
t_{d1}	Delay time, failsafe deactivate time(2)	C_L = 10 pF, See Figure 3 and Figure 6			11	ns
t_{d2}	Delay time, failsafe activate time(2)		0.2		2	µs
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL(1)} - t_{PLH(1)} \rvert$)	See Figure 3		200		ps
$t_{sk(o)}$	Output skew(3)			150		ps
$t_{sk(pp)}$	Part-to-part skew(4)				1.2	ns
t_r	Output signal rise time			0.8		ns
t_f	Output signal fall time			0.8		ns
t_{PHZ}	Propagation delay time, high level-to-high impedance output	See Figure 4		5.5	12	ns
t_{PLZ}	Propagation delay time, low level-to-high impedance output			4.4	12	ns
t_{PZH}	Propagation delay time, high impedance-to-high level output			3.8	12	ns
t_{PZL}	Propagation delay time, high impedance-to-low level output			7	12	ns

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) Not production tested but guaranteed to the limit.
(3) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all receivers of a single device with all of their inputs driven together.
(4) $t_{sk(pp)}$ is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

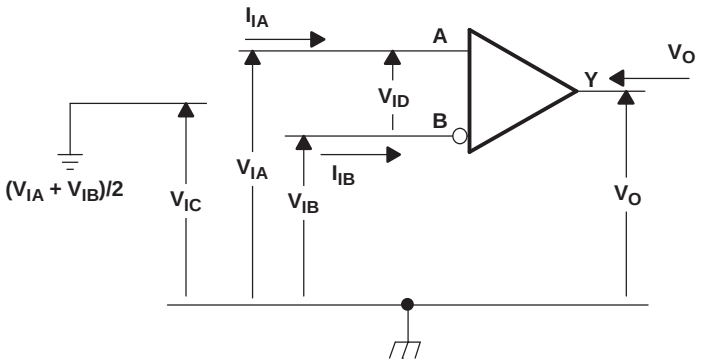
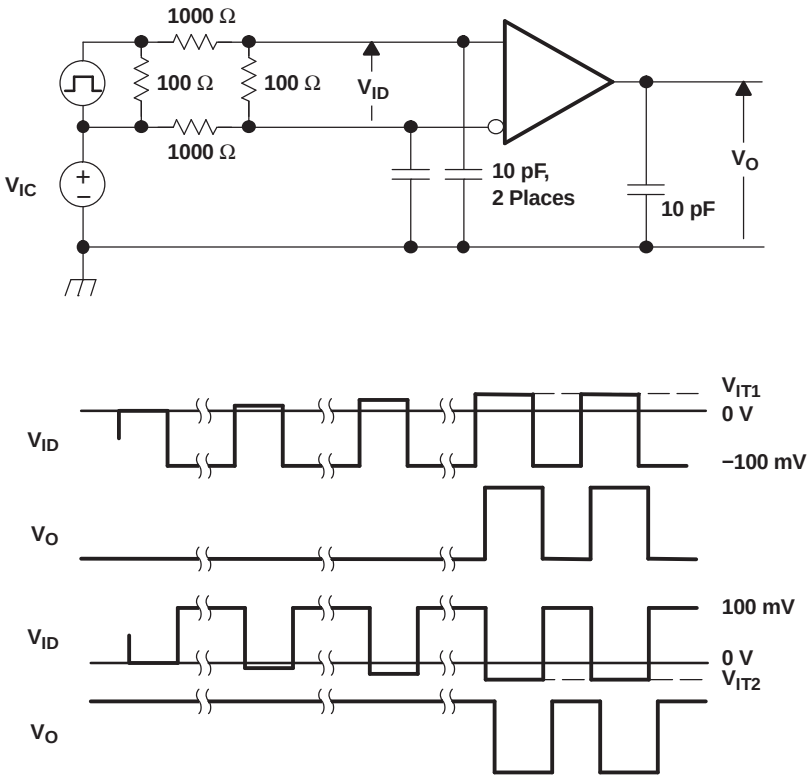


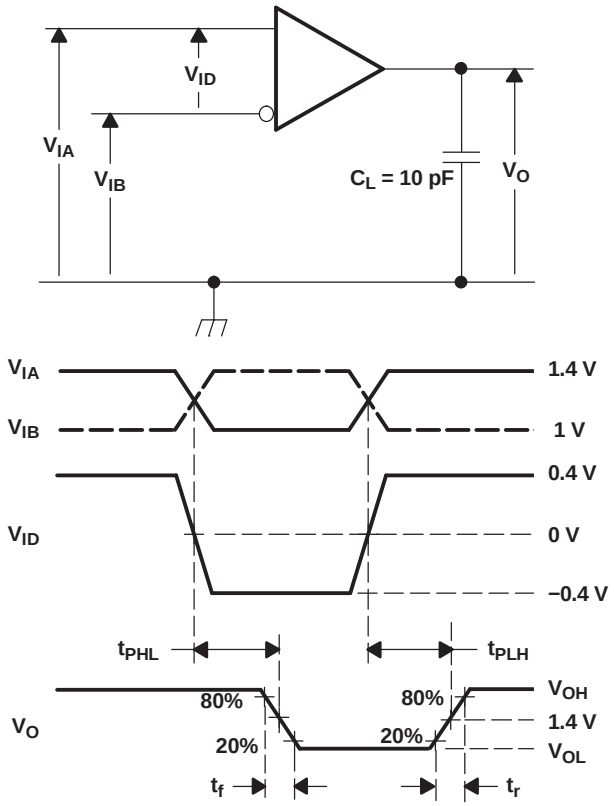
Figure 1. Voltage and Current Definitions

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NOTE: Input signal of 3 Mpps, duration of 167 ns, and transition time of <1 ns.

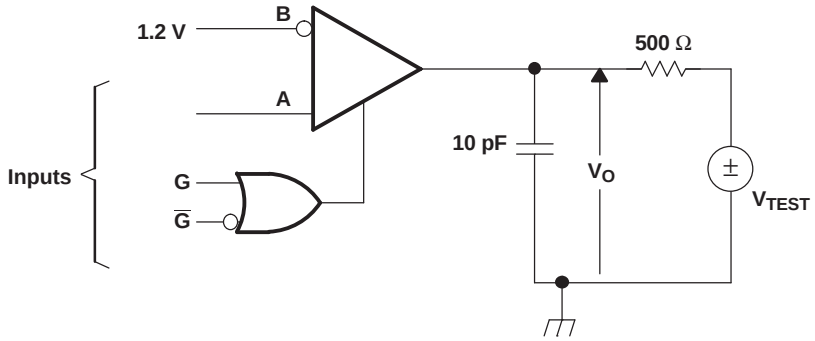
Figure 2. V_{IT1} and V_{IT2} Input Voltage Threshold Test Circuit and Definitions



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulsewidth = 10 ±0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 3. Timing Test Circuit and Waveforms

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NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ±10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

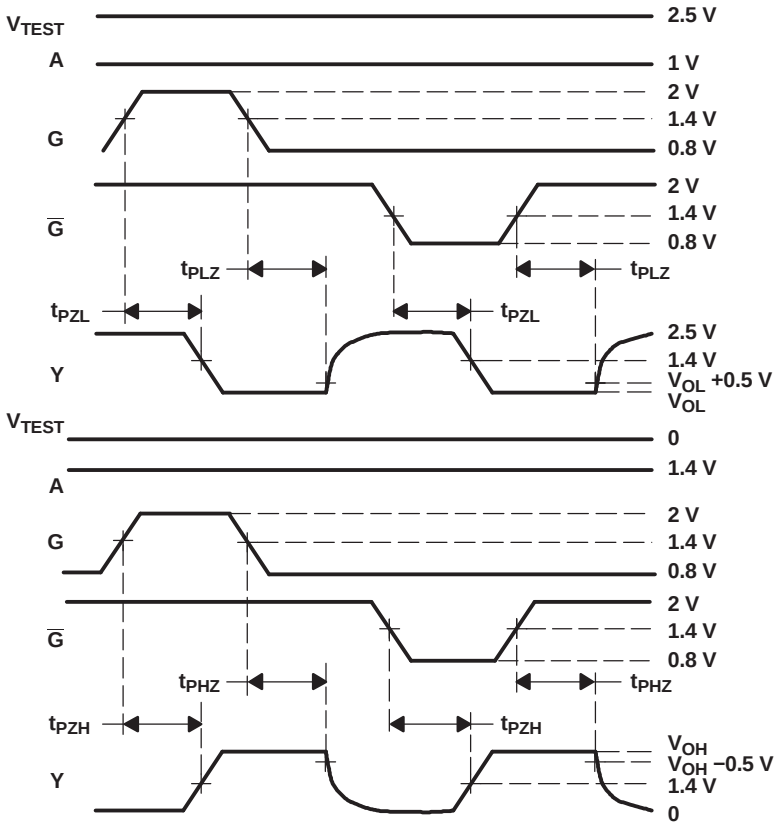


Figure 4. Enable/Disable Time Test Circuit and Waveforms

Table 2. Receiver Minimum and Maximum V_{IT3} Input Threshold Test Voltages

APPLIED VOLTAGES(1)		RESULTANT INPUTS		
V_{IA} (mV)	V_{IB} (mV)	V_{ID} (mV)	V_{IC} (mV)	Output
–4000	–3900	–100	–3950	L
–4000	–3968	–32	–3984	H
4900	5000	–100	4950	L
4968	5000	–32	4984	H

(1) These voltages are applied for a minimum of 1.5 µs.

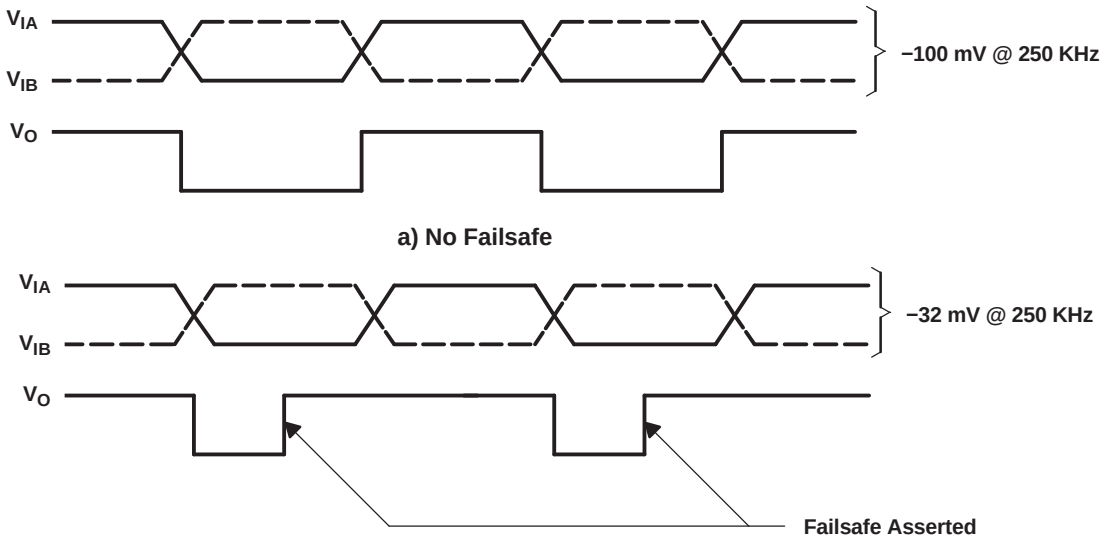


Figure 5. V_{IT3} Failsafe Threshold Test

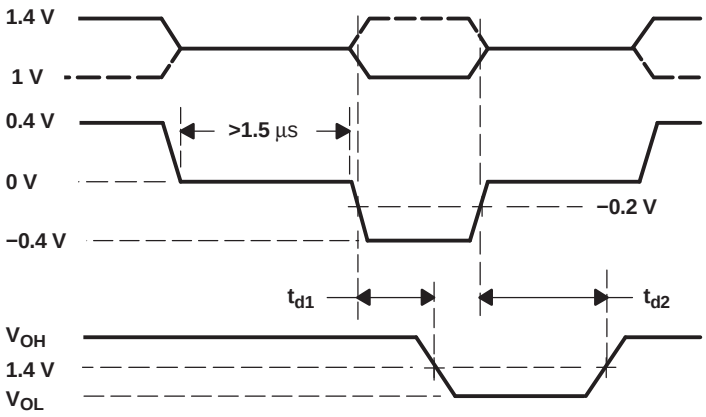


Figure 6. Waveforms for Failsafe Activate and Deactivate

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TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

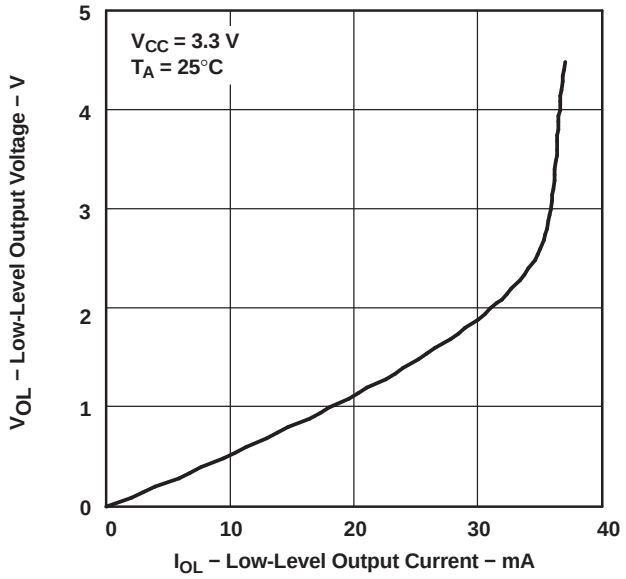


Figure 7.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

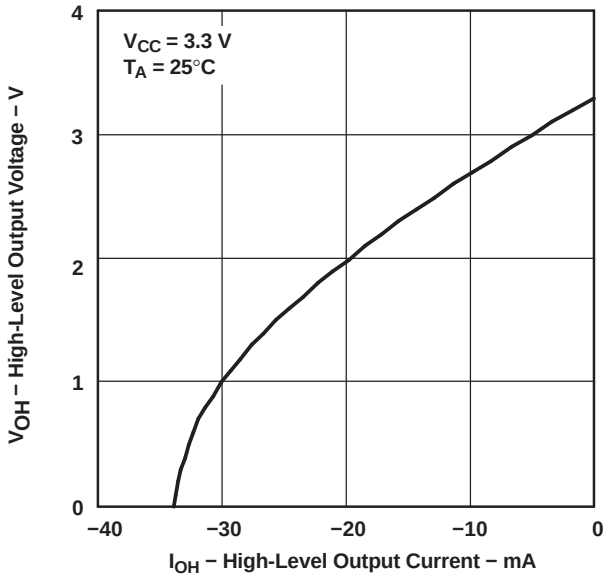


Figure 8.

LOW-TO-HIGH PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

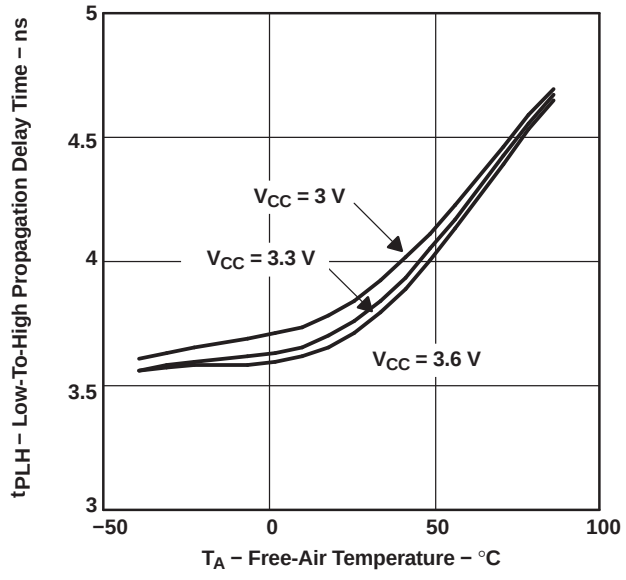


Figure 9.

HIGH-TO-LOW PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

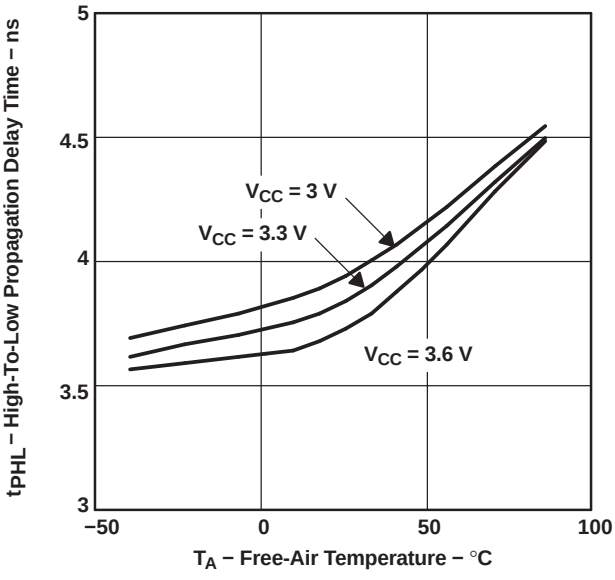


Figure 10.

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TYPICAL CHARACTERISTICS (continued)

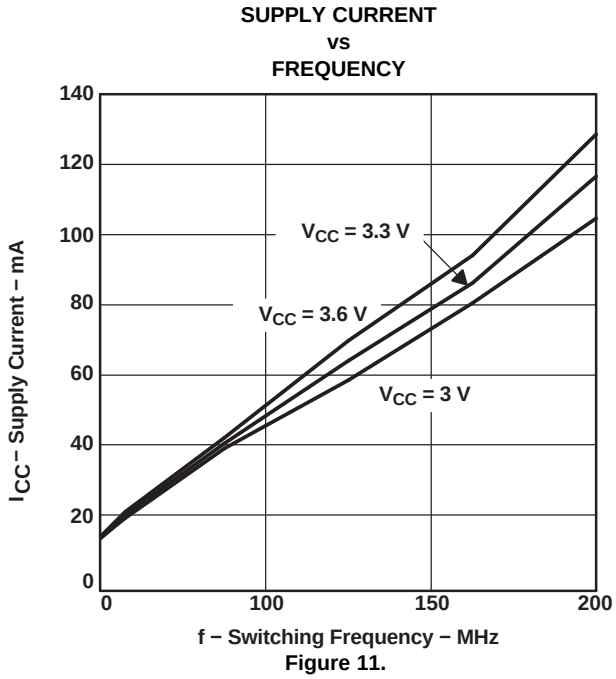
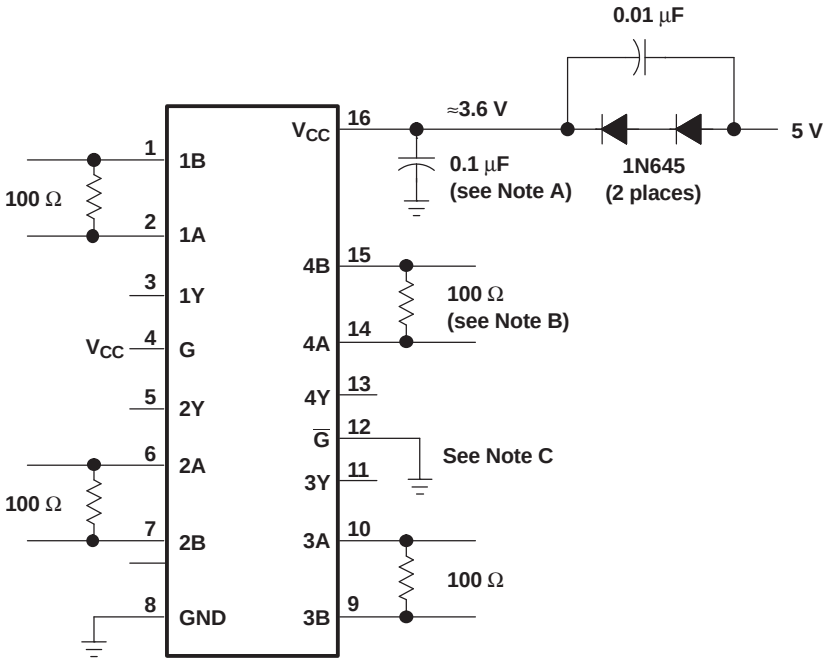


Figure 11.

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APPLICATION INFORMATION



A. Place a 0.1-µF Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitor should be located as close as possible to the device terminals.

B. The termination resistance value should match the nominal characteristic impedance of the transmission media with ±10%.

C. Unused enable inputs should be tied to V_{CC} or GND as appropriate.

Figure 12. Operation With 5-V Supply

RELATED INFORMATION

IBIS modeling is available for this device. Contact the local Texas Instruments sales office or the Texas Instruments Web site at www.ti.com for more information.

For more application guidelines, see the following documents:

- *Low-Voltage Differential Signalling Design Notes* (SLLA014)
- *Interface Circuits for TIA/EIA-644* (LVDS) (SLLA038)
- *Reducing EMI With LVDS* (SLLA030)
- *Slew Rate Control of LVDS Circuits* (SLLA034)
- *Using an LVDS Receiver With RS-422 Data* (SLLA031)

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ACTIVE FAILSAFE FEATURE

A differential line receiver commonly has a failsafe circuit to prevent it from switching on input noise. Current LVDS failsafe solutions require either external components with subsequent reductions in signal quality or integrated solutions with limited application. This family of receivers has a new integrated failsafe that solves the limitations seen in present solutions. A detailed theory of operation is presented in application note, *The Active Failsafe Feature of the SN65LVDS32B* (SLLA082A).

Figure 13 shows one receiver channel with active failsafe. It consists of a main receiver that can respond to a high-speed input differential signal. Also connected to the input pair are two failsafe receivers that form a window comparator. The window comparator has a much slower response than the main receiver and it detects when the input differential falls below 80 mV. A 600-ns failsafe timer filters the window comparator outputs. When failsafe is asserted, the failsafe logic drives the main receiver output to logic high.

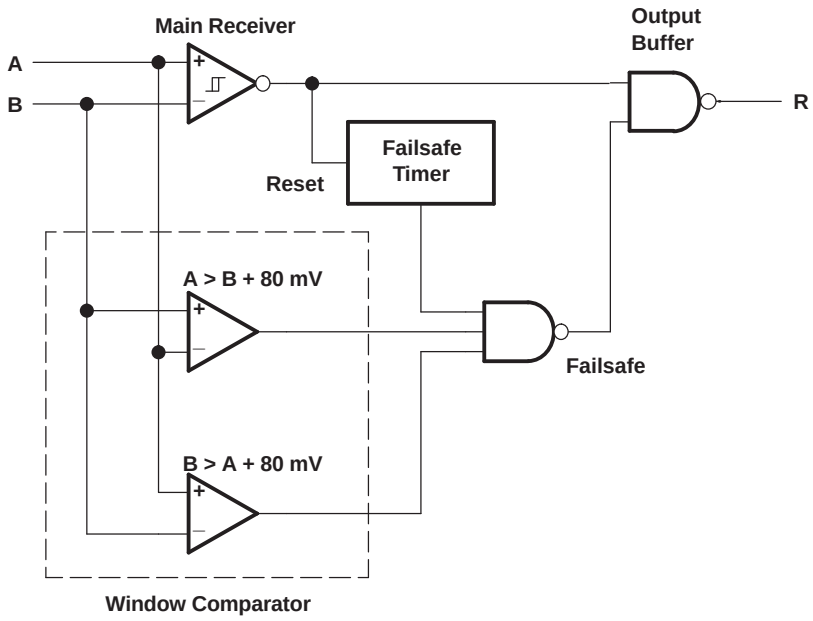


Figure 13. Receiver With Active Failsafe

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ECL/PECL-to-LVTTL CONVERSION WITH TI's LVDS RECEIVER

The various versions of emitter-coupled logic (i.e., ECL, PECL and LVPECL) are often the physical layer of choice for system designers. Designers know of the established technology and that it is capable of high-speed data transmission. In the past, system requirements often forced the selection of ECL. Now technologies like LVDS provide designers with another alternative. While the total exchange of ECL for LVDS may not be a design option, designers have been able to take advantage of LVDS by implementing a small resistor divider network at the input of the LVDS receiver. Texas Instruments has taken the next step by introducing a wide common-mode LVDS receiver (no divider network required) which can be connected directly to an ECL driver with only the termination bias voltage required for ECL termination (V_{CC} – 2 V).

Figure 14 and Figure 15 show the use of an LV/PECL driver driving five meters of CAT-5 cable and being received by Texas Instruments wide common-mode receiver and the resulting eye-pattern. The values for R3 are required in order to provide a resistor path to ground for the LV/PECL driver. With no resistor divider, R1 simply needs to match the characteristic load impedance of 50 Ω. The R2 resistor is a small value and is intended to minimize any possible common-mode current reflections.

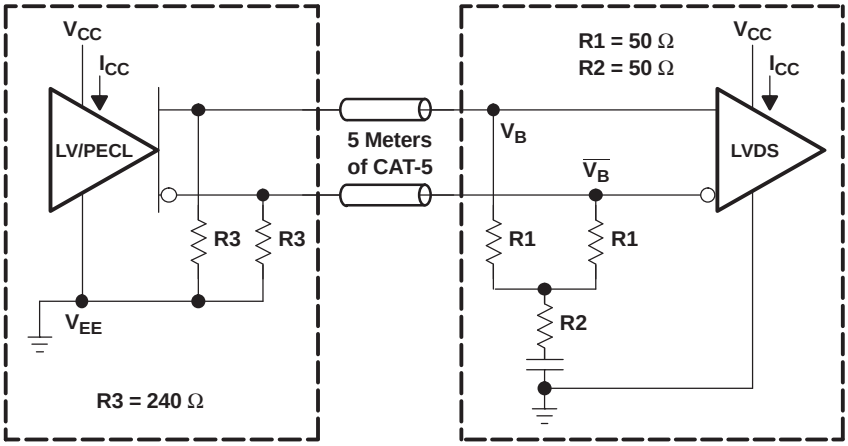


Figure 14. LVPECL or PECL to Remote Wide Common-Mode LVDS Receiver

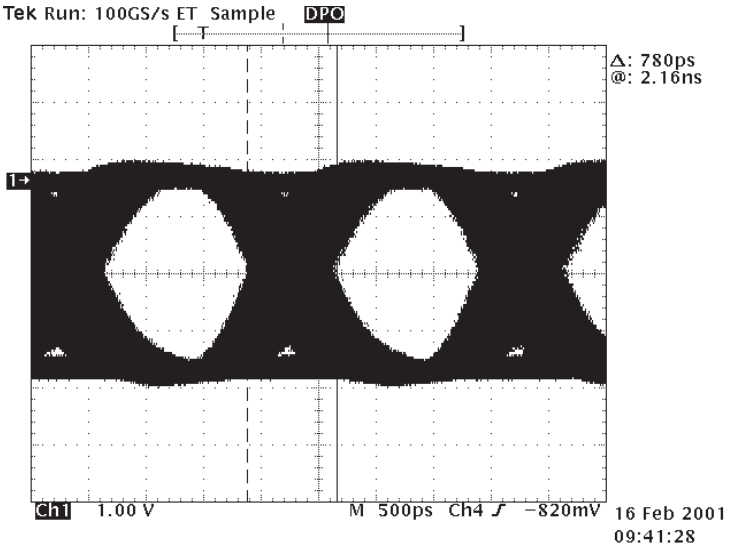


Figure 15. LV/PECL to Remote SN65LVDS33 at 500 Mbps Receiver Output (CH1)

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TEST CONDITIONS

- V_{CC} = 3.3 V
- T_A = 25°C (ambient temperature)
- All four channels switching simultaneously with NRZ data. The scope is pulse-triggered simultaneously with NRZ data.

EQUIPMENT

- Tektronix PS25216 programmable power supply
- Tektronix HFS 9003 stimulus system
- Tektronix TDS 784D 4-channel digital phosphor oscilloscope – DPO

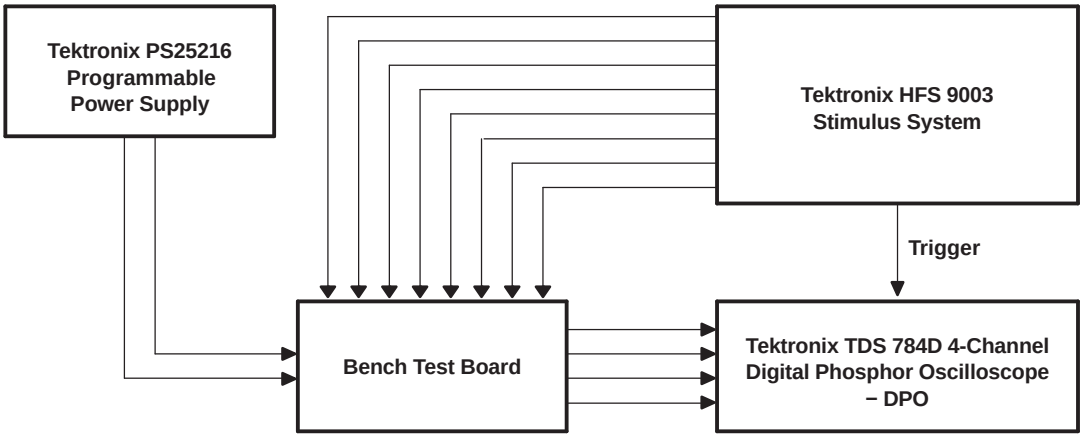
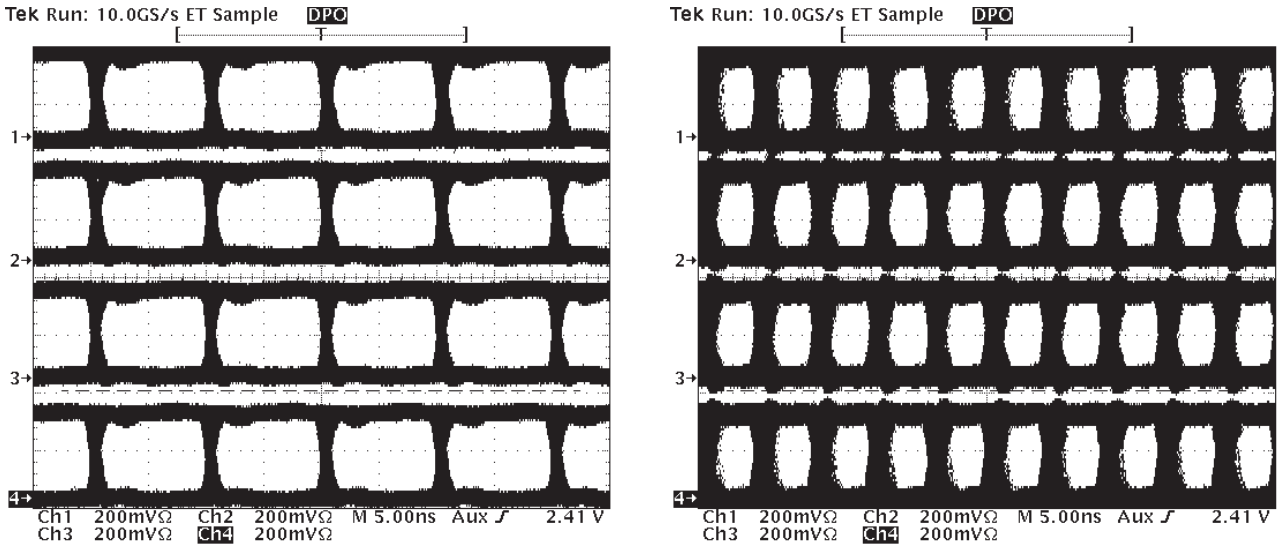


Figure 16. Equipment Setup



100 Mbit/s **200 Mbit/s**

Figure 17. Typical Eye Pattern SN65LVDS33

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REVISION HISTORY

This errata revision history highlights the technical changes made to the SGLS393 device specific errata to create the SGLS393C revision.

Changes from Revision B (February, 2012) to Revision C **Page**

- Deleted Evaluating the LVDS EVM (SLLA033) bullet in Related Information section 13

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-0724801VFA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-0724801VF A SNV55LVDS33W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

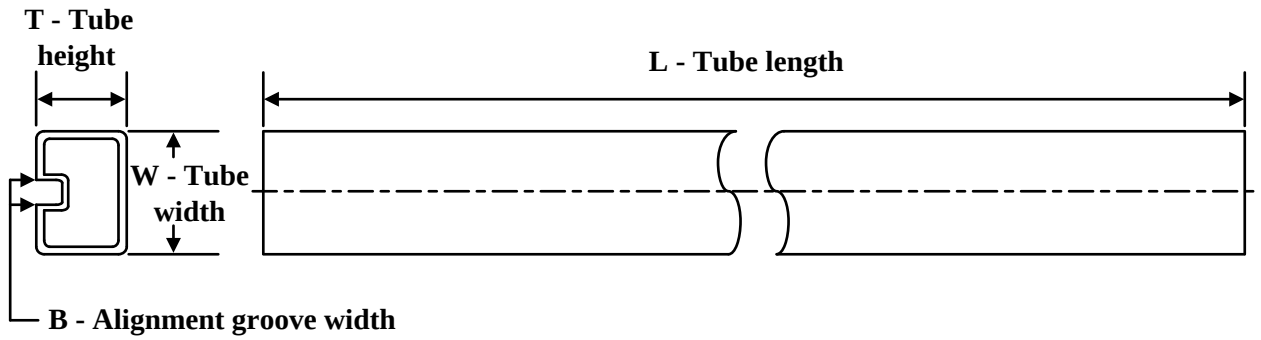
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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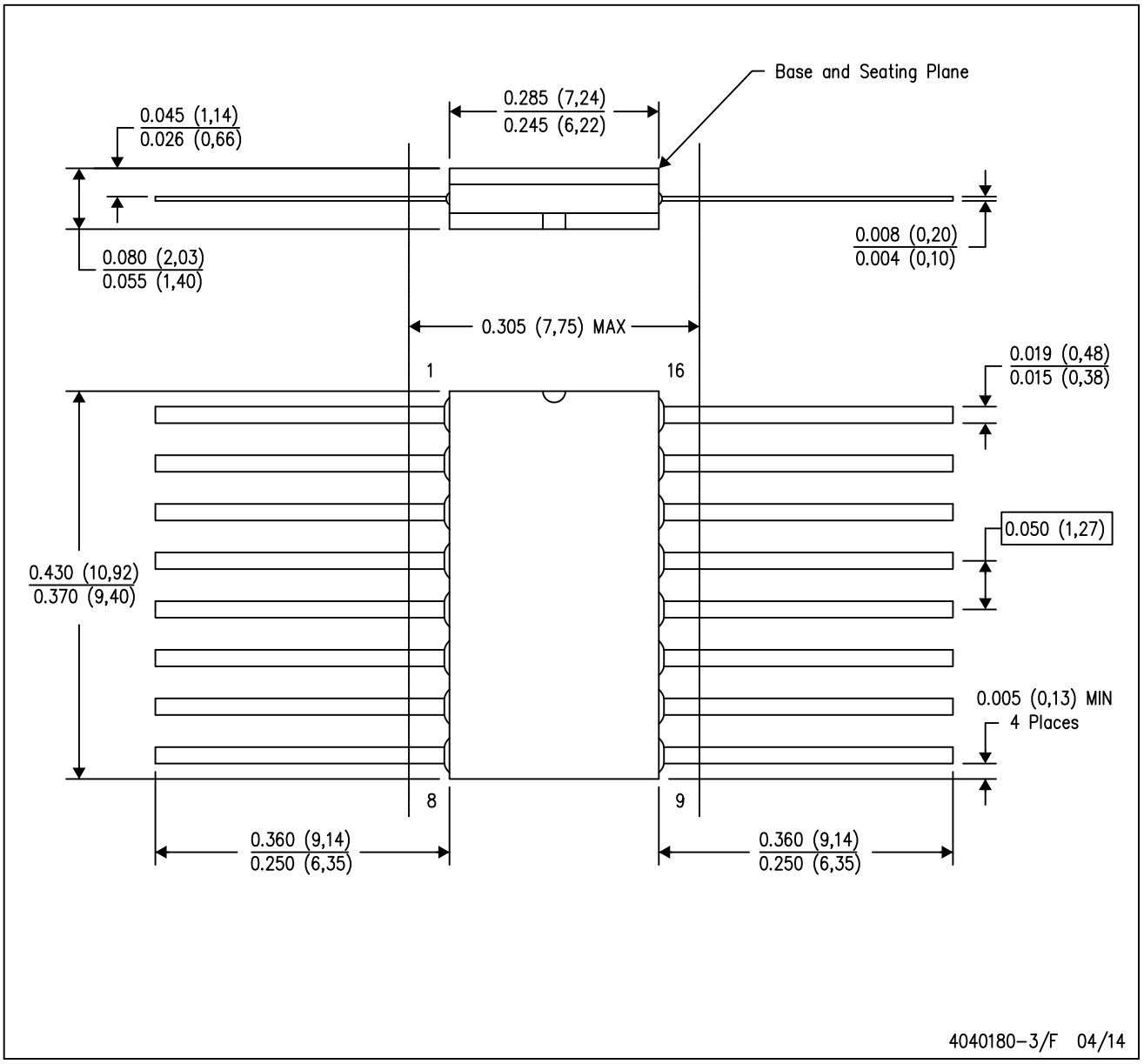
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-0724801VFA	W	CFP	16	25	506.98	26.16	6220	NA

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

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