

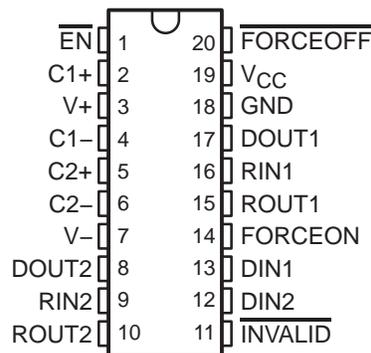
SN65C3223, SN75C3223

3-V TO 5.5-V MULTICHANNEL RS-232 COMPATIBLE LINE DRIVER/RECEIVER

SLLS538B – JUNE 2002 – REVISED OCTOBER 2004

- Operate With 3-V to 5.5-V V_{CC} Supply
- Operate Up To 1 Mbit/s
- Low Standby Current . . . 1 μ A Typ
- External Capacitors . . . $4 \times 0.1 \mu$ F
- Accept 5-V Logic Input With 3.3-V Supply
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- RS-232 Bus-Pin ESD Protection Exceeds ± 15 kV Using Human-Body Model (HBM)
- Applications
 - Battery-Powered Systems, PDAs, Notebooks, Laptops, Palmtop PCs, and Hand-Held Equipment

DB, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN65C3223 and SN75C3223 consist of two line drivers, two line receivers, and a dual charge-pump circuit with ± 15 -kV ESD protection pin to pin (serial-port connection pins, including GND). The devices provide the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 1 Mbit/s and a driver output slew rate of 24 V/ μ s to 150 V/ μ s

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If FORCEOFF is set low and EN is high, both drivers and receivers are shut off, and the supply current is reduced to 1 μ A. Disconnecting the serial port or turning off the peripheral drivers causes auto-powerdown to occur. Auto-powerdown can be disabled when FORCEON and FORCEOFF are high. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The INVALID output is used to notify the user if an RS-232 signal is present at any receiver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than -2.7 V or has been between -0.3 V and 0.3 V for less than 30 μ s. INVALID is low (invalid data) if the receiver input voltage is between -0.3 V and 0.3 V for more than 30 μ s. Refer to Figure 4 for receiver input levels.

ORDERING INFORMATION

T _A	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
0°C to 70°C	SOIC – DW	Tube of 25	SN75C3223DW	
		Reel of 2000	SN75C3223DWR	
	SSOP – DB	Reel of 2000	SN75C3223DBR	75C3223
		TSSOP – PW	Tube of 70	SN75C3223PW
-40°C to 85°C	SOIC – DW	Tube of 25	SN65C3223DW	
		Reel of 2000	SN65C3223DWR	
	SSOP – DB	Reel of 2000	SN65C3223DBR	65C3223
		TSSOP – PW	Tube of 70	SN65C3223PW
	TSSOP – PW	Reel of 2000	SN65C3223PWR	CA3223
		Reel of 2000	SN65C3223PWR	CB3223

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SN65C3223, SN75C3223 3-V TO 5.5-V MULTICHANNEL RS-232 COMPATIBLE LINE DRIVER/RECEIVER

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Function Tables

EACH DRIVER

INPUTS				OUTPUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

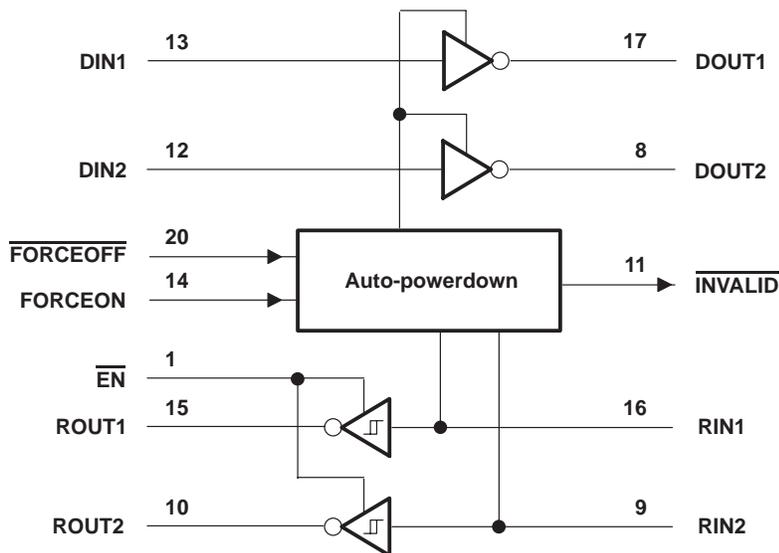
H = high level, L = low level, X = irrelevant, Z = high impedance

EACH RECEIVER

INPUTS			OUTPUT ROUT
RIN	EN	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	–0.3 V to 6 V
Positive output supply voltage range, $V+$ (see Note 1)	–0.3 V to 7 V
Negative output supply voltage range, $V-$ (see Note 1)	0.3 V to –7 V
Supply voltage difference, $V+ - V-$ (see Note 1)	13 V
Input voltage range, V_I : Driver, $\overline{FORCEOFF}$, FORCEON, \overline{EN}	–0.3 V to 6 V
Receiver	–25 V to 25 V
Output voltage range, V_O : Driver	–13.2 V to 13.2 V
Receiver, $\overline{INVALID}$	–0.3 V to $V_{CC} + 0.3$ V
Package thermal impedance, θ_{JA} (see Notes 2 and 3): DB package	70°C/W
DW package	58°C/W
PW package	83°C/W
Operating virtual junction temperature, T_J	150°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to network GND.
 2. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4 and Figure 6)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	$V_{CC} = 3.3$ V	3	3.3	3.6	V
		$V_{CC} = 5$ V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	$DIN, \overline{EN}, \overline{FORCEOFF},$ FORCEON	$V_{CC} = 3.3$ V		2	V
			$V_{CC} = 5$ V		2.4	
V_{IL}	Driver and control low-level input voltage	$DIN, \overline{EN}, \overline{FORCEOFF},$ FORCEON			0.8	V
V_I	Driver and control input voltage	$DIN, \overline{EN}, \overline{FORCEOFF},$ FORCEON			0	V
	Receiver input voltage				–25	
T_A	Operating free-air temperature	SN65C3223	–40			85
		SN65C3223	0			70

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at $V_{CC} = 3.3$ V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at $V_{CC} = 5$ V \pm 0.5 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_I	Input leakage current	$\overline{EN}, \overline{FORCEOFF},$ FORCEON			± 0.01	μ A
I_{CC}	Supply current	Auto-powerdown disabled	No load, $\overline{FORCEOFF},$ FORCEON at V_{CC}		0.3	1
		Powered off	No load, $\overline{FORCEOFF}$ at GND		1	10
		Auto-powerdown enabled	No load, $\overline{FORCEOFF}$ at V_{CC} , FORCEON at GND, All RIN are open or grounded		1	10

‡ All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25^\circ$ C.

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at $V_{CC} = 3.3$ V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at $V_{CC} = 5$ V \pm 0.5 V.



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DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OH}	High-level output voltage	DOUT at R _L = 3 kΩ to GND	5	5.4		V
V _{OL}	Low-level output voltage	DOUT at R _L = 3 kΩ to GND	-5	-5.4		V
I _{IH}	High-level input current	V _I = V _{CC}		±0.01	±1	μA
I _{IL}	Low-level input current	V _I at GND		±0.01	±1	μA
I _{OS}	Short-circuit output current‡	V _{CC} = 3.6 V, V _O = 0 V		±35	±60	mA
		V _{CC} = 5.5 V, V _O = 0 V		±35	±90	
r _o	Output resistance	V _{CC} , V+, and V- = 0 V, V _O = ±2 V	300	10M		Ω
I _{off}	Output leakage current	FORCEOFF = GND	V _O = ±12 V, V _{CC} = 3 V to 3.6 V		±25	μA
			V _O = ±10 V, V _{CC} = 4.5 V to 5.5 V		±25	

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

‡ Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Maximum data rate (see Figure 1)	R _L = 3 kΩ, One DOUT switching	C _L = 1000 pF		250		kbit/s
		C _L = 250 pF, V _{CC} = 3 V to 4.5 V		1000		
		C _L = 1000 pF, V _{CC} = 4.5 V to 5.5 V		1000		
t _{sk(p)}	Pulse skew§	C _L = 150 pF to 2500 pF, R _L = 3 kΩ to 7 kΩ, See Figure 2		300		ns
SR(tr)	Slew rate, transition region (see Figure 1)	V _{CC} = 3.3 V, R _L = 3 kΩ to 7 kΩ		18	150	V/μs

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

§ Pulse skew is defined as |t_{pLH} - t_{pHL}| of each channel of the same device.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.



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RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1 mA	V _{CC} - 0.6	V _{CC} - 0.1		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.6	2.4	V
		V _{CC} = 5 V		1.9	2.4	
V _{IT-}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.1		V
		V _{CC} = 5 V	0.8	1.4		
V _{hys}	Input hysteresis (V _{IT+} - V _{IT-})			0.5		V
I _{off}	Output leakage current	$\overline{\text{EN}} = V_{\text{CC}}$		±0.05	±10	µA
r _i	Input resistance	V _I = ±3 V to ±25 V	3	5	7	kΩ

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

NOTE 4: Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF,	See Figure 3		150		ns
t _{PHL}	Propagation delay time, high- to low-level output	C _L = 150 pF,	See Figure 3		150		ns
t _{en}	Output enable time	C _L = 150 pF, See Figure 4	R _L = 3 kΩ,		200		ns
t _{dis}	Output disable time	C _L = 150 pF, See Figure 4	R _L = 3 kΩ,		200		ns
t _{sk(p)}	Pulse skew‡	See Figure 3			50		ns

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

‡ Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

NOTE 4: Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.



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AUTO-POWERDOWN SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

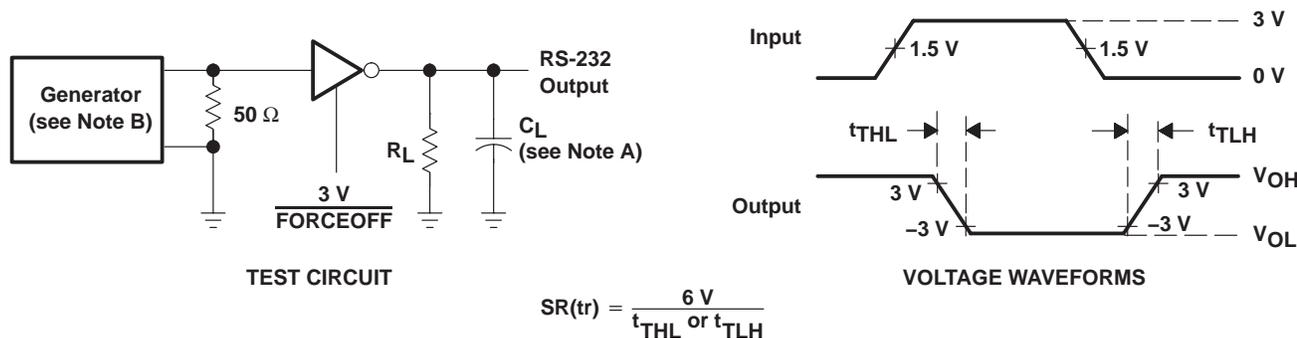
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{T+}(\text{valid})$	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$		2.7	V
$V_{T-}(\text{valid})$	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$	-2.7		V
$V_{T}(\text{invalid})$	Receiver input threshold for INVALID low-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$	-0.3	0.3	V
V_{OH}	INVALID high-level output voltage	$I_{OH} = -1 \text{ mA}$, $\overline{\text{FORCEOFF}} = V_{CC}$	$V_{CC} - 0.6$		V
V_{OL}	INVALID low-level output voltage	$I_{OL} = 1.6 \text{ mA}$, $\overline{\text{FORCEOFF}} = V_{CC}$		0.4	V

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		TYPT†	UNIT
t_{valid}	Propagation delay time, low- to high-level output	1	μs
t_{invalid}	Propagation delay time, high- to low-level output	30	μs
t_{en}	Supply enable time	100	μs

† All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

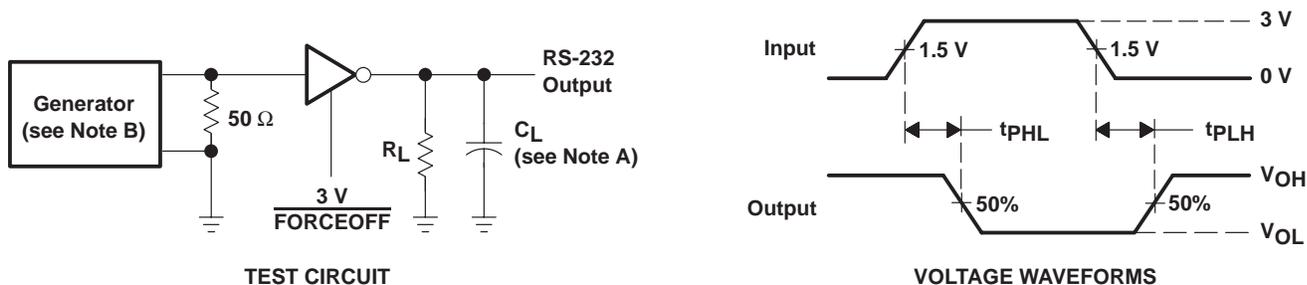
Figure 1. Driver Slew Rate

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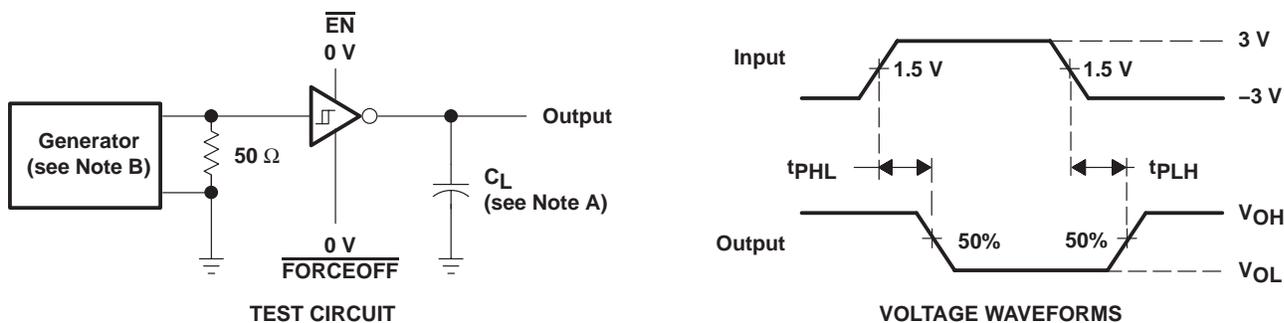
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PARAMETER MEASUREMENT INFORMATION



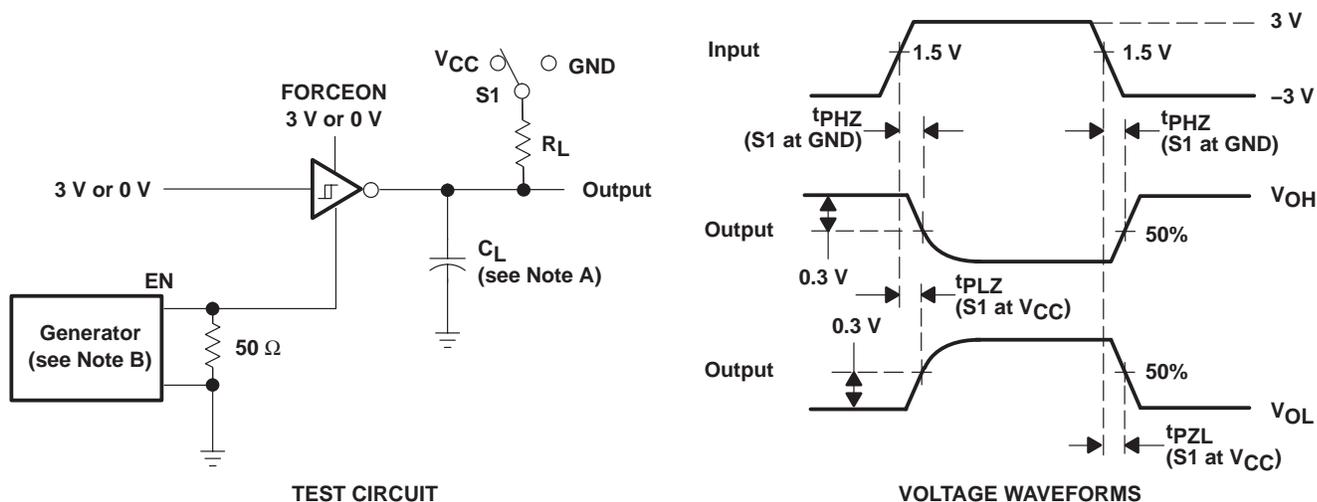
NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 2. Driver Pulse Skew



NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 3. Receiver Propagation Delay Times



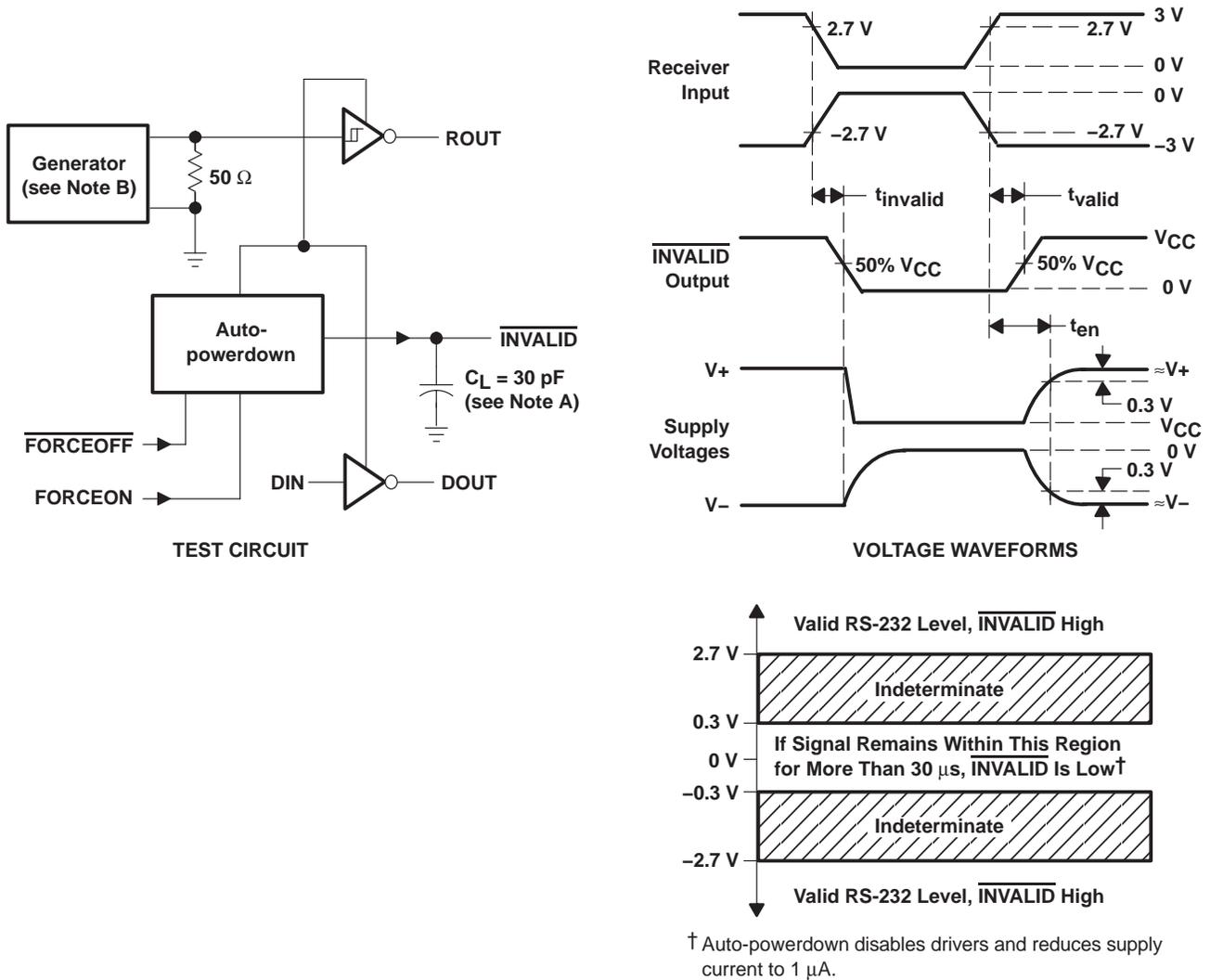
NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 4. Receiver Enable and Disable Times

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, $Z_0 = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

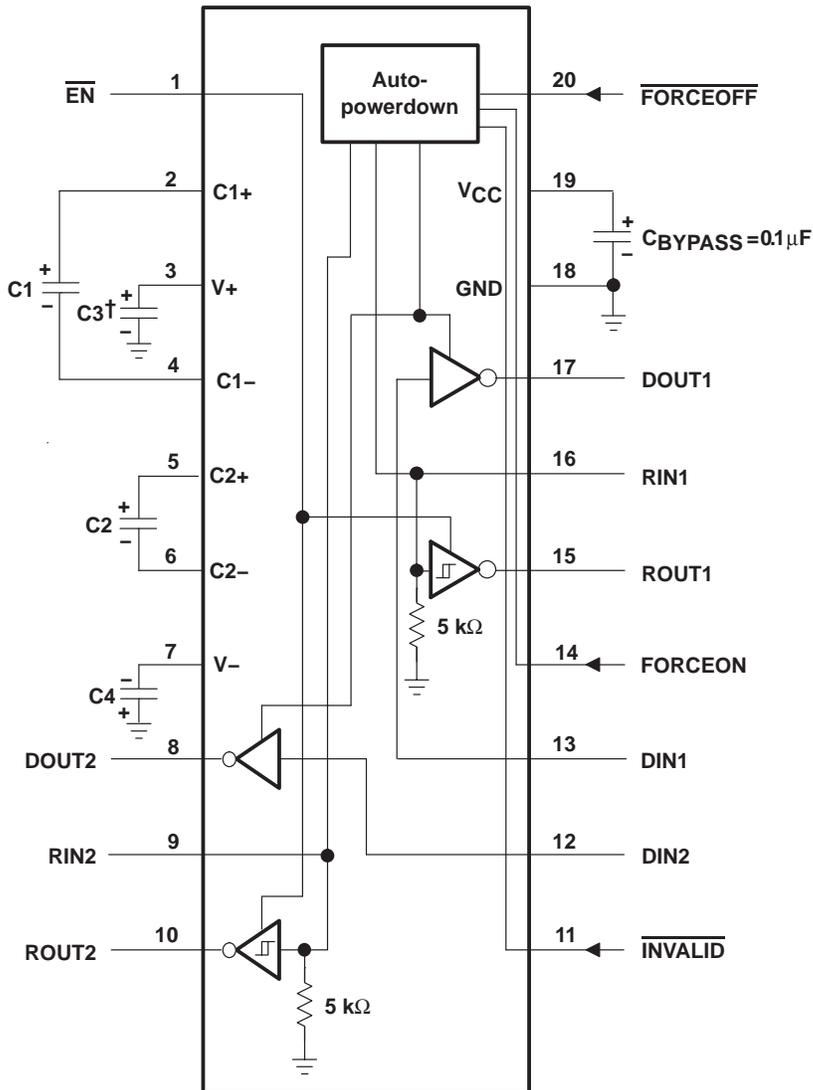
Figure 5. $\overline{\text{INVALID}}$ Propagation Delay Times and Supply Enabling Time

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APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.
NOTE A: Resistor values shown are nominal.

V_{CC} vs CAPACITOR VALUES

V _{CC}	C1	C2, C3, C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

Figure 6. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65C3223DBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3223
SN65C3223DBR.A	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3223
SN65C3223DW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3223
SN65C3223DW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3223
SN65C3223PW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 85	CB3223
SN65C3223PWR	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 85	CB3223
SN75C3223DBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3223
SN75C3223DBR.A	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3223
SN75C3223DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3223
SN75C3223DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3223
SN75C3223PW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	0 to 70	CA3223
SN75C3223PWR	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	0 to 70	CA3223

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

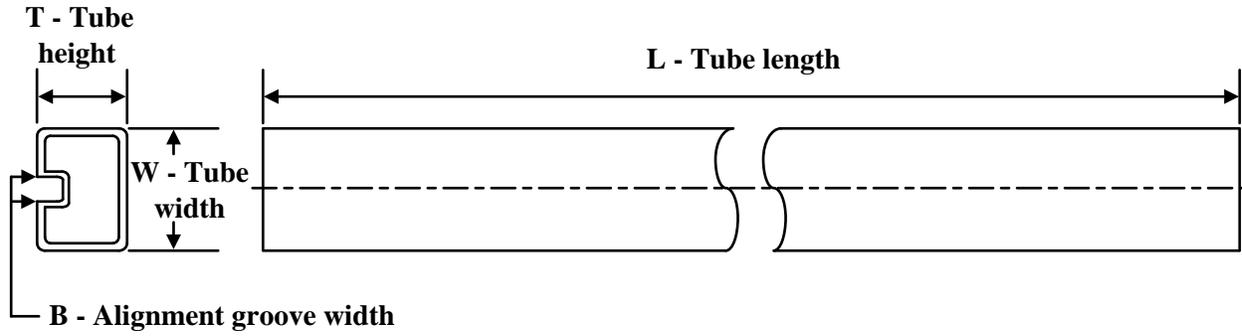

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C3223DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN75C3223DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN75C3223DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C3223DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN75C3223DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN75C3223DWR	SOIC	DW	20	2000	356.0	356.0	45.0

TUBE


*All dimensions are nominal

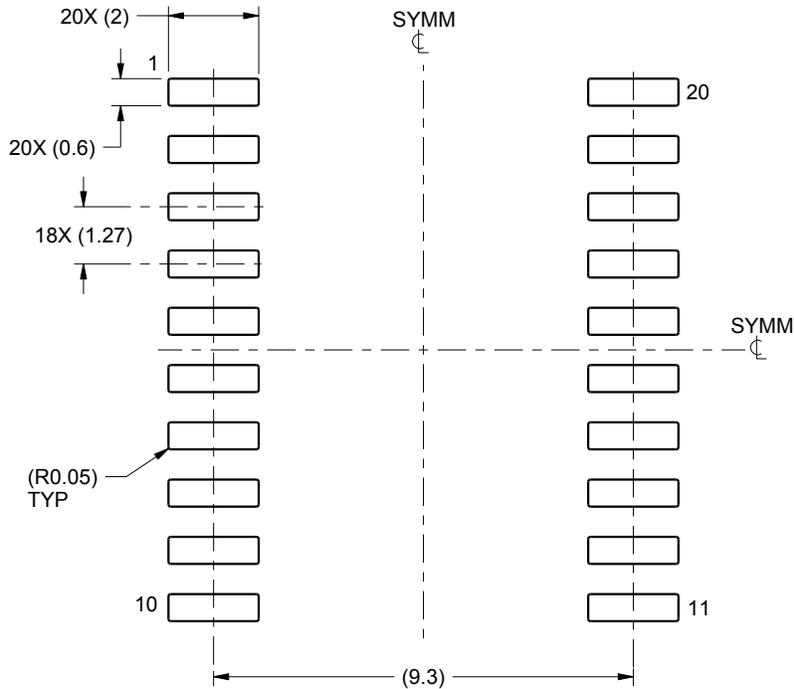
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65C3223DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN65C3223DW.A	DW	SOIC	20	25	507	12.83	5080	6.6

EXAMPLE BOARD LAYOUT

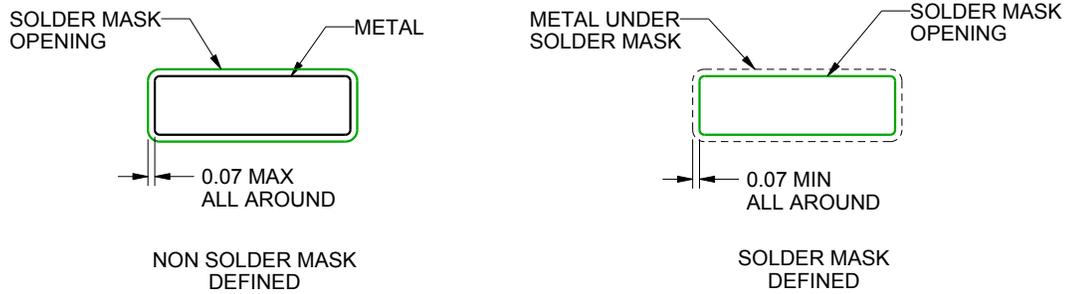
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

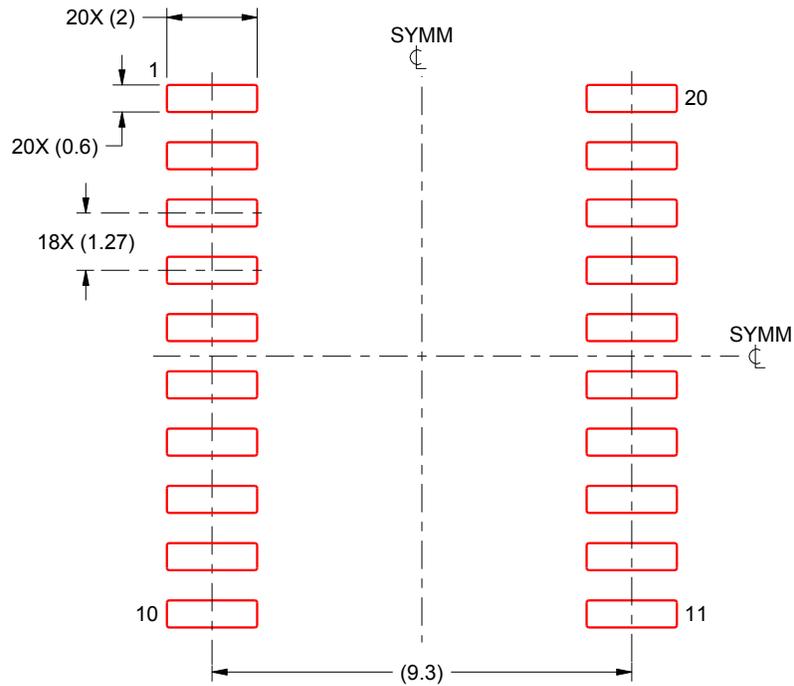
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

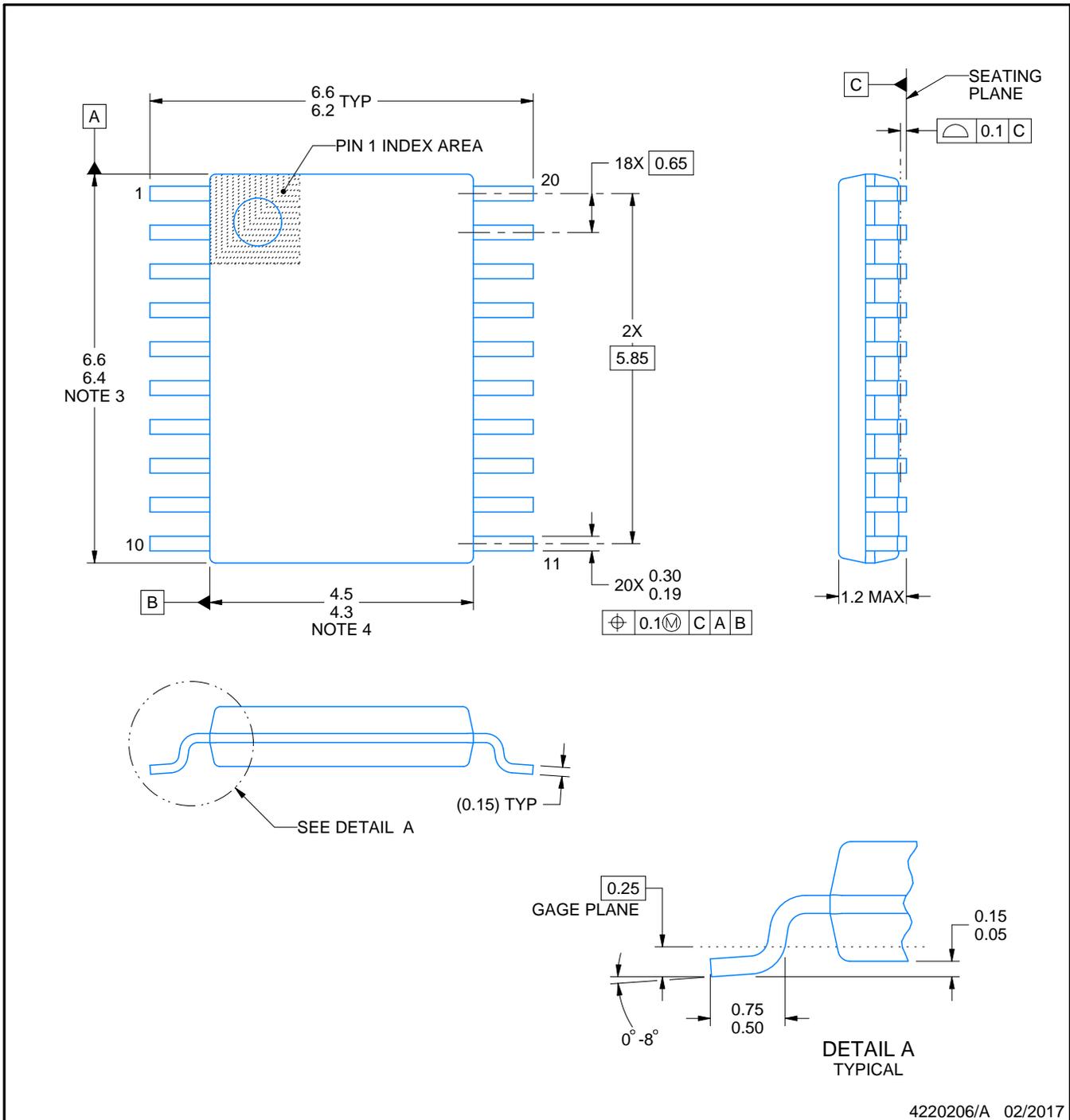
PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

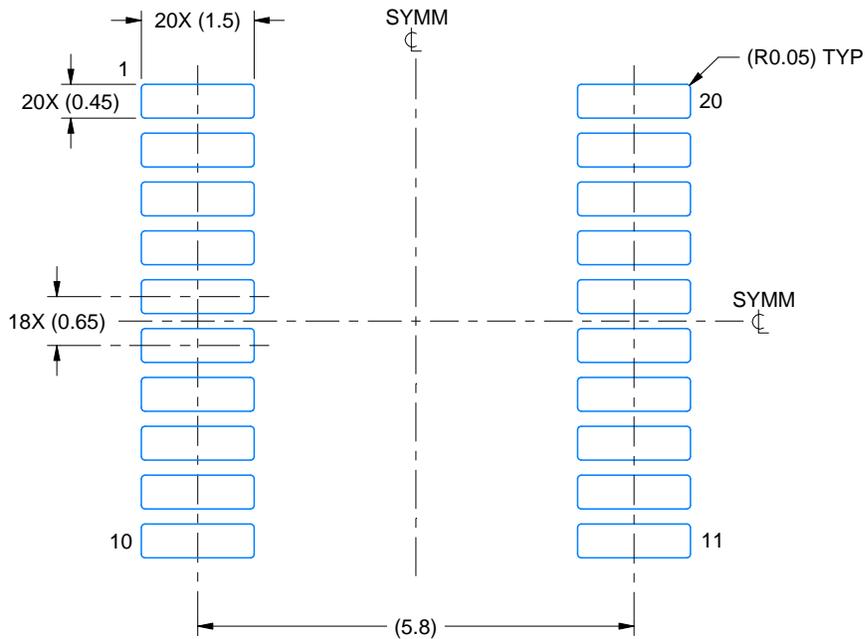
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

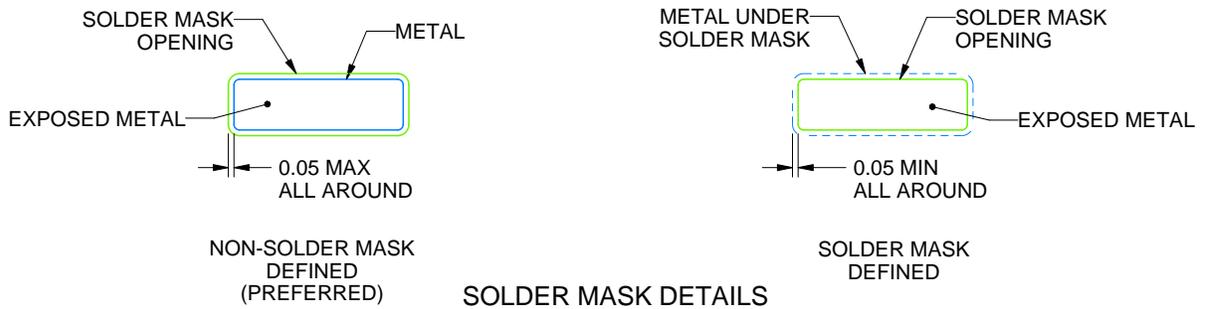
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

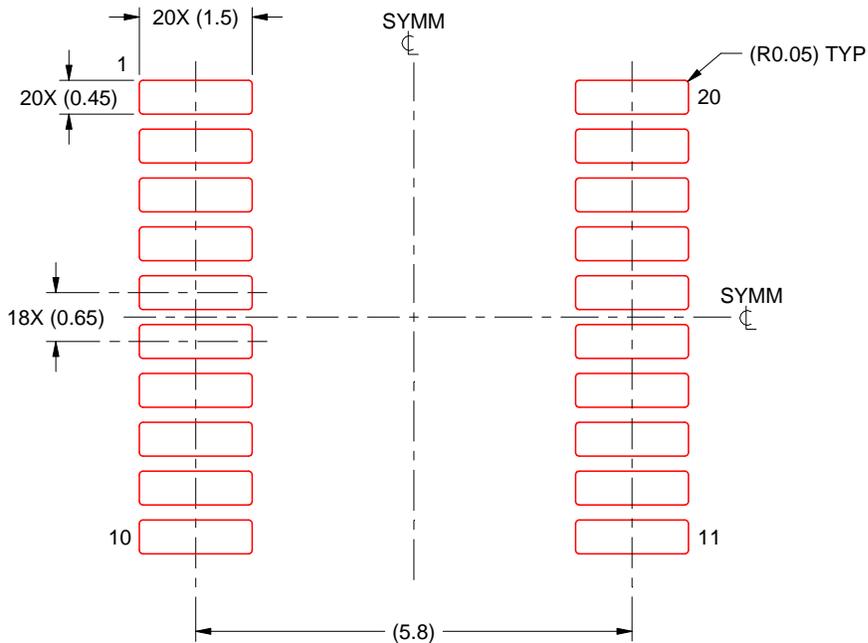
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

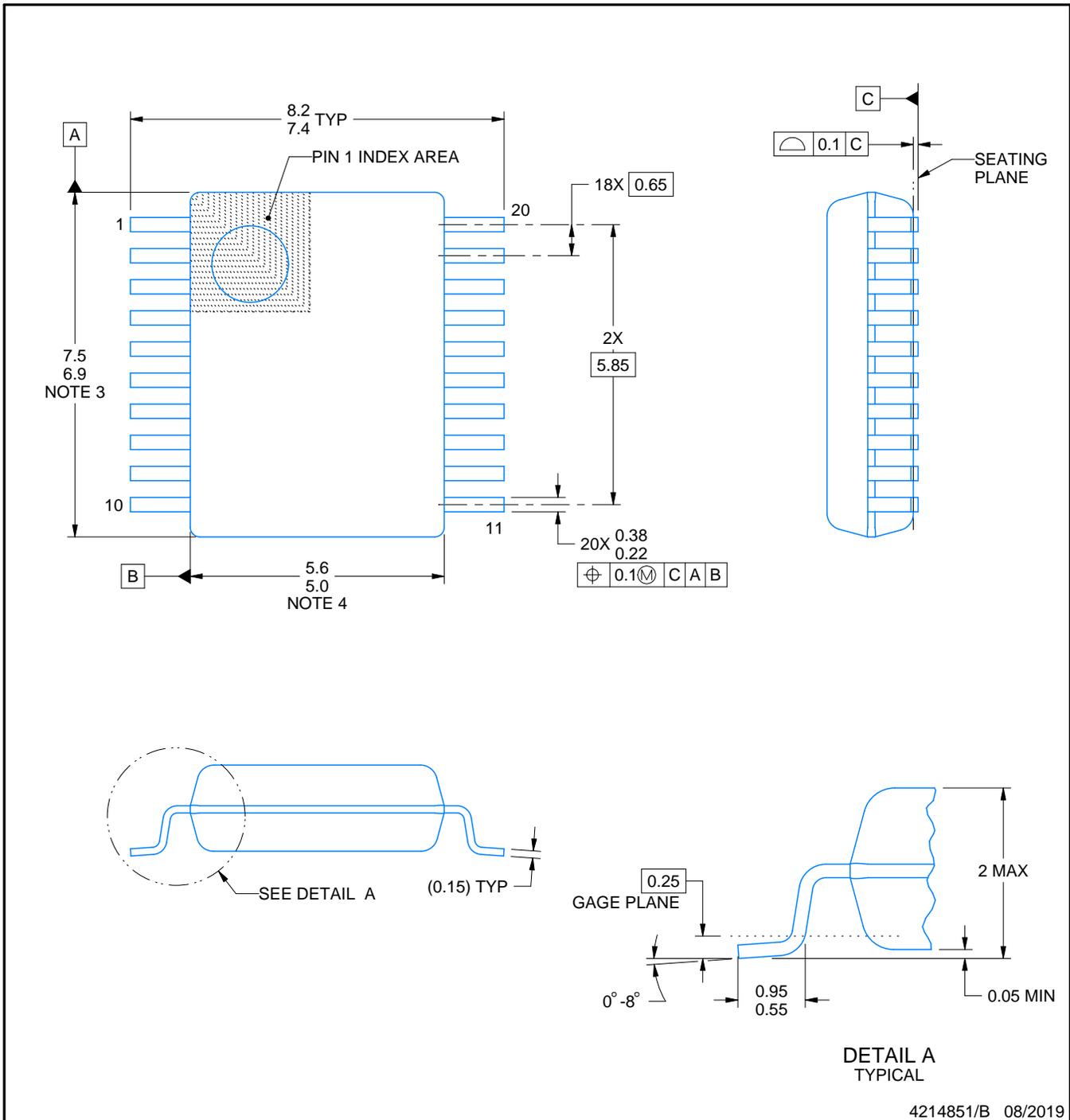
DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

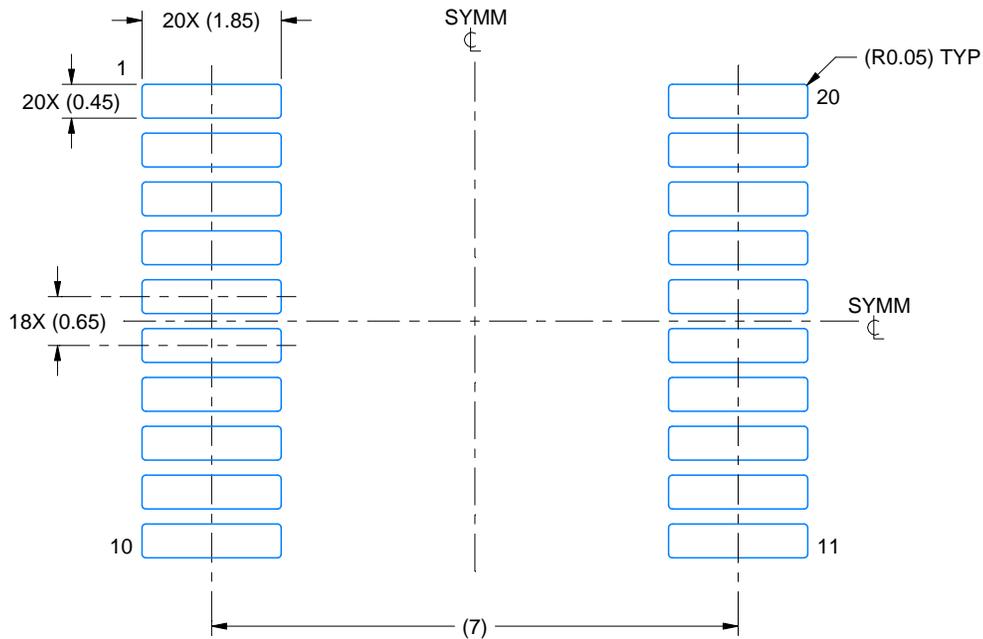
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

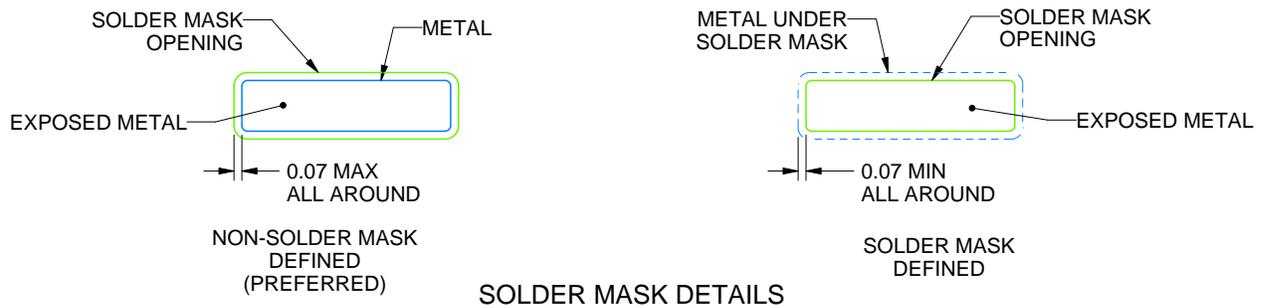
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

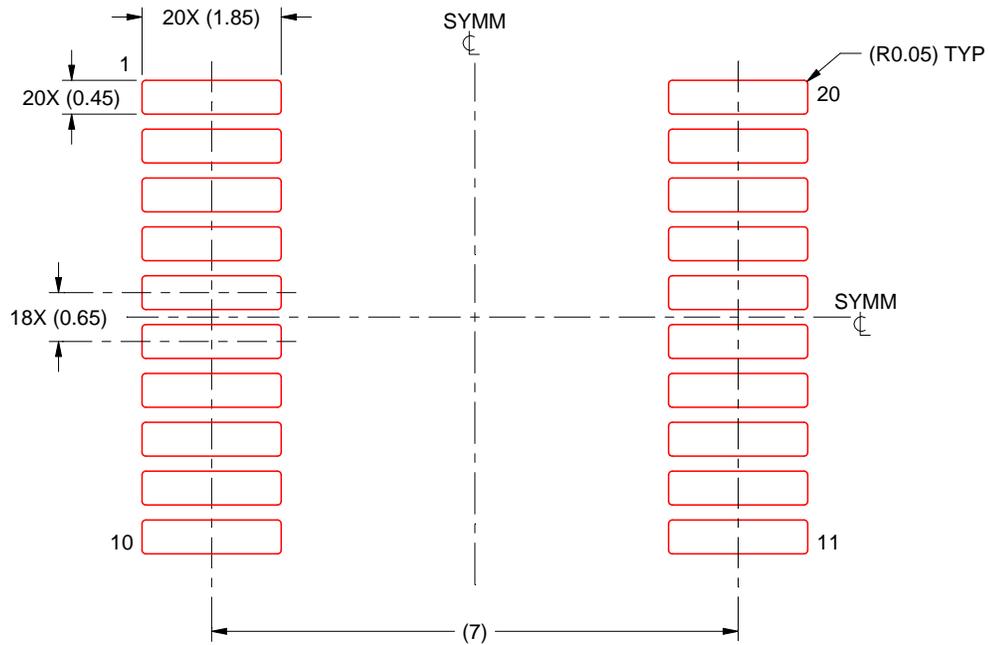
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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