

SNx5C3243 3-V To 5.5-V Multichannel RS-232 Compatible Line Driver and Receiver

1 Features

- Operates With 3-V to 5.5-V V_{CC} Supply
- Always-Active Noninverting Receiver Output (ROUT2B)
- Low Standby Current: 1 μ A Typical
- External Capacitors: $4 \times 0.1 \mu$ F
- Accepts 5-V Logic Input With 3.3-V Supply
- Inter-Operable With SN65C3238, SN75C3238
- Supports Operation From 250 kbit/s to 1 Mbit/s
- RS-232 Bus-Pin ESD Protection Exceeds ± 15 kV Using Human-Body Model (HBM)

2 Applications

- [Battery-powered systems](#)
- [Personel electronics](#)
- [Notebooks](#)
- [Laptops](#)
- [Palmtop PCs](#)
- [Hand-held equipment](#)

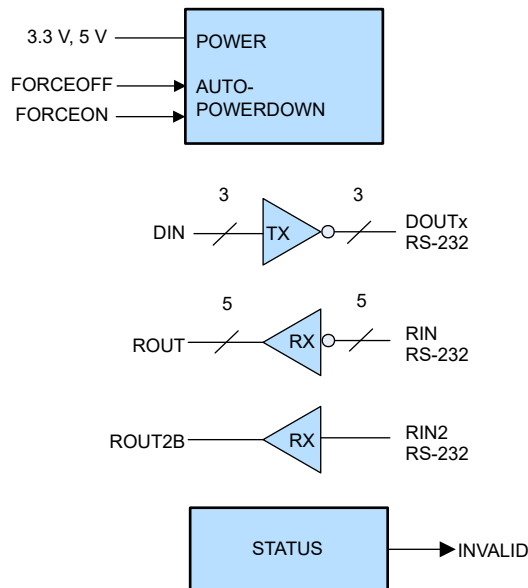
3 Description

The SN65C3243 and SN75C3243 consist of three line drivers, five line receivers, and a dual charge-pump circuit with ± 15 -kV ESD protection pin to pin (serial-port connection pins, including GND). This device provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. In addition, this device includes an always-active noninverting output (ROUT2B), which allows applications using the ring indicator to transmit data while the device is powered down. The device operates at data signaling rates up to 1 Mbit/s and an increased slew-rate range of 24 V/ μ s to 150 V/ μ s.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
SN65C3243 SN75C3243	SSOP (DB)	10.2 mm x 5.30 mm
	SOIC (DW)	17.9 mm x 7.50 mm
	TSSOP (PW)	9.70 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Circuit



Table of Contents

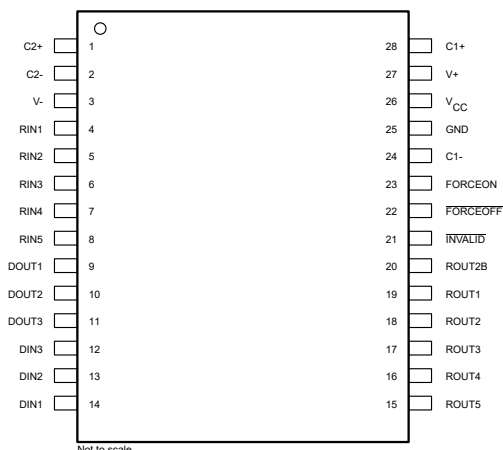
1 Features	1	6.10 Switching Characteristics: Receiver.....	7
2 Applications	1	6.11 Switching Characteristics: Auto-Powerdown.....	7
3 Description	1	7 Parameter Measurement Information	8
4 Revision History	2	8 Detailed Description	11
5 Pin Configuration and Functions	3	8.1 Overview.....	11
6 Specifications	4	8.2 Device Functional Modes.....	11
6.1 Absolute Maximum Ratings.....	4	9 Device and Documentation Support	13
6.2 ESD Ratings.....	4	9.1 Device Support.....	13
6.3 Recommended Operating Conditions.....	4	9.2 Receiving Notification of Documentation Updates....	13
6.4 Thermal Information.....	5	9.3 Support Resources.....	13
6.5 Electrical Characteristics.....	5	9.4 Trademarks.....	13
6.6 Electrical Characteristics, Driver Section.....	5	9.5 Electrostatic Discharge Caution.....	13
6.7 Electrical Characteristics, Receiver Section.....	6	9.6 Glossary.....	13
6.8 Electrical Characteristics, Auto-Powerdown Section.....	6	10 Mechanical, Packaging, and Orderable Information	13
6.9 Switching Characteristics: Driver.....	7		

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (September 2008) to Revision I (October 2022)	Page
• Added the <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Detailed Description</i> section, <i>Device and Documentation Support</i> , and <i>Mechanical, Packaging, and Orderable Information</i> sections.....	1
• Changed the I_{CC} Supply current auto-powerdown disabled MAX value from 1 mA to 1.2 mA in the <i>Electrical Characteristics</i>	5

5 Pin Configuration and Functions



**Figure 5-1. DB, DW, or PW Package, 28 Pin (SSOP, SOIC, TSSOP)
(Top View)**

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	C2+	—	Positive terminal of the voltage-doubler charge-pump capacitor
2	C2-	—	Negative terminal of the voltage-doubler charge-pump capacitor
3	V-	—	Negative charge pump output voltage
4	RIN1	I	RS-232 receiver inputs
5	RIN2		
6	RIN3		
7	RIN4		
8	RIN5		
9	DOUT1	O	RS-232 driver outputs
10	DOUT2		
11	DOUT3		
12	DIN3	I	Driver inputs
13	DIN2		
14	DIN1		
15	ROUT5	O	Receiver outputs
16	ROUT4		
17	ROUT3		
18	ROUT2		
19	ROUT1		
20	ROUT2B	—	Always-active noninverting receiver output;
21	INVALID	O	Invalid Output Pin
22	FORCEOFF	I	Auto Powerdown Control input (Refer to Truth Table)
23	FORCEON	I	Auto Powerdown Control input (Refer to Truth Table)
24	C1-	—	Negative terminal of the voltage-doubler charge-pump capacitor
25	GND	—	Ground
26	V _{CC}	—	3-V to 5.5-V supply voltage
27	V+	—	Positive charge pump output voltage
28	C1+	—	Positive terminal of the voltage-doubler charge-pump capacitor

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾		–0.3	6	V
V ₊	Positive-output supply voltage range ⁽²⁾		–0.3	7	V
V _–	Negative-output supply voltage range ⁽²⁾		0.3	–7	V
V ₊ – V _–	Supply voltage difference ⁽²⁾			13	V
V _I	Input voltage range	Driver (FORCEOFF, FORCEON)	–0.3	6	V
		Receiver	–25	25	
V _O	Output voltage range	Driver	–13.2	13.2	V
T _J	Operating virtual junction temperature			150	°C
T _{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network GND.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 on RS-232 bus pins DOUT1/2/3, RIN1/2/3/4/5 ⁽¹⁾	±15	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. .

6.3 Recommended Operating Conditions

see Figure 7-6 ⁽¹⁾

			MIN	NOM	MAX	UNIT
Supply voltage		V _{CC} = 3.3 V	3	3.3	3.6	V
		V _{CC} = 5 V	4.5	5	5.5	
V _{IH}	Driver and control high-level input voltage	DIN, FORCEOFF, FORCEON	V _{CC} = 3.3 V	2		V
			V _{CC} = 5 V	2.4		
V _{IL}	Driver and control low-level input voltage	DIN, FORCEOFF, FORCEON			0.8	V
V _I	Driver and control input voltage	DIN, FORCEOFF, FORCEON	0		5.5	V
V _I	Receiver input voltage		–25		25	V
T _A	Operating free-air temperature	SN65C3243	–40		85	°C
		SN75C3243	0		70	

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DB (SSOP)	DW (SOIC)	PW (TSSOP)	UNIT
		28 PINS	28 PINS	28 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	76.1	59.0	70.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	35.8	28.8	21.0	°C/W
R _{θJB}	Junction-to-board thermal resistance	37.4	30.3	29.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	7.4	7.8	1.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	37.0	30.0	28.8	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 7-6](#)) ⁽²⁾

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
I _I	Input leakage current	FORCEOFF, FORCEON		±0.01	±1	μA
I _{CC}	Supply current	Auto-powerdown disabled	No load, FORCEOFF and FORCEON = V _{CC} For DB and PW package	0.3	1.2	mA
		Auto-powerdown disabled	No load, FORCEOFF and FORCEON = V _{CC} For DW package	0.3	1	mA
		Powered off	No load, FORCEOFF = GND	1	10	μA
		Auto-powerdown enabled	No load, FORCEOFF = V _{CC} , FORCEON = GND, All RIN are open or grounded, All DIN are grounded	1	10	

- (1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

- (2) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.6 Electrical Characteristics, Driver Section

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 7-6](#))

PARAMETER	TEST CONDITIONS ⁽³⁾		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	All DOUT at R _L = 3 kΩ to GND	5	5.4		V
V _{OL}	Low-level output voltage	All DOUT at R _L = 3 kΩ to GND	–5	–5.4		V
V _O	Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V _{CC} , 3-kΩ to GND at DOUT3, DOUT1 = DOUT2 = 2.5 mA	±5			V
I _{IH}	High-level input current	V _I = V _{CC}		±0.01	±1	μA
I _{IL}	Low-level input current	V _I = GND		±0.01	±1	μA
I _{OS}	Short-circuit output current ⁽²⁾	V _{CC} = 3.6 V, V _O = 0 V		±35	±60	mA
		V _{CC} = 5.5 V, V _O = 0 V		±35	±90	
r _o	Output resistance	V _{CC} , V+, and V– = 0 V, V _O = ±2 V	300	10M		Ω
I _{off}	Output leakage current	FORCEOFF = GND	V _O = ±12 V, V _{CC} = 3 V to 3.6 V		±25	μA
			V _O = ±10 V, V _{CC} = 4.5 V to 5.5 V		±25	

- (1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

- (2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

- (3) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.7 Electrical Characteristics, Receiver Section

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 7-6](#))

PARAMETER	TEST CONDITIONS ⁽²⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = –1 mA	V _{CC} – 0.6	V _{CC} – 0.1	V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA		0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V	1.6	2.4	V
		V _{CC} = 5 V	1.9	2.4	
V _{IT–}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.1	V
		V _{CC} = 5 V	0.8	1.4	
V _{hys}	Input hysteresis (V _{IT+} – V _{IT–})		0.5		V
I _{off}	Output leakage current (except ROUT2B)	FORCEOFF = 0 V	±0.05	±10	μA
r _i	Input resistance	V _I = ±3 V to ±25 V	3	5	7 kΩ

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.8 Electrical Characteristics, Auto-Powerdown Section

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 7-5](#))

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V _{T+(valid)}	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}	2.7	V
V _{T–(valid)}	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}	–2.7	V
V _{T(invalid)}	Receiver input threshold for INVALID low-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}	–0.3	0.3 V
V _{OH}	INVALID high-level output voltage	I _{OH} = –1 mA, FORCEON = GND, FORCEOFF = V _{CC}	V _{CC} – 0.6	V
V _{OL}	INVALID low-level output voltage	I _{OL} = 1.6 mA, FORCEON = GND, FORCEOFF = V _{CC}	0.4	V

6.9 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 7-6](#))

PARAMETER	TEST CONDITIONS ⁽³⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
Maximum data rate (see Figure 7-1)	$R_L = 3\text{ k}\Omega$, One DOUT switching	$C_L = 1000\text{ pF}$	250		kbit/s
		$C_L = 250\text{ pF}$, $V_{CC} = 3\text{ V to }4.5\text{ V}$	1000		
		$C_L = 1000\text{ pF}$, $V_{CC} = 4.5\text{ V to }5.5\text{ V}$	1000		
$t_{sk(p)}$ Pulse skew ⁽²⁾	$C_L = 150\text{ pF to }2500\text{ pF}$, $R_L = 3\text{ k}\Omega\text{ to }7\text{ k}\Omega$, See Figure 7-2		25		ns
SR(tr) Slew rate, transition region (see Figure 7-1)	$C_L = 150\text{ pF to }1000\text{ pF}$, $R_L = 3\text{ k}\Omega\text{ to }7\text{ k}\Omega$, $V_{CC} = 3.3\text{ V}$		18	150	V/ μ s

- (1) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.
(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Test conditions are $C1\text{--}C4 = 0.1\text{ }\mu\text{F}$ at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; $C1 = 0.047\text{ }\mu\text{F}$, $C2\text{--}C4 = 0.33\text{ }\mu\text{F}$ at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

6.10 Switching Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽³⁾	TYP ⁽¹⁾	UNIT
t_{PLH} Propagation delay time, low- to high-level output	$C_L = 150\text{ pF}$, See Figure 7-3	150	ns
t_{PHL} Propagation delay time, high- to low-level output	$C_L = 150\text{ pF}$, See Figure 7-3	150	ns
t_{en} Output enable time	$C_L = 150\text{ pF}$, $R_L = 3\text{ k}\Omega$, See Figure 7-4	200	ns
t_{dis} Output disable time	$C_L = 150\text{ pF}$, $R_L = 3\text{ k}\Omega$, See Figure 7-4	200	ns
$t_{sk(p)}$ Pulse skew ⁽²⁾	See Figure 7-3	50	ns

- (1) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.
(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Test conditions are $C1\text{--}C4 = 0.1\text{ }\mu\text{F}$ at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; $C1 = 0.047\text{ }\mu\text{F}$, $C2\text{--}C4 = 0.33\text{ }\mu\text{F}$ at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

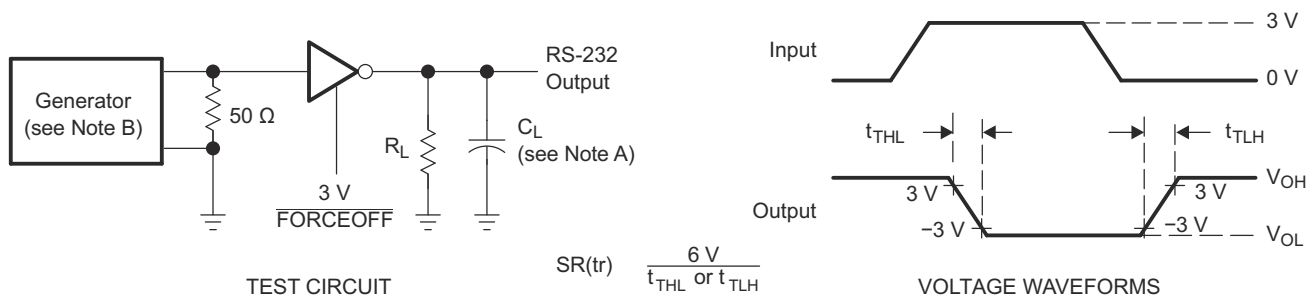
6.11 Switching Characteristics: Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 7-5](#))

PARAMETER	TYP ⁽¹⁾	UNIT
t_{valid} Propagation delay time, low- to high-level output	1	μ s
$t_{invalid}$ Propagation delay time, high- to low-level output	30	μ s
t_{en} Supply enable time	100	μ s

- (1) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

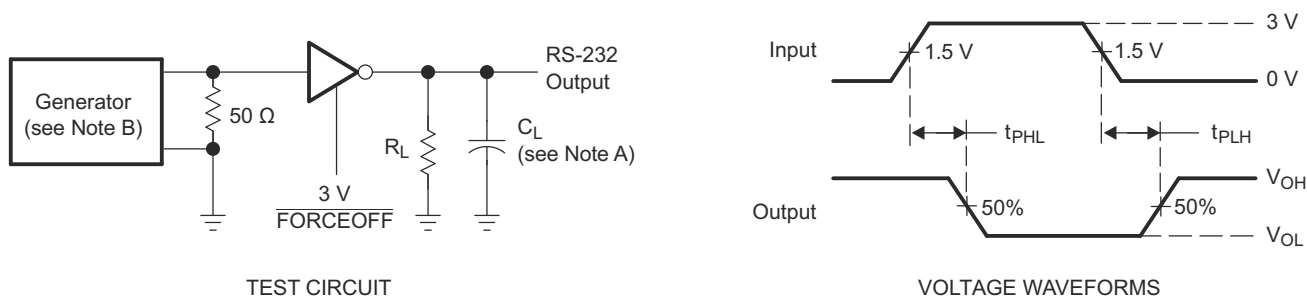
7 Parameter Measurement Information



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 1 Mbits, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

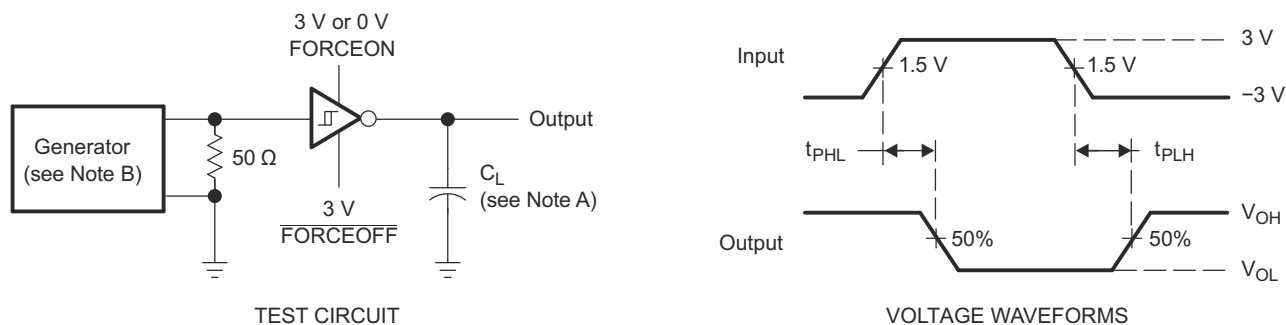
Figure 7-1. Driver Slew Rate



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 1 Mbits, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

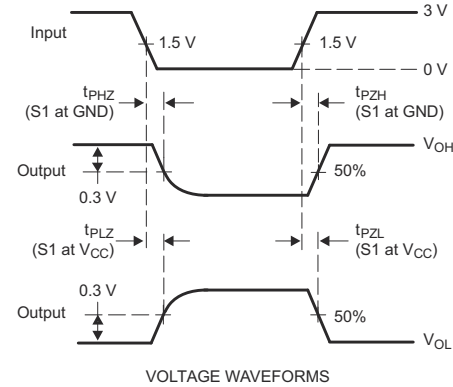
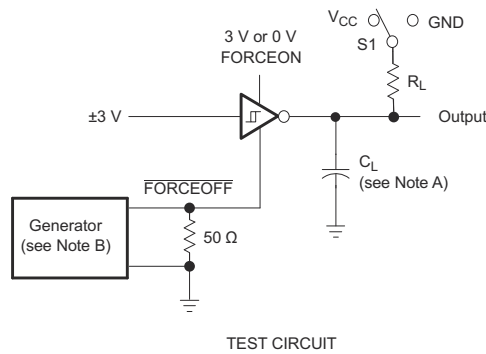
Figure 7-2. Driver Pulse Skew



A. C_L includes probe and jig capacitance.

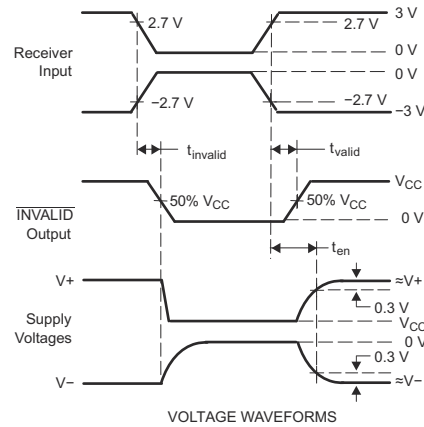
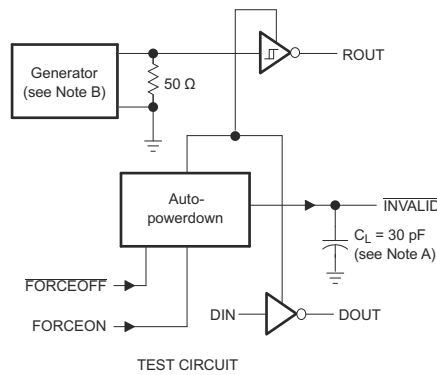
B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 7-3. Receiver Propagation Delay Times



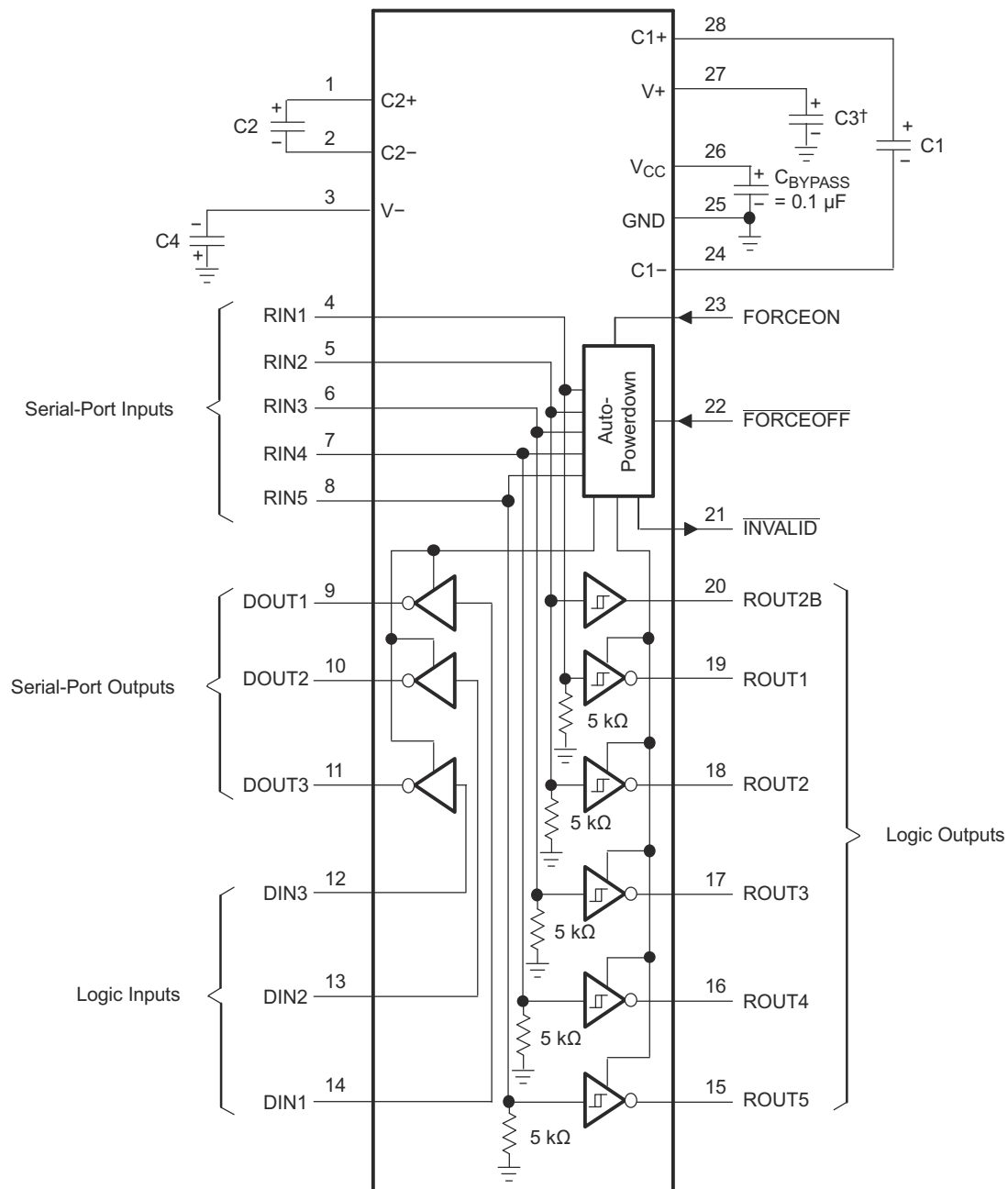
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.
- C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- D. t_{PZL} and t_{PZH} are the same as t_{en} .

Figure 7-4. Receiver Enable and Disable Times



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 5 Mbits, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

Figure 7-5. INVALID Propagation Delay Times and Supply Enabling Time



† C3 can be connected to V_{CC} or GND.

A. Resistor values shown are nominal.

Figure 7-6. Typical Operating Circuit and Capacitor Values

Table 7-1. V_{CC} vs Capacitor Values

V_{CC}	C1	C2, C3, and C4
3.3 V $\pm$ 0.3 V	0.1 μ F	0.1 μ F
5 V $\pm$ 0.5 V	0.047 μ F	0.33 μ F
3 V to 5.5 V	0.1 μ F	0.47 μ F

8 Detailed Description

8.1 Overview

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If FORCEOFF is set low, both drivers and receivers (except ROUT2B) are shut off, and the supply current is reduced to 1 μ A. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur.

Auto-powerdown can be disabled when FORCEON and FORCEOFF are high and should be done when driving a serial mouse. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The INVALID output is used to notify the user if an RS-232 signal is present at any receiver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than –2.7 V or has been between –0.3 V and 0.3 V for less than 30 μ s. INVALID is low (invalid data) if all receiver input voltages are between –0.3 V and 0.3 V for more than 30 μ s. Refer to Figure 7-5 for receiver input levels.

8.2 Device Functional Modes

8.2.1 Function Tables

Each Driver, DIN⁽¹⁾

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver, RIN⁽¹⁾

INPUTS				OUTPUTS			RECEIVER STATUS
RIN2	RIN1, RIN3–RIN5	FORCEOFF	VALID RIN RS-232 LEVEL	ROUT2B	ROUT2	ROUT1, ROUT3–5	
L	X	L	X	L	Z	Z	Powered off while ROUT2B is active
H	X	L	X	H	Z	Z	
L	L	H	YES	L	H	H	Normal operation with auto-powerdown disabled/enabled
L	H	H	YES	L	L	L	
H	L	H	YES	H	H	H	
H	H	H	YES	H	L	L	
Open	Open	H	YES	L	H	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

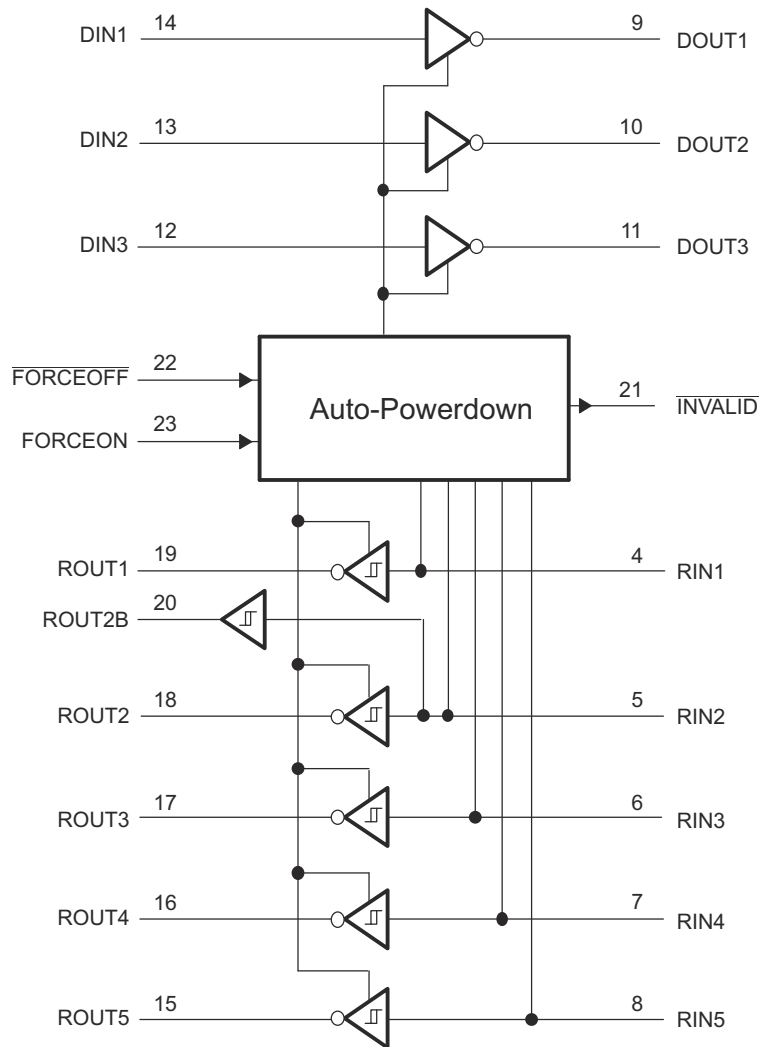


Figure 8-1. Logic Diagram (Positive Logic)

9 Device and Documentation Support

9.1 Device Support

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65C3243DBR	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243
SN65C3243DBR.A	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243
SN65C3243DW	Active	Production	SOIC (DW) 28	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243
SN65C3243DW.A	Active	Production	SOIC (DW) 28	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243
SN65C3243DWR	Active	Production	SOIC (DW) 28	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243
SN65C3243DWR.A	Active	Production	SOIC (DW) 28	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243
SN65C3243PWR	Active	Production	TSSOP (PW) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3243
SN65C3243PWR.A	Active	Production	TSSOP (PW) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3243
SN75C3243DBR	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243
SN75C3243DBR.A	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243
SN75C3243DW	Active	Production	SOIC (DW) 28	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243
SN75C3243DW.A	Active	Production	SOIC (DW) 28	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243
SN75C3243DWR	Active	Production	SOIC (DW) 28	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243
SN75C3243DWR.A	Active	Production	SOIC (DW) 28	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243
SN75C3243PW	Obsolete	Production	TSSOP (PW) 28	-	-	Call TI	Call TI	0 to 70	CA3243
SN75C3243PWR	Active	Production	TSSOP (PW) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3243
SN75C3243PWR.A	Active	Production	TSSOP (PW) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3243

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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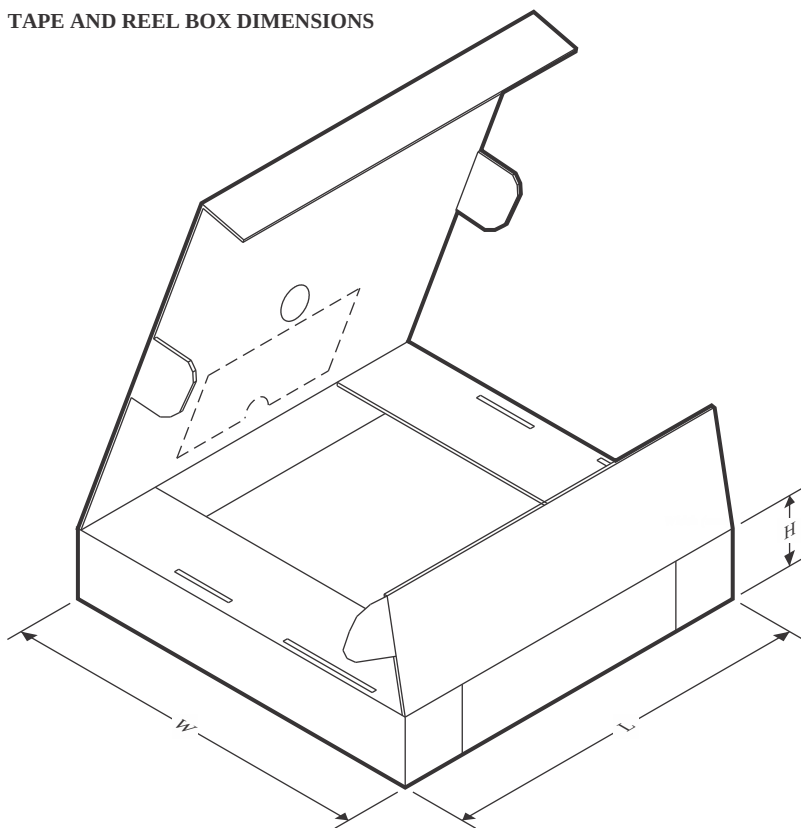
TAPE AND REEL INFORMATION



*All dimensions are nominal

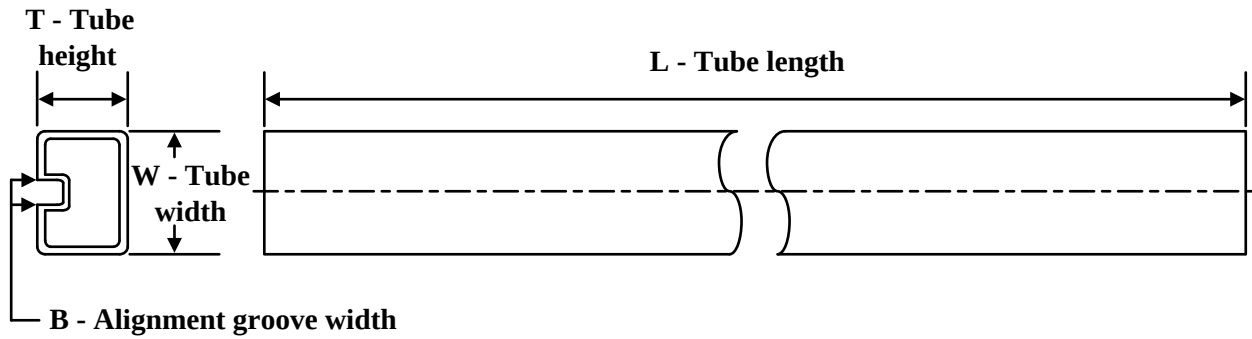
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C3243DBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN65C3243DWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN65C3243PWR	TSSOP	PW	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
SN75C3243DBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN75C3243DWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN75C3243PWR	TSSOP	PW	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C3243DBR	SSOP	DB	28	2000	353.0	353.0	32.0
SN65C3243DWR	SOIC	DW	28	1000	350.0	350.0	66.0
SN65C3243PWR	TSSOP	PW	28	2000	353.0	353.0	32.0
SN75C3243DBR	SSOP	DB	28	2000	353.0	353.0	32.0
SN75C3243DWR	SOIC	DW	28	1000	350.0	350.0	66.0
SN75C3243PWR	TSSOP	PW	28	2000	353.0	353.0	32.0

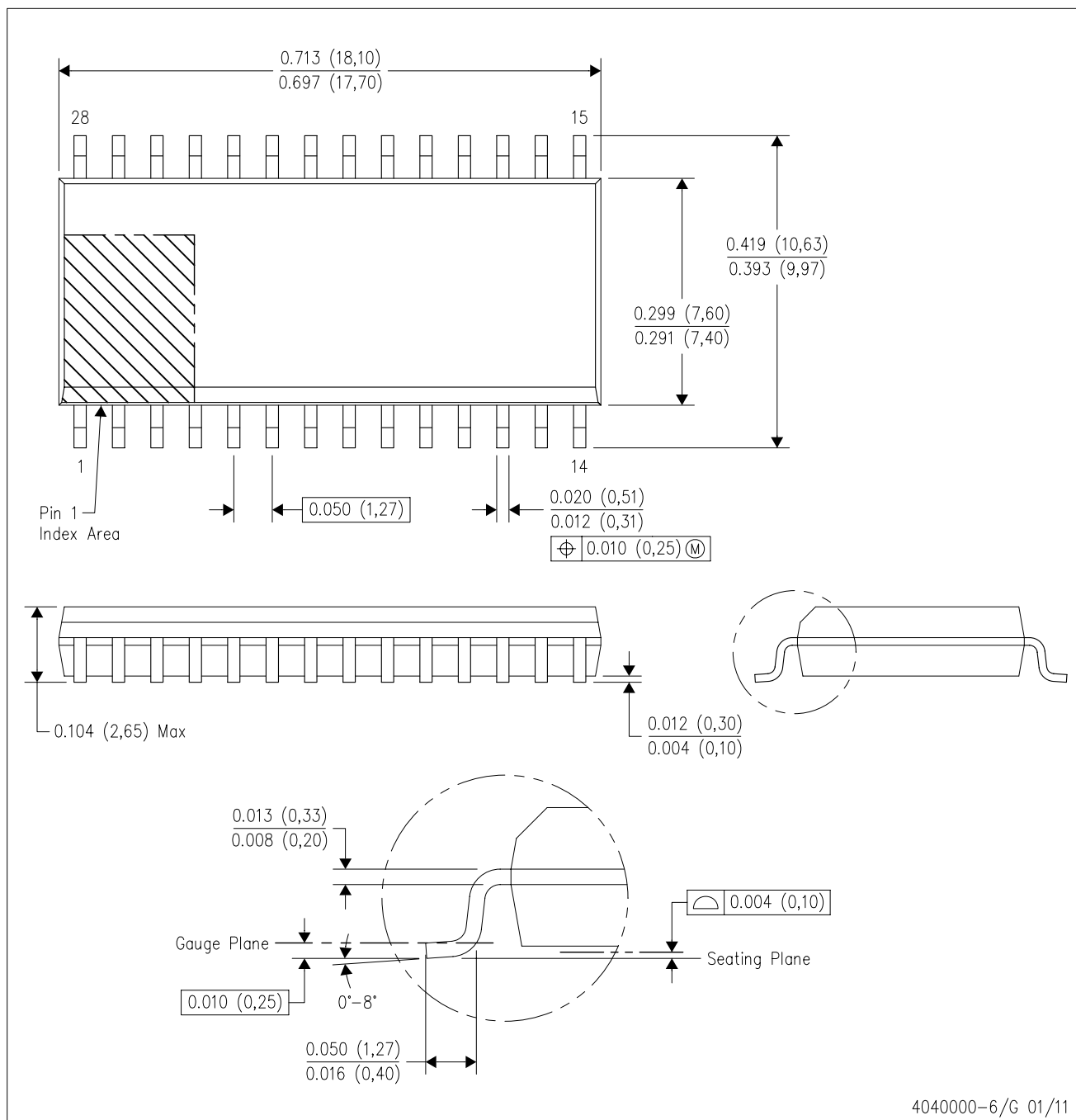
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65C3243DW	DW	SOIC	28	20	506.98	12.7	4826	6.6
SN65C3243DW.A	DW	SOIC	28	20	506.98	12.7	4826	6.6
SN75C3243DW	DW	SOIC	28	20	506.98	12.7	4826	6.6
SN75C3243DW.A	DW	SOIC	28	20	506.98	12.7	4826	6.6

DW (R-PDSO-G28)

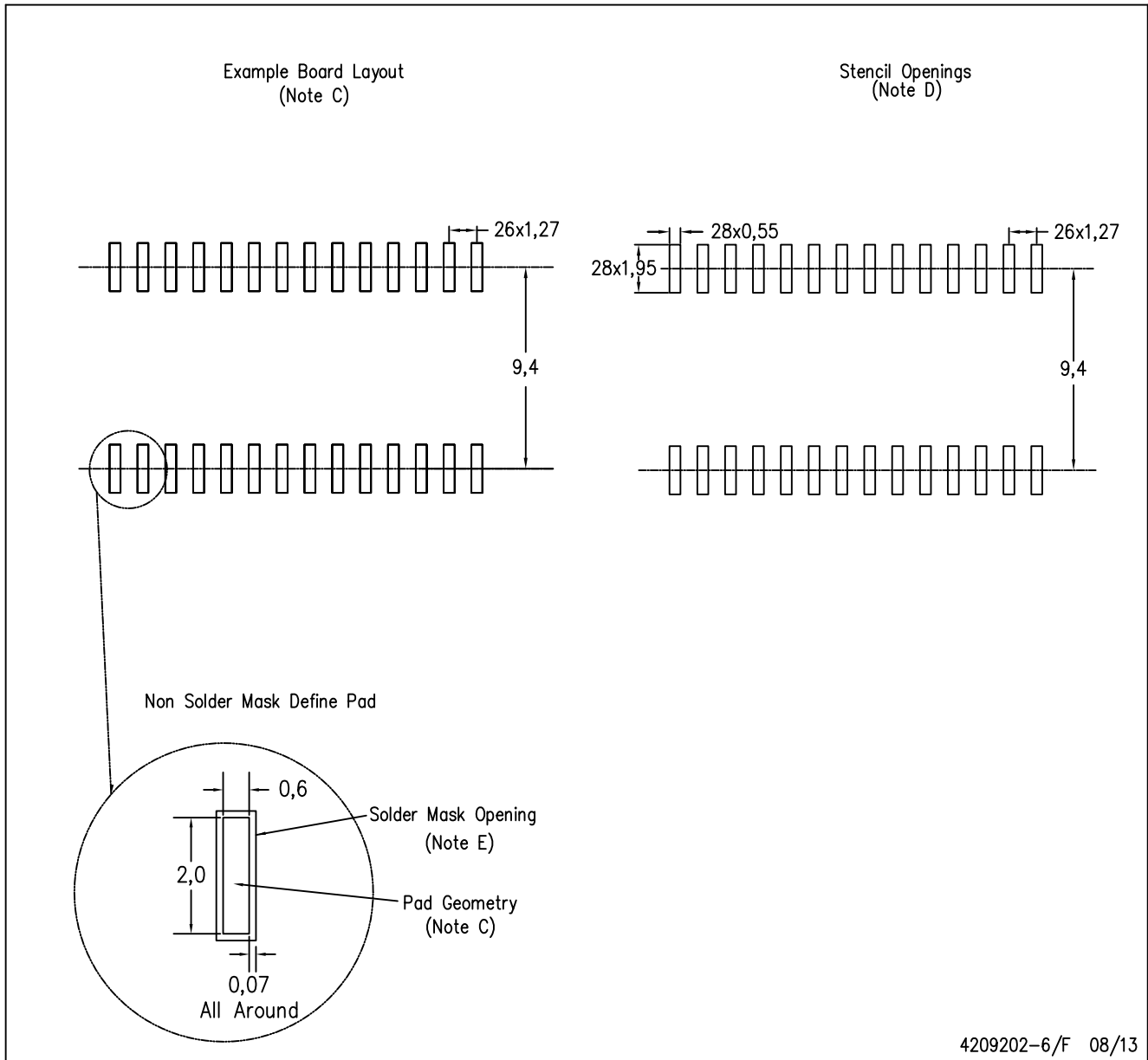
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AE.

DW (R-PDSO-G28)

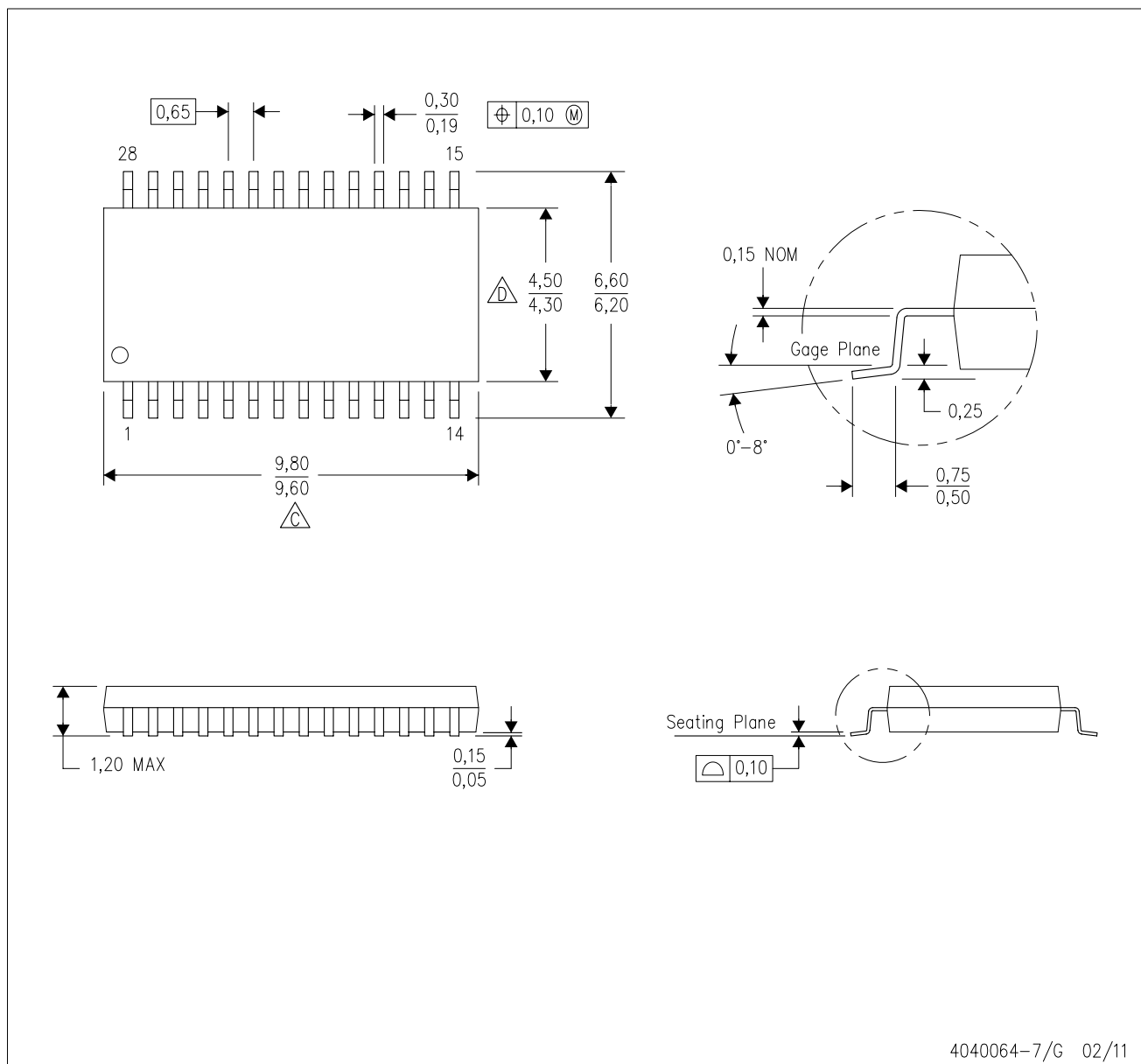
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

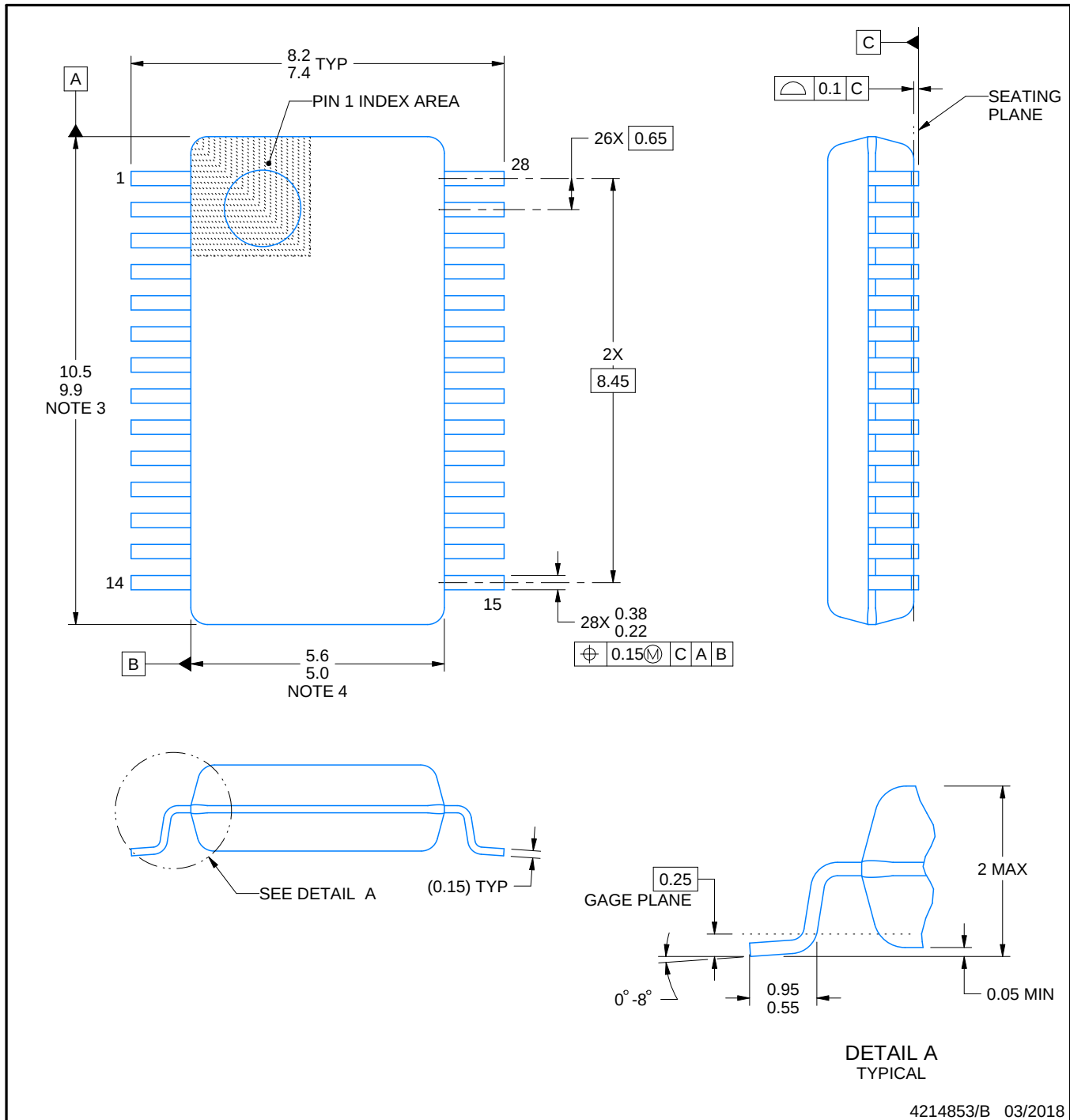
PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



4040064-7/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153



4214853/B 03/2018

NOTES:

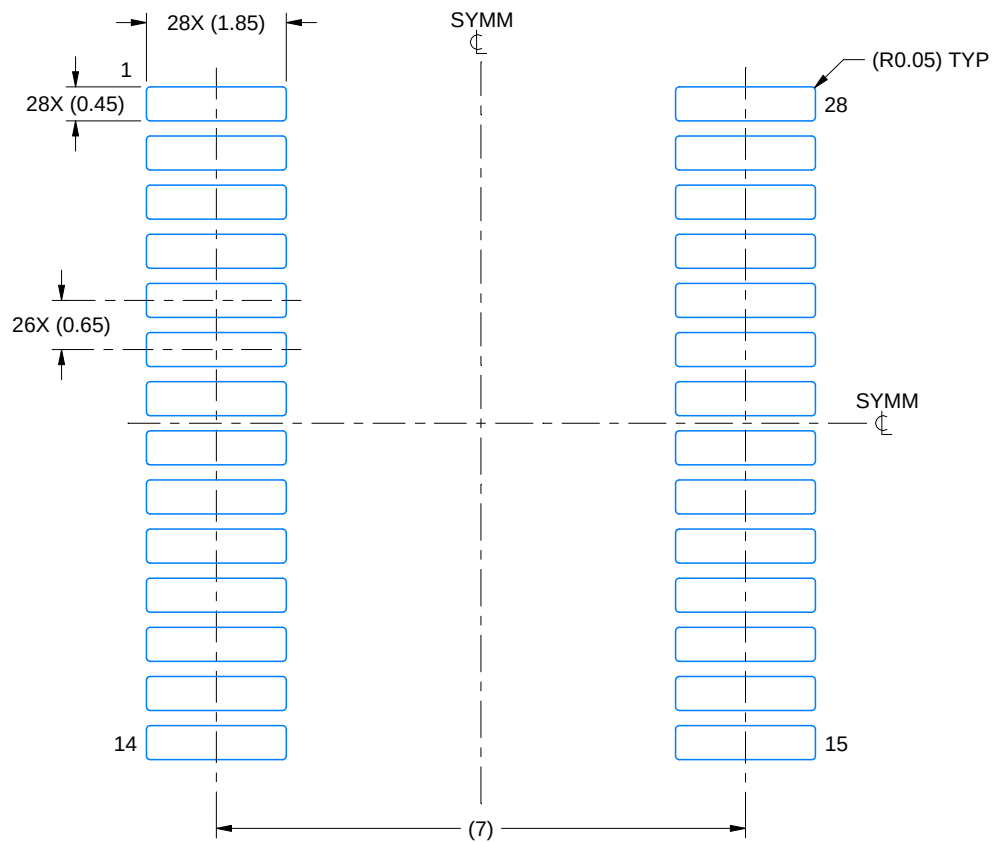
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

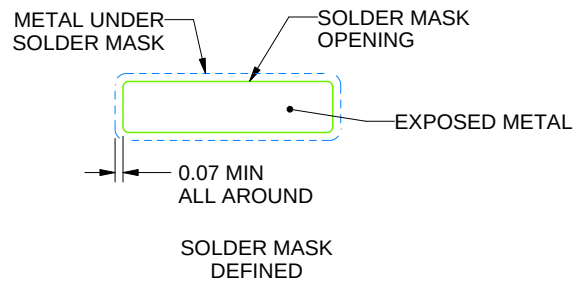
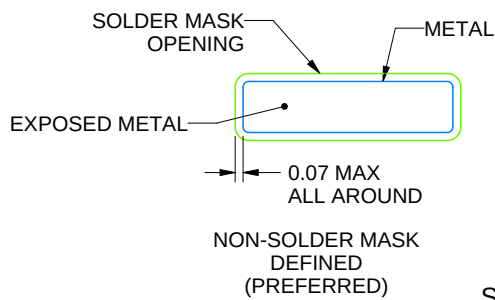
DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214853/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

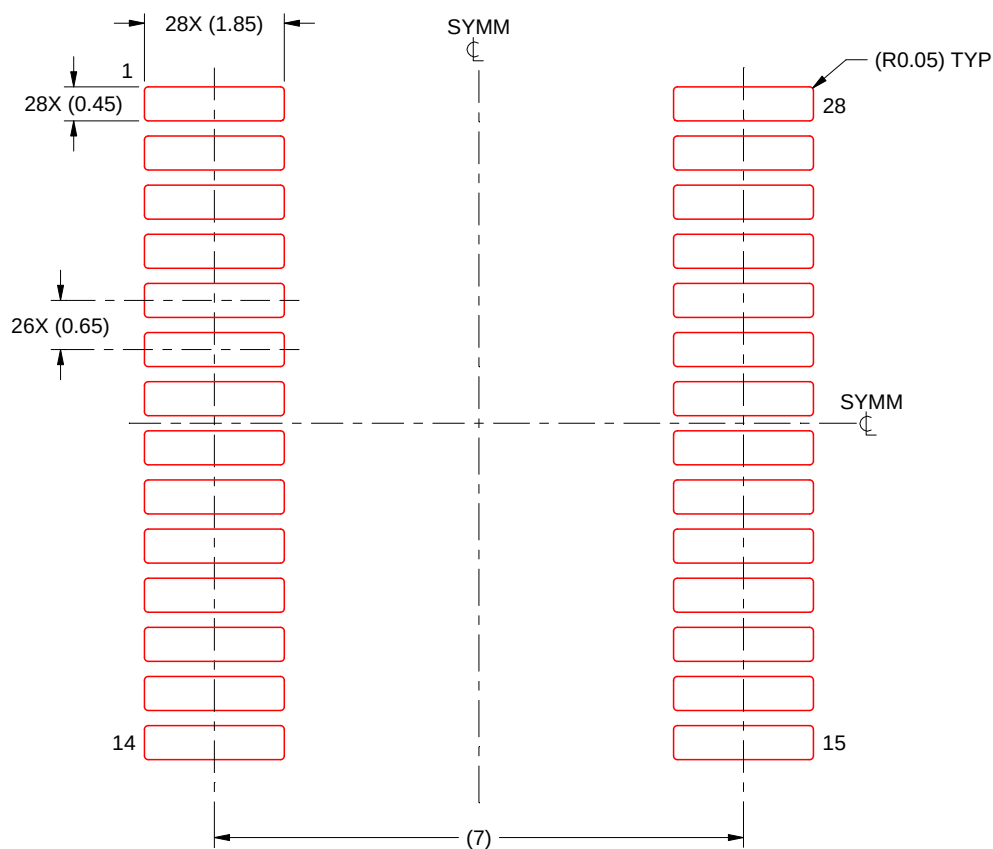
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025