3.3-V Differential PECL/LVDS to TTL Translator

Check for Samples: SN65EPT21

FEATURES

- **1 ns Propagation Delay**
- **F_{max} > 300MHz**
- **Operating Range: V_{CC} = 3.0 V to 3.6 V with GND = 0 V**
- **24-mA TTL Output**
- **Built-In Temperature Compensation**
- **Drop-In Compatible to the MC10EPT21, MC100EPT21**

APPLICATIONS

- **Data and Clock Transmission Over Backplane**
- **Signaling Level Conversion for Clock or Data**

DESCRIPTION

The SN65EPT21 is a differential PECL-to-TTL translator. It operates on +3.3 V supply and ground only. The device includes circuitry to maintain inputs at Vcc/2 when left open.

The V_{BB} pin is a reference voltage output for the device. When the device is used in single-ended mode, the unused input should be tied to V_{BB}. This reference voltage can also be used to bias the input when it is ac coupled. When it is used, place a 0.01µF decoupling capacitor between V_{CC} and V_{BB}. Also limit the sink/source current to < 0.5 mA to V_{BB}. Leave V_{BB} open when it is not used.

The SN65EPT21 is housed in an industry standard SOIC-8 package and is also available in an optional TSSOP-8 package.

PIN ASSIGNMENT(Add pullup on BOTH inputs)

D or DGK PACKAGE
(TOP VIEW)

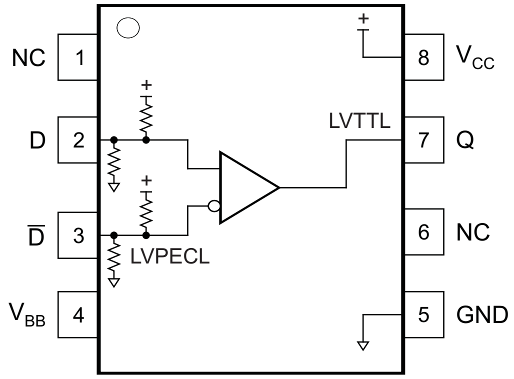

Table 1. Pin Descriptions

PIN	FUNCTION
Q	LVTTL/LVCMOS Output
D, $\overline{D}$	Differential LVPECL/LVDS/CML Input
V_{CC}	Positive Supply
V_{BB}	Output Reference Voltage
GND	Ground
NC	No Connect
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65EPT21D/DR	EPT21	SOIC	NiPdAu
SN65EPT21DGK/DGKR	SSSI	MSOP	NiPdAu

(1) Leaded device options are not initially available; contact a sales representative for further details.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

PARAMETER	CONDITIONS	VALUE	UNIT
Absolute PECL mode supply voltage	V_{CC} (GND = 0 V)	3.8	V
Sink/source current, V_{BB}		±0.5	mA
PECL input voltage	GND = 0 V, $V_I \leq V_{CC}$	0 to 3.8	V
Operating temperature range		–40 to 85	°C
Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	POWER RATING $T_A < 25°C$ (mW)	THERMAL RESISTANCE, JUNCTION-TO-AMBIENT NO AIRFLOW	DERATING FACTOR $T_A > 25°C$ (mW/°C)	POWER RATING $T_A = 85°C$ (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
MSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
θ_{JB}	Junction-to-board thermal resistance	SOIC		79		°C/W
		MSOP		120		
θ_{JC}	Junction-to-case thermal resistance	SOIC		98		°C/W
		MSOP		74		

KEY ATTRIBUTES

CHARACTERISTICS		VALUE
Internal input pull-down resistor		50 kΩ
Internal input pull-up resistor		50 kΩ
Moisture sensitivity level		Level 1
Flammability rating (oxygen index: 28 to 34)		UL 94 V-0 at 0.125 in
Electrostatic discharge	Human body model	2 kV
	Charged-device model	2 kV
	Machine mode	200 V
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test		

PECL DC CHARACTERISTICS

At V_{CC} = 3.3 V, GND = 0.0 V (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	T_A = –40°C			T_A = 25°C			T_A = 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage, single-ended		2075		2420	2075		2420	2075		2420	mV
V_{IL}	Low-level input voltage, single-ended		1355		1675	1355		1675	1355		1675	mV
V_{BB}	Output reference voltage		1910	2009	2160	1910	2034	2160	1910	2026	2160	mV
V_{IHCMR}	High-level input voltage, common-mode range, differential	See (3)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	High-level input current				150			150			150	µA
I_{IL}	Low-level input current		-150			-150			-150			µA

(1) The device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

(2) Input parameters vary 1:1 with V_{CC}.

(3) $V_{IHCMR(min)}$ varies 1:1 with GND, $V_{IHCMR(max)}$ varies 1:1 with V_{CC}. V_{IHCMR} range is referenced to the most positive side of the differential input signal

TTL DC CHARACTERISTICS

At V_{CC} = 3.3 V, GND = 0.0, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	Power supply current	Output is HIGH	5	9	20	mA
I_{CCL}	Power supply current	Output is LOW	8	7.5	26	mA
V_{OH}	High-level output voltage	I_{OH} = –3.0 mA	2.4	3.05		V
V_{OL}	Low-level output voltage	IOL = 24 mA		0.32	0.5	V
I_{OS}	Output short circuit current		–180	–100	–80	mA

(1) The device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

AC CHARACTERISTICS

At V_{CC} = 3.0 V to 3.6 V, GND = 0.0 V (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	T_A = –40°C			T_A = 25°C			T_A = 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Maximum switching frequency (Figure 1–Figure 3)		300			300			300			MHz
t_{PLH}	Propagation delay	At 1.5 V	1000	1394	1800	1000	1444	1800	1000	1481	1800	ps
t_{PHL}	Propagation delay	At 1.5 V	1000	1140	1900	1000	1280	1900	1000	1421	1900	ps
t_{JITTER}	Random clock jitter (RMS)			2.25	5		3.2	5		3.4	5	ps
t_{SKEW}	Duty Cycle Skew(3)			94	250		78	250		62	250	ps
t_{SKPP}	Part-to-Part Skew(3)				500			500			500	ps
V_{PP}	Input swing	See (4)	150		1200	150		1200	150		1200	mV
t_r/t_f	Output rise/fall times	Q, $\overline{Q}$ (0.8V - 2.0V))	250	500	900	250	500	900	250	500	900	ps

(1) The device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

(2) R_L = 500 Ω to GND and C_L = 20 pF to GND. See Figure 4. Measured with 750mV, 50% duty cycle clock source

(3) Skews are measured between outputs under identical transitions

(4) $V_{PP(min)}$ is minimum input swing for which ac parameters are assured.

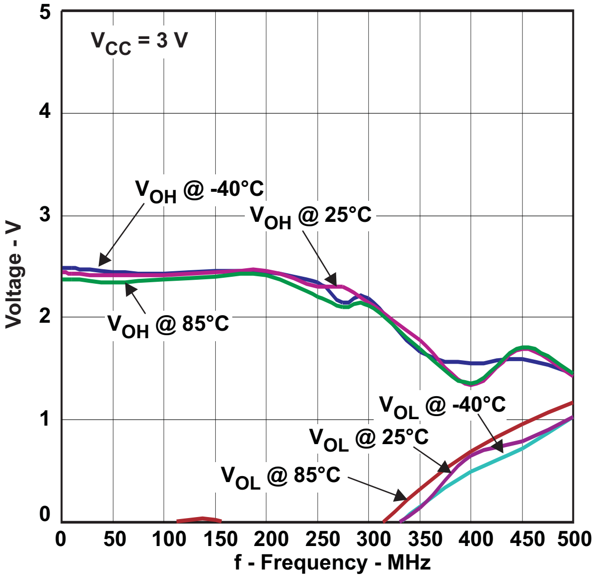

Figure 1. Maximum Switching Frequency V_{CC}= 3.0 V

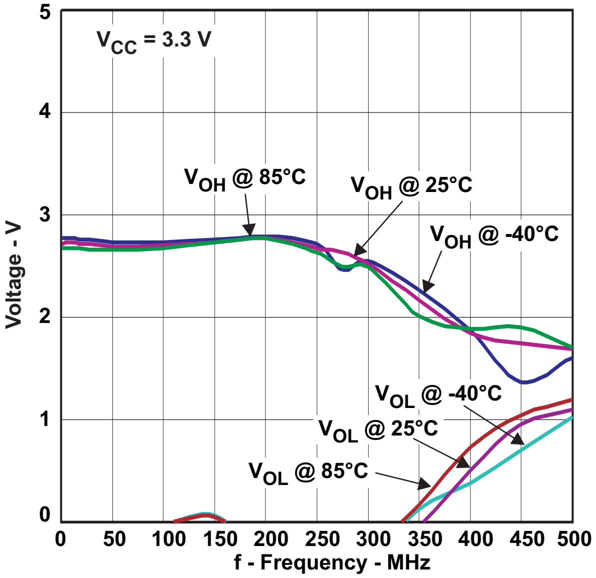

Figure 2. Maximum Switching Frequency V_{CC}= 3.3 V

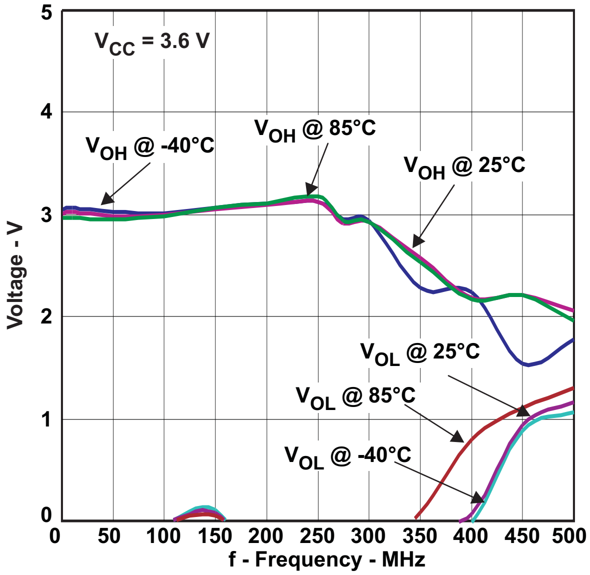

Figure 3. Maximum Switching Frequency V_{CC}= 3.6 V

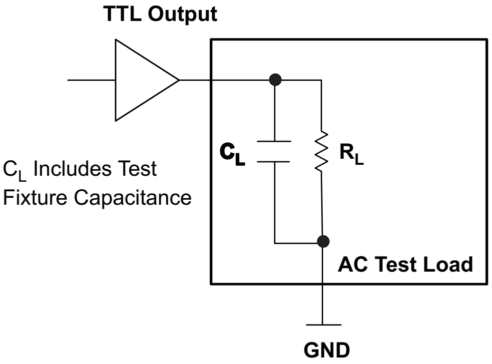

Figure 4. TTL Output AC Test Loading Condition

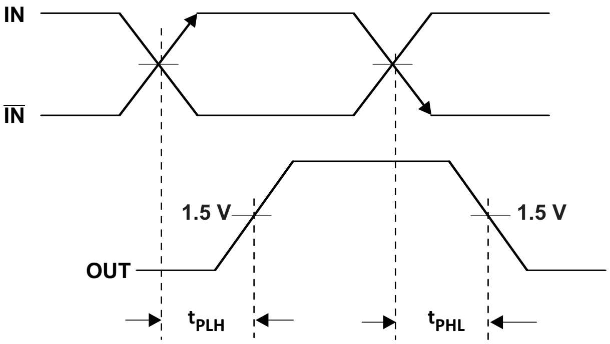

Figure 5. Output Propagation Delay

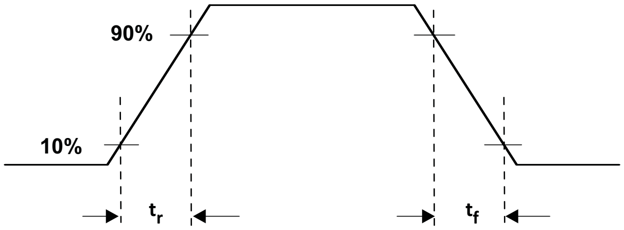

Figure 6. Output Rise and Fall Times

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65EPT21D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	EPT21
SN65EPT21D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	EPT21
SN65EPT21DGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SSSI
SN65EPT21DGK.B	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SSSI
SN65EPT21DGKG4	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SSSI
SN65EPT21DGKG4.B	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SSSI
SN65EPT21DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-40 to 85	SSSI
SN65EPT21DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SSSI
SN65EPT21DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	EPT21
SN65EPT21DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	EPT21

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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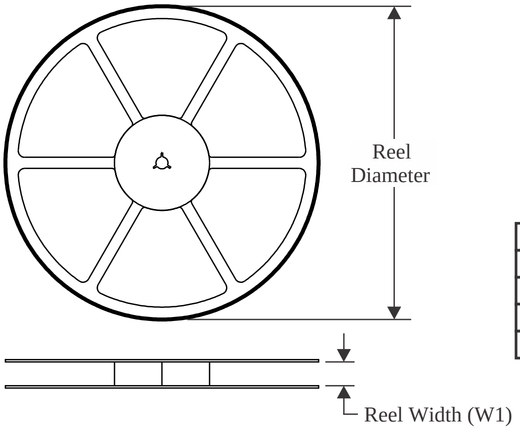
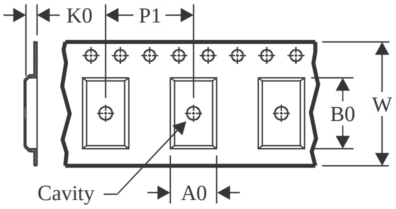
TAPE AND REEL INFORMATION

REEL DIMENSIONS

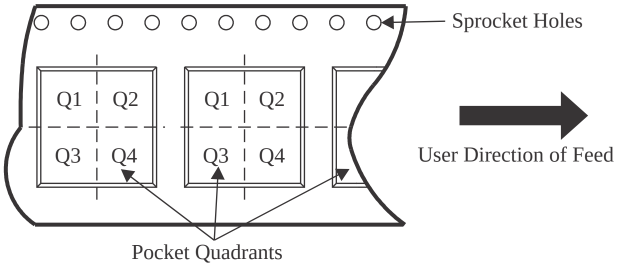


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

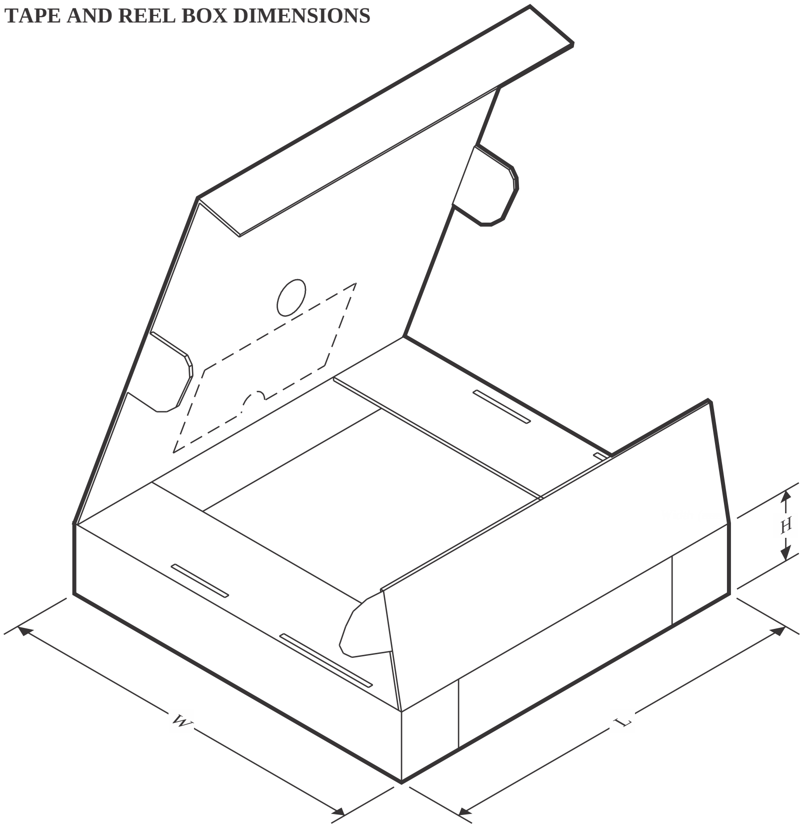
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65EPT21DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

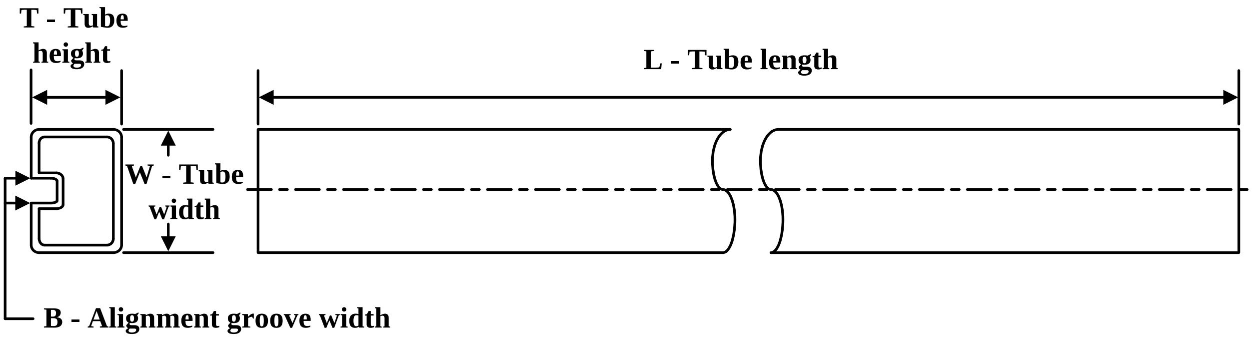
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

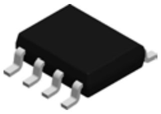
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65EPT21DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65EPT21D	D	SOIC	8	75	506.6	8	3940	4.32
SN65EPT21D.B	D	SOIC	8	75	506.6	8	3940	4.32
SN65EPT21DGK	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
SN65EPT21DGK.B	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
SN65EPT21DGKG4	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
SN65EPT21DGKG4.B	DGK	VSSOP	8	80	330.2	6.6	3005	1.88

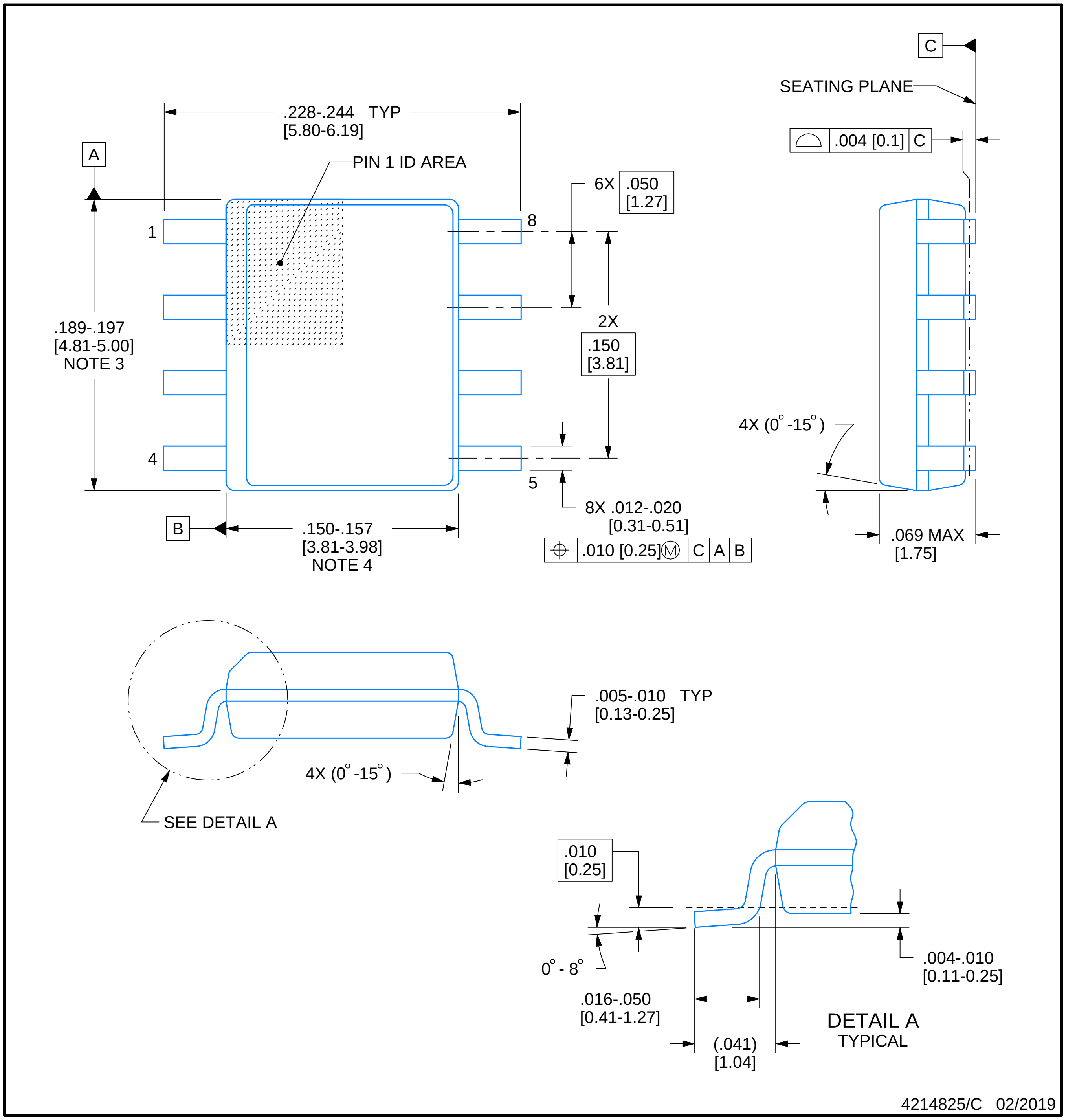


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

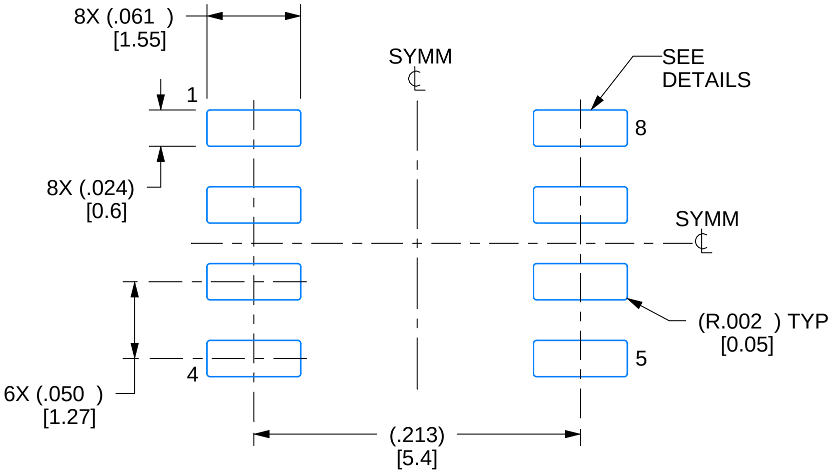
SMALL OUTLINE INTEGRATED CIRCUIT



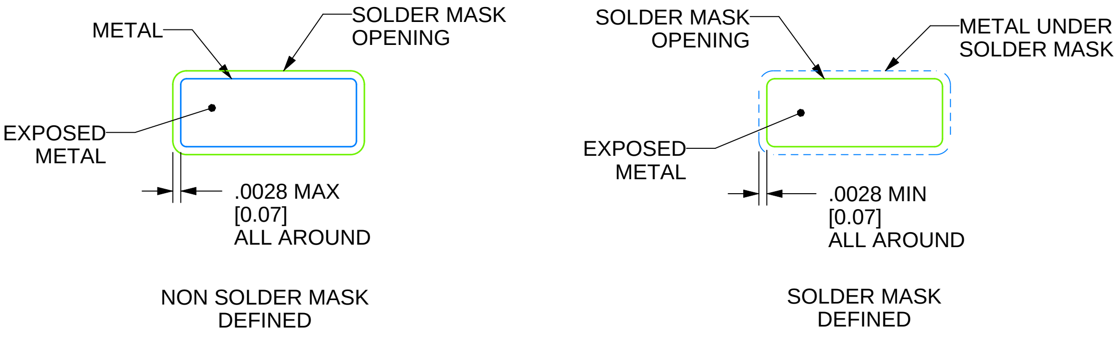
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



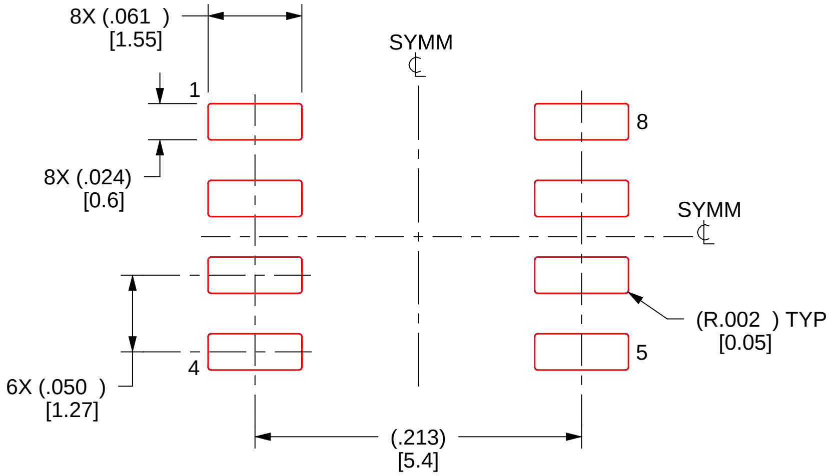
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

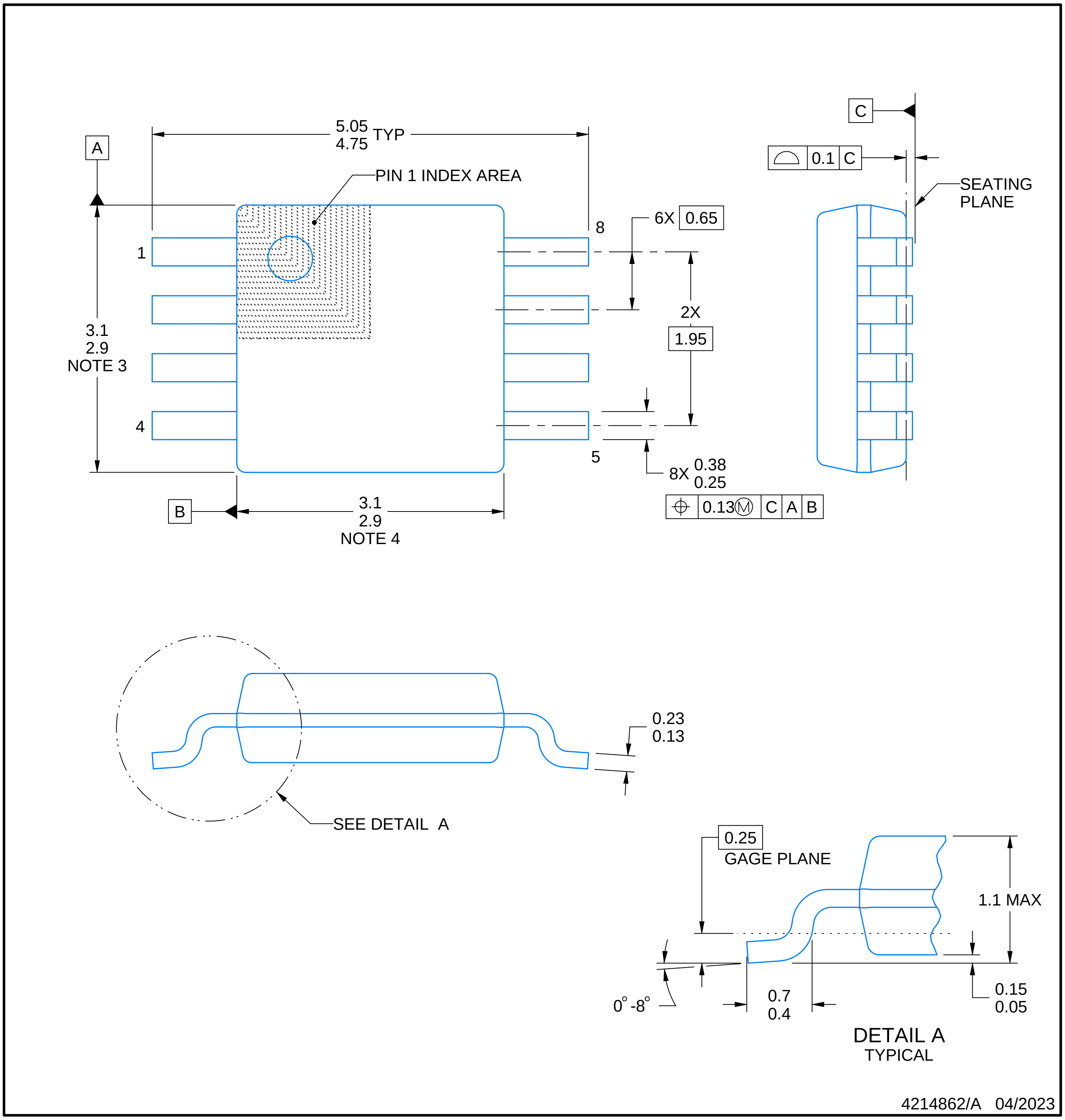


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

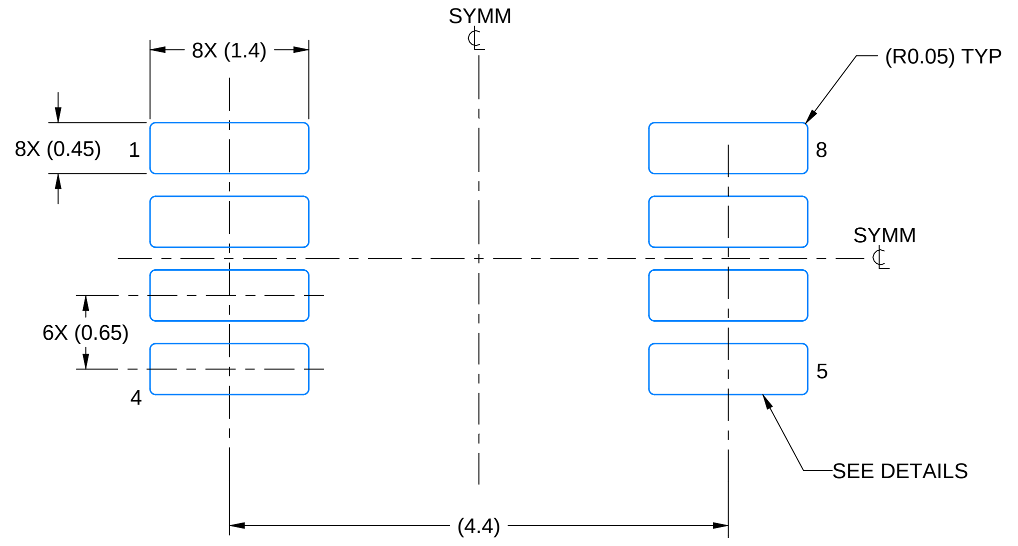
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



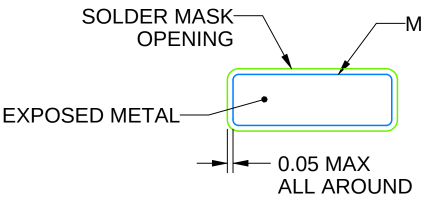
PowerPAD is a trademark of Texas Instruments.

NOTES:

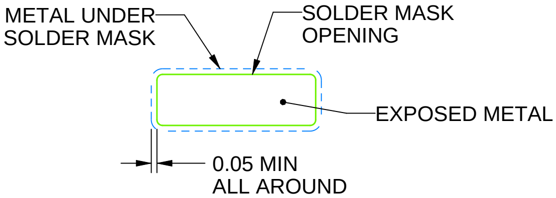
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK
DEFINED
(PREFERRED)



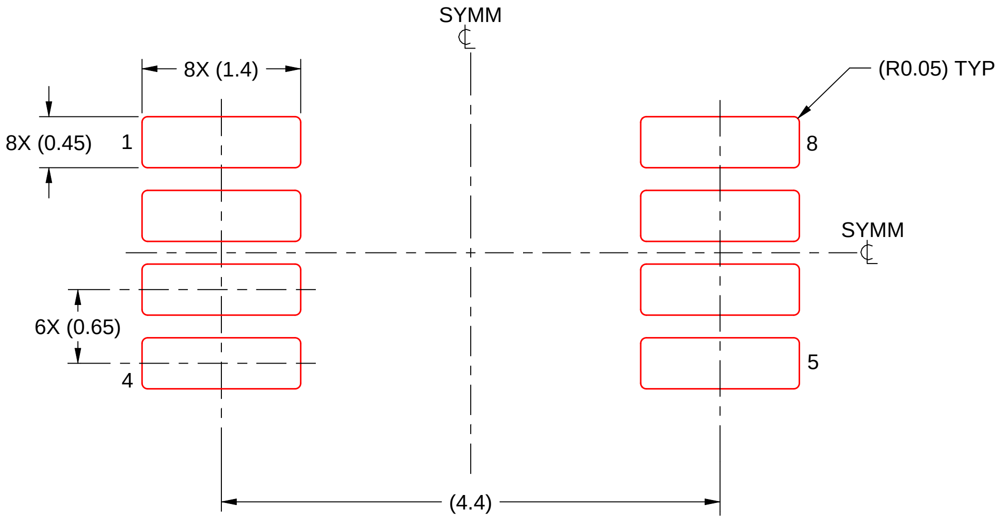
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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